PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : C23C 16/00, C30B 23/06 — A1

(11) International Publication Number: **WO 00/03056**

(43) International Publication Date: 20 January 2000 (20.01.00)

(21) International Application Number: PCT/US99/15070

(22) International Filing Date: 30 June 1999 (30.06.99)

(30) Priority Data:
09/113,934 10 July 1998 (10.07.98) US

(71) Applicant: ASM AMERICA, INC. [US/US]; 3440 East University Drive, Phoenix, AZ 85034–7200 (US).

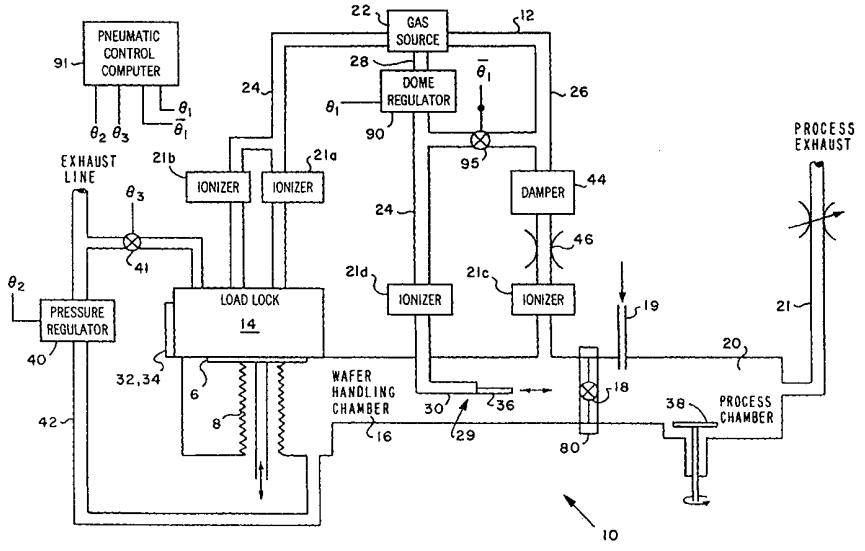
(72) Inventors: DOLEY, Allan, D.; 16015 S. 35 Street, Phoenix, AZ 85044 (US). GOODWIN, Dennis, L.; 4268 W. Park Avenue, Chandler, AZ 85226 (US). O'NEILL, Kenneth; 3426 E. Cherokee Street, Phoenix, AZ 85044 (US). VRIJBURG, Gerben; 2710 S. Las Flores, Mesa, AZ 85202 (US). RODRIGUEZ, David; 13602 N. 44th Street #208, Phoenix, AZ 85032 (US). AGGARWAL, Ravinder; 819 W. Royal Palms, Gilbert, AZ 85233 (US).

(74) Agents: ROBINSON, Richard, K. et al.; 12900 Preston Road, LB–41, Suite 1202, North Dallas Bank Tower, Dallas, TX 75230 (US).

(81) Designated States: JP, KR, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: SYSTEM AND METHOD FOR REDUCING PARTICLES IN EPITAXIAL REACTORS



(57) Abstract

An apparatus and method for reducing particles in reactors. The apparatus (10) includes an enclosure for processing the semiconductor wafers. The enclosure has a wafer handling chamber (16) connected by an isolation gate valve (18) to a processing chamber (20). Additionally, the apparatus includes: pipes (24, 26) for delivering a purge gas into the wafer handling chamber (16); a pilot operated back pressure regulator (40) for regulating the delivery and removal of the purge gas from the enclosure for reducing disturbances from the purge gas entering into the enclosure; a flow regulated Bernoulli wand (36) for lifting and holding a single wafer; ionizers (21a–21d) in the purge gas lines entering the wafer handling chamber and load locks for ionizing the purged gas molecules, the ionized gas discharges all the static inside the semiconductor equipment and prevents the wafer from attracting charged particles; and means for reducing gas flow turbulence when switching valves within the reactor.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	**ES**	Spain	**LS**	Lesotho	**SI**	Slovenia
AM	Armenia	**FI**	Finland	**LT**	Lithuania	**SK**	Slovakia
AT	Austria	**FR**	France	**LU**	Luxembourg	**SN**	Senegal
AU	Australia	**GA**	Gabon	**LV**	Latvia	**SZ**	Swaziland
AZ	Azerbaijan	**GB**	United Kingdom	**MC**	Monaco	**TD**	Chad
BA	Bosnia and Herzegovina	**GE**	Georgia	**MD**	Republic of Moldova	**TG**	Togo
BB	Barbados	**GH**	Ghana	**MG**	Madagascar	**TJ**	Tajikistan
BE	Belgium	**GN**	Guinea	**MK**	The former Yugoslav Republic of Macedonia	**TM**	Turkmenistan
BF	Burkina Faso	**GR**	Greece			**TR**	Turkey
BG	Bulgaria	**HU**	Hungary	**ML**	Mali	**TT**	Trinidad and Tobago
BJ	Benin	**IE**	Ireland	**MN**	Mongolia	**UA**	Ukraine
BR	Brazil	**IL**	Israel	**MR**	Mauritania	**UG**	Uganda
BY	Belarus	**IS**	Iceland	**MW**	Malawi	**US**	United States of America
CA	Canada	**IT**	Italy	**MX**	Mexico	**UZ**	Uzbekistan
CF	Central African Republic	**JP**	Japan	**NE**	Niger	**VN**	Viet Nam
CG	Congo	**KE**	Kenya	**NL**	Netherlands	**YU**	Yugoslavia
CH	Switzerland	**KG**	Kyrgyzstan	**NO**	Norway	**ZW**	Zimbabwe
CI	Côte d'Ivoire	**KP**	Democratic People's Republic of Korea	**NZ**	New Zealand		
CM	Cameroon			**PL**	Poland		
CN	China	**KR**	Republic of Korea	**PT**	Portugal		
CU	Cuba	**KZ**	Kazakstan	**RO**	Romania		
CZ	Czech Republic	**LC**	Saint Lucia	**RU**	Russian Federation		
DE	Germany	**LI**	Liechtenstein	**SD**	Sudan		
DK	Denmark	**LK**	Sri Lanka	**SE**	Sweden		
EE	Estonia	**LR**	Liberia	**SG**	Singapore		

SYSTEM AND METHOD FOR REDUCING PARTICLES IN EPITAXIAL REACTORS

BACKGROUND OF THE INVENTION

Technical Field of the Invention

The invention relates to the process of forming films of material on semiconductor wafers through the use of carrier gases within a reactor chamber. In particular, the present invention relates to the epitaxial deposition of specific materials onto a silicon wafer and to a system and method for reducing or eliminating particulate matter and the resulting particle-related defects on the finished wafer.

In most semiconductor manufacturing equipment used for growth of films of material onto semiconductor wafers, the wafers are loaded in one or multiple load locks and transported through a wafer handling chamber to a reactor, where the actual material is deposited onto the semiconductor wafers by means of gases or vapors. The gas in the load lock, wafer handling chamber and reactor must be as particle-free as possible in order to reduce the number of defects on the semiconductor wafer surface.

Improvements in the capabilities of semiconductor manufacturing equipment continues at an astonishing rate. As capabilities of lithography and etching equipment increases the circuit density on a wafer increases and with the increase in circuit density the specification for particle free environment within the processing equipment also increases. In addition to the resulting circuit density that has been achieved with the improvements in lithography and etching, the size of wafers has increased to 300 mm. Semiconductor manufacturers require further production improvements through the increase in the yields of semiconductor devices from the equipment use to manufacture those devices. The implementation of epitaxial layers, both homoepitaxial and heteroepitaxial, on an

underlying substrate layer has a great impact on the yields of the associated semiconductor wafers. A primary example is the growth of epitaxial silicon on a semiconductor wafer substrate. Growth of an epitaxial silicon layer is typically performed in a chemical vapor deposition process in which the wafers are heated while a gaseous silicon compound is passed over the wafer to affect pyrolysis or decomposition. Epitaxial depositions in general and silicon epitaxial deposition in particular are integral parts of VLSI processing, especially for the advanced bipolar, NMOS and CMOS technologies, since many of the components of the individual transistors and devices are formed in an epitaxial layer.

The ability to process good quality advanced NMOS, CMOS and bipolar IC chips using epitaxy is strongly dependent on maintaining a substantially defect-free state (1) for the bulk semiconductor wafer and for the surface of the bulk wafer, and (2) during the step of depositing the epitaxial silicon layer. Simply put, and as discussed below, elimination of both sub-surface and surface defects is crucial to obtaining good yields in current and future technologies, particularly as those technologies process toward a sub-micron minimum device feature size.

Surface defects are usually related to undesirable particles. It is extremely critical for sub-micron minimum device feature sizes and for large chip areas that the undesirable particles be eliminated, since a single defect in such devices can cause nonfunctionality of the device and as few as one defect per square centimeter (about 80 defects per four inch wafer) can have catastrophic effects on wafer processing yields. It is a characteristic of epitaxial processing that the crystallographic nature and defect level of the deposited epitaxial layer or epi layer reflects the parent or bulk substrate wafer. Thus, for example, stacking faults on the substrate can give rise to

epitaxial stacking faults, and dislocations in the substrate can be transmitted through the epi layer. In addition, epitaxial defects such as pits and micro-contamination result from the bulk substrate wafer surface particles. As a consequence, even where the parent substrate is substantially defect-free (the introduction of substantially defect-free silicon wafer starting material in the mid 1970's offered this possibility), the growth of defect-free epitaxial layers requires the elimination of particles on the surface of the parent substrate wafer. Unfortunately, using present day epitaxial processing technology, the elimination or substantial decrease in unwanted particles and the associated achievement of very low particle-related defect densities are accomplished by extensive runs and wafer inspection resulting in very low wafer yields.

Although the semiconductor manufacturing equipment is constructed so that particles cannot enter through the walls or with the gas flow, particles may enter the semiconductor manufacturing equipment by other means, such as when semiconductor wafers are put into a load lock, during equipment maintenance or through some other indirect source. Particles generated during the process are removed by the laminar flow of the purge gas. The particles may be transported to the inner surfaces of the equipment and adhere thereon. If particles are present in the gas, or suddenly released from the inner surfaces of the equipment, the particles may be transported to the surface of the semiconductor wafer and cause defects. Undesirable particles including the particles that are to be deposited on the semiconductor wafer during the manufacturing process can be attracted to, deposited and retained on the inner surfaces of the semiconductor manufacturing equipment. Once attracted to the inner surfaces of the semiconductor manufacturing equipment, several different forces including

molecular forces (Van der Waals force), capillary forces, and electrostatic forces retain the undesirable particles on the inner surfaces of the semiconductor manufacturing equipment. If for some reason these particles were to be released then they can become airborne and settle on the surfaces of the semiconductor wafers and create defects in the resulting processed wafer. Air turbulence is one way in which these undesirable particles may be freed from their attachment to the inner surfaces of the semiconductor manufacturing equipment.

Once airborne the movement of particles inside the semiconductor manufacturing equipment is subject to several different forces; gravity, the fluid drag of the surrounding gas flow, and electrostatic force. Gravity is a very weak force on small particles. Normally, a purge with a particle-free gas is maintained through the semiconductor manufacturing equipment in order to create a particle-free environment. Any particles that are released from the inner surfaces of the equipment are transported by the fluid drag of the purge gas to the gas exhaust. However, electrostatic force negatively affects the removal of particles by the purge gas flow. Particles may be transported to semiconductor wafers by the electrostatic force and remain there during the processing of the semiconductor wafer which will result in defects on the surface of the wafers.

Retention of particles by electrostatic force is erratic since a sudden electrostatic discharge may remove the electrostatic force. The particles released from the inner walls of the equipment may be transported to the surface of a semiconductor wafer and cause defects. Thus it is desirable to eliminate the electrostatic force between particles and the inner walls of the semiconductor manufacturing equipment, so the gas purge flow can remove

the retained particles from the inner surfaces of the equipment.

It takes a large amount of energy to release the particles that are retained on the inner surfaces by molecular force. Therefore particles that are retained by the molecular force on the inner surfaces of the equipment are very likely to stay there indefinitely and not cause any defects on semiconductor wafers.

Capillary force is reduced by the reduction of moisture in the equipment. The moisture is reduced by use of construction materials with low moisture permeability and the use of a particle and moisture free gas flow through the equipment. A dry particle-free gas purge such as dry nitrogen evaporates moisture and purges particles that are only being retained by the capillary force on the inner surfaces of the equipment.

U.S. Patent Number 5,373,806 to Logar (Logar) is an example of an attempt to solve the problem of retained particles. In Logar, electrostatic charges are reduced by heating the substrate to a specific temperature lower than the processing temperature prior to production deposition by the use of a radiant source of energy. This is an extra step that must be taken in the manufacturing process, increasing production time and cost.

Typically particles are removed from the inner surface of the wafer handling chamber and the load locks by purging the wafer handling chamber with a particle-free gas. The semiconductor wafers are transported through the wafer handling chamber and load locks. A laminar flow of gas is provided so that particles can be picked up and carried with the purge gas through an exhaust outlet located within the wafer handling chamber and load locks. However, when a sudden pressure or flow change occurs, the gas flow becomes turbulent, causing particles to be stirred up and

transported to the surface of any semiconductor wafer that happen to be in the wafer handling chamber.

Existing systems used to regulate the pressure inside the semiconductor manufacturing equipment often employ the use of a single stage back pressure regulator that is located between a processing chamber and an exhaust outlet. However, the single stage back pressure regulator has difficulty regulating pressure for a large flow of gas.

Another problem with the existing system occurs when a gate valve that isolates the wafer handling chamber from the load lock or processing chamber is opened. If there is a pressure difference between the two chamber, the gas flow in one chamber is diverted to the second chamber, which results in turbulence within the both chambers. Because the single stage back pressure regulators do not completely open, particles, vapors and gases back stream from the exhaust outlet into both chambers.

Thus, it would be a distinct advantage to have an apparatus and method for reducing particles in a epitaxial reactor during the processing of semiconductor wafers. It is an object of the present invention to provide such an apparatus and method.

SUMMARY OF THE INVENTION

A method and apparatus for reducing particles in an epitaxial reactor used in processing of semiconductor wafers and includes an enclosure for processing the semiconductor wafers. A purge gas delivery system removes undesirable particles from the enclosure. Included in the system is a pilot operated back pressure regulator for regulating the exhaust of the purge gas from the enclosure. The system also includes an ionizing source for conditioning the purge gas that is integrally connected to the purge gas delivery system.

The pilot operated back pressure regulator includes a dome regulator for adjusting purge gas flow, a valve for

actuating the dome regulator, and a pressure regulator for delivering the pilot gas to the dome regulator.

The enclosure has a wafer handling chamber and a processing chamber. A robotic arm located within the wafer handling chamber has a Bernoulli wand end affecter that lifts and transporting the semiconductor wafers between the wafer handling chamber and processing chamber. There is included a damper mechanism for dampening the pressure rise when the Bernoulli wand releases a wafer either into a wafer cassette or on to a wafer scepter located within the processing chamber.

The wafer handling chamber is connected by an isolating gate valve to the processing chamber. The isolating gate valve is opened and closed according to a procedure that reduces the disturbances when there is a pressure difference between the wafer handling chamber and the processing chamber.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a diagram of the semiconductor manufacturing equipment, showing gas purge lines that are associated with the load locks and the wafer handling chamber according to the teachings of the present invention;

Figure 2 is a perspective view of the semiconductor manufacturing equipment illustrating the load locks, the wafer handling chamber and an epitaxial reactor;

Figure 3 is a schematic of an isolation valve assembly in the preferred embodiment of the present invention;

Figure 4 is a schematic diagram illustrating the dome loaded regulator circuit in a preferred embodiment of the present invention;

Figure 5 is a schematic diagram of the pilot operated back pressure regulator in the preferred embodiment of the present invention; and,

Figure 6 is a cross sectional side view of the pilot operated back pressure regulator in the preferred embodiment of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS

Referring to figures 1 and 2 wherein figure 1 includes a diagram of a piece of semiconductor manufacturing equipment (an epitaxial reactor 10), illustrating a gas purge system 12 that is associated with a wafer transport chamber that includes load locks 14 and 15, and a wafer handling chamber 16. The epitaxial reactor 10 is partitioned into the wafer handling chamber 16, load locks 14 and 15, and a process chamber 20 that is isolated from the load locks 14 and 15 and the wafer handling chamber 16 by isolation gate valve 18.

Prior to processing any semiconductor wafers, the load locks 14 and 15 and wafer handling chamber 16 are purged by purge gas from the gas source 22 that includes a control system. This purge gas flows from the source 22 through the pipes 24 and 26 into the load locks 14 and 15 and wafer handling chamber 16.

In operation, cassettes of semiconductor wafers (not shown) are placed in the load locks 14 and 15 through load lock portals 32 and 34. After loading the wafer cassettes in the load locks 14 and 15, the load lock portals 32 and 34 are closed to isolate the wafers from the surrounding atmosphere. The load locks are purged by the purge gas from the gas source 22. The purge gas such as dry nitrogen flows through the pipes 24 into the load locks 14 and 15. The purge gas purges out oxygen, moisture and undesirable particles that enters the load locks 14 and 15 when the load lock portals 32 and 34 are opened to receive the wafer cassettes.

After completing the purge, the load locks 14 and 15 are opened to the wafer handling chamber by the lowering of the cassette by an elevator 8 which breaks the air tight

seal typically located at edge 6, and the wafers are transported sequentially from the cassettes to the process chamber 20 by a transfer arm 29 that has a Bernoulli wan 36 end affecter. While the wafers are transported through the wafer handling chamber 16, the wafer handling chamber 16 is purged by a gas from the gas source 22.

The purge gas from the gas source is made slightly conductive by passing it through ionizer 21a which is connected to load lock 14, ionizer 21b which is connected to load lock 15, ionizer 21c which is connected to the wafer handling chamber 16 and ionizer 21d which is connected to the Bernoulli wand 36 by a flexible tube 30 that is connected to the robotic arm 29. In the embodiment shown, the gas is the same as the purge gas. The ionizers 21a, 21b, 21c, and 21d reduces or removes electrostatic forces from inside the epitaxial reactor 10. The slightly conductive purge gas can discharge any particles from the wafers or inner surfaces of the chamber subject to the purge.

The ionizers may be devices such as Model 2201 ss (alpha particle ionizer manufactured by NRD, Inc. of Grand Island, New York or preferably an electronic ionizer, such as the model 4210 manufactured by Ion Systems of Berkeley, California.

The purge gas flows, under pressure, through the ionizers 21a, 21b, 22c, and 21d. The flow rate of the nitrogen purge gas is measured at 15 standard liters per minute (slm), as a Low Flow rate and at 50 slm per minute as a High Flow rate. The flow rate is dependent on the volume of chambers and is selected to be as high as possible without creating turbulence.

A flow rate of 15 slm is common because a higher rate of flow causes turbulence and may stir up and drive particles into suspension with the purge gas. A High Flow rate is only used during maintenance mode when there are no

wafers in the epitaxial reactor 10, because it stirs up particles and facilitates the cleaning of the equipment. However, when the purge gas is slightly conductive, any static in the equipment is reduced or eliminated so that the particles are not attracted to surfaces by electrostatic force, such as the semiconductor wafers (not shown).

Preferably, the ionizers 21a, 21 b, 21c and 21d, to maximize their effectiveness, are located as close to the load locks 14 and 15 and the wafer handling chamber 16 as possible. Additionally, there should be no bends in the piping that connects the ionizers 21a 21 b, 21c and 21d to the load locks 14 and 15 and the wafer handling chamber 16.

Subsequent to the purging of the load locks 14 and 15 and wafer handling chamber 16, the isolation valve 18 is opened. The transfer arm 29 is used to move the wafers from the load lock 14 or 15 into the process chamber 20 for wafer processing. The transfer arm 29, including a low ingestion Bernoulli wand 36, is within the wafer handling chamber 16. In operation, the Bernoulli wand 36 picks up the semiconductor wafers one at a time from the cassettes (not shown) in one of the load locks 14 and 15. Each wafer is then transported through an open isolation gate valve 18 to a susceptor 38 within the process chamber 20. The Bernoulli wand 36 is used to reduce particle accumulation within the epitaxial reactor 10 by avoiding contact with the top and bottom surfaces of the wafers. The Bernoulli wand 36 utilizes a novel non-spiking gas system and uses nitrogen gas, through wand gas supply line 28. However, when the Bernoulli wand 36 picks up a wafer and releases it onto the susceptor 38 in the process chamber 20, the resulting impulse of gas released into the wafer handling chamber 16 causes a pressure spike and a resulting turbulence of gas in the wafer handling chamber 16. Any turbulence causes particles that are present within the

wafer handling chamber 16 to be disturbed and lifted into suspension in the purging gas. The particles thus can be transported to a wafer surface, however the presence of a damper 44 that dampers the pressure spikes generated from the operation of the Bernoulli wand 36 and prevents the generating of a pressure spike and the resulting turbulence.

When using a Bernoulli wand 36, the gas flow is turned off to drop a wafer at its destination, the remaining gas is vented into the wafer handling chamber 16. This sudden burst of gas flow causes a sudden pressure rise. In order to render the gas flow constant, the damper 44 and orifice 46 is utilized to reduce the pressure spike in the wafer handling chamber 16. When a wafer is released, the dome regulator 90 is shut off and, simultaneously, valve 95 is opened to release the remaining gas flow into the damper 44 and flow resisting orifice 46. When the size of the damper 44 and the size of the orifice 46 are properly sized, the gas flow increase is gradually released into the wafer handling chamber 16 to compensate for the sudden burst. The orifice 46 is sized to provide a tuning mechanism for regulating pressure bursts into the wafer handling chamber 16.

The damper 44 and orifice 46 is used in conjunction with the back pressure regulator 40 that is located in the exhaust line 42 that is connected to the wafer handling chamber 16. The back pressure regulator 40 maintains a constant pressure in the wafer handling chamber 16 and the load locks 14 and 15. When the elevator 8 is sealently pressed against the edge 6, the valve 41 is opened so that the gas load locks 14 and 15 can be vented.

Another area in which the gas flow is disturbed occurs when the isolation gate valve 18 is suddenly opened or closed when transporting wafers between the wafer handling chamber 16 and the process chamber 20. In order to minimize

this gas flow disturbance, the isolation gate valve includes a valve assembly 80 that is constructed to allow the isolation gate valve 18 to open only a minute amount to allow the pressure to equalize between the wafer handling chamber 16 and the process chamber 20. Figure 3 is a schematic of the isolation gate valve assembly 80. Once the pressure is equalized between the wafer handling chamber 16 and the process chamber 20, the isolation gate valve 18 continues to open at a fast rate. This results in a minimum disturbance in pressure and gas flow while still allowing fast actuation of the isolation gate valve 18.

The isolation gate valve assembly 80 includes an actuator 82 which is mechanically connected with the isolation gate valve 18, enabling the isolation gate valve 18 to open. Additionally, the isolation gate valve 18 is mechanically connected with a second actuator 84, that actuates the initial opening of the isolation gate valve 18 in a controlled way, allowing the equalization of pressure between the wafer handling chamber 16 and the process chamber 20. The actuator 84 also may control the final closing of the isolation gate valve in a controlled manner. This isolation gate valve assembly 80 provides a multi-speed isolation gate valve, which can reduce or eliminate gas flow bursts which occur in the initial stage of prior art isolation gate valves.

After each wafer is processed, the isolation gate valve 18 is opened and the Bernoulli wand 36 retrieves the processed wafer and loads the wafer into a cassette within one of the load locks (14 or 15). After all of the wafers have been processed, the cassette located within the load lock is removed through one of the portals (32 or 34).

Disturbance of the flow and pressure of the purge gas may also occur during the sudden opening or closing of gas valves which feeds gas into the semiconductor manufacturing equipment. A dome loaded regulator circuit 90 is utilized

to feed gas into the semiconductor manufacturing equipment. Figure 4 is a schematic diagram illustrating the dome loaded regulator circuit 90 and includes a dome loaded regulator 92, a valve 94, a pressure regulator 96 and a needle valve 98. The gas flow into the equipment is increased incrementally by the dome loaded regulator 92 which is pneumatically actuated by the valve 94, which controls a restricted gas flow. The gas flow originates from the pressure regulator 96. In addition, the needle valve 98 controls the amount of restriction of the gas flow. However, the needle valve 98 may be a plurality of needle valves and check valves, to regulate different ramp-up and ramp-down flow rates of the purge gas.

Figure 5 is a schematic diagram of the pilot operated back pressure regulator 40 in the preferred embodiment of the present invention. The pilot operated back pressure regulator 40 includes a pneumatically actuated throttle valve 50 which is actuated by a pressure relay system 52. The pressure relay system 52 is normally a 22:1 ratio pressure relay that adjusts the opening of the pneumatically actuated throttle valve 50 from the sensed pressure across the throttle valve 50 and conduits 101 and 102. The pilot operated back pressure regulator 40 also includes a variable load springs 54 and a throttle valve actuator 56. Additionally, the pilot operated back pressure regulator 40 includes a throttle valve input 58.

Figure 6 is a cross sectional side view of the pilot operated back pressure regulator 40 in the preferred embodiment of the present invention. Referring to Figure 6, the operation of the pilot operated back pressure regulator 40 will now be explained. In order to regulate the pressure within the wafer handling chamber 16, the pilot operated back pressure regulator 40 uses the pneumatically actuated throttle valve 50 to regulated the pressure. The pilot operated back pressure regulator 40

includes the pressure relay system 52, which is a 22:1 pressure relay in the preferred embodiment, and the pneumatically actuated throttle valve 50. The pressure relay system 52 includes a large piston 58 which drives a small pressure reducing regulator 60. A high pressure pilot supply (80 PSI in the preferred embodiment), is feed in through a passage 62. The variable load spring 54 opens the small pressure regulator 60. The opening of the small pressure regulator 60 allows a dynamic flow from a chamber 64 to enter a chamber 68 via a passage 66. The dynamic flow then flows through a bleed passage 70 to a passage 72. From the passage 72, the dynamic flow is exhausted through an output 74 of the pilot operated back pressure regulator 40. This dynamic flow creates a bias pressure on the throttle valve actuator 56 at a level just below the pressure required to drive the throttle valve 50 open. The size of the bleed passage 70, chamber 68, and a chamber 57 determines the response time and pressure differential necessary to drive the throttle valve 50 open. The smaller the bleed passage 70 and chamber 57, the faster the response of the pilot operated back pressure regulator 40. A small increase in pressure at an input 76 for the pilot operated back pressure regulator 40 is transmitted, via a channel 78, to the top of the large piston 58 through the passage 66 driving the small regulator 60 to a higher pressure that is multiplied by the ratio of the pressure relay. This increases the pressure at the top of throttle valve actuator 56 and drives the throttle valve 50 open, relieving the pressure at the input 76 of the pilot operated back pressure regulator 40 and thereby regulating the pressure at the throttle valve input 58.

CLAIMS

WHAT IS CLAIMED IS:

1. An apparatus for processing semiconductor wafers comprising: a reactor chamber for processing the semiconductor wafers; a wafer transport chamber having a transport means for unloading and loading semiconductor wafers from and to the reactor chamber; a gas delivery system operatively connected to deliver gas to the wafer transport chamber; and an ionization means for conditioning the gas prior to delivery to the wafer transport chamber.

2. The apparatus of Claim 1 wherein the wafer transport chamber includes a gas outlet and the apparatus further comprises: a pilot operated back pressure regulator connected to the gas outlet for regulating the gas in the wafer transport chamber.

3. The apparatus of Claim 2 wherein the pilot operated back pressure regulator includes: a pneumatically driven throttle valve having an adjustable valve opening, the valve opening being connected to the outlet; and a pressure sensing relay system connected to sense the pressure across the pneumatically driven throttle valve and to adjust the adjustable valve opening in response to the sensed pressure.

4. The apparatus of Claim 2 wherein the ionization means includes a first ionizer connected to the transport means and a first line connecting the first ionizer to the gas delivery system, the apparatus further comprising: a dome loaded regulator integrally connected in the first line and the delivery system for regulating the delivery of gas to the first ionizer.

5. The apparatus according to Claim 4 wherein the ionization means includes a second ionizer connected to the wafer transport chamber and a second line connecting the gas delivery system to the second ionizer further comprising: a damper connected in line with the gas delivery system; and a gas flow restricting means located between the damper and the second ionizer.

6. The apparatus according to Claim 5 further comprising: an isolation valve located between the reactor chamber and the wafer transport chamber; and means for controlling opening of the isolation valve at, at least a first speed followed by a second speed.

7. The apparatus according to Claim 1 further comprising: an isolation valve located between the reactor chamber and the wafer transport chamber; and means for controlling opening of the isolation valve at, at least a first speed followed by a second speed.

8. The apparatus of Claim 1 wherein the ionization means includes a first ionizer connected to the transport system means and a first line connecting the first ionizer to the gas delivery system, the apparatus further comprising: a dome loaded regulator integrally connected to the gas delivery system in the first line for regulating the delivery of gas to the first ionizer.

9. The apparatus according to Claim 1 wherein the ionization means includes a second ionizer connected to the wafer transport chamber and a second line connecting the gas delivery system to the second ionizer further comprising: a damper connected in line with the gas delivery system in the first line; and a gas flow

restricting means located between the damper and the first ionizer.

10. An apparatus for processing semiconductor wafers, comprising: a reactor chamber for processing semiconductor wafers; a wafer transport chamber having a gas outlet and means for unloading and loading semiconductor wafers from and to the reactor chamber; a gas delivery system operatively connected to deliver gas to the wafer transport chamber; and a pilot operated back pressure regulator connected to the gas outlet for regulating the gas in the wafer transport chamber.

11. The apparatus of Claim 10 wherein the pilot operated back pressure regulator includes: a pneumatically driven throttle valve having an adjustable valve opening and the valve opening being connected to the outlet and a pressure sensing relay system connected to sense the pressure across the pneumatically driven throttle valve and to adjust the adjustable valve opening in response to the sensed pressure.

12. The apparatus of Claim 10 wherein the gas delivery system includes at least a gas source and a first line connecting the gas source to the wafer transport chamber, the apparatus further comprising: a dome loaded regulator integrally connected to the gas delivery system in the first line for regulating the delivery of gas to the wafer transport chamber.

13. The apparatus according to Claim 12 wherein the gas delivery system further includes a second line connecting the gas source to the wafer transport system, the apparatus further comprising: a damper connected in line with the gas delivery system in the second line; and a gas flow

restricting means located in line between the damper and the wafer transport chamber.

14. The apparatus according to Claim 12 further comprising: an isolation valve located between the reactor chamber and the wafer transport chamber; and means for controlling opening of the isolation valve at, at least a first speed followed by a second speed.

15. The apparatus according to Claim 10 wherein the gas delivery system includes at least a gas source and a first line connecting the gas source to the wafer transport chamber, the apparatus further comprising: a damper connected in line with the gas delivery system in the first line; and a gas flow restricting means located in line between the damper and the wafer transport chamber.

16. The apparatus according to claim 10 further comprising: an isolation valve located between the reactor chamber and the wafer transport chamber; and means for controlling opening of the isolation valve at, at least a first speed followed by a second speed.

17. An apparatus for processing semiconductor wafers comprising: a reactor chamber for processing semiconductor wafers; a wafer transport chamber having a means for unloading and loading semiconductor wafers from and to the reactor chamber; a gas delivery system operatively connected to the wafer transport chamber; and a dome loaded regulator integrally connected by a first line to the gas delivery system in the first line for controlling the delivery of gas into the wafer transport enclosure.

18. The apparatus of Claim 17 wherein the gas delivery system further includes a second line connecting the gas source to the wafer transport system, the apparatus further comprising: a damper connected in line with the gas delivery system in the second line and a gas flow restricting means located between the damper and the wafer transport chamber.

19. The apparatus according to Claim 18 further comprising: an isolation valve located between the reactor chamber and the wafer transport chamber; and means for controlling opening of the isolation valve at least a first speed followed by a second speed.

20. The apparatus according to Claim 17 further comprising: an isolation valve located between the reactor chamber and the wafer transport chamber; and means for controlling opening of the isolation valve at least a first speed followed by a second speed.

21. An apparatus for processing semiconductor wafers comprising: a reactor chamber for processing semiconductor wafers; a wafer transport chamber having means for unloading and loading semiconductor wafers from and to the reactor chamber; a gas delivery system operatively connected to deliver gas to the wafer transport chamber; a damper connected to the gas delivery system; and a gas flow restricting means located between the damper and the wafer transport enclosure.

22. The apparatus according to Claim 21 further comprising: an isolation valve located between the reactor chamber and the wafer transport chamber; and means for controlling opening of the isolation valve at, at least a first speed followed by a second speed.

23. An apparatus for processing semiconductor wafers comprising: a reactor chamber for processing semiconductor wafers; a wafer transport chamber having a means for unloading and loading semiconductor wafers from and to the reactor chamber; an isolation valve located between the reactor chamber and the wafer transport chamber; and means for controlling opening of the insolation valve at, at least a first speed followed by a second speed.

24. An apparatus for processing semiconductor wafers comprising: a load lock chamber; a reactor chamber for processing semiconductor wafers; a wafer transport chamber connected between the load lock chamber and the reactor chamber and having a means for transferring semiconductor wafers between the reactor chamber and the load lock chamber; an isolation valve located between the load lock chamber and the wafer transport chamber; and means for controlling opening of the insolation valve at, at least a first speed followed by a second speed.

25. A method of processing semiconductor wafers in a semiconductor reactor having a wafer transport chamber and a reactor chamber the method comprising the steps of: reducing particles in the wafer handling chamber including the steps of; delivering a gas to the wafer handling chamber, and conditioning the gas with an ionizing means.

26. The method according to Claim 25 wherein the wafer transport chamber includes a gas outlet and the step of reducing particles further comprises: the step of regulating the gas pressure in the wafer transport chamber with a pilot operated back pressure regulator operatively connected to the gas outlet.

27. The method according to Claim 26 wherein the wafer transport chamber includes a transport means connected to the gas delivery system by a first line and in a first ionizer in the first line, the method further comprising the steps of: regulating the delivery of the gas to the ionization means with a dome loaded regulator.

28. The method according to Claim 27 wherein the ionization means includes a second ionizer connected to the wafer transport chamber by a second line, the method further comprising the steps of: in line dampening the delivery of the gas to the second ionizer means and restricting the flow of gas to the second ionizer means.

29. The method according to Claim 28 wherein the semiconductor equipment further includes an isolation valve located between the reactor chamber and the wafer transport chamber and the method of reducing particles further includes the steps of : initially opening the isolation valve at a first speed followed by a second speed.

30. The method according to Claim 25 wherein the wafer transport chamber includes a transport means connected to the gas delivery system by a first line and a first ionizer in the first line, the method further comprising the steps of: regulating the delivery of the gas to the first ionizer with a dome loaded regulator.

31. The method according to Claim 25 wherein the ionization means includes a first ionizer connected to the wafer transport chamber by a first line, the method further comprising the steps of: in line dampering the delivery of the gas to the first ionizer and restricting the flow of gas to the first ionizer.

32. The method according to Claim 25 wherein the semiconductor equipment further includes an isolation valve located between the reactor chamber and the wafer transport chamber and the method of reducing particles further includes the steps of : initially opening the isolation valve at a first speed followed by a second speed.

33. A method of processing semiconductor wafers in a semiconductor reactor having a wafer transport chamber having a gas outlet and a reactor chamber, the method comprising the steps of: reducing particles in the wafer handling chamber including the steps of; delivering a gas to the wafer handling chamber, and regulating the gas pressure in the wafer transport chamber with a pilot operated back pressure regulator operatively connected to the gas outlet.

34. The method according to Claim 33 wherein the gas delivery system includes at least a gas source and a first line connecting the gas source to the wafer transport chamber, the method further comprising the steps of: regulating the delivery of the gas to the wafer transport chamber in the first line with a dome loaded regulator.

35. The method according to Claim 33 wherein the gas delivery system further includes a second line connecting the gas source to the wafer transport system, the method further comprising the steps of; in the second line, dampering the delivery of the gas to the wafer transport chamber means and restricting the flow of gas to the wafer transport chamber.

36. The method according to Claim 35 wherein the semiconductor equipment further includes an isolation valve located between the reactor chamber and the wafer transport chamber and the method of reducing particles further includes the steps of: initially opening the isolation valve at a first speed followed by a second speed.

37. The method according to Claim 33 wherein the semiconductor equipment further includes an isolation valve located between the reactor chamber and the wafer transport chamber and the method of reducing particles further includes the steps of : initially opening the isolation valve at a first speed followed by a second speed.

38. A method of processing semiconductor wafers in a semiconductor reactor having a wafer transport chamber and a reactor chamber, the method comprising the steps of: reducing particles in the wafer handling chamber including the steps of; delivering a gas to the wafer handling chamber, and regulating the delivery of the gas to the wafer transport chamber with a dome loaded regulator.

39. The method according to Claim 38 wherein the gas delivery system includes at least a gas source and a first line connecting the gas source to the wafer transport system chamber, the method further comprising the steps of; in the first line: dampering the delivery of the gas to the wafer transport chamber means and restricting the flow of gas to the wafer transport chamber.

40. The method according to Claim 38 wherein the semiconductor equipment further includes an isolation valve located between the reactor chamber and the wafer transport chamber and the method of reducing particles further includes the steps of: initially opening the isolation valve at a first speed followed by a second speed.

41. A method of processing semiconductor wafers in a semiconductor reactor having a wafer transport chamber having a gas outlet and a reactor chamber, the method comprising the steps of: reducing particles in the wafer handling chamber including the steps of; delivering a gas to the wafer handling chamber, and in line dampering the delivery of the gas to the wafer transport chamber means and restricting the flow of gas to the wafer transport chamber.

42. The method according to claim 41 wherein the semiconductor equipment further includes an isolation valve located between the reactor chamber and the wafer transport chamber and the method of reducing particles further includes the steps of: initially opening the isolation valve at a first speed followed by a second speed.

43. A method of processing semiconductor wafers in a semiconductor reactor having a wafer transport chamber having a gas outlet and a reactor chamber, and an isolation valve located between the reactor chamber and the wafer transport chamber, the method comprising the steps of: reducing particles in the wafer handling chamber including the steps of; delivering a gas to the wafer handling chamber, and initially opening the isolation valve at a first speed followed by a second speed.

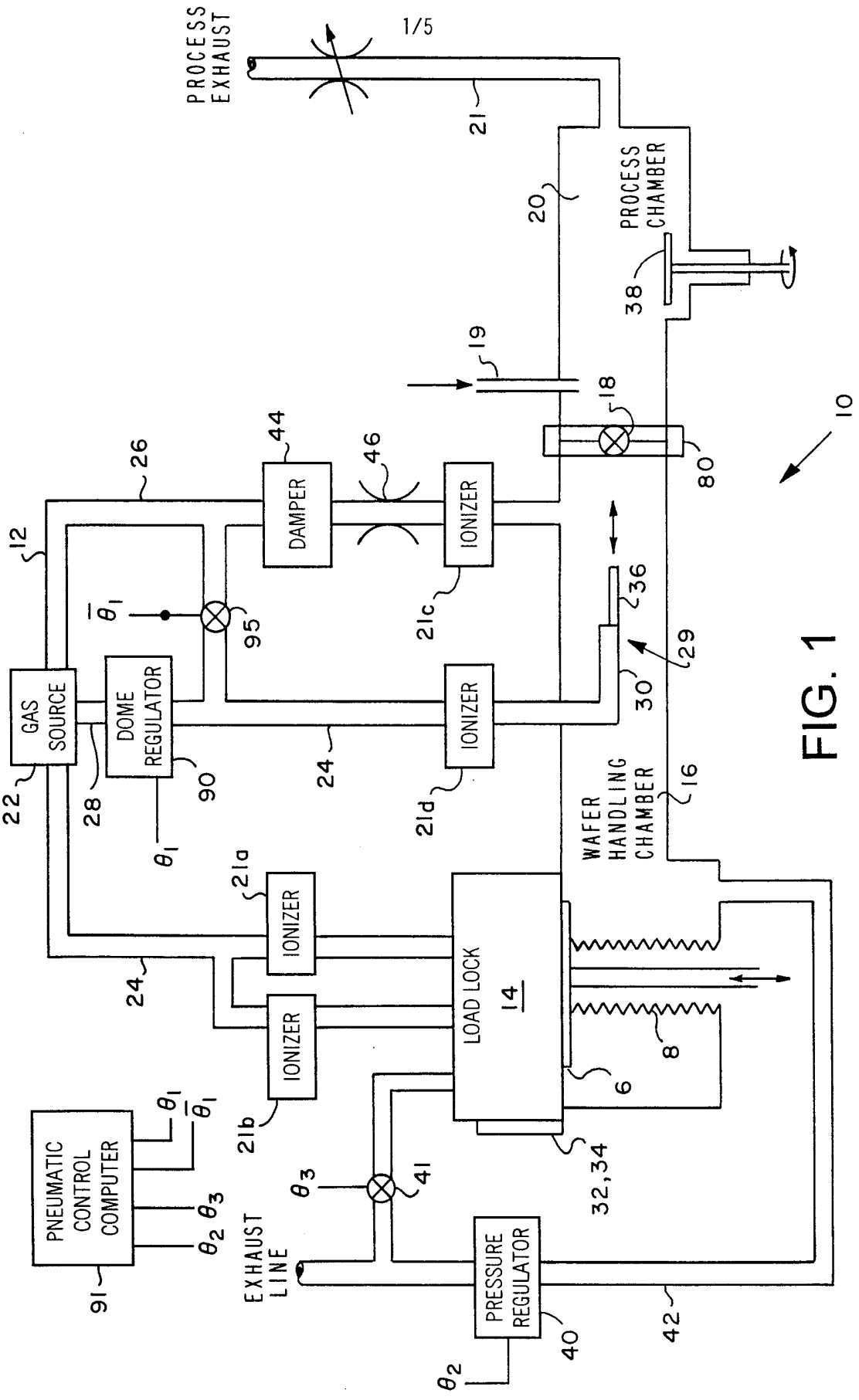

PROCESS EXHAUST
1/5
21
20
PROCESS CHAMBER
38
19
18
80
10
44
46
DAMPER
IONIZER
26
12
$\bar{\theta}_1$
95
21c
36
29
30
GAS SOURCE
DOME REGULATOR
IONIZER
22
28
90
24
21d
WAFER HANDLING CHAMBER
16
θ_1
21a
IONIZER
LOAD LOCK 14
24
IONIZER
8
6
21b
θ_1
$\bar{\theta}_1$
θ_3
41
32,34
PNEUMATIC CONTROL COMPUTER
θ_2 θ_3
EXHAUST LINE
PRESSURE REGULATOR
91
40
42
θ_2

FIG. 1

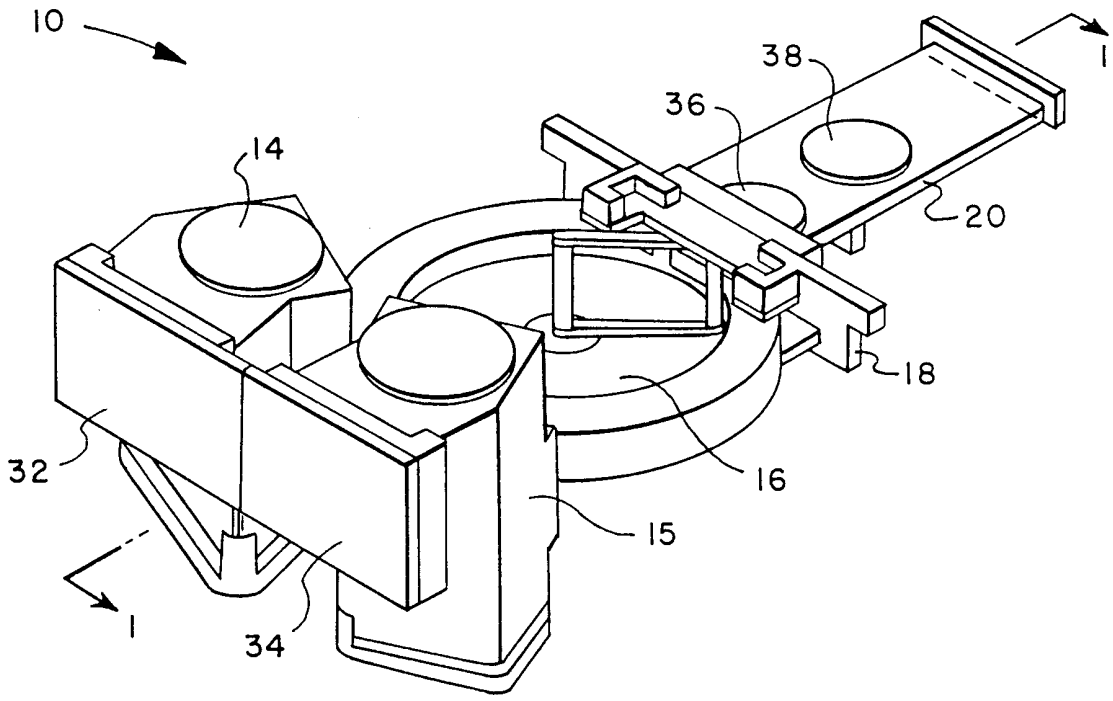


FIG. 2

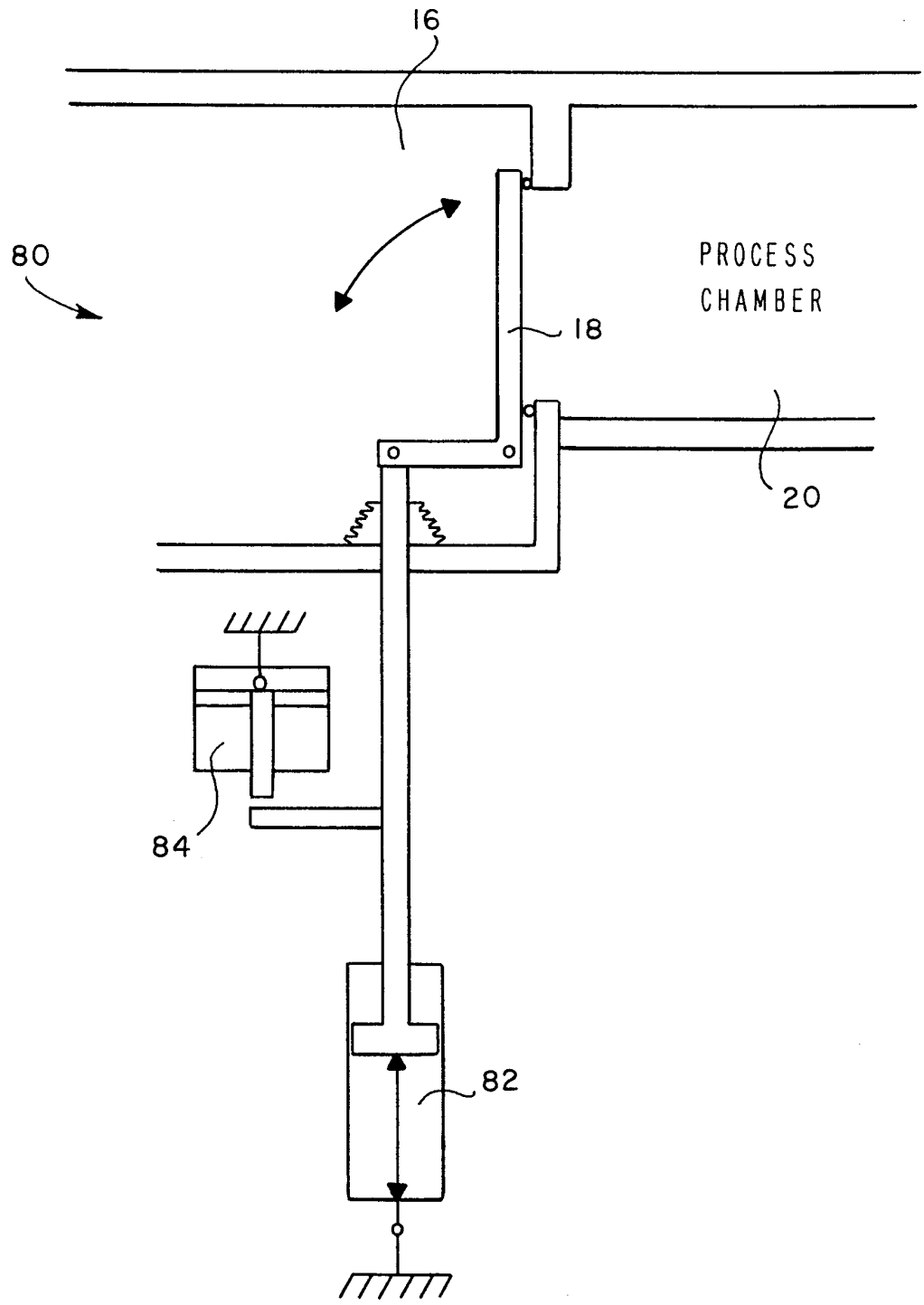


FIG. 3

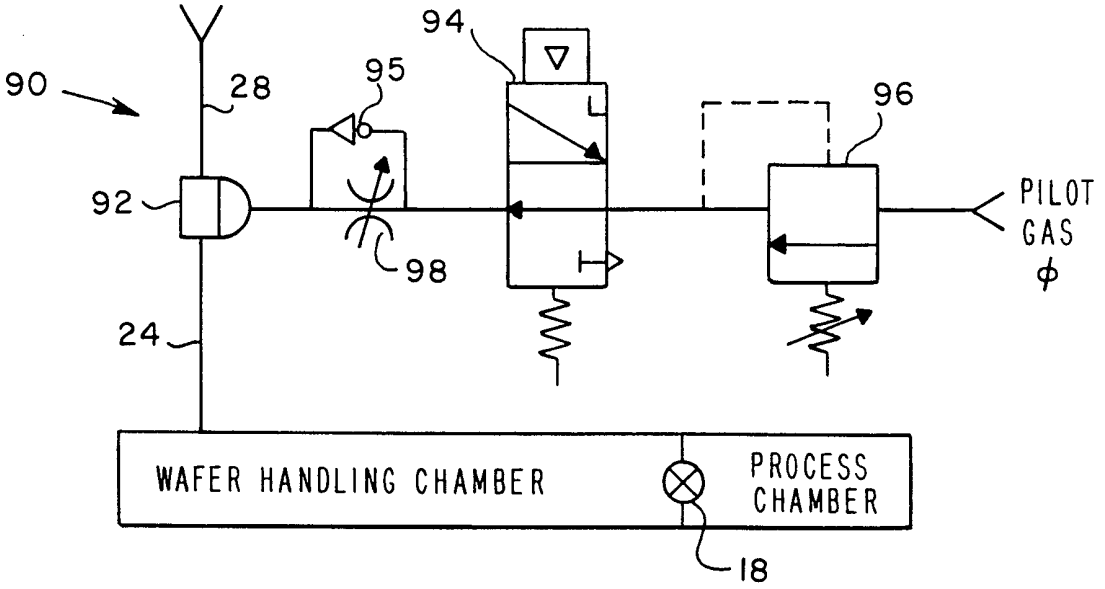

90
28
95
94
96
92
98
PILOT
GAS
24
WAFER HANDLING CHAMBER
PROCESS
CHAMBER
18

FIG. 4

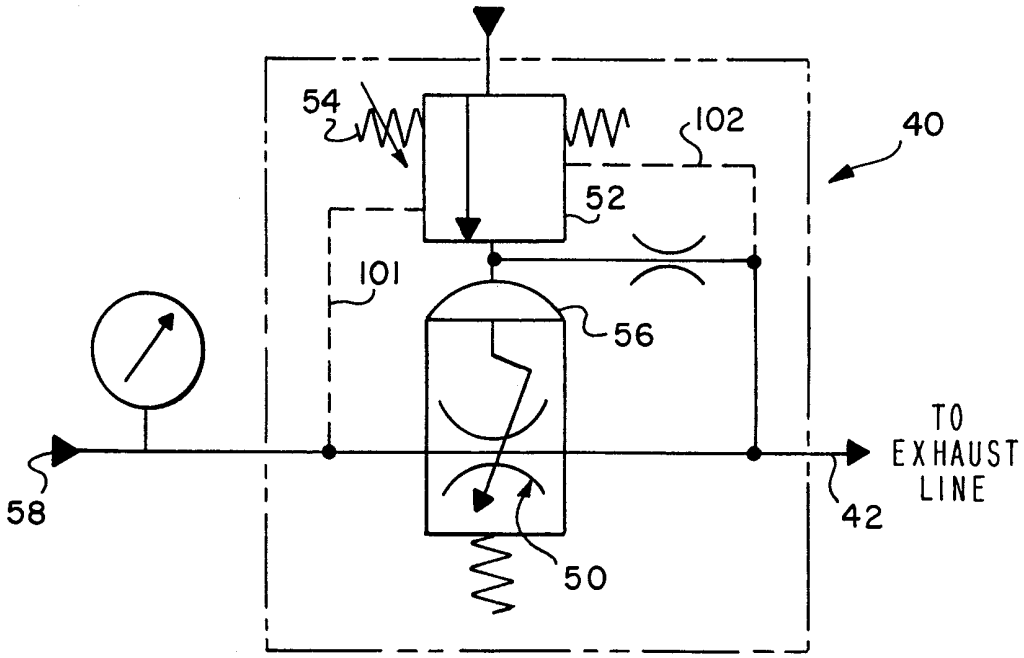

54
102
40
52
101
56
TO
EXHAUST
LINE
58
42
50

FIG. 5

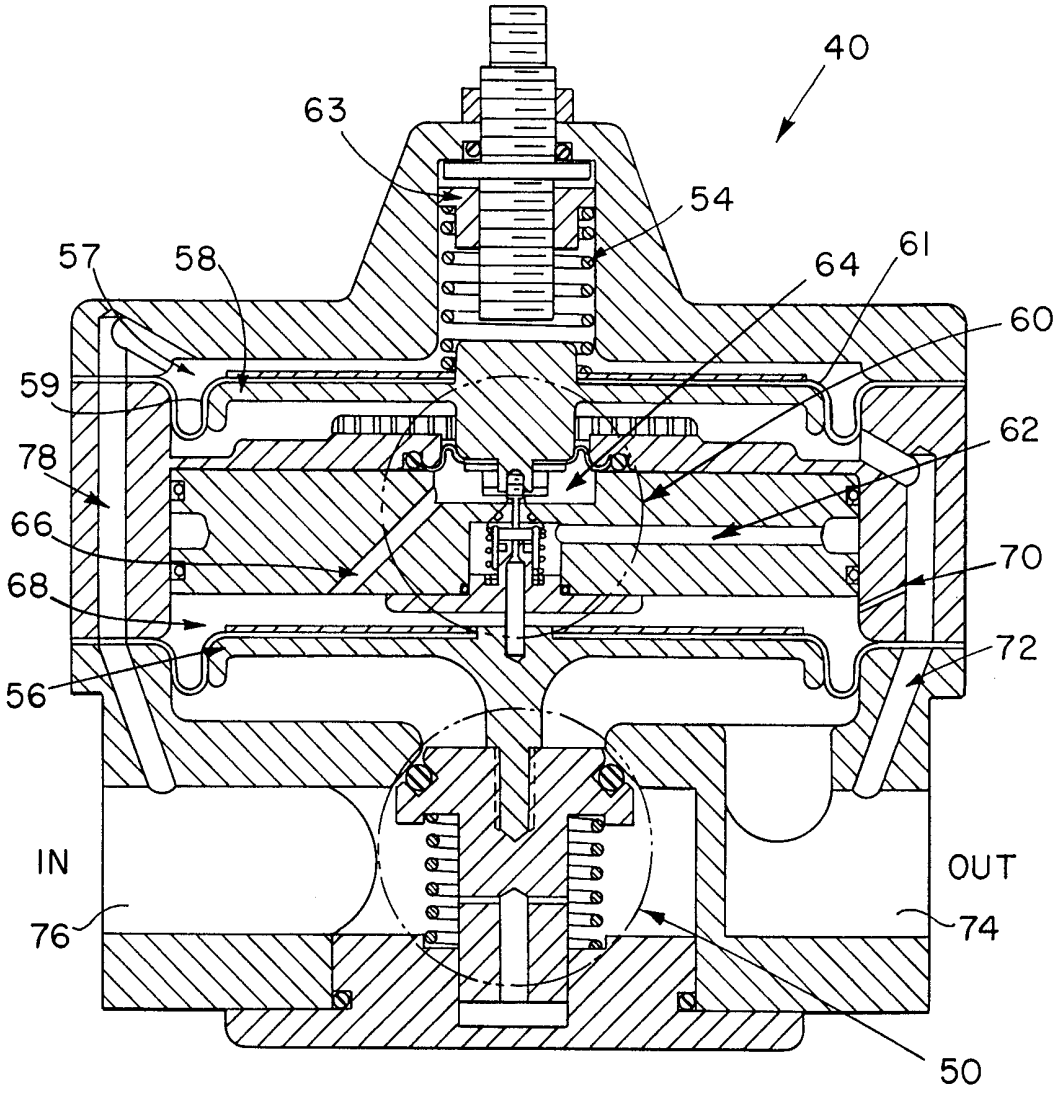


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/15070

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :C23C 16/00; C30B 23/06.
US CL :118/715, 723IR, 723ME, 725; 117/106.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 118/715, 723IR, 723ME, 725; 117/106.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,366,557 A (YU) 22 November 1994, see entire document.	1-43
A	US 5,373,806 A (LOGAR) 20 December 1994, see entire document.	1-43

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
28 SEPTEMBER 1999	21 OCT 1999
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer JEFFRIE R. LUND Telephone No. (703) 308-0661

Form PCT/ISA/210 (second sheet)(July 1992)★