Abstract Title: Reconfigurable system for processing digital data symbols

A data processing system 10 has a reconfigurable logic unit 11 and a storage unit 12-14. Data symbols are placed in the storage unit sequentially. One or more data symbols are processed by the logic unit. The logic unit is then reconfigured and the symbols are processed again. This may be repeated with more configurations to carry out more processing tasks. The storage unit may have two memory units 12,13 so that the symbols being processed may be read from one unit and written to the other. The system may be a digital radio receiver which carries out an FFT calculation in the first configuration and a PSK demodulation in the second configuration. In this case, the symbol is an OFDM symbol.

Fig. 2
Fig. 1

Fig. 2

Fig. 3
Reconfigurable Logic System

The present invention relates to a reconfigurable system architecture and particularly dynamic reconfiguration in a system where data is to be processed sequentially within a predetermined period. One such system is an Orthogonal Frequency Division Multiplex (OFDM) digital broadcasting system where processing is to be carried out within an OFDM symbol time but the invention can be adapted for use in any similar system.

The following will be described with reference to digital broadcasting systems. However it will be appreciated that the present invention can also be applied to other systems which operate on the same principles as digital broadcasting systems and in particular which utilise similar processing techniques as are used in digital broadcasting systems.

In digital broadcasting systems, the OFDM technique is used to modulate (at the transmitter) and demodulate (at the receiver) data. Demodulation is one part of the overall process used to determine information relating to modulated data which has been sent from a transmitter and received by a receiver on which the OFDM hardware is contained. The OFDM hardware is typically formed of a plurality of separate components connected appropriately on an integrated chip. In a typical DAB (Digital Audio Broadcasting) receiver such components include an FFT and DQPSK demodulator. Other standards such as DVB (Digital Video Broadcasting) may use another type of phase shift keying but in common with DAB utilises an FFT.

There is always a desirability for integrated chip (IC) manufacturers to reduce the physical size of the IC as this reduces costs and improves efficiency. The present invention aims to achieve this by providing a reconfigurable logic module which can be configured to perform the functions of any of the conventional components.

The invention uses dynamic or run-time reconfiguration (RTR) which has the capability of reconfiguring logic resources at the run-time of an application. Using RTR, hardware resources can be provided as required. To address the potential overheads due to
additional hardware and reconfiguration time when using RTR, time-slicing in combination with memory management is used to efficiently handle the processing tasks within restricted symbol based period such as the OFDM symbol period.

A further requirement to enable such a module to be used in OFDM processing is that the processing should be completed on an OFDM symbol within the OFDM symbol period.

By reducing the number of active chip elements, this also reduces power consumption which is particularly advantageous for portable (battery-powered) devices.

In order that the present invention be more readily understood, an embodiment thereof will be described with reference to the accompanying drawing in which:

Fig. 1 is a simplified schematic block diagram showing a portion of a conventional DAB receiver;

Fig. 2 is a simplified schematic block diagram showing a portion of a DAB receiver according to one embodiment of the present invention;

Fig. 3 shows a schematic block diagram of the reconfigurable module shown in Fig. 2;

Fig. 4 is a process diagram showing the processing performed with respect to time on a symbol input into reconfigurable module of Fig. 2 and 3, and a schematic diagram showing the interaction between the reconfigurable unit and various memory units of the reconfigurable module of Fig. 2 and 3.

An embodiment will be described in relation to transmission mode 1 of the DAB standard and the implementation of the invention for this mode. However, the invention is not restricted for such use and can be adapted for use in other DAB transmission modes and other symbol based systems.
Fig. 1 shows certain components of a conventional DAB receiver. A signal is received by the DAB receiver 1 via an antenna (not shown).

The signal is in the form of a DAB frame which comprises a null symbol and a plurality of OFDM symbols. Such a frame is known in the art. In DAB transmission mode 1 frame there are 76 OFDM symbols each having a symbol period of 1.246 ms. At the beginning of each symbol is a guard interval of period 0.246 ms and following this is the effective symbol which has a period of 1 ms giving the total symbol period of each symbol as 1.246 ms.

The signal is processed in RF front-end 2, filtered and converted to an intermediate frequency or directly to baseband. An ADC (not shown) converts the resulting signal to a digital representation and digital front-end 3 processes the signal to generate a digital complex baseband signal. The components constituting the digital front-end 3 are known to the skilled person and will not be described in detail herein.

This baseband signal is OFDM demodulated by applying an FFT 4. Each carrier is then differentially demodulated using DQPSK 5 (differential demodulation) and deinterleaving is performed by deinterleaver 6. A Viterbi decoder 7 performs error correction on the resulting signal. Further processing is carried out and an audio signal is output by the receiver 1. The various steps carried out by the receiver are known in the art and will not be described in detail.

One embodiment of the invention is concerned with the FFT 4 and the DQPSK demodulator 5 and the manner in which the functionality of each of these components can be adapted so as to remove the need for two separate components and therefore save chip space and costs associated therewith.

With reference to Fig. 2 and 3, a reconfigurable module 10 is provided instead of the two components FFT 4 and DQPSK demodulator 5 shown in Fig. 1.

The module 10 comprises a reconfigurable logic unit 11. Such a unit can be any unit which can be reconfigured in a relatively short space of time and is preferably a hybrid
reconfigurable logic unit adapted to operate with a reconfiguration time which is significantly less than a symbol period of the OFDM symbol. Conventional programmable logic units (PLUs) could be theoretically used as long as their reconfiguration time is relatively short compared to the OFDM symbol period. The preferred configuration is achieved using a coarse grain unit which is configured at a logic block level (compared to a fine grain unit which reconfigures at a gate level). Such a unit allows rapid reconfiguration, yet is flexible enough to be reconfigured between different functions.

The module 10 further comprises a first memory unit 12, second memory unit 13 and a third memory unit 14. Each are arranged to communicate with the reconfigurable logic unit 11. Further the first and second memory unit 12, 13 are arranged to receive OFDM symbols sequentially from the digital front end 3 for processing by the logic unit 11 and output processed results for further processing by the receiver.

The third memory unit 14 can communicate with both the first and second memory unit 12,13 and temporarily store data therefrom. This memory 14 can also be read from by the logic unit 11.

Each of the memory units 12,13,14 are in the form of random access memory (RAM). In this embodiment, memory 12,13 are RAM of 2048x24 bits and memory 14 is DDRAM which is 1536x16 bits. This can differ to the RAM12,13 as long as it is capable of storing the minimum amount of data which can be usefully processed by the logic unit 11. Although the memory is shown as forming part of the module 10, it will be appreciated that the memory may already be on-board a conventional receiver and this could be adapted for use by the logic unit 11. Further, other types of memory may be utilised.

Figure 4 shows the sequence diagram of the various parts of the module 10 with respect to time and the corresponding interaction between the parts of the module 10 for five successive symbols, s-2 s-1, s, s+1, s+2, during three successive symbol periods Ts(i-1), Ts(i), Ts(i+1), where data for each symbol are input during one symbol
period, processed during the next symbol period, and output during the symbol period
after, when the logic unit 11 is in a first mode configuration and when in a second mode
configuration. As mentioned above, the reconfigurable resources could be shared
between two processing configurations and in this embodiment the first configuration is
FFT processing followed by a second configuration which is DQPSK processing, but
unlike the conventional arrangement, it is performed on the same silicon, with
reconfiguration taking place between the two configurations. It is also possible to
perform frequency de-interleaving (soft decision) at the same time as DQPSK since this
only requires different memory address mapping. For complete de-interleaving, time
de-interleaving is also required but this is performed outside the symbol time period.
Two RAMs 12,13 in a ping-pong arrangement are used during FFT processing, one for
serial I/O of samples from previous and to subsequent blocks, respectively, and the
other one as working memory for storing intermediate results between butterfly stages.
The other RAM 14 (DDRAM) is also required to store the samples of the previous
symbol for differential demodulation.

The following sequence occurs for processing one symbol s (refer to Fig. 4):

1. During symbol time Ts(i-1), 2N samples of symbol s are stored in the memory 12
   at the rate they are coming in. During this symbol time, symbol s-1 is processed
   on the reconfigurable logic unit 11.

2. At the beginning of symbol time Ts(i), the reconfigurable logic unit 11 is
   configured to perform the N-point FFT (the size depends on transmission mode
   (TM), e.g. 2048-point FFT for TM 1). Since all required samples were stored in
   the memory 12 (which is now the working memory) during the previous symbol
   time, the FFT can be performed as fast as possible, in only a fraction of the
   symbol time. The intermediate results of the various butterfly stages (e.g. six
   stages for TM 1), are stored in and read from the DDRAM 14.

3. When FFT processing is finished, the reconfigurable logic unit 11 is reconfigured
   with the DQPSK context, while the memory 12 contents remain unchanged. The
   DDRAM 14 contains the FFT results of the previous symbol. Reconfiguration is
   carried out in any appropriate manner such that information is conveyed to the
   reconfigurable logic unit 11 to define the required configuration.
(4) When the reconfiguration is completed, DQPSK commences. The FFT results, which are still located in the FFT working RAM 12, are the DQPSK inputs from the current symbol.

(5) The DQPSK inputs from the previous symbol are loaded from the DDRAM 14.

(6) At the same time, the respective samples of the current symbol are written to the DDRAM 14, as they will be needed for DQPSK processing of the following symbol.

(7) When the DQPSK (potentially including soft-decision) is completed, the results are written back to the FFT working memory 12, from where they can be used for further processing. Provided there are enough resources available for the DQPSK configuration, frequency deinterleaving could also be carried out at this point, that is, the soft-decision metrics could be written to different locations in the RAM according to the frequency deinterleaving look-up tables. These would make a separate RAM obsolete and hence save further resources.

(8) The reconfigurable logic unit 11 is reconfigured for the next context. This could be the FFT context for the next symbol, or, if there is time left during the current symbol period $T_s$, for further processing, such as Viterbi decoding.

(9) During symbol time $T_s(i-1)$, the soft-decision metrics corresponding to symbols are read from memory (now I/O RAM again) for further processing.

Although on the initial start up of the reconfigurable module 10, one RAM 12 is utilised for the first symbol received, both RAMS 12,13 swap functions on each symbol and are both active until the reconfigurable module 10 is switched off and processing is terminated.

Accordingly with the preferred embodiment, within one OFDM symbol period it is possible to perform OFDM for all samples, store the results, reconfigure the logic resources, process DQPSK while storing results in memory. Before the next symbol starts, the reconfigurable logic unit will need to be reconfigured back to its initial state.
It will be appreciated that various modifications exist to the preferred embodiment. For example, the invention is not limited for use in TM 1 of DAB but can be used in the other three modes which each have a relatively shorter symbol period than TM 1. In this case the reconfiguration of the reconfigurable logic unit need not occur after processing of every symbol but after a number of symbols.

Further, the invention can be adapted for use in other symbol based systems such as DVB and DRM where OFDM symbols are processed sequentially within a symbol period. DAB is based on DQPSK demodulation, which uses respective samples from two consecutive symbols to process the output. The reconfiguration set-up may be adapted for use with other demodulation methods. It is also possible to adapt the method for use in a digital transmitter as well as a receiver.

Although this embodiment refers to the use of a reconfigurable logic unit to perform the function of an FFT and DQPSK (and potentially soft decision), this is only an example of taking two processing blocks to share the same resources. Any set of processing blocks can be chosen as long as there is sufficient time to execute them sequentially and the memory required to temporarily store partial results of the overall processing is not inconveniently large.
Claims:

1. Reconfigurable system architecture for sequentially processing a plurality of digital data symbols comprising;
   a processing logic unit for performing a processing task, wherein the logic unit is reconfigurable between a plurality of logic configurations, each logic configuration representative of a different processing task;
   a storage unit for sequentially receiving a plurality of digital data symbols, each symbol having a first time duration, wherein the logic unit is arranged to be reconfigured between the plurality of logic configurations such that the processing task of each logic configuration is performed on at least one data symbol within the first time duration.

2. The architecture of claim 1, wherein the processing task in a second logic configuration follows the processing task in the first logic configuration in an overall predetermined processing task.

3. The architecture of claim 1 or 2, wherein the processing task of each logic configuration is performed on the plurality of data symbols within the first time duration.

4. The architecture of claim 1, 2, or 3, wherein the data symbol is an OFDM symbol and the first time duration is the OFDM symbol period.

5. The architecture of claim 4, wherein the processing task of the first logic configuration is an FFT calculation and the processing task of the second logic configuration is a PSK demodulation.

6. The architecture of any preceding claim wherein the storage unit comprises a first and second memory unit, and when the logic unit is in a first logic configuration, the first memory unit is adapted to receive a first symbol for processing by the processing logic unit and the second memory unit is adapted to temporarily store results of processing by the processing logic unit.
7. The architecture of claim 6 further comprising a third memory unit for temporarily storing processed and unprocessed data from the first and second memory unit.

8. A digital radio receiver comprising the reconfigurable system architecture of any preceding claim and a receiving means to receive a data frame comprising a plurality of OFDM symbols.

9. The digital radio receiver of claim 6, wherein a first logic configuration of the plurality of logic configurations represents an FFT processing task and a second logic configuration of the plurality of logic configurations represents a DQPSK processing task.

10. A method of sequentially processing a plurality of digital data symbols each of a predetermined duration, the method comprising:

   a) receiving a first digital data symbol;
   b) performing a first processing task on the symbol using a processing logic unit;
   c) storing a result of the first processing task;
   d) reconfiguring the processing logic unit to perform a second processing task on the result of the first processing task;
   e) outputting the results of the second processing task, wherein steps a) to e) are carried out within the predetermined duration.

11. The method of claim 10 wherein the first and second processing task are performed on a plurality of digital data symbols within the predetermined duration.

12. The method of claim 10 or 11 wherein the first processing task is an FFT calculation and the second processing task is a PSK demodulation.
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Claims searched: 1-12  Date of search: 23 April 2007

Patents Act 1977: Search Report under Section 17

Documents considered to be relevant:

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