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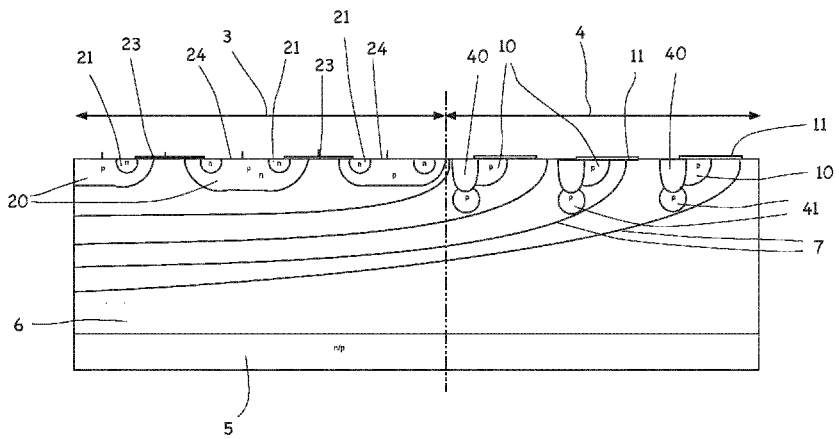

FIG. 5

(57) Abstract: A termination region (4) of a vertical DMOSFET or IGBT is described, in which surface p-rings (10) are combined with oxide/polysiliconf i I led trenches (40), buried p-rings (41) and optional surface field plates (11), so as to obtain an improved distribution of potential field lines (7) in the termination region (4). The combination of surface ring termination (10, 11) and deep ring termination (41) offers a significant reduction in the area of the termination region (4).

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EDGE TERMINATION FOR SEMICONDUCTOR DEVICES AND CORRESPONDING FABRICATION METHOD

TECHNICAL FIELD

The present invention relates to termination arrangements for semiconductor devices and, in particular but not exclusively, to termination arrangements for high voltage (HV) semiconductor devices such as diodes, transistors or insulated gate bipolar transistors (IGBTs) which are required to withstand reverse voltages of hundreds or thousands of volts.

BACKGROUND OF THE INVENTION

A high voltage semiconductor device typically comprises a termination region which electrically isolates the device from the surrounding substrate and/or from the device's package. The termination region must ensure that the active area of the device is protected from high voltages, and that the device breakdown voltage of the device is as high as possible.

For high voltage devices such as DMOSFETs or IGBTs, a lightly doped drift region may be terminated in such a way as to ensure the optimum distribution of field or potential lines which is important to achieve the full voltage rating of the device. In order to be effective, such a termination area should preferably have a higher voltage-withstanding capability than the interior (active) area of the device.

Electrical termination can be achieved by dielectric materials or/and by reverse-biased pn-junctions. Under dielectric isolation, a dielectric insulator material such as an oxide of silicon may be used, in which case electrical termination may be achieved by forming oxide-filled trenches in the termination area surrounding the device's active area. Such termination trenches may be effective at distributing the potential or field lines laterally through the substrate body, but may leave the charge and potential distribution at the surface relatively uncontrolled.

Alternatively, a junction isolation termination may be used, in which reverse-biased p-n junctions help to achieve the required distribution of field or

potential lines through the termination area. Surface guard-rings of opposite doping to the drift region may be used, for example, to distribute the potential across the termination area near the surface of the substrate. However, such termination arrangements are less effective at preventing crowding of the potential lines in the substrate body near the surface. Furthermore, such prior art termination arrangements typically either involve extra fabrication steps and/or masks, or the fabrication process may impose limitations on the geometries and/or configurations of the termination elements.

US 2008/042172 A1 refers to a prior art MOS transistor, which comprises trench gates in the active cell area and termination trench gates in the termination area, which are surrounded by one contiguous p doped layer.

In US 2009/090968 A1 a prior art MOS device is described having in the termination region p guard rings, which are covered by a field plate electrode.

SUMMARY OF THE INVENTION

An aim of the present invention is to overcome at least some of the disadvantages of prior art termination arrangements. To this end, the invention foresees a fabrication method as set out in claim 1 and a semiconductor device as set out in claim 6. Further variants of the invention are set out in the dependent claims 2 to 5 and 7 to 11.

By combining the fabrication of termination trenches and buried guard-rings with the fabrication of surface guard rings, it is possible to achieve a superior termination efficiency (ie reduced termination area and/or increased breakdown-voltage) while minimising the amount of additional fabrication processing required. The addition of field plates over the termination trenches and/or the surface guard rings may further improve the termination efficiency.

By having an arrangement of the termination trenches and deep lying buried guard rings, which abut the termination trenches, the electric field is kept at a high depth in the termination area up to such an buried termination trench so that the potential lines of the electric field are guided laterally outward from the active area,

which increases the breakdown voltage. Due to the surface guard rings abutting the termination trenches on the side of the termination trenches towards the edge of the substrate the electric field is further spreaded outward from the active area, but still efficiently terminated before the next outwards lying termination trench, i.e. the electric field is terminated better controlled, but still within a short lateral distance.

It is important to have the drift layer abutting each termination trench on the side towards the active cell area and to have the surface guard rings being arranged only on the side towards the edge of the substrate so that the electric field is directed to terminate in the region beyond, i.e. outwards the termination trench (i.e. on the side towards the edge of the substrate). The presence of the surface guard ring on the side of the termination trench towards the active cell area would foil the effect of directing the potential lines away from the active cell area.

In an exemplary embodiment, the presence of the field plate connecting the termination trench with the surface guard ring contributes to the effect of terminating the electric field within a short, but controlled lateral distance from the active cell area and protects the surface of the substrate.

Thus the inventive semiconductor device enables to have a device with an efficient field termination within a small distance so that the device can be operated more reliable and can be designed more compact than prior art devices, i.e. the termination area (i.e. lateral extension of the termination area) can be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be described in more detail with reference to the accompanying drawings, in which:

Figure 1 shows, in schematic, cross-section view, an example of an n-channel DMOS device terminated using p-rings and field plates, as known in the prior art.

Figure 2 shows, in schematic, cross-section view, an example of a trench-gated n-channel device terminated using p-rings and field plates, as known in the prior art.

Figure 3 shows, in schematic, cross-section view, an example of an n-channel DMOS device terminated using trenches and buried p-rings, as known in the prior art.

Figure 4 shows, in schematic, cross-section view, an example of a trench-gated n-channel device terminated using trenches and buried p-rings, as known in the prior art.

Figure 5 shows, in schematic, cross-section view, an example of an n-channel DMOS device terminated using trenches, buried guard rings and surface guard rings in accordance with the invention.

Figure 6 shows, in schematic, cross-section view, an example of a trench-gated n-channel device terminated using trenches, buried guard rings and surface guard rings in accordance with the invention.

Figure 7 shows, in schematic, cross-section view, an example of an n-channel DMOS device terminated using trenches, buried guard rings and surface guard rings in accordance with the invention.

Figure 8 shows, in schematic, plan view, an example of a generic device terminated in accordance with the invention.

It should be noted that the drawings are provided as an aid to understanding certain principles underlying the invention, and should not be taken as implying any limitation in the scope of protection sought. Where the same reference signs have been used in more than drawing, these are intended to refer to the same or corresponding features. However, the use of different reference signs should not be taken as indicating a difference between the features to which the signs refer.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 shows an example of a cross-sectional view of an n-channel depletion MOSFET or IGBT as known in the prior art. The active cell area 3 comprises an array of power MOSFET or IGBT cells, each having a p-doped body region 20 (i.e. of the second conductivity type) surrounding two p-n junctions formed between the two n-doped regions 21 (i.e. of the first conductivity type) and the p-doped body (well) region 20. Two gate connections 23 (each shared with a neighbouring cell in this example case) are provided for controlling the current flow from the p-n junctions into the drift region 6, and through the device substrate 6 (in form of an n- drift layer) to the drain/cathode layer 5 (n-doped in the case of an n-channel DMOSFET, or p-doped in the case of an n-channel IGBT). Power is supplied to each device cell via an emitter/anode contact 24.

Figure 1 also shows how the MOSFET or IGBT may be terminated using guard rings 10 and field-plates 11 distributed across edge-termination area 4. The potential lines 7 may be prevented from concentrating around the edge of the active area 3 by the inclusion of p-doped guard rings 10 formed in the surface of the substrate material. Each of the guard rings 10 forms a weakly-doped p-n junction between the lightly p-doped guard ring 10 and the lightly n-doped drift region 6 and, under reverse-biased conditions, serves to reduce the amount of electric field crowding at the substrate surface by spreading the depletion layer further out towards the edge of the substrate 6, past further guard rings 10 at successively lower potentials, until the high charge density present in the active area 3 is tapered to zero across the termination area 4. Field plates 11 serve to distribute the potential yet more evenly near the surface, thereby avoiding concentrations of potential lines (“crowding”).

Figure 2 shows a cross-sectional view of an n-channel trench gated MOSFET or IGBT. As in the device shown in figure 1, the active cell area 3 of the device is extended by a termination area 4 of the substrate 6. The termination area 4 uses surface p-rings (guard rings) 10, which partially replace the drift layer material 6 at and near the surface of the termination area 4. Field plates 11 are also added to the edge of each of the the p-rings 10. As with the example device of figure 1, the guard rings 10 and field plates 11 serve to deflect the potential lines 7 and prevent a concentration of potential lines in the surface region of the termination area 4.

Figures 3 and 4 show similar devices to those depicted in figures 1 and 2 respectively, but terminated with termination trenches 40 instead of the surface p-rings 10 of figures 1 and 2. Each of the termination trenches 40 may be filled with a dielectric material such as a silicon oxide, or a conductive material such as polysilicon. A p-doped region 41 may be formed at or near the end or tip of each termination trench 40, to provide enhanced deflection of the potential lines around the end of the termination trench 40. The deep p-doped regions 41, also referred to as deep or buried guard rings 41, are known to be an effective alternative to the surface guard rings 10 described with reference to figures 1 and 2.

Note that the devices described with reference to figures 1 to 4 are depletion mode devices, in which a dedicated p-n junction depletes in the off-state so as to withstand the off-state voltage. In other words, the depleted region electrically isolates the p-doped region and the n-doped region from one another.

Figure 5 shows a first embodiment of an inventive MOSFET. the lightly n-doped region 6 part may be referred to as the “drift region”, the “lightly-doped region” or the “reverse voltage supporting region”. For a power device made by starting with a substrate of low n- doping concentration, the drift layer 6 in the finalized power device shall be the layer of unamended doping concentration by manufacturing steps. Exemplarily, the drift layer 6 has a constantly low doping concentration. Therein, the substantially constant doping concentration of the drift layer 6 means that the doping concentration is substantially homogeneous throughout the drift layer 6, however without excluding that fluctuations in the doping concentration within the drift layer being in the order of a factor of one to five may be possibly present due to e.g. a fluctuations in the epitaxial growth process. The final drift layer thickness and doping concentration is chosen due to the application needs. An exemplary doping concentration of the drift layer 6 is between $5 * 10^{12}$ cm^{-3} and $5 * 10^{14}$ cm^{-3}.

However, the implementation of the invention is not limited to such devices; other possibilities include, for example, its use in superjunction (SJ) or other types of device which require terminating. In an SJ device, the drift region may typically be replaced by alternating highly doped p and n layers which, under mutual

charge compensation, can completely deplete in the off-state and support a high voltage across the device.

Similarly, while the figures show one particular doping scheme (eg n-channel MOSFETS), it would of course be possible to use different (eg reversed) doping schemes.

Figures 5 and 6 illustrate an example of a termination arrangement which makes use of the principles of the present invention. The active areas 3 of the devices depicted in figures 5 and 6 correspond to the active areas of figures 1 and 2, or 3 and 4, respectively. The substrate 6 comprises an (n-) doped drift layer. In the active cell area, the device comprises main electrical contacts on a first and second main side on opposing sides of the substrate. The substrate 6 comprises an active cell area 3, which is surrounded laterally (i.e. in a plane parallel the main sides) by a termination area 4, which extends to the edge of the substrate (lateral surface sides of the substrate).

In the termination areas 4, by contrast, the devices shown in figures 5 and 6 combine the principles of termination trenches 40 with buried guard rings 41, and a variant of the surface guard rings 10, wherein the guard rings have a different conductivity type than the drift layer, in this example the guard rings are p doped. In both of the example devices shown in figures 5 and 6, the termination area 4 comprises termination trenches 40 and buried guard rings 41 which provide a primary termination effect by guiding the potential lines 7 laterally outward from the active area 3. Each termination trench 40 also has an outer adjacent surface guard ring 10, abutting the outward side of the termination trench 40, to guide the potential lines 7, which would otherwise curve around the termination trenches as indicated in figures 3 and 4, and may form local crowding of potential lines 7 near the outer side of each termination trench 40, to spread them further outward and away from the termination trench 40. Thus, the presence of p-doped buried guard rings 41 under the termination trenches 40 releases part of the electric field deeper into the device silicon, hence the breakdown voltage is increased. The termination trenches 40 may be filled with oxide or polysilicon, for example. The surface of the termination area 4 adjacent to each termination trench 40 is kept protected from high electric fields by aligning surface p-rings 10 with the outer side of the termination trenches 40. The

surface may be further protected by forming field plates (eg of dielectric oxide) at the edge of each surface p-ring (10).

The termination trenches 40, with their buried p-rings 41, and the surface p-rings 10 (rings of the second conductivity type), may be fabricated in self-aligning fashion. An n- doped substrate 6 may be provided. For example, the surface p-rings 10 may be formed first (eg by implantation and diffusion) in the substrate 6, and then the termination trenches 40 may be etched or otherwise formed such that the outward edge of one of the termination trenches (edge outwards from the active cell area 3, i.e. towards the substrate edge) intersects with an inward part (towards the active cell area 3) of its abutting surface p-ring. The termination trenches 40 may be formed in conventional fashion by removing the substrate material. Once the termination trenches 40 have been opened, then the buried p-rings 41 may be formed under the termination trenches 40 by implantation (doping) the substrate body in the region 41 adjacent to the bottom of each termination trench 40. Advantageously, the number of process steps and/or masks required may be reduced by forming the surface p-rings 10 in the termination area 4 and the p-well bodies 20 or body 32 using the same mask and the same doping process. Thus, for the example device illustrated in figure 5, the fabrication process may advantageously be configured such that the same mask and process is used not only for the surface p-rings 10 in the termination area 4, but also the device cell body (p-well) regions 20 in the active area. For the example device illustrated in figure 6, the fabrication process may advantageously be configured such that the same mask and/or process is used not only for the termination trenches 40 in the termination area 4, but also for the device cell trench-gates 30 of the device cells in the active area 3. Additionally, in the fabrication process for the example device shown in figure 6, a single mask and/or process may advantageously be used for forming the surface p-rings 10 in the termination area 4 and the p-body layer 32 in the active area 3.

Surface field plates 11 may also be formed, partially or fully covering each termination trench 40 and its abutting surface guard-ring 10, and extending outward beyond the surface guard-ring 10 over the surface of the drift region 6 (n- doped region, i.e. of a second conductivity type, which conductivity type is different than the

first conductivity type) which separates the termination trenches 40. The electric field distribution over the termination area 4 may be controlled by suitable choice of the dimensions and spacing of termination trenches 40, surface p-rings 10 and buried p-rings 41.

Figure 7 shows an example of some dimensions of the termination trenches 40, buried p-rings 41, surface p-rings 10 and field plates 11. Although only two termination trenches 40 are illustrated in figure 7, it should be understood that this number may in practice be significantly greater - for example as many as 15 or 20 or more, distributed across the termination area 4.

By way of example, the distance 16 between the edge of the active area 3 and the first termination trench 40 may be between 5 μm to 10 μm (eg 7 μm), for example. The mesa width 15 (ie the separation distance between adjacent termination trenches 40) may for example be 7-20 μm, and may increase in the direction away from the active area 3. The trench depth 9 may be between 4 and 7 μm (eg 5.2 μm), the trench width 17 may be between the minimum permitted by the fabrication process and 4 μm, for example (eg 1.2 μm). The peak doping concentration of the buried p-rings 41 may be between 10^{16} cm^{-3} and 10^{18} cm^{-3} (eg 10^{17} cm^{-3}), and a doping concentration at a doping depth of 2 μm may be between 10^{15} cm^{-3} and 10^{16} cm^{-3} (eg 5×10^{15} cm^{-3}). The height 8 of the deep p-ring (buried guard ring) 41 may be between 2 and 5 μm (eg 3-4 μm). The lateral extent of the surface p-rings (guard rings) 10 may be between 1 and 5 μm, and preferably between 1 and 2μm - eg 1.5 μm, while the vertical extent (depth) of the surface p-rings (guard rings) 10 is preferably substantially the same as the depth of the p-wells (body region) 20 of the device cells in the active area 3. Similarly, the doping concentration of the surface p-rings (guard rings) 10 is preferably substantially the same as that of the p-wells 20 of the device cells in the active area 3. For devices with these preferred dimensions, the field plate width 12 may be between 3 and 8 μm, for example, or more preferably between 4 and 6 μm (eg 4.5 μm). The guard-rings/trench/field-plates termination may be made using standard device processing techniques such as implantation, diffusion, etch and refill. The dimensions and distances of the surface 10 and deep 41 guard rings, the field plates 11 and the

oxide/polysilicon filled trenches 40 can be varied to suit the required reverse breakdown voltage.

The combination of the surface and deep ring termination, the dielectric/trench termination and the field plates offers a significant area reduction in the termination area required the effective junction termination of high-voltage devices which may be required to withstand reverse voltage of 5 kV, 6 kV or more. At lower voltages (eg 1.3 kV), the termination described here has been found to offer a reduction of 30% or more in the minimum radial extent of the termination area.

Figure 8 shows a schematic plan view of a simplified example of a termination area comprising termination trenches 40 and field plates 11. Not visible are the surface guard rings 10 (obscured by the field plate 11) and the buried guard rings 41 (under the termination trenches 40). In a real implementation of the termination arrangements described above, the number of termination structures (termination trench 40, buried guard-ring 41, surface guard-ring 10 and field plate 11) would be significantly greater than the two shown in figure 8.

Claims

1. A method of fabricating a semiconductor power device, wherein the semiconductor power device comprises a semiconductor substrate (6) having an active cell area (3), which comprises a drift layer of a first conductivity type, and an edge termination area (4) up to a substrate edge, and wherein the method comprises:

a first step of forming a plurality of surface guard rings (10) of a second conductivity type different from the first conductivity type, which are separated from each other, in the surface of the edge termination area (4),

a second step of removing substrate material (6) so as to form a plurality of termination trenches (40) extending down from the surface of the edge termination area (4), such that each surface guard ring (10) abuts an adjacent termination trench (40) on a side towards the substrate edge and the drift layer abuts said termination trench (40) on a side towards the active cell area (3),

a third step of forming a buried guard ring (41) of the second conductivity type in the substrate material adjacent to the bottom of each termination trench (40), and

a fourth step of filling each termination trench (40) with a dielectric material or a conductive material.

2. The method according to claim 1, wherein a fifth step of, for each termination trench (40), forming a field plate (11) over a part of a termination trench (40) and its abutting surface guard ring (10).
3. The method according to one of the claims 1 to 2, wherein the first step is performed before the second step such that, for each of the plurality of termination trenches (40), the substrate material removed in the second step includes a portion of one of the surface guard rings (10).
4. The method according to one of claims 1 to 3, wherein the active cell area (3) comprises a plurality of trench-gate device cells (30, 31, 33), and wherein the

second step comprises forming trenches (30) of the trench-gate device cells (30, 31, 33) during the same fabrication process or processes as the termination trenches (40).

5. The method according to one of claims 1 to 4, wherein the active cell area (3) comprises a plurality of active device cells (20, 21, 23, 24), each comprising a body region (20), and wherein the first step comprises forming the body regions (20) of the active device cells (20, 21, 23, 24) during the same fabrication process or processes as the surface guard rings (10).
6. The method according to claim 4 or claim 5, wherein each active device cell (20, 21, 23, 24) comprises a gate connection (23) and/or a power connection (24), and wherein the fifth step comprises forming the gate connection (23) and/or power connection (24) during the same fabrication process or processes as the field plate (11).
7. A semiconductor power device comprising a semiconductor substrate (6), which has an active cell area (3), which comprises a drift layer of a first conductivity type, and an edge termination area (4) up to a substrate edge, wherein the edge termination area (4) comprises:

a plurality of surface guard rings (10) of a second conductivity type different from the first conductivity type, which are separated from each other, disposed in the surface of the substrate (6),

a plurality of termination trenches (40) extending down from the surface of the substrate (6), such that each surface guard ring (10) abuts an adjacent termination trench (40) on a side towards the substrate edge and the drift layer abuts said termination trench (40) on a side towards the active cell area (3), and

a plurality of buried guard rings (41), each buried guard ring (41) being disposed in the substrate (6) adjacent to a bottom of one of the termination trenches (40).

8. A semiconductor power device according to claim 6, wherein at least one field plate (11) is disposed over a part of a termination trench (40) and its abutting surface guard ring (10).

9. A semiconductor power device according to one of the claims 7 to 8, wherein each termination trench (40) is provided with a termination trench field plate (11) disposed at least partly over the termination trench (40) and over a second substrate surface region abutting to the termination trench (40).
10. A semiconductor power device according to one of the claims 8, wherein the termination trench field plate (11) of the said termination trench (40) and the surface guard ring field plate (11) of the abutting surface guard ring (10) are contiguous.
11. A semiconductor power device according to one of claims 7 to 10, wherein the active cell area (3) comprises a plurality of trench-gate device cells (30, 31, 33), and wherein the termination trenches (40) are filled with the same material as the trench-gate trenches (30) of the trench-gate devices (30, 31, 33).
12. A semiconductor power device according to one of claims 7 to 11, wherein the active cell area (3) comprises a plurality of active device cells (20, 21, 23, 24), each comprising a body region (20) of the second conductivity type, and wherein the surface guard rings (10) has the same doping concentration profile as the body regions (20) of the active device cells (20, 21, 23, 24).
13. A semiconductor power device according to claim 12, wherein each active device cell (20, 21, 23, 24) comprises a gate connection (23) and/or a power connection (24), and wherein the termination trench (40) and surface guard ring field plates (11) comprise the same material as the gate connections (23) and/or power connections (24) of the active device cells (20, 21, 23, 24).

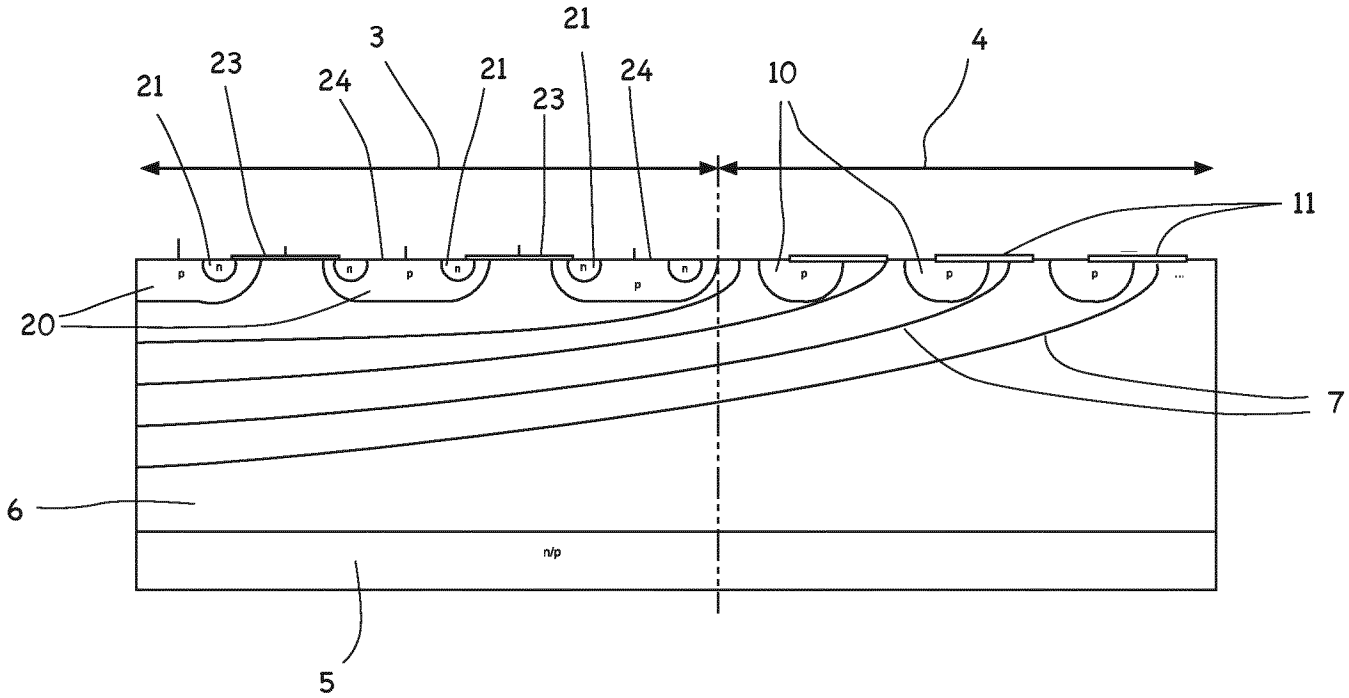
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FIG. 1

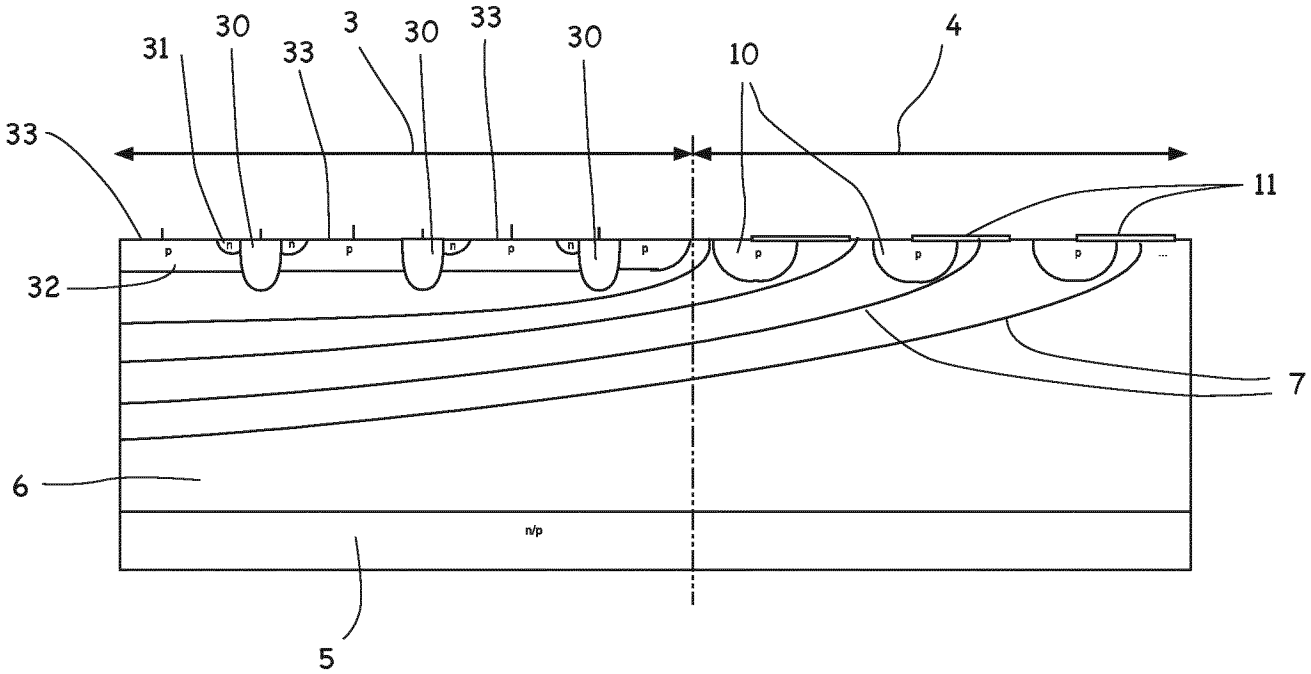
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FIG. 2

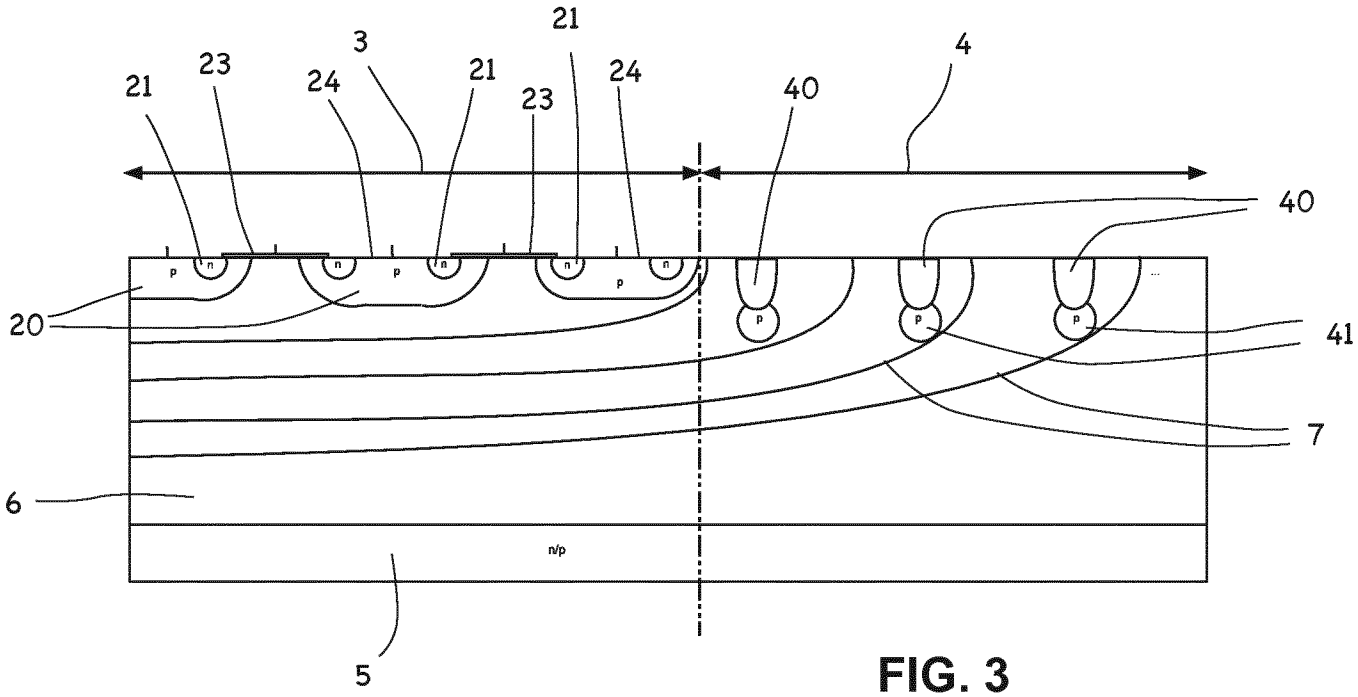
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FIG. 3

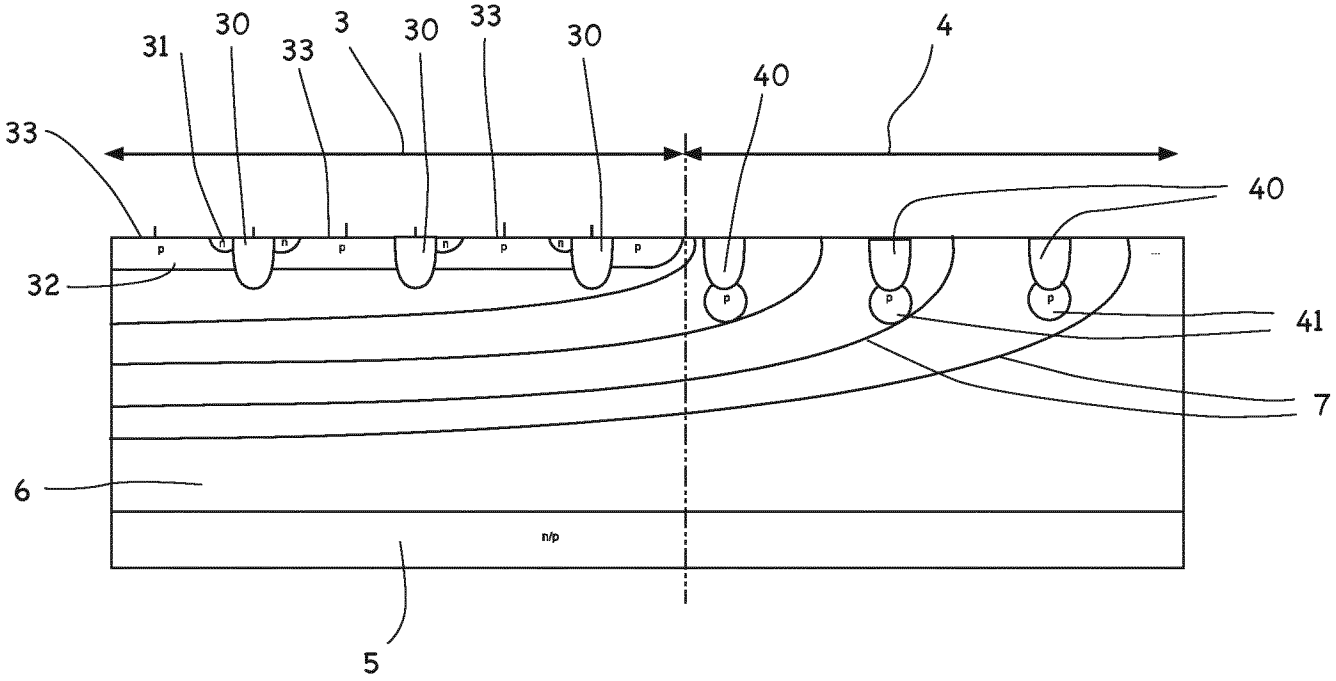
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FIG. 4

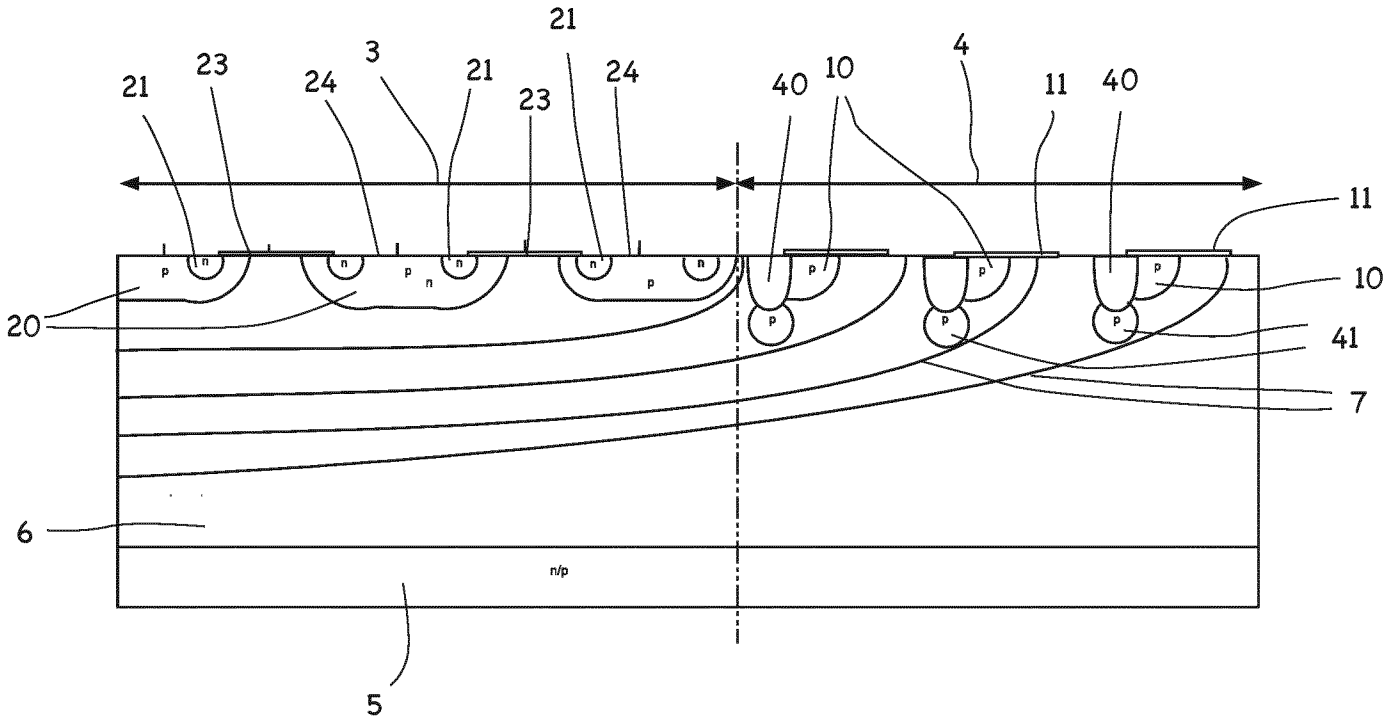
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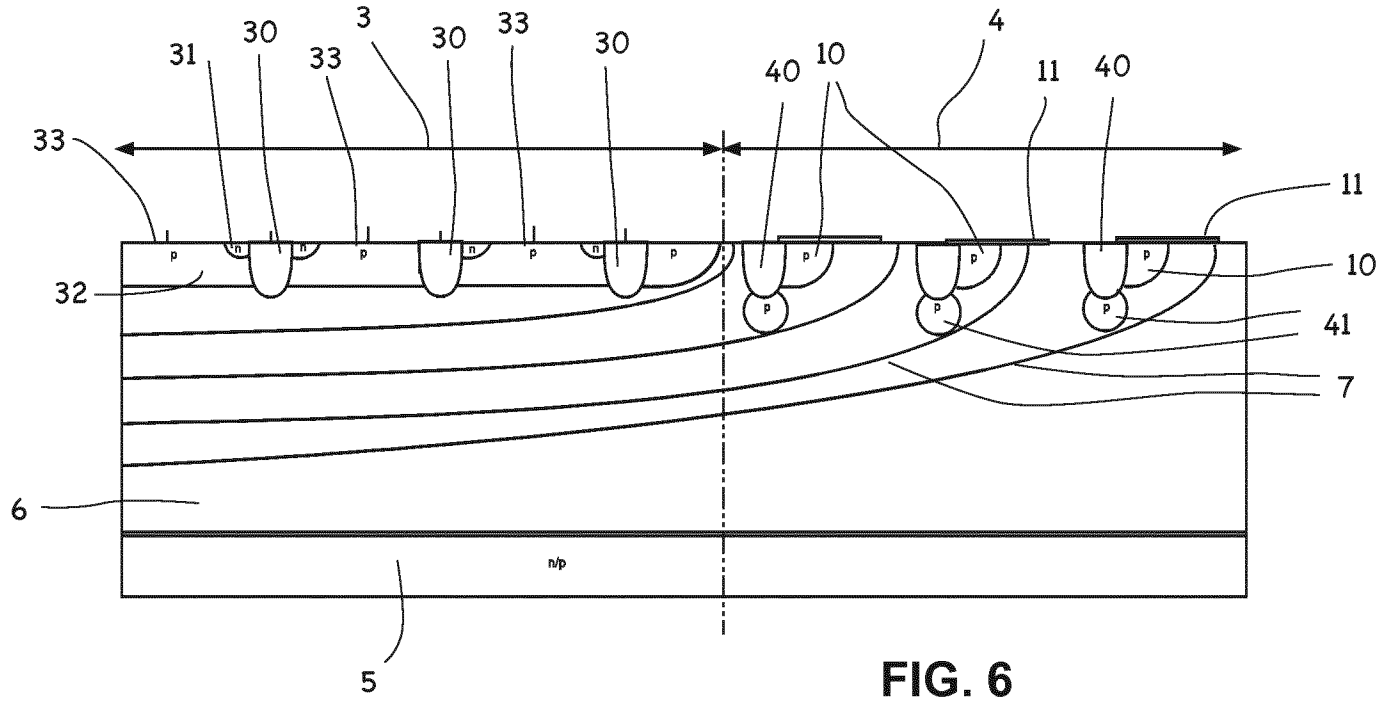
FIG. 5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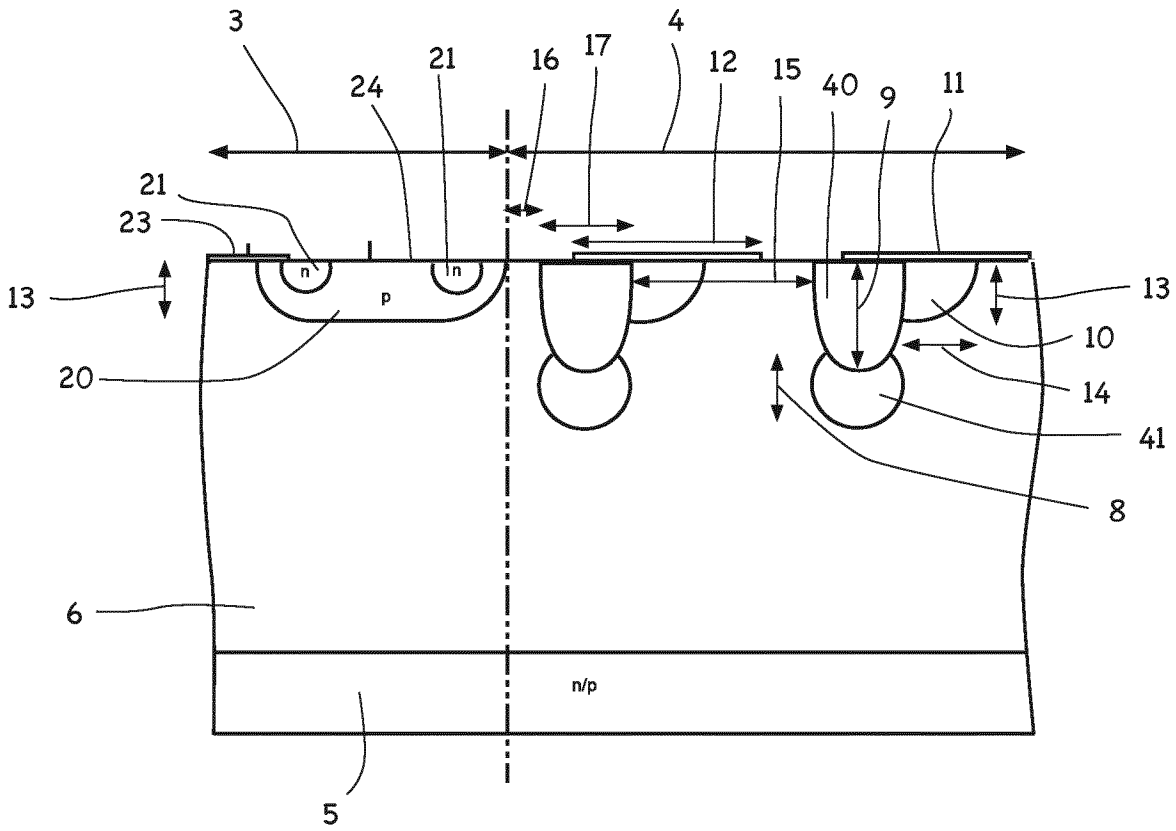
n/p

FIG. 6


3
24
21
16
17
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12
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11
21
23
13
n
p
n
13
10
20
14
41
8
6
n/p
5

FIG. 7

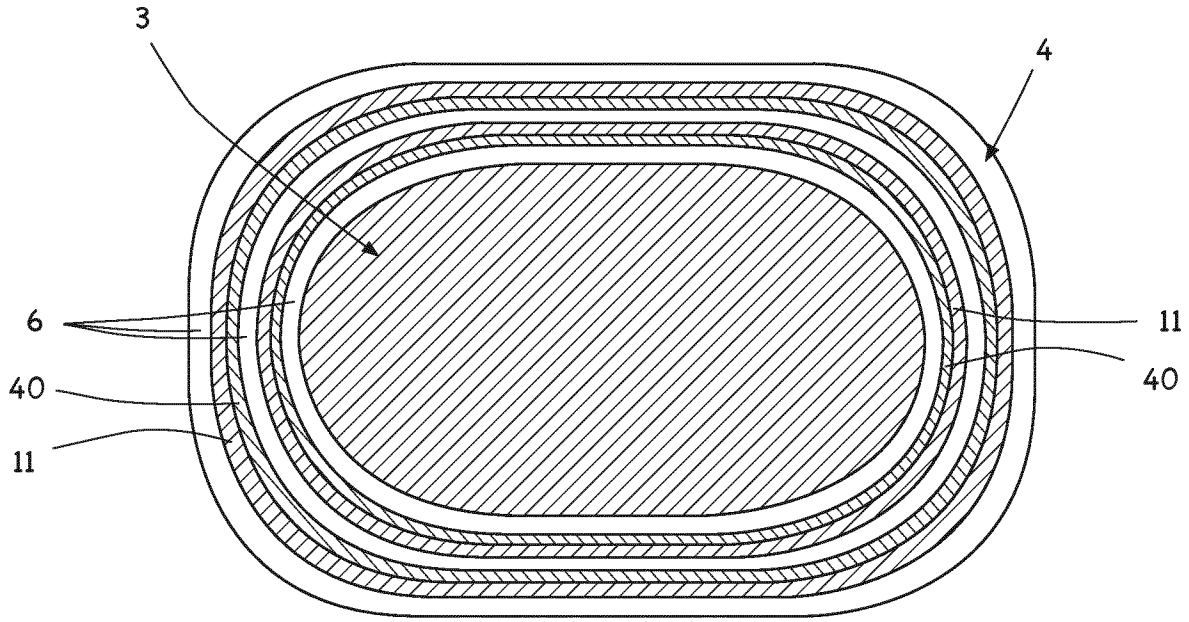
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FIG. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2014/076443

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/06 H01L29/78 H01L29/739 H01L21/336 H01L21/331
ADD. H01L29/40

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008/042172 A1 (HIRLER F ET AL) 21 February 2008 (2008-02-21) paragraphs [0017] - [0034]; figure 1 paragraph [0037] - paragraph [0039]; figure 3 paragraph [0041] - paragraph [0042]; figure 4 paragraph [0044]; figure 5 paragraph [0046] - paragraph [0053]; figures 6A-6D	1-13
A	US 2009/090968 A1 (ONO S ET AL) 9 April 2009 (2009-04-09) paragraph [0030]; figures 1,3	2,8-10
X,P	WO 2014/048046 A1 (INST OF MICROELECTRONICS CAS ET AL) 3 April 2014 (2014-04-03) abstract; figures 2-5	1,4,5,7, 12

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 December 2014	12/01/2015

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2014/076443

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008042172 A1	21-02-2008	DE 102006036347 A1	17-04-2008
		JP 5089284 B2	05-12-2012
		JP 2008103683 A	01-05-2008
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WO 2014048046 A1	03-04-2014	CN 103715232 A	09-04-2014
		WO 2014048046 A1	03-04-2014