

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization International Bureau



(43) International Publication Date  
19 May 2005 (19.05.2005)

PCT

(10) International Publication Number  
**WO 2005/045914 A1**

(51) International Patent Classification<sup>7</sup>: **H01L 21/31**

(21) International Application Number:

PCT/US2004/024904

(22) International Filing Date: 30 July 2004 (30.07.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:  
10/690,060 21 October 2003 (21.10.2003) US

(71) Applicant (for all designated States except US):  
**FREESCALE SEMICONDUCTOR, INC. [US/US]**  
6501 William Cannon Drive West, Austin, TX 78735 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **DOUGAN, James, N. [GB/US]**; 7010 Avignon Drive, Round Rock, TX 78681 (US). **SMITH, Lesley, A. [GB/US]**; 5806 Cedar Cliff Drive, Austin, TX 78759 (US).

(74) Agents: **KING, Robert, L. et al.**; Corporate Law Department, Intellectual Property Section, 7700 West Parmer Lane, MD: TX32/PL02, Austin, TX 78729 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

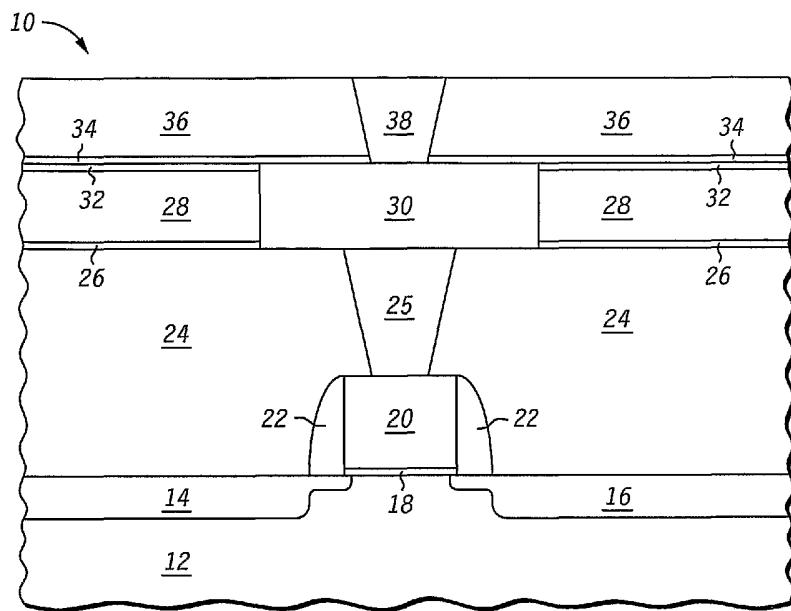
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

[Continued on next page]

(54) Title: METHOD OF FORMING A LOW K DIELECTRIC IN A SEMICONDUCTOR MANUFACTURING PROCESS



(57) Abstract: A low K dielectric composite layer (26, 28) is formed of a low K barrier layer (26) and a low K dielectric layer (28) on the barrier layer (26). The barrier layer (26), which is deposited with the result of having a hydrophobic top surface, is treated with an oxygen plasma to convert the surface from hydrophobic to hydrophilic. A subsequent water-based clean is very effective in removing yield-reducing defects on the barrier layer (26) due to the conversion of the surface of the barrier layer (26). After the water-based clean, the low K dielectric layer (28) is formed on the surface of the barrier layer (26) to achieve the composite layer (26, 28) that has a low K.

WO 2005/045914 A1



*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

## **METHOD OF FORMING A LOW K DIELECTRIC IN A SEMICONDUCTOR MANUFACTURING PROCESS**

### Field of the Invention

5        This invention relates to integrated circuit manufacturing, and more particularly, to the formation of low k dielectric films in integrated circuit manufacturing.

### Related Art

10      In the manufacturing of semiconductors, one of the developments has been the use of low k dielectrics-for an interlayer dielectric (ILD), the layer between conducting layers above the semiconductor substrate. This low K dielectric is to reduce capacitive coupling between conductors that are used as interconnect. Reducing this capacitive coupling is particularly important in  
15      cases where speed is a high priority, which is often the case. The low K materials are typically neither the best insulators nor the easiest to manufacture with high yield. Often barrier layers and capping layers are required in order to achieve all of the characteristics necessary for successful operation. These additional layers add steps, which complicate the process and potentially  
20      introduce yield problems.

      Thus, there is a need for low K dielectrics in semiconductor manufacturing that can be made with less adverse effects on yield.

Brief Description of the Drawings

The present invention is illustrated by way of example and not limited by the accompanying figures, in which like references indicate similar elements, and in which:

5 FIG. 1 is a cross section of a semiconductor device structure made according to an embodiment of the invention; and

FIG. 2 is a flow diagram of a process according the embodiment of the invention used in making the device of FIG. 1.

Skilled artisans appreciate that elements in the figures are illustrated for 10 simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve the understanding of the embodiments of the present invention.

Detailed Description of the Drawings

In one form, a low k barrier layer, which is deposited with a hydrophobic surface, is treated with an oxygen plasma to convert the surface to being hydrophilic. The hydrophilic surface is then cleaned with a scrub. The scrub 5 has a significantly increased effectiveness due to the surface being hydrophilic. After the treatment a low K dielectric layer is formed on the surface. This is better understood by reference to the drawings and the following description.

Shown in FIG. 1 is a semiconductor device 10 comprising a semiconductor substrate 12, a drain region 14 formed in substrate 12, a source 10 region 16 formed in substrate 12, a gate dielectric 18 over substrate 12 and substantially between drain 14 and source 16, a gate 20 over gate dielectric 18, a sidewall spacer 22 around gate 22, a dielectric layer 24 over and around gate 20, a contact 25 on gate 20, a low k barrier dielectric layer 26 on dielectric layer 24, a low K dielectric layer 28 on low k barrier dielectric layer 26, a capping layer 15 32 on low K dielectric layer 28, a conductive layer 30 on via 25 and surrounded by layers 26, 28, and 30, a low k barrier layer 34 on capping layer 32, a low K dielectric layer 36 on low k barrier layer 34, and a via 38 on conductive layer 30 and surrounded by layers 34 and 36. Semiconductor substrate 12 is preferably an SOI substrate in which the semiconductor is silicon or it can be another type 20 of semiconductor substrate of another semiconductor material. Gate 20 is preferably silicon but could be other materials such as a metal or composite of different layers. Contact 25 is preferably tungsten but could be another type of conductive material. Via 38 is preferably copper but could be another type of conductive material. Conductor layer 30 is preferably copper but may be 25 another conductive material. Capping layer 32 is preferably an oxide formed using tetraethylorthosilicate (TEOS), but may other dielectric materials. Dielectric 24 is a composite of layers with the top layer preferably being either SiCOH or an oxide formed using fluorine and TEOS (FTEOS). A CMP process is applied to dielectric layer 24 so that the material on the surface of layer 24

after the CMP processing may vary. A preferred combination of material over layer 24 prior to performing the CMP process is silicon rich oxide, silicon rich oxynitride, TEOS oxide, which results in the top surface of layer 24 not being the same across the wafer on which device 10 is performed. Semiconductor 5 device 10 is a conventional structure that can be formed by conventional means except for the method in forming the composite layer of low k barrier layer 26 and low K dielectric 28 and the composite layer of low k barrier layer 34 and low K dielectric layer 36.

The method of forming these composite layers is shown in flow diagram 10 50 of FIG. 2. Flow diagram 50 comprises steps 52, 54, 56, and 58. In step 52 a layer is deposited that has a hydrophobic surface, which is true of low k barrier layers 26 and 34. Barrier layers 26 and 34 are preferably SiCN. Low K dielectric layers 28 and 36 are preferably SiCOH. SiCN has been found to be an effective barrier in protecting SiCOH from layer 24. SiCN has the 15 characteristic of having a hydrophobic surface. The SiCN also has been found to have particles on its surface. A scrub clean has been found not remove all of the particles. One possible reason for the clean being less than fully effective is that the surface of the SiCN layer, as deposited, is hydrophobic. Furthermore a scrub clean has been found to damage the structure of the SiCN creating a new 20 type of defect. Step 54 is to convert the surface of the SiCN layer from being hydrophobic to hydrophilic. This is achieved with an oxygen plasma. The deposition of the SiCN and the subsequent plasma treatment of the SiCN layer are preferably performed in situ. Because SiCN is a plasma deposition, the subsequent oxygen plasma step can easily be performed without having to 25 remove the wafers from the deposition chamber. Thus, layer 26 is deposited and then treated in the same chamber. In the same way but after the deposition and CMP processing of conductor 30, layer 34 is also deposited and treated in the same chamber.

Step 56 is to perform a scrub of the surface of the layer that has been plasma treated. Thus layer 26 is treated with a scrub clean after layer 26 has been treated with oxygen plasma. This is also true for layer 34. The scrub clean is a water-based clean. The water is preferably de-ionized and further 5 includes ammonium hydroxide. This is a conventional composition for a water-based clean such as a scrub clean.

Step 58 is to perform the deposition of the next layer, which is low K dielectric layer 28 over low k barrier layer 26 and low K dielectric layer 36 over barrier layer 34. This combination of steps 52-58 combines to complete a 10 composite layer useful as a low K dielectric.

One theory for the benefit of this method is that the plasma deposition of the barrier layer results in particles on the surface of the barrier which can cause yield-reducing defects; these particles are not effectively removed by a scrub because the surface of the barrier layer is hydrophobic; and the post-deposition 15 plasma treatment of the surface of the barrier layer converts the surface of the barrier layer to hydrophilic so that the scrub is effective in removing the particles without the subsequent generation of a new defect type. Another theory is that the plasma treatment causes there to be less adhesion between the particles and the barrier layer so the subsequent scrub is more effective. In any 20 event, the process has resulted in a significant improvement in yield.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims 25 below. For example, other dielectric and barrier materials may be used that benefit from a plasma treatment followed by a water-based clean. Another material may also be hydrophobic as deposited and be converted to hydrophilic with a plasma treatment. The plasma treatment may be other than by oxygen. The low K material may be something other than SiCN and SiCOH and may be

spun-on instead of by plasma. The water-based clean need not necessarily be a scrub process but simply using a water-based solution without requiring a scrubber. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are

5 intended to be included within the scope of present invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to

10 be construed as a critical, required, or essential feature or element of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed

15 or inherent to such process, method, article, or apparatus.

CLAIMS

1. A method of forming a layer over a semiconductor substrate comprising:  
providing a semiconductor substrate;

5 forming a first dielectric layer overlying said substrate, said first

dielectric layer comprising a hydrophobic surface;

converting said hydrophobic surface to a hydrophilic surface;

scrubbing said hydrophilic surface; and

forming a second dielectric layer overlying said first dielectric layer.

10

2. The method of claim 1, wherein said first dielectric layer comprises silicon, carbon and nitrogen.

15 3. The method of claim 1, wherein converting said hydrophobic surface to said hydrophilic surface is by an oxygen plasma.

4. The method of claim 1, wherein said second dielectric layer comprises silicon, carbon, oxygen and hydrogen.

20 5. The method of claim 2, wherein converting said hydrophobic surface to said hydrophilic surface is by an oxygen plasma.

6. The method of claim 5, wherein said second dielectric layer comprises silicon, carbon, oxygen and hydrogen.

25

7. The method of claim 6, scrubbing said hydrophilic surface with a water-based clean.

8. The method of claim 7, wherein said water-based clean comprises ammonium hydroxide.
9. The method of claim 5, wherein said first dielectric comprises silicon, 5 nitrogen, and carbon.
10. The method of claim 9, scrubbing said hydrophilic surface with a water-based clean.
- 10 11. The method of claim 10, wherein said water-based clean comprises ammonium hydroxide.
12. The method of claim 5, wherein the step of forming said first dielectric layer and the step of converting said hydrophobic surface to a hydrophilic 15 surface, are performed in situ.
13. The method of claim 1, wherein forming said first dielectric layer and converting said hydrophobic surface to a hydrophilic surface are performed in situ.
- 20 14. The method of claim 1, wherein forming the first dielectric is plasma deposited and converting is by plasma.
15. A method of forming a layer over a semiconductor substrate comprising:  
25 providing a semiconductor substrate;  
forming a first dielectric layer overlying said substrate;  
treating said first dielectric layer with an oxygen plasma;  
cleaning said first dielectric layer with a water-based solution; and

forming a second dielectric layer overlying said cleaned first dielectric layer.

16. The method of claim 15, treating said first dielectric layer with said oxygen plasma such that a hydrophobic surface of said first dielectric layer is converted to a hydrophilic surface.

17. The method of claim 16, wherein the step of cleaning said first dielectric layer comprises scrubbing said first dielectric layer with said water-based solution.

18. The method of claim 17, wherein said water-based solution comprises ammonium hydroxide.

15 19. The method of claim 18, wherein said first dielectric layer comprises silicon, carbon and nitrogen.

20. The method of claim 15, wherein said first dielectric layer comprises silicon, carbon and nitrogen.

20

21. The method of claim 20, wherein the step of forming said first dielectric layer occurs in a first chamber.

22. The method of claim 21, wherein the step of treating said first dielectric layer with said oxygen plasma occurs in said first chamber.

25 23. A method for forming a semiconductor structure:  
providing a semiconductor substrate;

forming a first dielectric layer comprising silicon, carbon and nitrogen overlying said substrate;  
treating said first dielectric layer with an oxygen plasma;  
scrubbing said first dielectric layer; and  
5 forming a second dielectric layer overlying said first dielectric layer.

24. The method of claim 23, wherein said first dielectric layer has a hydrophobic surface.

10 25. The method of claim 24, wherein said step of treating said first dielectric layer converts substantially all of said hydrophobic surface to a hydrophilic surface.

15 26. The method of claim 23, wherein the step of scrubbing comprises scrubbing with a water-based cleaning solution.

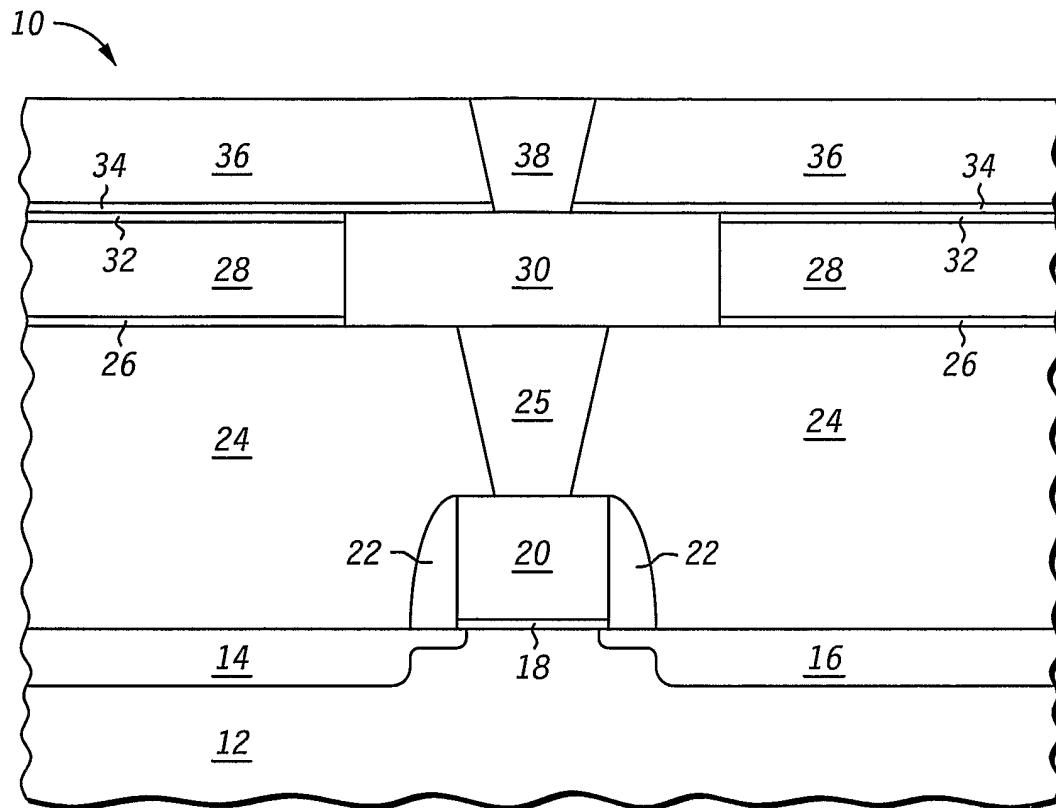
27. The method of claim 26, wherein said water-based cleaning solution comprises ammonium hydroxide.

20 28. The method of claim 27, wherein the step of scrubbing comprises mechanical cleaning and chemical cleaning.

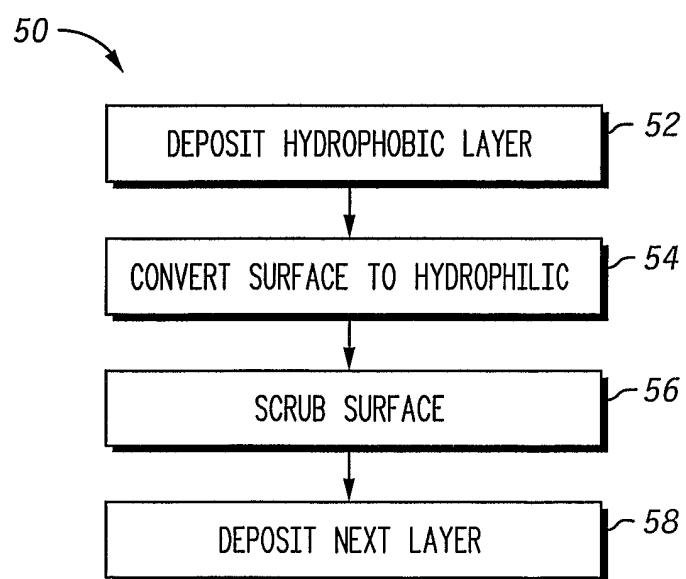
29. The method of claim 23, wherein forming the first dielectric layer comprises:

25 forming the first dielectric layer of silicon of silicon, carbon, and nitrogen; wherein forming the first dielectric and treating the first dielectric layer are performed in situ.

1/1



*FIG. 1*



*FIG. 2*

# INTERNATIONAL SEARCH REPORT

International application No.

PCT/US04/24904

## A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H01L 21/31  
US CL : 438/778

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/58, 642-652; 438/770, 798, 931, 704-712

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched  
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
NONE

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P ---	US 2003/0228769 A1 (CHEN et al) 11 December 2003 (11.12.2003), Figure 1B; paragraph 0021.	1, 2, 4, 13-15, 20-24, 26-29
A,P		-----
Y	US 5,607,773 A (AHLBURN et al) 04 March 1997 (04.03.1997), Column 3.	3, 5-12, 16-19, 25
Y	US 6,386,212 B1 (ROBINSON) 14 May 2002 (14.05.2002), column 3, line 57.	1, 2, 4, 13-15, 20-24, 26-29
Y	US 2003/0155657 A1 (TONEGAWA et al) 21 August 2003 (21.08.2003), Figure 5B; paragraphs 0064, 0072, 0082, 0083.	27, 28
		1, 2, 4, 13, 14, 25

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents:	
"A"	document defining the general state of the art which is not considered to be of particular relevance
"E"	earlier application or patent published on or after the international filing date
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O"	document referring to an oral disclosure, use, exhibition or other means
"P"	document published prior to the international filing date but later than the priority date claimed
"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&"	document member of the same patent family

Date of the actual completion of the international search

26 September 2004 (26.09.2004)

Date of mailing of the international search report

17 NOV 2004

Name and mailing address of the ISA/US

Mail Stop PCT, Attn: ISA/US  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450

Facsimile No. (703) 305-3230

Authorized officer

JOSE G. DEES

Telephone No. (571) 272-1607

