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#### **Declarations under Rule 4.17:**

- as to applicant's entitlement to apply for and be granted a
  patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

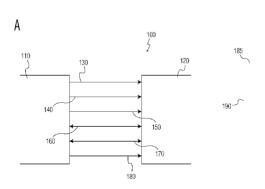
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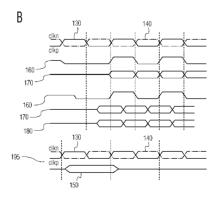
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(54) Title: LATENCY OPTIMIZED RESYNCHRONIZATION SOLUTION FOR DDR/DDR2 SDRAM READ PATH





(57) **Abstract:** An apparatus for synchronizing memory data signals is provided. The apparatus comprises a first interface circuit (110) that is configured to generate a differential clock signal in a strobe domain and to convey a data signal to a data bus (110), a second interface circuit (120) in a clock domain that is configured to receive the data signal (170) from the data bus and a synchronization circuit that is configured to adjust the data signal (170) between the strobe domain and the clock domain such that integrity of information encoded by the data signal is preserved. Methods of using the apparatus are also disclosed.

### INTERNATIONAL SEARCH REPORT

International application No PCT/IB2007/051617

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EPO-Internal, WPI Data												
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