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3D RESISTIVE MEMORY

BACKGROUND

[0001] A resistive memory system, such as a resistive random access memory (ReRAM), has resistive memory elements that can be set to an “ON” state with a low resistance or reset to an “OFF” state with a high resistance. Each resistive memory element may be placed with a selector at a cross-point between a bit line and a word in a cross-point configuration. The selector allows the characteristic of a selected resistive memory element to dominate over partially selected resistive memory elements and minimizes leakage currents in the unselected devices. One type of resistive memory element is a memristor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] In the drawings:

Fig. 1 is a front cross-sectional view of a stack on a substrate in examples of the present disclosure;

Fig. 2 shows an equivalent circuit diagram superimposed over multilayer structures in the stack of Fig. 1 in examples of the present disclosure;

Fig. 3 is a top view of a three-dimensional (3D) memory array with stacks of Fig. 1 in examples of the present disclosure;

Fig. 4 is a top view of a 3D memory array with stacks of Fig. 1 in other examples of the present disclosure;

Fig. 5 is a simplified circuit diagram of a 3D memory array with the stacks of Fig. 1 in examples of the present disclosure;

Fig. 6 is a method for constructing the 3D memory array of Fig. 5 in examples of the present disclosure;

Fig. 7 is a method for constructing the 3D memory array of Fig. 5 in other examples of the present disclosure;

Fig. 8, 9, 10, 11, 12, 13, 14, and 15 are cross-sectional views of a stack formed using the method of Fig. 7 in examples of the present disclosure;

Fig. 16 is a front cross-sectional view of a stack on a substrate in examples of the present disclosure;

Fig. 17 shows an equivalent circuit diagram superimposed over multilayer structures in the stack of Fig. 16 in examples of the present disclosure;

Fig. 18 is a top view of a 3D memory array with stacks of Fig. 16 in examples of the present disclosure;

Fig. 19 is a top view of a 3D memory array with stacks of Fig. 16 in other examples of the present disclosure;

Fig. 20 is a simplified circuit diagram of a 3D memory array with the stacks of Fig. 16 in examples of the present disclosure;

Fig. 21 is a method for constructing the 3D memory array of Fig. 20 in examples of the present disclosure;

Fig. 22 is a method for constructing the 3D memory array of Fig. 20 in other examples of the present disclosure; and

Fig. 23 is a block diagram of a 3D memory system with the 3D memory array of Fig. 5 or 20 in examples of the present disclosure.

[0003] Use of the same reference numbers in different figures indicates similar or identical elements.

DETAILED DESCRIPTION

[0004] As used herein, the term “includes” means includes but not limited to, the term “including” means including but not limited to. The terms “a” and “an” are intended to denote at least one of a particular element. The term “based on” means based at least in part on. The term “or” is used to refer to a nonexclusive such that “A or B” includes “A but not B,” “B but not A,” and “A and B” unless otherwise indicated. The term “above” is used to refer to a layer on or above another layer.

[0005] The cost to three-dimensionally stack layers in a resistive memory system increases dramatically as the number of layers increases due to the use of fine lithography for each layer. The specifications for selectors in a cross-point memory array are also demanding. Thus what is needed is a three-dimensional (3D) resistive memory system that can be constructed with a minimal number of fine masks and use transistors instead of selectors to select a desired resistive memory element and minimize current from partially selected resistive memory elements.

[0006] Fig. 1 is a front cross-sectional view of a stack 100-1 on a substrate 102 in examples of the present disclosure. Stack 100-1 may be one of multiple stacks of the same or similar construction that form a three-dimensional (3D) memory array. Stack 100-1 includes repeating multilayer structures 104-1, 104-2, and 104-3 (collectively as “multilayer structures 104” or individually as a generic “multilayer structure 104”) of the same or similar construction. Although three (3) multilayer structures 104 are shown, stack 100 may include a lesser or greater number of multilayer structures 104. Each multilayer structure 104 includes a first insulator layer 106, a first metal layer 108 above the first insulator layer 106, a second insulator layer 110 above the first metal layer 108, and a second metal layer 112 above the second insulator layer 110. First insulator layer 106 may be silicon dioxide (SiO_2), aluminum oxide (Al_2O_3), or silicon nitride (SiN_3) having a thickness of 10-60 nm, first metal layer 108 may be chromium (Cr) having a thickness of 10-100nm, second insulator layer 110 may be SiO_2 , Al_2O_3 having a thickness of 20-60 nm, and second metal layer 112 may be aluminum having a thickness of 20-60 nm. Stack 100-1 may include an individual first insulator layer 106 above multilayer structure 104-3, and an individual first metal layer 108 above the first insulator layer 106 to cap off stack 100-1.

[0007] Stack 100-1 includes a vertical string 114-1 of resistive memory structures. String 114-1 may be one of multiple strings of the same or similar construction in stack 100-1. String 114-1 may be formed on lateral surfaces of multilayer structures 104 in stack 100-1 exposed by a hole (indicated through a phantom line of symmetry 150 that passes through the middle of the hole) or a trench. Etching the hole where strings 114-1 is to be formed may use a fine mask but otherwise stack 100-1 does not use fine lithography. The trench may be one of multiple trenches etched to form stack 100-1.

[0008] String 114-1 includes a resistive memory layer 116, a vertical channel layer 118, a vertical gate dielectric layer 120, and a vertical gate layer 122. Resistive memory layer 116

may be a metal oxide such titanium dioxide (TiO_2), tantalum pentoxide (Ta_2O_5), or a sub-oxide of Ta_2O_5 having a thickness of 1-20 nm, vertical channel layer 118 may be polysilicon having a thickness of 20-200 nm, vertical gate dielectric layer 120 may be SiO_2 or hafnium oxide (HfO_2) having a thickness of 20-100 nm, and vertical gate layer 122 may be titanium nitride (TiN), titanium tungsten (TiW), tungsten (W), or aluminum (Al) having a thickness of 20-50 nm. Resistive memory layer 116 resides in undercuts of second metal layers 112 (hereafter “second metal undercuts”). Vertical channel layer 118 is formed on the lateral surfaces of first insulator layers 106, first metal layers 108, second insulator layers 110, and the upper and lower edges of resistive memory layer 116 at the mouth of the second metal undercuts. Vertical channel layer 118 is not formed on resistive memory layer 116 in the interior of the second metal undercuts. Vertical gate dielectric layer 120 conforms to vertical channel layer 118 and resistive memory layer 116 in the interior of the second metal undercuts. Vertical gate layer 122 conforms to vertical gate dielectric layer 120 and may fill in the second metal undercuts.

[0009] Fig. 2 shows an equivalent circuit diagram superimposed over multilayer structures 104-2 and 104-3 to illustrate current paths in string 114-1 in examples of the present disclosure. The structures of Fig. 2 may be repeated for additional numbers of multilayer structures 104.

[0010] In each multilayer structure 104, a first (e.g., lower) portion of resistive memory layer 116 in the second metal undercut between the second metal layer 112 and the vertical channel layer 118 forms a first (e.g., lower) resistive memory element (collectively as “first resistive memory element 202” or individually as a generic “first resistive memory element 202”), and a second (e.g., upper) portion of resistive memory layer 116 in the second metal undercut between the second metal layer 112 and the vertical channel layer 118 forms a second (e.g., upper) resistive memory element (collectively as “second resistive memory element 204” or individually as a generic “second resistive memory element 204”). The first resistive memory element 202 is separated by the second insulator layer 110 from the first metal layer 108. For example, resistive memory layer 116 in multilayer structure 104-2 forms a first resistive memory element 202-2 and a second resistive memory element 204-2, and resistive memory layer 116 in multilayer structure 104-3 forms a first resistive memory element 202-3 and a second resistive memory element 204-3.

[0011] Each multilayer structure 104 includes a vertical switch (collectively as “vertical

switches 206” or individually as a generic “vertical switch 206”) that selectively couples the first resistive memory element 202 and the first metal layer 108 in the multilayer structure 104 to provide a current path from the second metal layer 112 through the first resistive memory element 202 to the first metal layer 108 in the multilayer structure 104. For example, in multilayer structure 104-2, a vertical switch 206-2 selectively couples first resistive memory element 202-2 and first metal layer 108-2 to provide a current path from second metal layer 112-2 through first resistive memory element 202-2 to first metal layer 108-2. Vertical switch 206-2 may be a field effect transistor (FET) that includes portions of vertical channel layer 118, vertical gate dielectric layer 120, and vertical gate layer 122 on lateral surfaces of first resistive memory element 202-2, second insulator layer 110-2, first metal layer 108-2, and first insulator layer 106-2. When second metal layer 112-2 is at a higher voltage than first metal layers 108-2, a current flows through first resistive memory element 202-2 to access (read or write) memory element 202-2. Similarly a vertical switch 206-3 selectively couples first resistive memory element 202-3 and first metal layer 108-3 to provide a current path from second metal layer 112-3 through first resistive memory element 202-3 to first metal layer 108-3. As there are rows of devices extending back into the page that would be biased by the application of voltages to metals 112-2, 108-3, and 108-2, a column selection occurs by transistor selection circuitry in complementary metal-oxide-semiconductor (CMOS) electronics in the substrate (described and shown later).

[0012] When a multilayer structure 104 (“first multilayer structure”) has an upper neighboring multilayer structure 104 (“second multilayer structure”), a vertical switch 206 of the second multilayer structure selectively connects the second resistive memory element 204 in the first multilayer structure and a first metal layer 108 in the second multilayer structure to provide a current path from the second metal layer 112 of the first multilayer structure through the second resistive memory element 204 of the first multilayer structure to the first metal layer 108 of the second multilayer structure. For example, a vertical switch 206-3 in multilayer structure 104-3 selectively connects second resistive memory element 204-2 in multilayer structure 104-2 and a first metal layer 108-3 in multilayer structure 104-3 to provide a current path from second metal layer 112-2 of multilayer structure 104-2 through second resistive memory element 204-2 to first metal layer 108-3. When second metal layer 112-2 is at a higher voltage than first metal layers 108-2 and 108-3, currents flow through first and second resistive memory elements 202-2 and 204-2 to access (read or write) both memory elements at the same time.

[0013] Similarly, when the first multilayer structure has a lower neighboring multilayer structure 104 (“third multilayer structure”), the vertical switch 206 of the first multilayer structure selectively connects a second resistive memory element 204 in the third multilayer structure and the first metal layer 108 in the first multilayer structure to provide a current path from a second metal layer 110 of the third multilayer structure through the second resistive memory element 204 of the third multilayer structure to the first metal layer 108 of the first multilayer structure.

[0014] Fig. 3 is a top view of a 3D memory array 300 with stacks 100-1 and 100-2 on substrate 102 in examples of the present disclosure. Stack 100-1 has vertical strings 114-1, 114-2, and 114-3 (collectively as “strings 114” or generically as an individual “string 114”) formed in holes etched into stack 100-1. These holes may be of any shape such as circular or square. Although three (3) strings 114 are shown, stack 100-1 may include a lesser or greater number of strings 114. Stack 100-1 also has a terraced end 302 that exposes first metal layers 108 and second metal layers 112. Stack 100-2 has the same or similar construction as stack 100-1. Although two (2) stacks (collectively as “stacks 100” or generically as an individual “stack 100”) are shown, 3D memory array 300 may include a lesser or greater number of stacks 100. The whole structure is covered with a dielectric in which holes are etched down to contact the various steps of terrace ends 302. The stack can be selected by applying appropriate voltages and measuring current flow through the various electrodes contacting the terrace steps.

[0015] Fig. 4 is a top view of a 3D memory array 400 with stacks 100-1 and 100-2 on substrate 102 in other examples of the present disclosure. Stack 100-1 has strings 114-1, 114-2, and 114-3 formed on a side of stack 100-1 formed by a trench 402. Although three (3) strings 114 are shown, stack 100-1 may include a lesser or greater number of strings 114. For example, additional strings 114-4, 114-5, and 114-6 may be formed on another side of stack 100-1 formed by another trench 404. Ideally the various strings 114 would be isolated from each other by patterning on the sidewall of trenches 402 and 404. For example, some patterned protective resist with the vertical strips would be applied. Then all the layer material between the strips would be removed including the undercut with chemical etching. Stack 100-2 has the same or similar construction as stack 100-1. Although two (2) stacks 100 are shown, 3D memory array 400 may include a lesser or greater number of stacks 100.

[0016] Fig. 5 is a simplified circuit diagram of a 3D memory array 500 with stacks 100-1 and

100-2 in examples of the present disclosure. Although two (2) stacks 100 are shown, 3D memory array 500 may have a greater or less number of stacks 100. Strings 114 in stack 100 have one end (e.g., a lower end) selectively connected to a supply voltage by string selection circuits 504 -1, 504-2, and 504-3 (collectively as “string selection circuits 504” or generically as an individual “string selection circuit 504”), which are controlled by bit lines 506-1, 506-2 and word lines 508-1, 508-2, 508-3. Pairs of memory elements 202 and 204 connected to the same second metal layer 112 are said to be located in the same memory plane. For the sake of clarity, plane selection circuits used to select a memory plane is not shown but they may be of the same or similar constructions as string selection circuits 504.

[0017] To access a pair of memory elements, the string 114 containing the pair is selected by applying appropriate voltages to a bit line and a word line to turn the corresponding string selection circuit 504, which then turns on all vertical switches 206 in that string. For example, to access a pair 510 of memory elements 202-2 and 204-2, string 114-1 is selected by turning on string selection circuit 504-1, which then turns on all vertical switches 206 in string 114-1. A memory plane with pair 510 is selected by applying appropriate voltages to turn on the corresponding plane selection circuits, which apply a higher voltage to the second metal layer 112 of the memory plane than the two first metal layers 108 located above and below the second metal layer 112. The two first metal layers 108 may be coupled to sensing or programming circuits to read or write memory elements 202-2 and 204-2. The second metal layer 112 in any adjacent memory plane is floated to isolate the memory planes. As described, vertical switches or transistors 206 are used instead of selectors to select a pair of resistive memory elements and minimize current from partially selected resistive memory elements.

[0018] Fig. 6 is a method 600 for constructing 3D memory array 500 (Fig. 5) with stacks 100 (Fig. 1) in examples of the present disclosure. Although the blocks in method 600, and any method described hereafter, are illustrated in a sequential order, these blocks may also be performed in parallel or in a different order than those described herein. Also, the various blocks may be combined into fewer blocks, divided into additional blocks, or eliminated based upon the desired implementation. Method 600 may begin in block 602.

[0019] In block 602, multiple layers are repeatedly deposited on substrate 102 (Fig. 1). These layers includes first insulator layer 106 (Fig. 1), first metal layer 108 (Fig. 1), second insulator layer 110 (Fig. 1), and second metal layer 112 (Fig. 1). Block 602 may be followed

by block 604.

[0020] In block 604, holes or trenches are etched in the resulting structure. Block 604 may be followed by block 606.

[0021] In block 606, first insulator layers 106 (Fig. 1) in the structure are undercut by removing second metal layers 112 exposed by the holes or the trenches. Block 606 may be followed by block 608.

[0022] In block 608, resistive memory layer 116 (Fig. 1) is formed in undercuts created in second metal layers 112. Block 608 may be followed by block 610.

[0023] In block 610, vertical channel layer 118 (Fig. 1) is formed over lateral surfaces of the structure exposed by the holes or trenches but not over resistive memory layer 116 in the interior of the second metal undercuts. Block 610 may be followed by block 612.

[0024] In block 612, vertical gate dielectric layer 120 (Fig. 1) is formed over channel layer 118. Block 612 may be followed by block 614.

[0025] In block 614, vertical gate layer 122 (Fig. 1) is formed over gate dielectric layer 120.

[0026] Fig. 7 is a method 700 for constructing 3D memory array 500 (Fig. 5) with stacks 100 (Fig. 1) in examples of the present disclosure. Method 700 may be a variation of method 600. Method 700 may begin in block 702.

[0027] In block 702, lower level circuits are formed in substrate 102 (Fig. 1). These circuits may include CMOS accessing circuits such as a column decoder, a row decoder, a memory plane decoder, string selection circuits, and memory plane selection circuits. Block 702 may be followed by block 704.

[0028] In block 704, multiple layers are repeatedly deposited on substrate 102 (Fig. 1). These layers includes first insulator layer 106 (Fig. 1), first metal layer 108 (Fig. 1), second insulator layer 110 (Fig. 1), and second metal layer 112 (Fig. 1). The deposition process may be atomic layer deposition, sputtering, plasma enhanced chemical vapor deposition, or other deposition methods creating uniform materials. Block 704 corresponds to block 602 (Fig. 6) in method 600 (Fig. 6). Block 704 may be followed by block 706.

[0029] In block 706, trenches are etched in the resulting structure to form stacks with

multilayer structures 104 (Fig. 1). The etching may be the Bosch process, direction ion sputtering, or any other etching process producing high aspect ratio features through the layer. Fig. 8 shows a front cross-sectional view of a representative stack 800 in examples of the present disclosure. Block 706 may be followed by optional block 708 when strings of resistive memory structure are to be formed in holes.

[0030] In optional block 708, holes are etched into stacks 800. The etching may be the Bosch process, direction ion sputtering, or any other etching process producing high aspect ratio features through the layer. Optional block 708 may be followed by block 710.

[0031] In block 710, as shown in Fig. 9, first insulator layers 106 (Fig. 1) in the structure are undercut by preferentially etching second metal layers 112 exposed by the holes or the trenches. For example, the exposed second metal layers 112 are wet etched to form second metal undercuts 902. Block 710 corresponds to block 606 (Fig. 6) in method 600. Block 710 may be followed by block 712.

[0032] In block 712, as shown in Fig. 10, resistive memory layer 116 is deposited over and conforms to the lateral surfaces of stacks 800, including second metal undercuts 902 (Fig. 9), exposed by the holes or trenches. The deposition process may be any conformal deposition process such as chemical vapor deposition with a low sticking coefficient so that the step terraces are covered. Block 712 corresponds to block 608 in method 600. Block 712 may be followed by block 714.

[0033] In block 714, as shown in Fig. 10, a sacrificial layer 1002 is deposited over and conforms to resistive memory layer 116. Sacrificial layer 102 may be SiO₂ or Al if the other metals are not Al. The deposition process may be any conformal deposition method such as a chemical vapor deposition with a low sticking coefficient so that the steps are covered. Block 714 may be followed by block 716.

[0034] In block 716, as shown in Fig. 11, the holes or trenches are cut to remove part of sacrificial layer 1002 and resistive memory layer 116 so they remain within second metal undercuts 902. The etching process may be an anisotropic etching that removes the vertical deposition not on the undercut portion. Block 716 may be followed by block 718.

[0035] In block 718, as shown in Fig. 12, vertical channel layer 118 is deposited over and conforms to the lateral surfaces of stacks 800, including resistive memory layer 116 and

sacrificial layer 1002 within second metal undercuts 902, exposed by the holes or trenches. The deposition process may be any conformal deposition process such as chemical vapor deposition with a low sticking coefficient so that the steps are covered. Block 718 may be followed by block 720.

[0036] In block 720, as shown in Fig. 12, vertical gate dielectric layer 120 is deposited over and conforms to vertical channel layer 118. The deposition process may be any conformal deposition process such as chemical vapor deposition with a low sticking coefficient so that the steps are covered. Block 720 corresponds to block 612 (Fig. 6) of method 600. Block 720 may be followed by block 722.

[0037] In block 722, as shown in Fig. 13, sacrificial layer 1002 (Fig. 10) with channel and gate dielectric overlay is removed so no channel and the gate dielectric materials remain within second metal undercuts 902. Sacrificial layer 1002 (Fig. 10) with channel and gate dielectric overlay may be removed with a wet etch. Note that vertical channel layer 118 remains over the lateral edges of resistive memory layer 116 at the mouths of the second metal undercuts. Blocks 718, 720, and 722 correspond to block 610 (Fig. 6) of method 600 that forms vertical channel layer 118. Block 722 may be followed by block 724.

[0038] In block 724, as shown in Fig. 14, additional gate dielectric material is deposited over the lateral surfaces of stacks 800 exposed by the holes or trenches so vertical gate dielectric layer 120 again covers resistive memory layer 116 within second metal undercuts 902. Block 724 corresponds to block 612 (Fig. 6) of method 600. Block 724 may be followed by block 726.

[0039] In block 726, as shown in Fig. 14, vertical gate layer 122 is deposited over and conforms to vertical gate dielectric layer 120. The deposition process may be any conformal deposition process such as chemical vapor deposition with a low sticking coefficient so that the steps are covered. Vertical gate layer 122 may fill in second metal undercuts 902. Block 726 corresponds to block 614 (Fig. 6) of method 600. Block 726 may be followed by optional block 728.

[0040] In optional block 728, when strings 114 of resistive memory structures are formed on trench sidewalls of stacks 800, vertical gate layer 122, vertical gate dielectric layer 120, vertical channel layer 118, and resistive memory layer 116 are etched to form individual and isolated strings 114. Patterned protective resist in vertical strips may be applied. Then all the

layer materials between the strips would be removed including those in the undercut with chemical etching. Optional block 728 may be followed by block 730.

[0041] In block 730, as shown by a side cross-sectional view in Fig. 15, one end of stacks 800 are etched to form a terraced end 1502 to expose first metal layers 108 and second metal layers 112. The etching process may be an anisotropic etch that removes the vertical deposition not on the undercut portion. The etching process may even etch some of first metal layers 108 and first insulator layers 106. For example, if the etching process is caused by ion bombardment, only surfaces which are parallel or at a tilt of less than 90 degrees will get etched. Surfaces on the underside will be protected from etching. The direction etching can etch straight down like a drill and remove layers on the side wall namely 108 and 106. The exposed first metal layers 108 and second metal layers 112 may then be connected by conductors to a memory plane decoder to receive appropriate voltages for selecting a memory plane.

[0042] Fig. 16 is a front cross-sectional view of a stack 1600-1 on a substrate 1602 in examples of the present disclosure. Stack 1600-1 may be one of multiple stacks of the same or similar construction that form a 3D memory array. Stack 1600-1 includes repeating multilayer structures 1604-1, 1604-2, 1604-3, and 1604-4 (collectively as “multilayer structures 1604” or individually as a generic “multilayer structure 1604”). Although four (4) multilayer structures 1604 are shown, stack 1600-1 may include a lesser or greater number of multilayer structures 1604. Each multilayer structure 1604 includes a gate layer 1606 and an insulator layer 1608 above the gate layer 1606. Gate layer 1606 may be TiW, molybdenum (Mo), Al, or Ti having a thickness of 10-50 nm, and insulator layer 1608 may be SiO₂, Si₃N₄, HfO₂, or some combination of dielectrics having a thickness of 10-200 nm.

[0043] Stack 1600-1 also includes a vertical gate dielectric layer 1616 formed lateral surfaces of multilayer structure 1604 exposed by a hole or trench, a vertical channel layer 1618 on the vertical gate dielectric layer 1616, and a vertical resistive memory layer 1620 on the vertical channel layer 1618. Vertical gate dielectric layer 1616 may be SiO₂, Si₃N₄, HfO₂ having a thickness of 10-30 nm, vertical channel layer 1618 may be polysilicon or a transition metal oxide such as indium gallium tin oxide having a thickness of 10-40 nm, and vertical resistive memory layer 1620 may be tantalum dioxide (TaO₂), TiO₂, or HfO₂ having a thickness of 3-25 nm.

[0044] Fig. 17 shows an equivalent circuit diagram superimposed over stack 1600-1 in examples of the present disclosure. Stack 1600-1 includes a string 1702-1 of resistive memory structures. String 1702-1 includes vertical switches 1704-1, 1704-2, 1704-3, and 1704-4 (collectively as “vertical switches 1704” or individually as a generic “vertical switch 1704”) coupled in series. Vertical switches 1704 may be FET transistors each formed with a gate layer 1604 and portions of vertical gate dielectric layer 1616 and vertical channel layer 1618 in the same memory plane as the gate layer 1604. Note that insulator layers 1606 are of a thickness that vertical switches 1704 are coupled in series even though gate layers 1604 do not overlap parts of channel layer 1618.

[0045] String 1702-1 also includes resistive memory elements 1708-2, 1708-3, and 1708-4 (collectively as “resistive memory elements 1708” or individually as a generic “resistive memory element 1708”) formed in vertical resistive memory layer 1620. A resistive memory element 1708 laterally offset from a gate layer 1604 of a vertical switch 1704 is said to be in located in the same memory plane as the vertical switch 1704. Each resistive memory element 1708 is coupled in parallel to a vertical switch 1704 in the same memory plane.

[0046] The on resistance of vertical switches 1704 is lower than both the on and off resistance of resistive memory elements 1708 so that when a vertical switch 1704 is turned on a current passes through the vertical switch 1740 and bypasses the resistive memory element 1708 coupled parallel to the vertical switch 1740. The off resistance of vertical switches 1704 is greater than both the on and off resistance of resistive memory elements 1708 so that when a vertical switch 1704 is turned off a current bypasses the vertical switch 1740 and passes through the resistive memory element 1708 coupled parallel to the vertical switch 1740. The switch on resistance is 1-50 kOhms so both the on and off resistance of resistive memory elements 1 should be at least 100 kOhms and higher. To read a resistive memory element 1708 of a particular memory plane, all vertical switches 1704 but the one for the memory plane is turned on so current passes through the resistive memory element 1708 in that memory plane.

[0047] Fig. 18 is a top view of a 3D memory array 1800 with stacks 1600-1 and 1600-2 on substrate 1602 in examples of the present disclosure. Stack 1600-1 has strings 1702-1, 1702-2, and 1702-3 (collectively as “strings 1702” or individually as a generic “string 1702”) formed in holes etched into stack 1600-1. Although three (3) strings 1702 are shown, stack 1600-1 may include a lesser or greater number of strings 1702. Stack 1600-1 also has a

terraced end 1802 that exposes gate layers 1604. Stack 1600-2 has the same or similar construction as substrate 1600-1. Although two (2) stacks (collectively as “stacks 1600” or generically as an “individual stack 1600”) are shown, 3D memory array 1800 may include a lesser or greater number of stacks 1600.

[0048] Fig. 19 is a top view of a 3D memory array 1900 with stacks 1600-1 and 1600-2 on substrate 1602 in other examples of the present disclosure. Stack 1600-1 has strings 1702-1, 1702-2, and 1702-3 formed on a side of stack 1600-1 formed by a trench 1902. Although three (3) strings 1702 are shown, stack 1600-1 may include a lesser or greater number of strings 1702. For example, additional strings 1702-4, 1702-5, and 1702-6 may be formed on another side of stack 1600-1 formed by a trench 1904. Stack 1600-2 has the same or similar construction as stack 1600-1. Although two (2) stacks (collectively as “stacks 1600” or generically as an “individual stack 1600”) are shown, 3D memory array 1800 may include a lesser or greater number of stacks 1600.

[0049] Fig. 20 is a simplified circuit diagram of a 3D memory array 2000 with stacks 1600-1 and 1600-2 in examples of the present disclosure. Although two (2) stacks 1600 are shown, 3D memory array 2000 may have a greater or less number of stacks 1600. Strings 1702 in a stack 1600 have one end (e.g., the top end) coupled to a supply voltage and another end (e.g., the lower end) selectively coupled to ground by string selection circuits 2004-1, 2004-2, and 2004-3 (collectively as “string selection circuits 2004” or generically as an individual “string selection circuit 2004”), which are controlled by bit lines 2006-1, 2006-2 and word lines 2008-1, 2008-2, 2008-3. Resistive memory elements 1708 that are connected to the same gate layer 1604 are said to be located in the same memory plane. For the sake of clarity, plane selection circuits used to select a memory plane is not shown but they may be of the same or similar constructions as string selection circuits 504.

[0050] To access a memory element 1708, the string 1702 containing the memory element 1708 is selected by applying appropriate voltages to a bit line and a word line to turn the corresponding string selection circuit 2004, which provides a potential difference from one end of the string 1702 to the other end. For example, to access memory element 1708-2 in string 1702-1, string 1702-1 is selected by turning on string selection circuit 2004-1. The memory plane with memory element 1708-2 is selected by applying appropriate voltages to turn on the corresponding plane selection circuits, which turn on vertical switches 1704-1, 1704-3, and 1704-4 but not vertical switch 1704-2 of the memory plane with the resistive

memory element 1708-2 being accessed, which forces a current to pass through resistive memory element 1708-2 in that memory plane.

[0051] Fig. 21 is a method 2100 for constructing 3D memory array 2000 (Fig. 20) with stacks 1600 (Fig. 16) in examples of the present disclosure. Method 2100 may begin in block 2102.

[0052] In block 2102, multiple layers are repeatedly deposited on substrate 1602 (Fig. 16). These layers include gate layer 1604 and insulator layer 1606 (Fig. 1). Block 2102 may be followed by block 2104.

[0053] In block 2104, holes or trenches are etched in the resulting structure. Block 2104 may be followed by block 2106.

[0054] In block 2106, vertical gate dielectric layer 1616 (Fig. 16) is deposited over lateral surfaces of the structure exposed by the holes or trenches. Block 2106 may be followed by block 2108.

[0055] In block 2108, vertical channel layer 1618 (Fig. 16) is deposited over vertical gate dielectric layer 1616. Block 2108 may be followed by block 2110.

[0056] In block 2110, resistive memory layer 1620 (Fig. 16) is deposited over the vertical channel layer 1618.

[0057] Fig. 22 is flowchart of a method 2200 for constructing 3D memory array 2000 (Fig. 20) with stacks 1600 (Fig. 16) in examples of the present disclosure. Method 2200 may be a variation of method 2100. Method 2200 may begin in block 2202.

[0058] In block 2202, lower level circuits are formed in substrate 1602 (Fig. 16). These circuits may include CMOS accessing circuits such as a column decoder, a row decoder, a memory plane decoder, string selection circuits, and memory plane selection circuits. Block 2202 may be followed by block 2204.

[0059] In block 2204, multiple layers are repeatedly deposited on substrate 1602 (Fig. 16). These layers include gate layer 1604 and insulator layer 1606 (Fig. 1). The deposition process may be atomic layer deposition, sputtering, plasma enhanced chemical vapor deposition, or other deposition methods creating uniform materials. Block 2204 corresponds

to block 2102 (Fig. 21) in method 2100 (Fig. 21). Block 2204 may be followed by block 2206.

[0060] In block 2206, trenches are etched in the resulting structure to form stacks 1600 as shown in Fig. 18 or 19. The etching process may be the Bosch process, direction ion sputtering, or any other etching process producing high aspect ratio features through the layer. Block 2206 may correspond to block 2104 (Fig. 21) of method 2100 when strings 1702 are formed on trench sidewalls. Block 2206 may be followed by optional block 2208 when strings of resistive memory structure are to be formed in holes.

[0061] In optional block 2208, holes are etched into stacks 1600. The etching process may be the Bosch process, direction ion sputtering, or any other etching process producing high aspect ratio features through the layer. Optional block 2208 corresponds to block 2104 of method 2100 when strings 1702 are formed in holes. Optional block 2208 may be followed by block 2210.

[0062] In block 2210, vertical gate dielectric layer 1616 (Fig. 16) is deposited over and conforms to lateral surfaces of stacks 1600 exposed by the holes or trenches. The deposition process may be atomic layer deposition, sputtering, plasma enhanced chemical vapor deposition, or other deposition methods creating uniform materials. Block 2210 corresponds to block 2106 (Fig. 21) of method 2100. Block 2210 may be followed by block 2212.

[0063] In block 2212, vertical channel layer 1618 (Fig. 16) is deposited over and conforms to vertical gate dielectric layer 1616. The deposition process may be atomic layer deposition, sputtering, plasma enhanced chemical vapor deposition or other deposition methods creating uniform materials. Block 2212 corresponds to block 2108 (Fig. 21) of method 2100. Block 2212 may be followed by block 2214.

[0064] In block 2214, resistive memory layer 1620 (Fig. 16) is deposited over and conforms to the vertical channel layer 1618. The deposition process may be atomic layer deposition, sputtering, plasma enhanced chemical vapor deposition or other deposition methods creating uniform materials. Block 2214 corresponds to block 2110 (Fig. 21) of method 2100. Block 2212 may be followed by optional block 2216.

[0065] In optional block 2216, when strings 1702 of resistive memory structures are formed on trench sidewalls of stacks 1600, resistive memory layer 1620, vertical channel layer 1618,

and vertical gate dielectric layer 1616 are etched to form individual and isolated strings 1702. The etching may be the Bosch process, direction ion sputtering, or any other etching process producing high aspect ratio features through the layer. Optional block 2216 may be followed by block 2218.

[0066] In block 2218, as shown in Figs. 18 and 19, one end of stacks 1600 are etched to form terraced end 1802 to expose gate layers 1604. The etching may be the Bosch process, direction ion sputtering, or any other etching process producing high aspect ratio features through the layer. The exposed gate layers 1604 may then be connected by conductors to a memory plane decoder to receive appropriate voltages for selecting a memory plane.

[0067] Fig. 23 is a block diagram of a 3D memory system 2300 in examples of the present disclosure. System 2300 includes 3D memory array 500 or 2000 (Fig. 5 or 20), a row decoder 2302, a column decoder 2304, a memory plane decoder 2306, a controller or state machine 2308, and voltage supplies 2310. Controller 2308 may use row decoder 2302 and column decoder 2304 to select a string of resistive memory structure, and memory plane decoder 2306 to select a memory plane of the selected string. Controller 2308 applies the appropriate voltages from voltage supplies 2310 to access (read or write) selected resistive memory elements.

[0068] Various other adaptations and combinations of features of the examples disclosed are within the scope of the invention.

CLAIMS

What is claimed is:

Claim 1: A memory array, comprising:

a substrate;

stacks on the substrate, each stack comprising:

multilayer structures, each multilayer structure comprising:

a first insulator layer;

a first metal layer above the first insulator layer;

a second insulator layer above the first metal layer; and

a second metal layer above the second insulator layer; and

strings of resistive memory structures, each string of resistive memory structures comprising, in each multilayer structure:

a resistive memory element in an undercut of the second metal layer, the resistive memory element being separated by the second insulator layer from the first metal layer; and

a vertical switch that selectively connects the resistive memory element and the first metal layer to provide a current path from the second metal layer through the resistive memory element to the first metal layer.

Claim 2: The memory array of claim 1, wherein:

the vertical switch comprises:

a vertical channel on lateral surfaces of the first metal layer, the second insulator layer, and the resistive memory element;

a vertical gate dielectric on the vertical channel; and

a vertical gate on the gate dielectric; and

the vertical channel, the vertical gate dielectric, and the vertical gate form a transistor that connects the resistive memory element and the first metal layer.

Claim 3: The memory array of claim 1, wherein:

each string of resistive memory structures further comprises, in each multilayer structure, another resistive memory element in the undercut of the second metal layer; and

another vertical switch selectively connects the other resistive memory element and another first metal layer in another multilayer structure to provide another current path from the second metal layer through the other resistive memory element to the other first metal layer.

Claim 4: The memory array of claim 3, wherein:

the resistive memory element comprises a first portion of a resistive memory layer deposited in the undercut, the first portion being located between the second metal layer and the vertical channel; and

the other memory element comprises a second portion of the resistive memory layer deposited in the undercut, the second portion being located between the second metal layer and the other vertical channel.

Claim 5: The memory array of claim 1, wherein:

each string of resistive memory structures is formed in a hole or on a trench sidewall of a stack;

each stack has a terraced end exposing the first metal layer and the second metal layer in each multilayer structure; and

the substrate comprises accessing circuits.

Claim 6: A method to form a memory array, comprising:

repeatedly depositing layers to form a structure on a substrate, the layers comprising a first insulator layer, a first metal layer above the insulator layer, a second insulator layer above the first metal layer, and a second metal layer above the second insulator layer;

cutting holes or trenches in the structures;

undercutting second metal layers in the structures that are exposed by the holes or the trenches;

forming a resistive memory layer in the undercuts;

forming a vertical channel layer on lateral surfaces of the structures that are exposed by the holes or the trenches but not on the resistive memory layer in an interior of the undercuts;

forming a vertical gate dielectric layer over the channel layer; and

forming a vertical gate layer over the gate dielectric layer.

Claim 7: The method of claim 6, wherein, in each multilayer structure comprising the first insulator layer, the first metal layer, the second insulator layer, and the second metal layer:

the resistive memory layer forms a resistive memory element in each undercut; and

the vertical channel layer, the vertical gate dielectric layer, and the vertical gate layer form a transistor that selectively connects the resistive memory element and the first metal layer to provide a current path from the second metal layer through the resistive memory element to the first metal layer.

Claim 8: The method of claim 7, wherein, in each multilayer structure in each multilayer structure comprising the first insulator layer, the first metal layer, the second insulator layer, and the second metal layer:

the resistive memory material forms another resistive memory element in each undercut; and

the vertical channel layer, the vertical gate dielectric layer, and the vertical gate layer form another transistor that selectively connects the other resistive memory element

and another first metal layer in another multilayer structure to provide another current path from the second metal layer through the other resistive memory element to the other first metal layer.

Claim 9: The method of claim 6, further comprising:

forming accessing circuits in the substrate before repeatedly depositing the layers on the substrate;

cutting the structure to form stacks; and

etching the stacks to form terraced ends that expose first metal layers and second metal layers.

Claim 10: A memory array, comprising:

a substrate;

stacks on the substrate, each stack comprising:

strings of resistive memory structures, each string of resistive memory structure comprising:

vertical switches coupled in series; and

resistive memory elements, each resistive memory element being coupled in parallel to a vertical switch in a same plane.

Claim 11: The memory array of claim 10, wherein:

the vertical switches comprise transistors and transistors in a same plane have gates comprising a same metal layer;

each stack comprises:

multilayer structures, each multilayer structure comprising a gate layer and an insulator layer above the gate layer;

a vertical gate dielectric layer on lateral surfaces of the multilayer structures;

a vertical channel layer on the vertical gate dielectric layer; and

a vertical resistive memory layer on the vertical channel layer;

the vertical gate layer and portions of the vertical gate dielectric layer and vertical channel layer in a same plane as the gate layer forms a vertical switch, and a portion of the vertical resistive memory layer in the same plane as the gate layer forms a resistive memory element coupled in parallel to the vertical switch.

Claim 12: The memory array of claim 11, wherein:

the vertical gate dielectric layer, the vertical channel layer, and the vertical resistive memory layer are formed in a hole or on a trench sidewall of a stack;

each stack has a terraced end exposing the gate layer in each multilayer structure; and

the substrate comprises accessing circuits.

Claim 13: A method to form a memory array, comprising:

repeatedly depositing layers on a substrate, the layers comprising a gate layer and an insulator layer above the gate layer;

cutting holes or trenches to expose lateral surfaces of the structures;

depositing a gate dielectric layer over the lateral surfaces of the structure exposed by the holes or the trenches;

depositing a channel layer on the gate dielectric layer; and

depositing a resistive memory layer on the channel layer.

Claim 14: The method of claim 13, wherein:

the gate layer and portions of the vertical gate dielectric layer and vertical channel layer in a same plane as the gate layer forms a vertical switch; and

a portion of the vertical resistive memory layer in the same plane as the gate layer forms a resistive memory element coupled in parallel to the vertical switch.

Claim 15: The method of claim 13, further comprising:

forming accessing circuits in the substrate before repeatedly depositing the layers on the substrate;

cutting the structure to form stacks; and

etching the stacks to form terraced ends that expose gate layers.

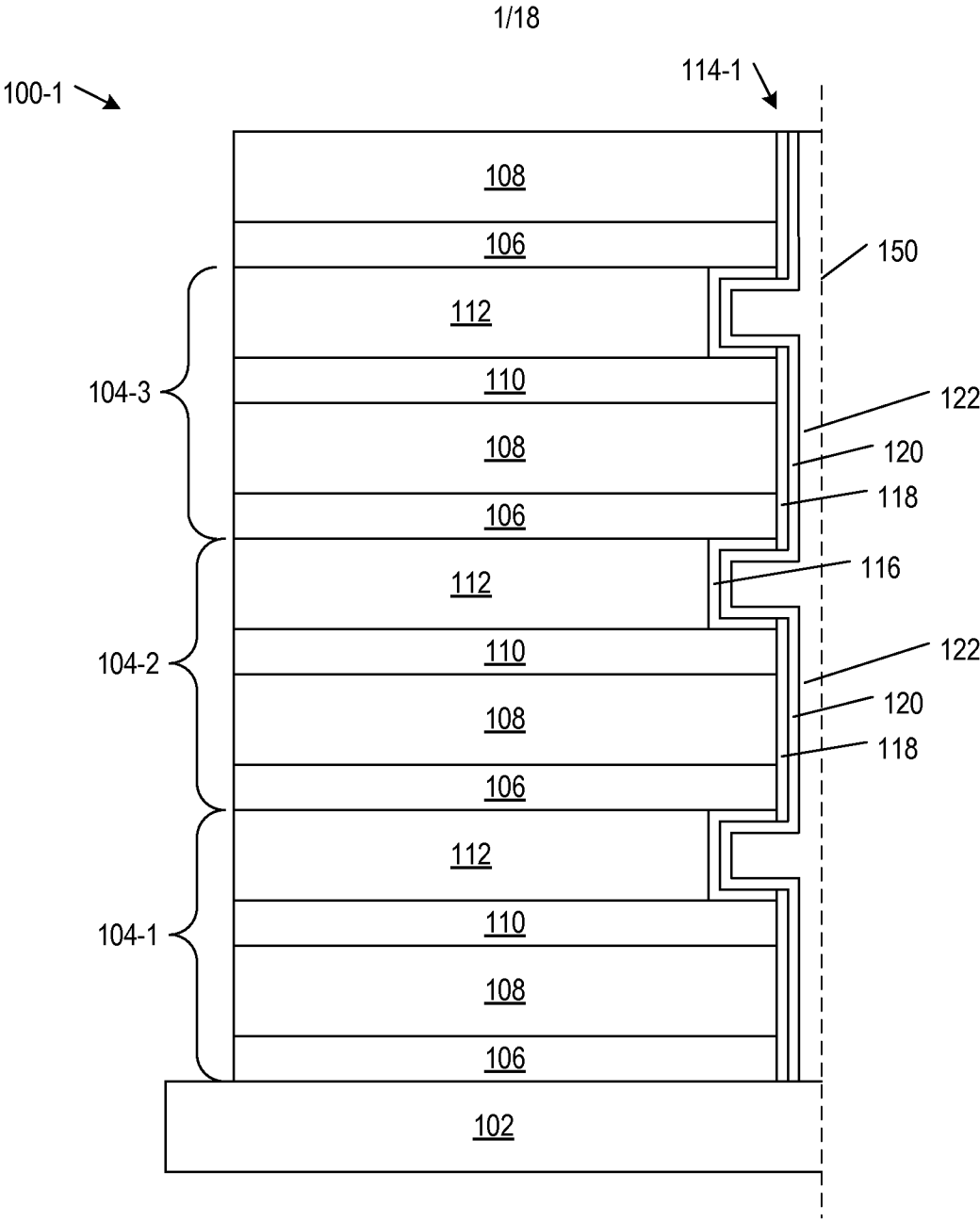


FIG. 1

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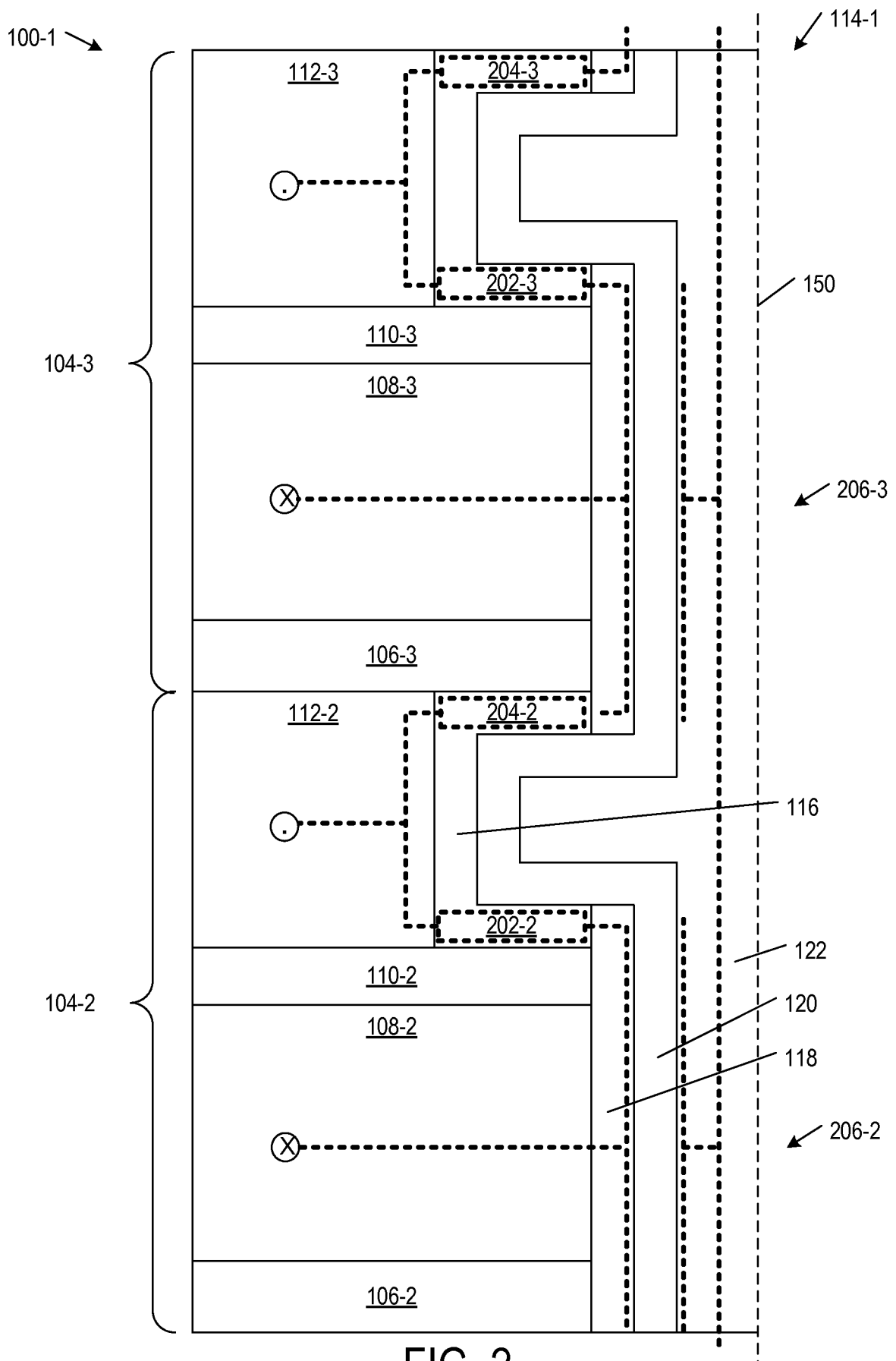


FIG. 2

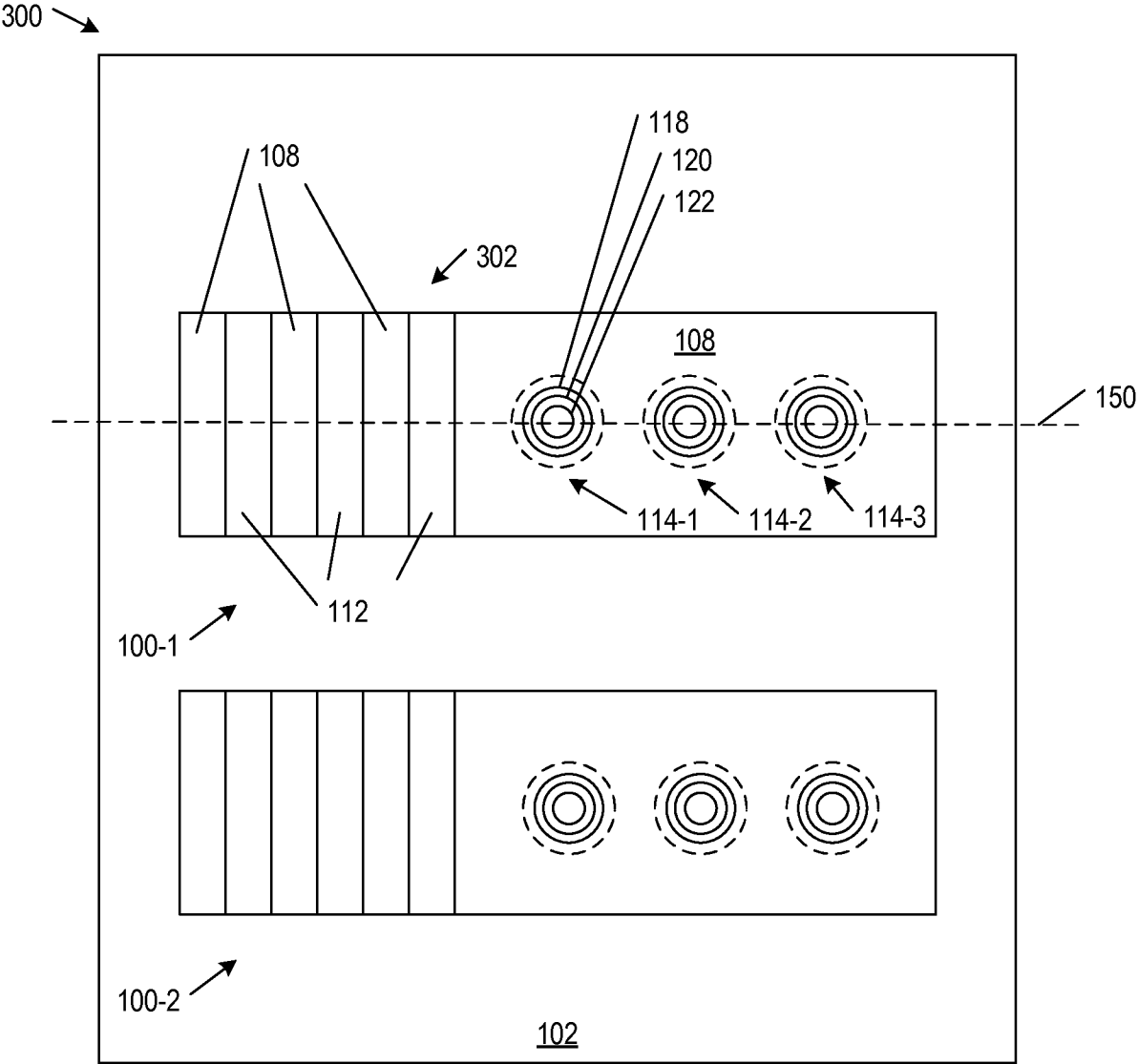


FIG. 3

400 →

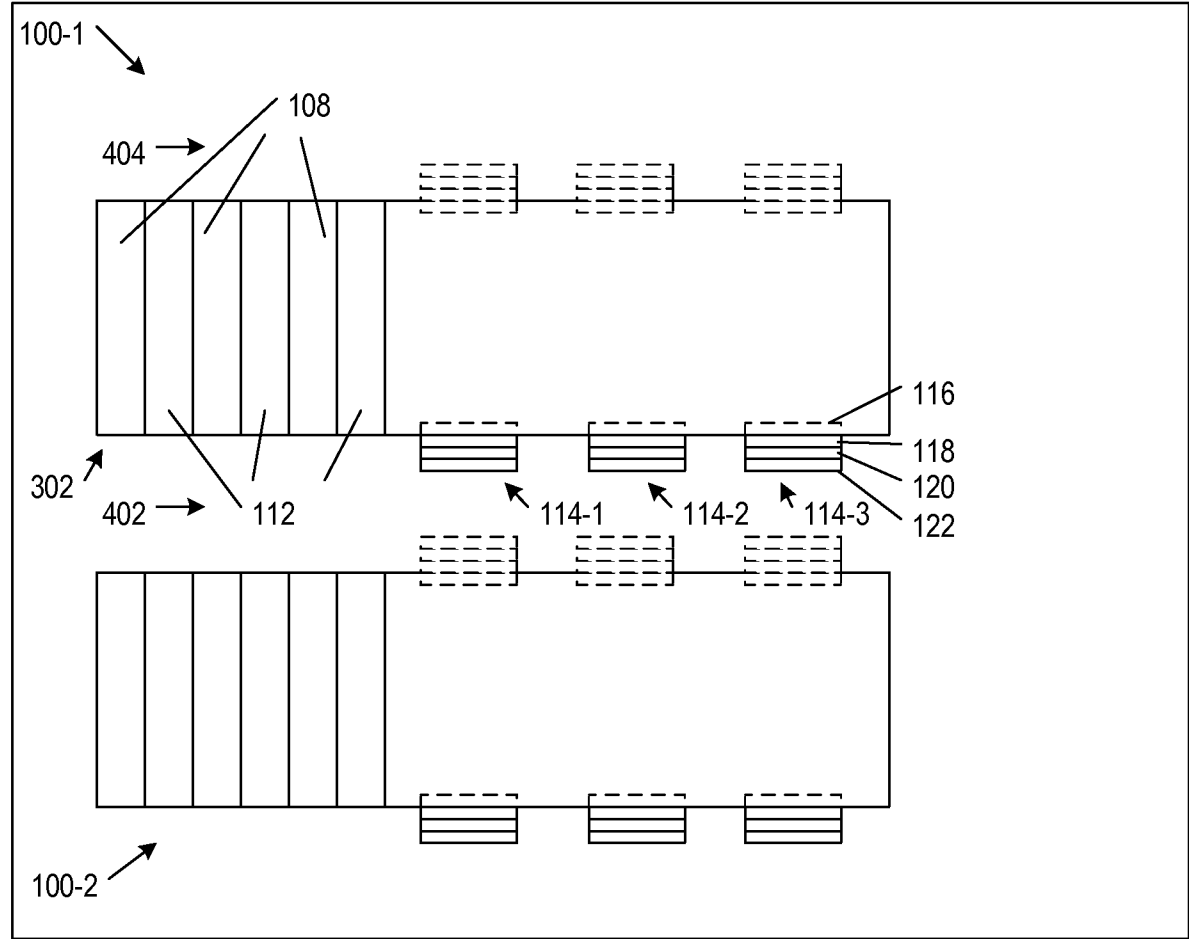


FIG. 4

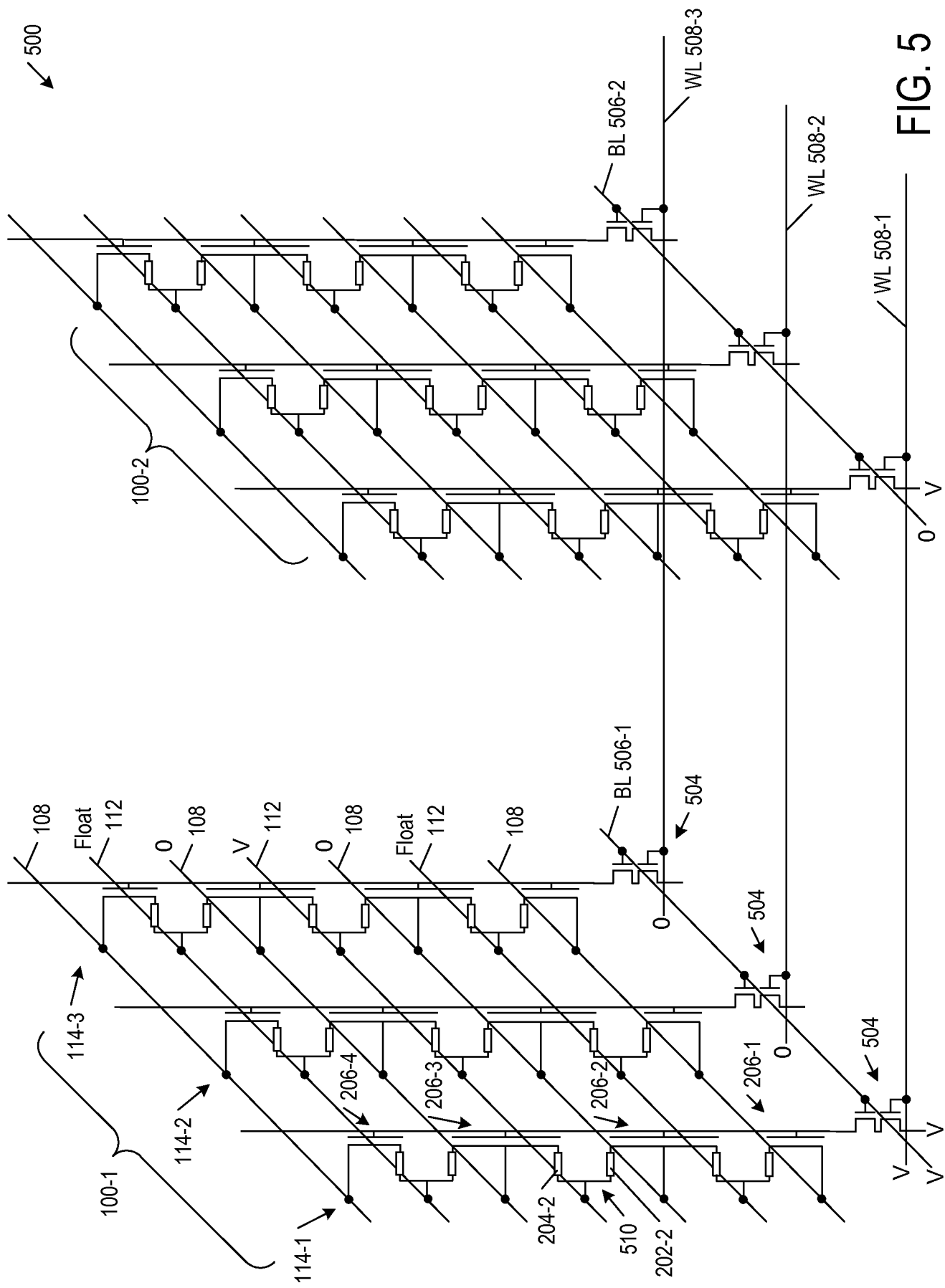


FIG. 5

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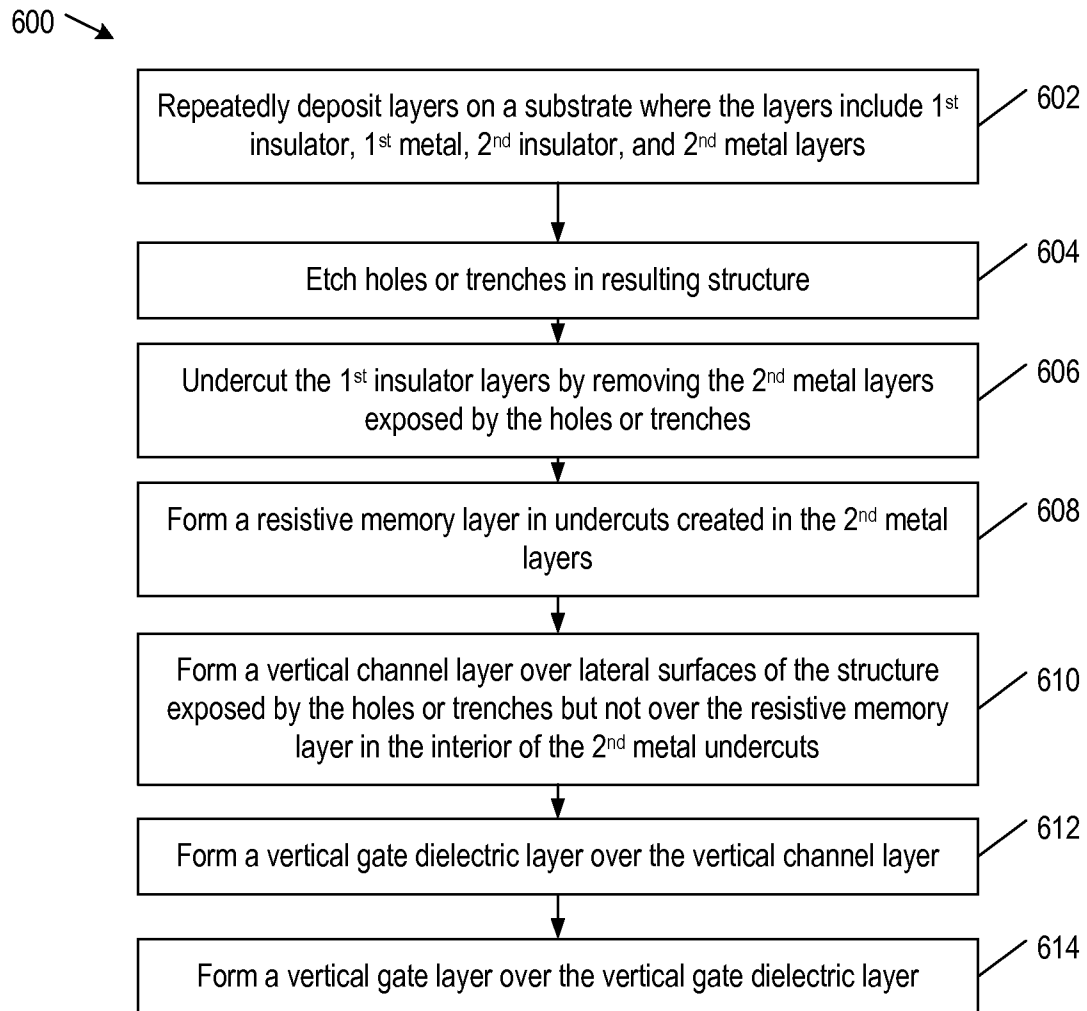


FIG. 6

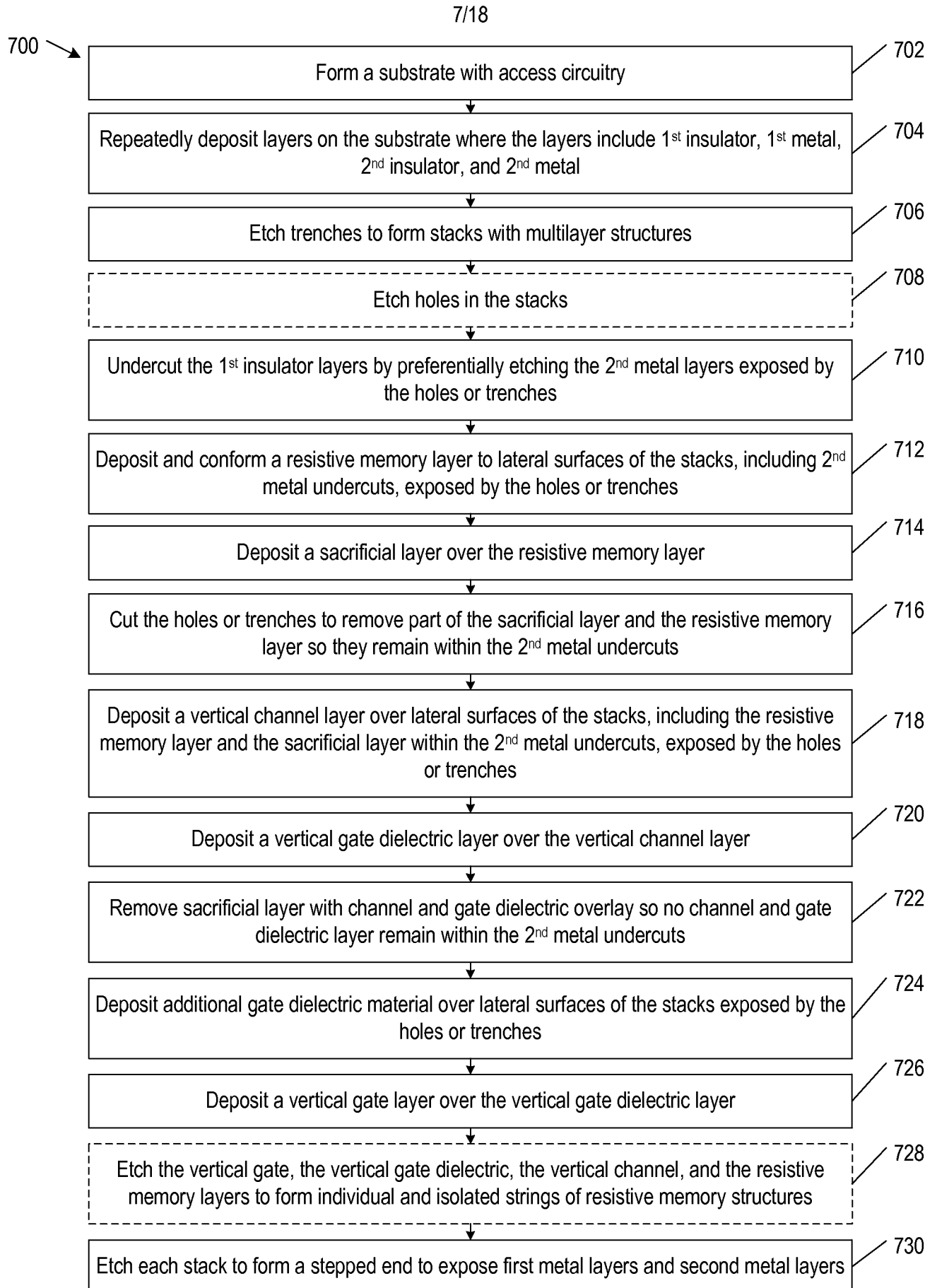


FIG. 7

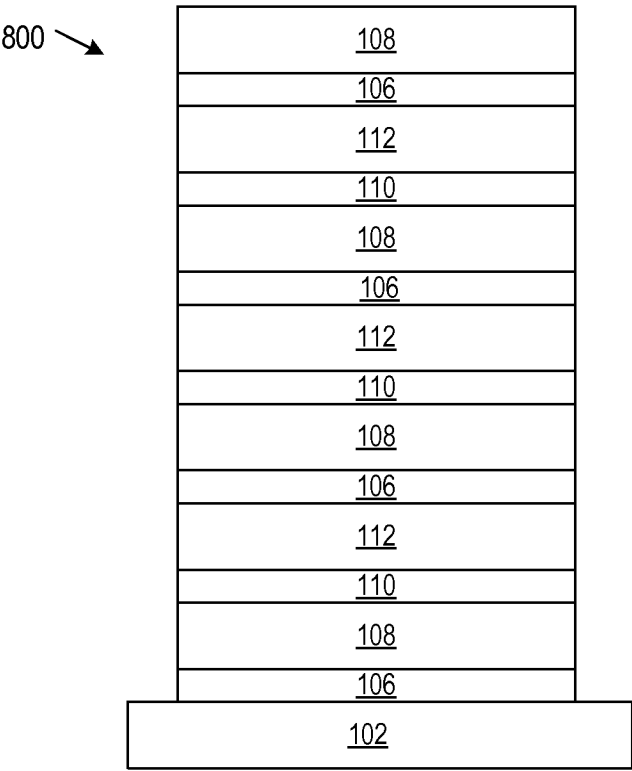


FIG. 8

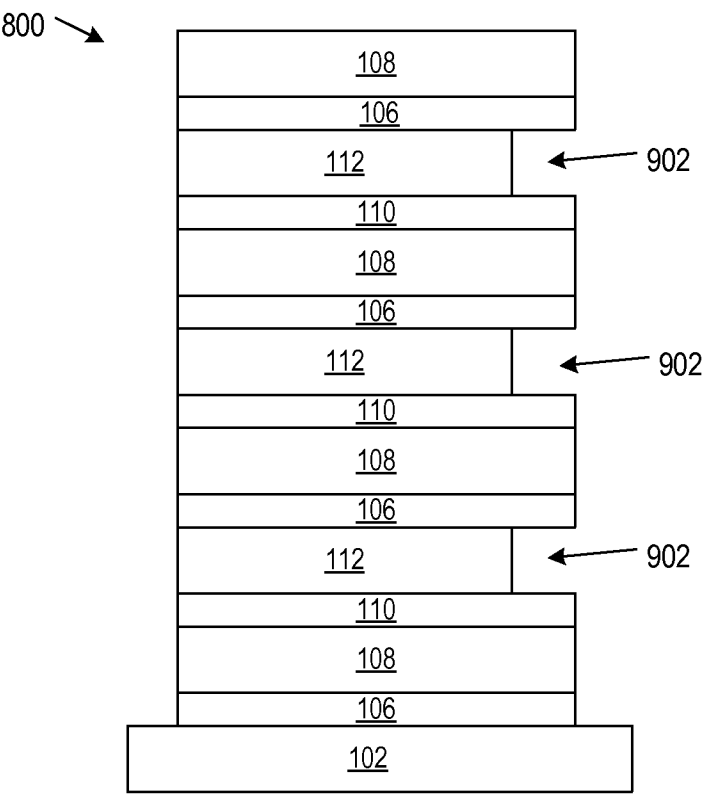


FIG. 9

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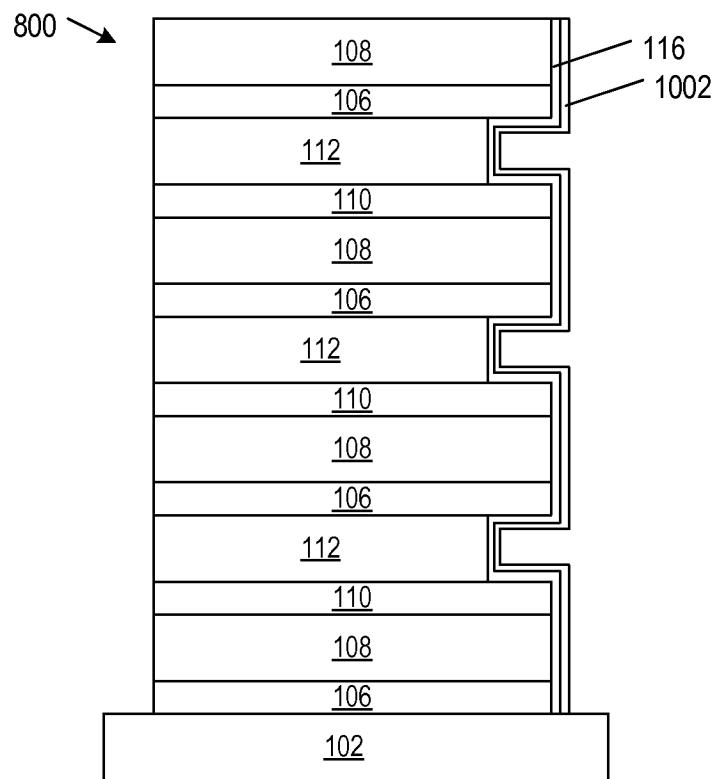


FIG. 10

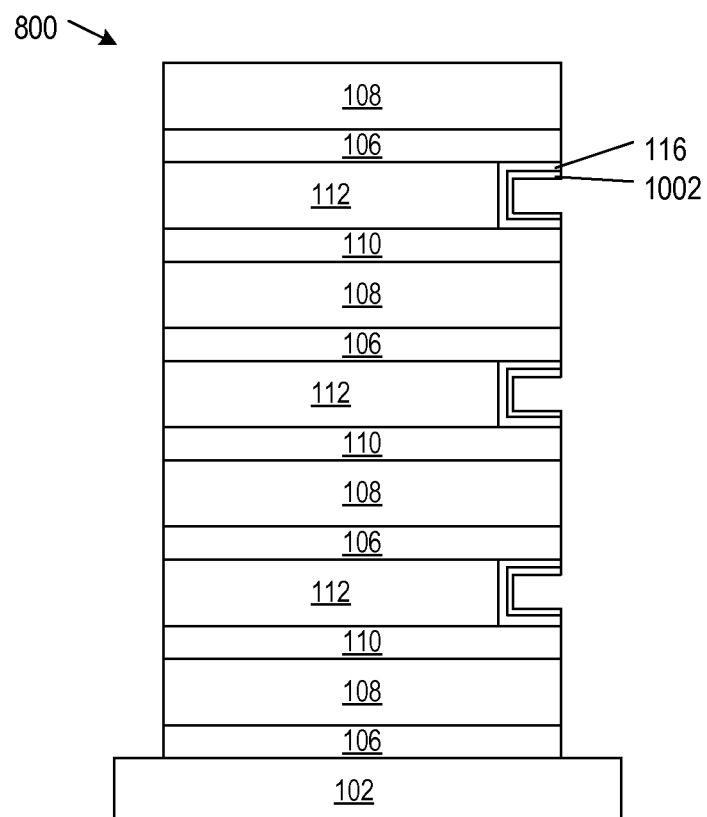


FIG. 11

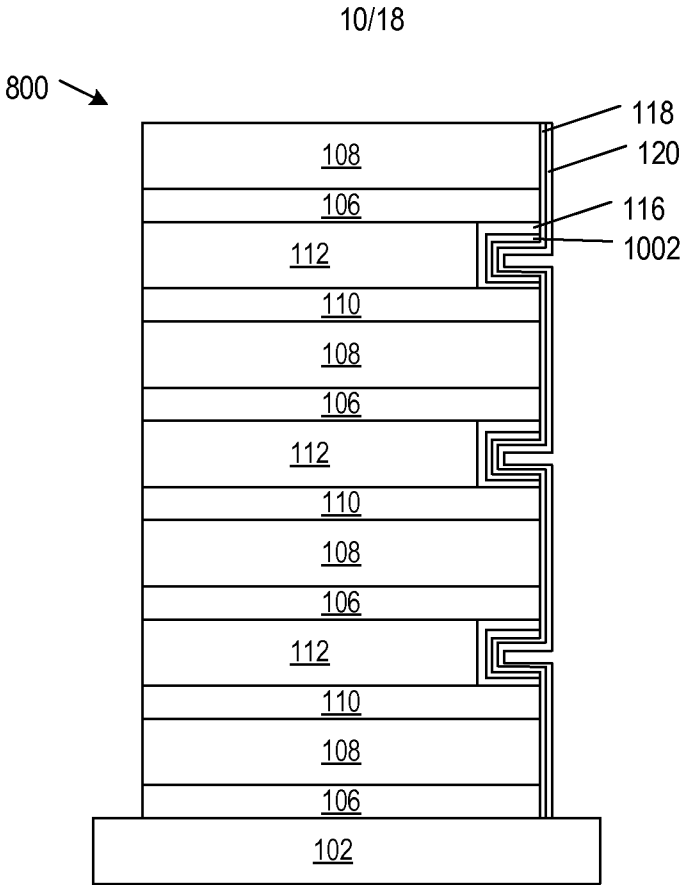


FIG. 12

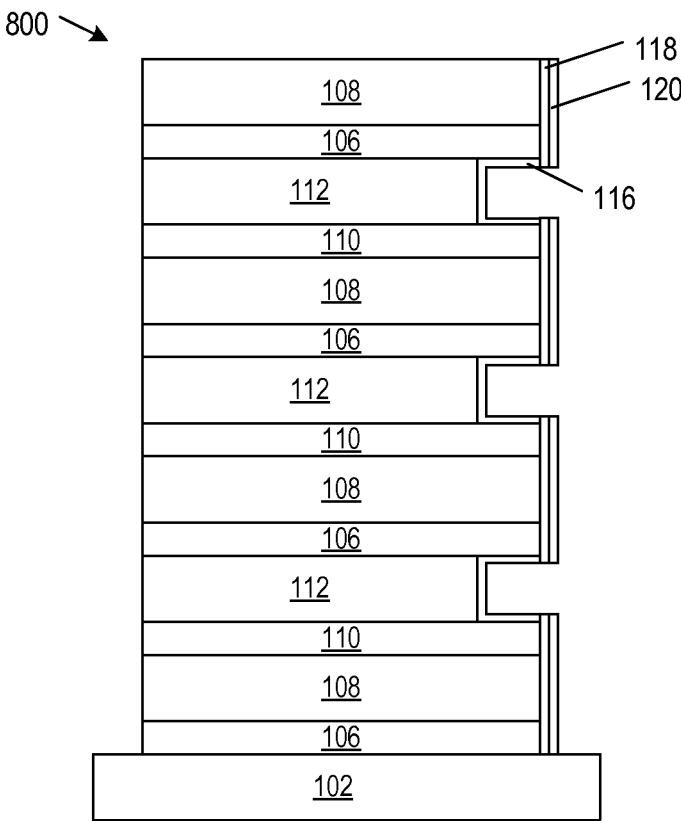


FIG. 13

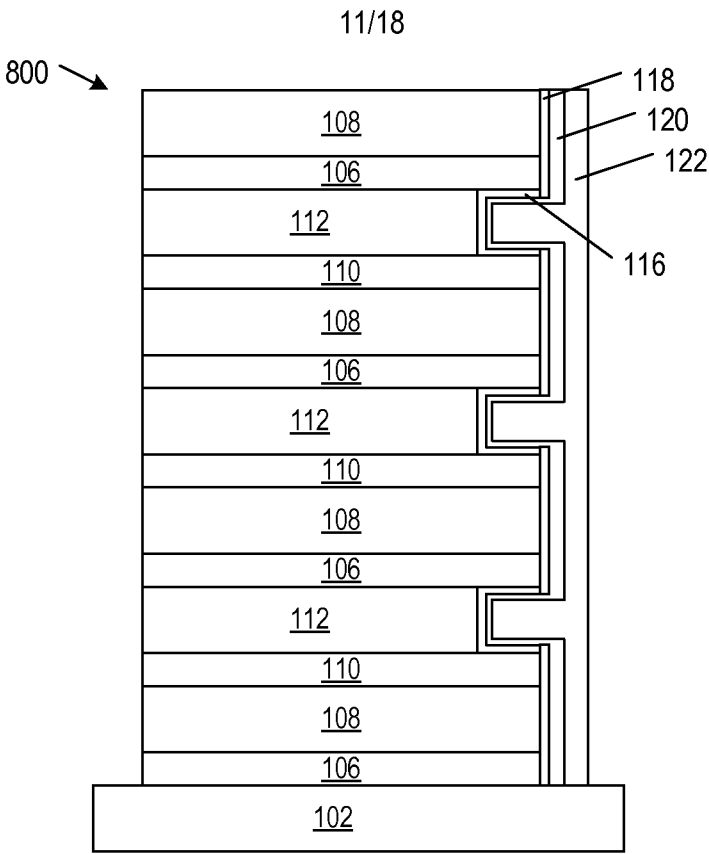


FIG. 14

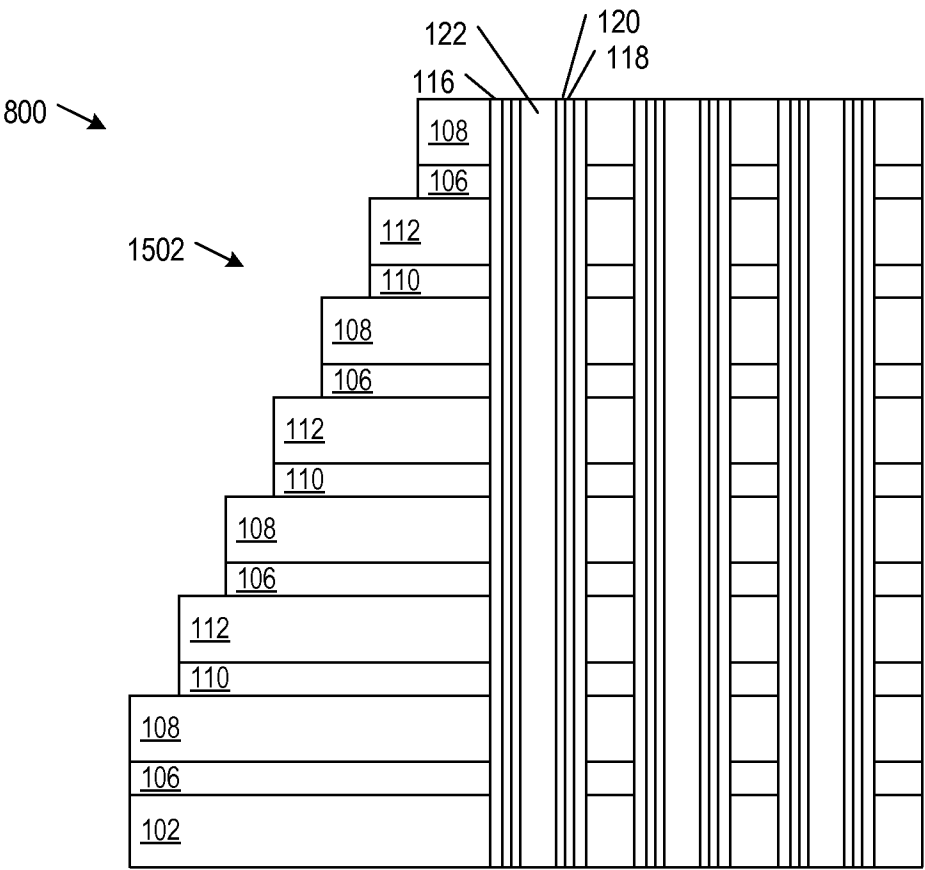


FIG. 15

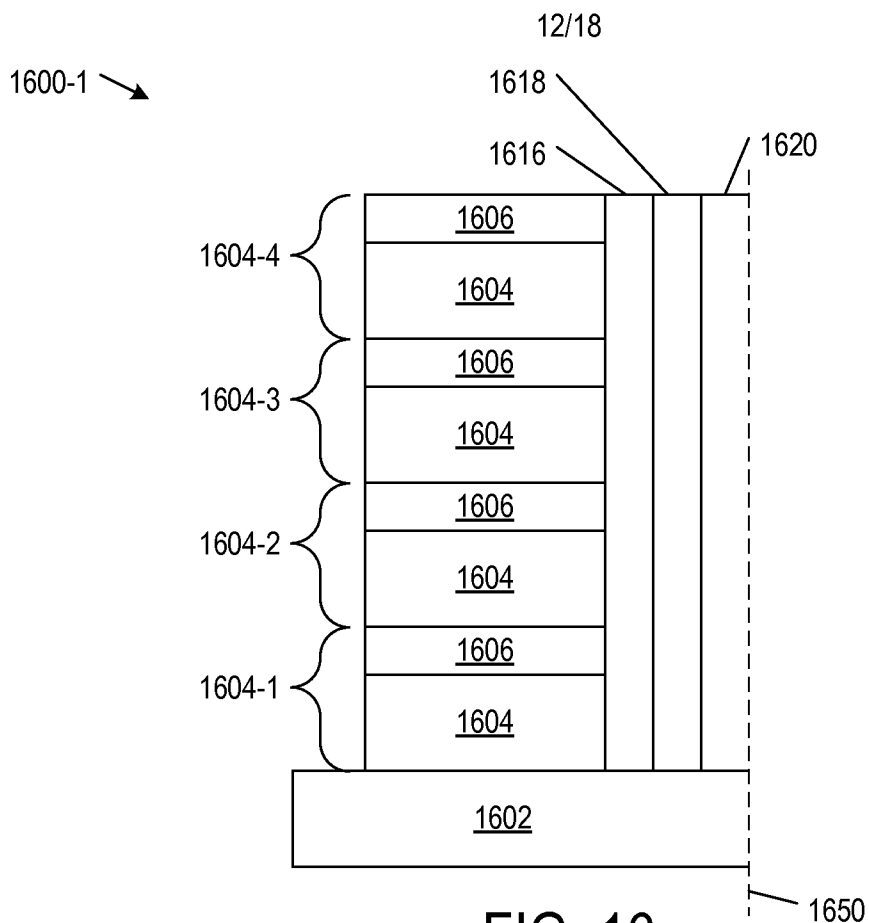


FIG. 16

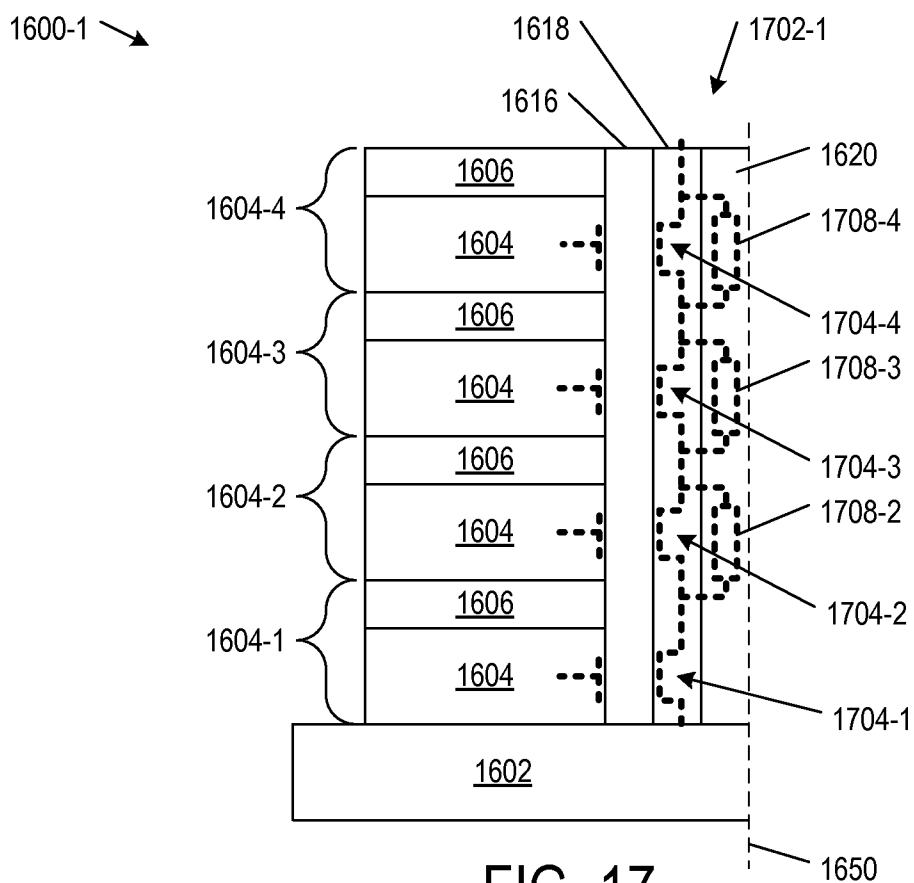


FIG. 17

1800 ↘

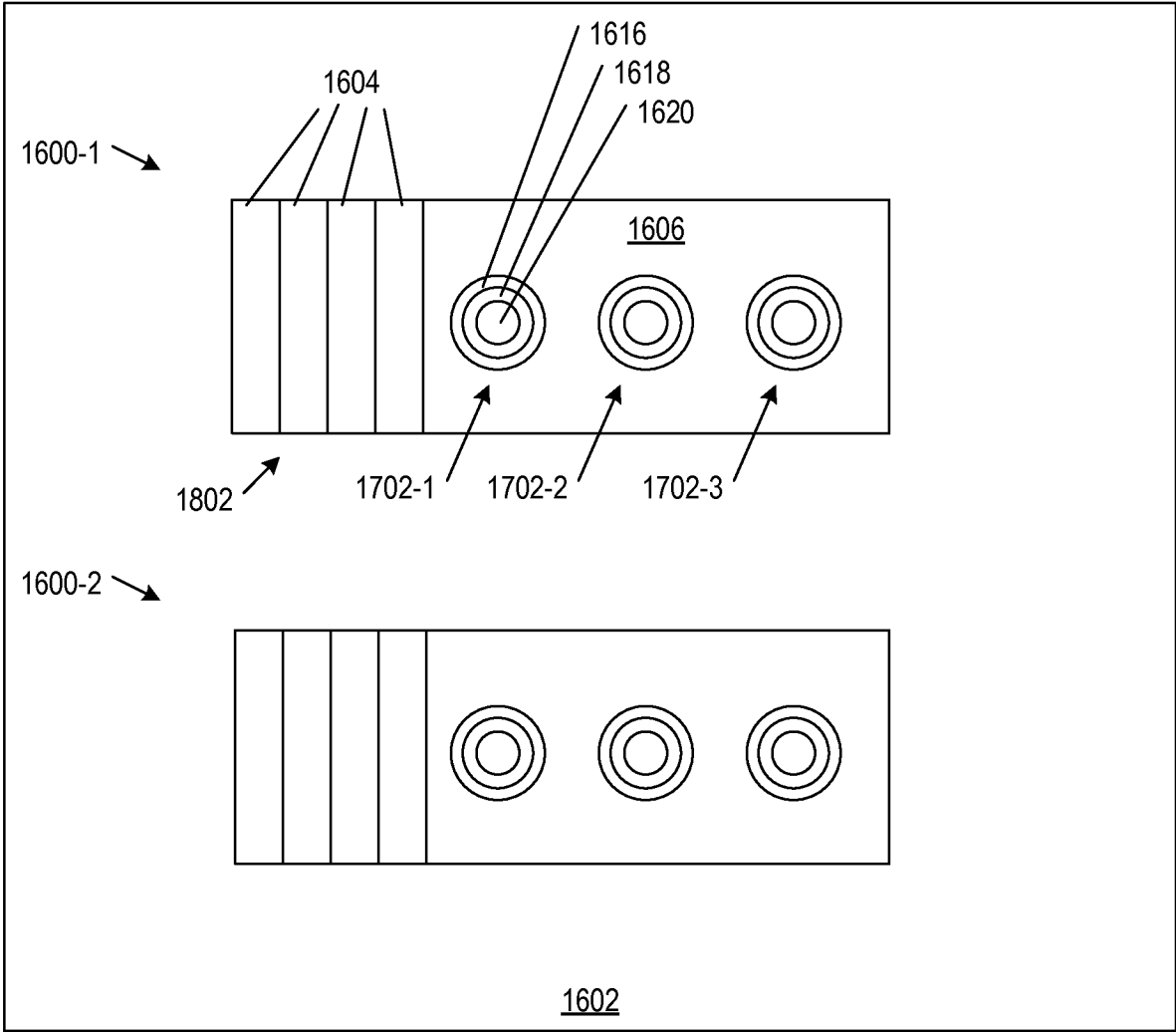


FIG. 18

1900 ↘

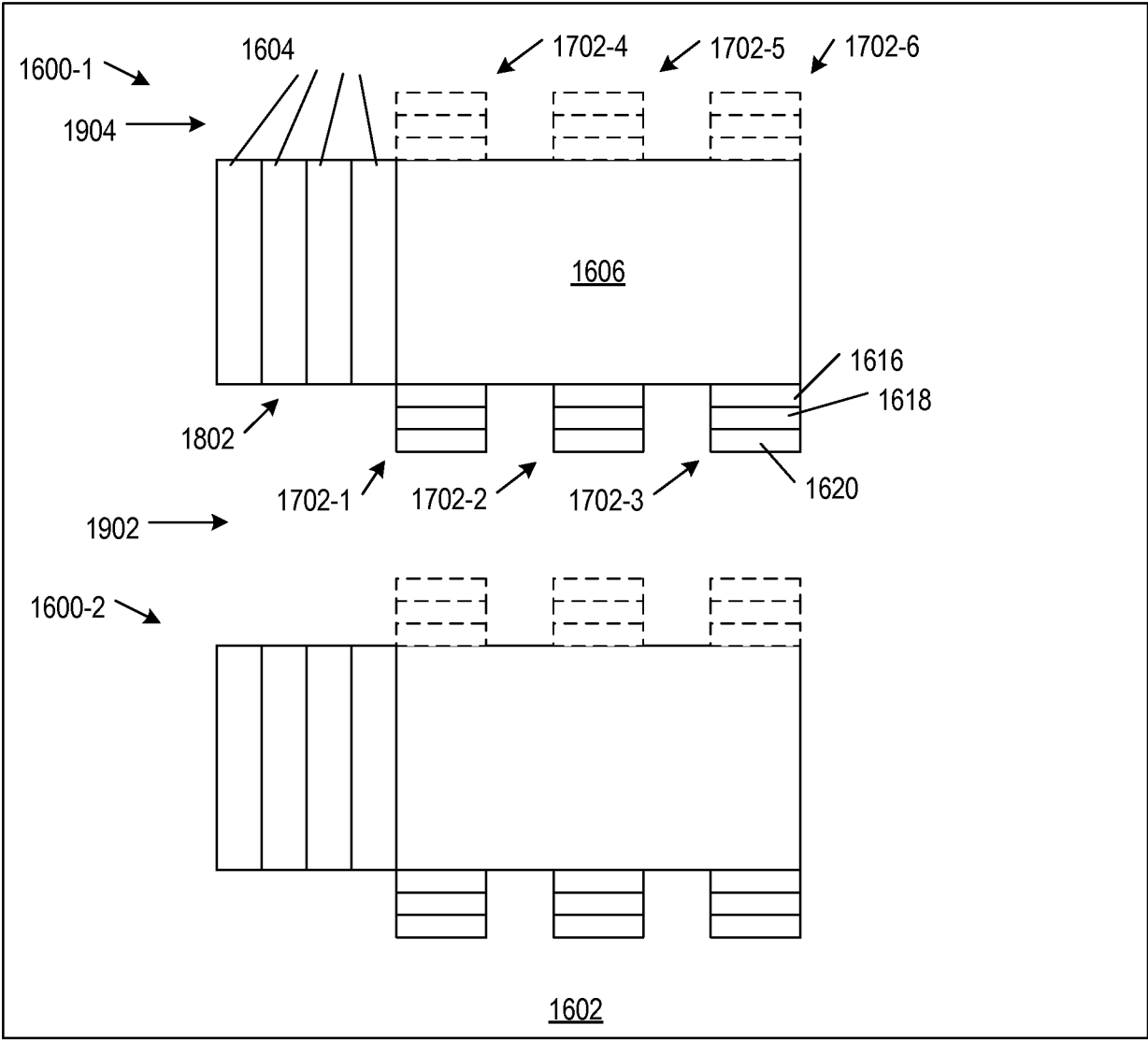


FIG. 19

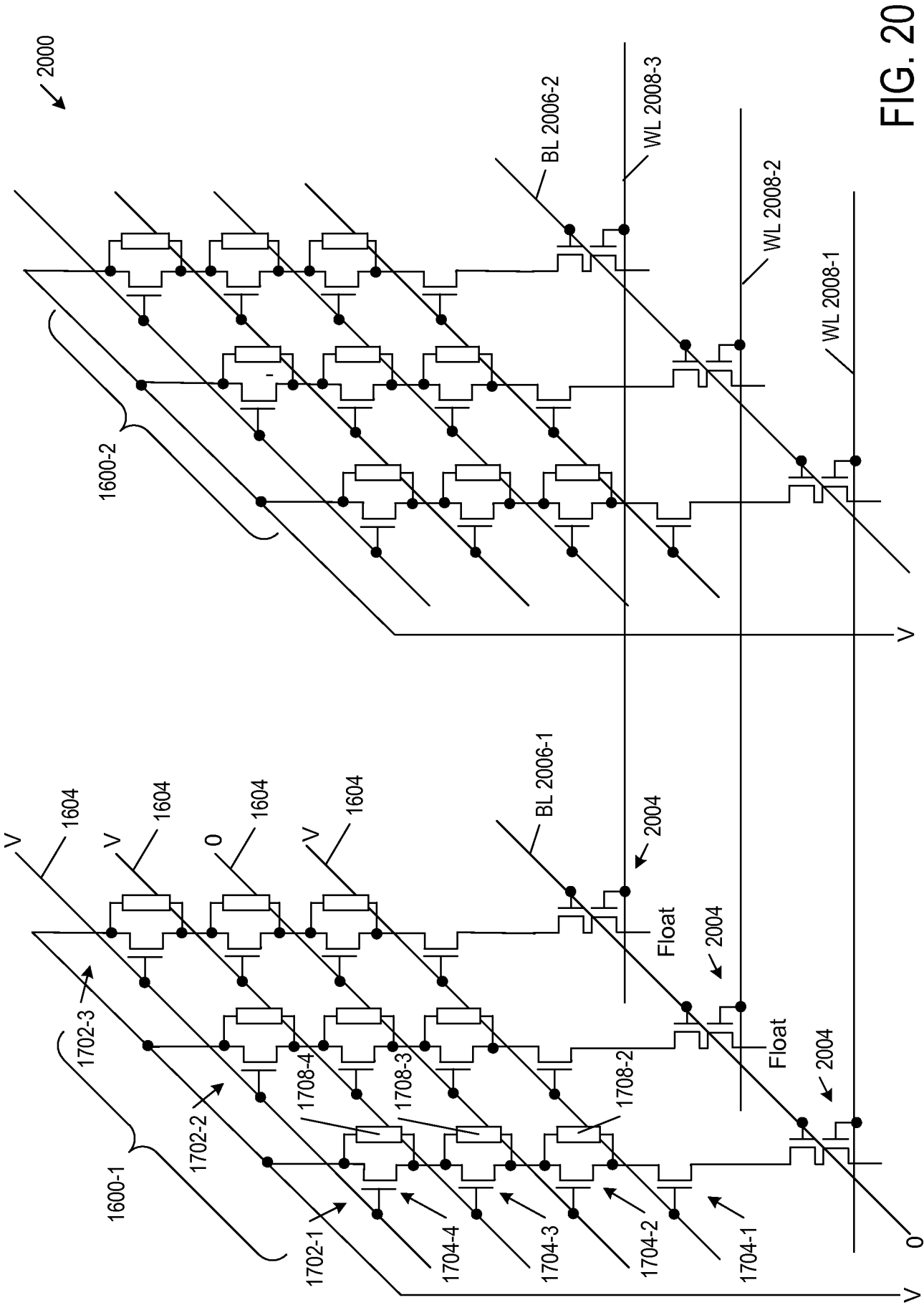


FIG. 20

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2100 →

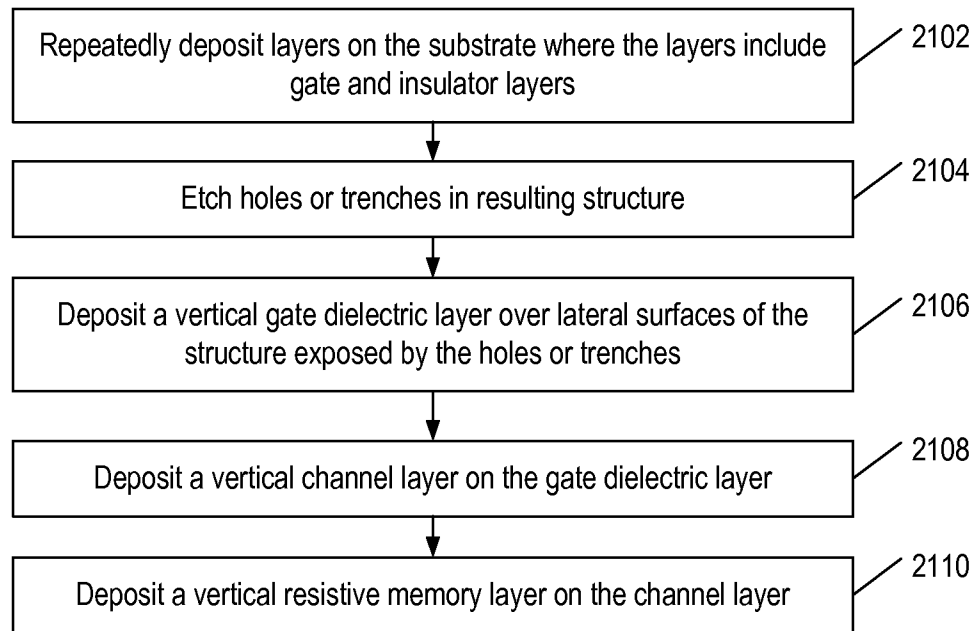


FIG. 21

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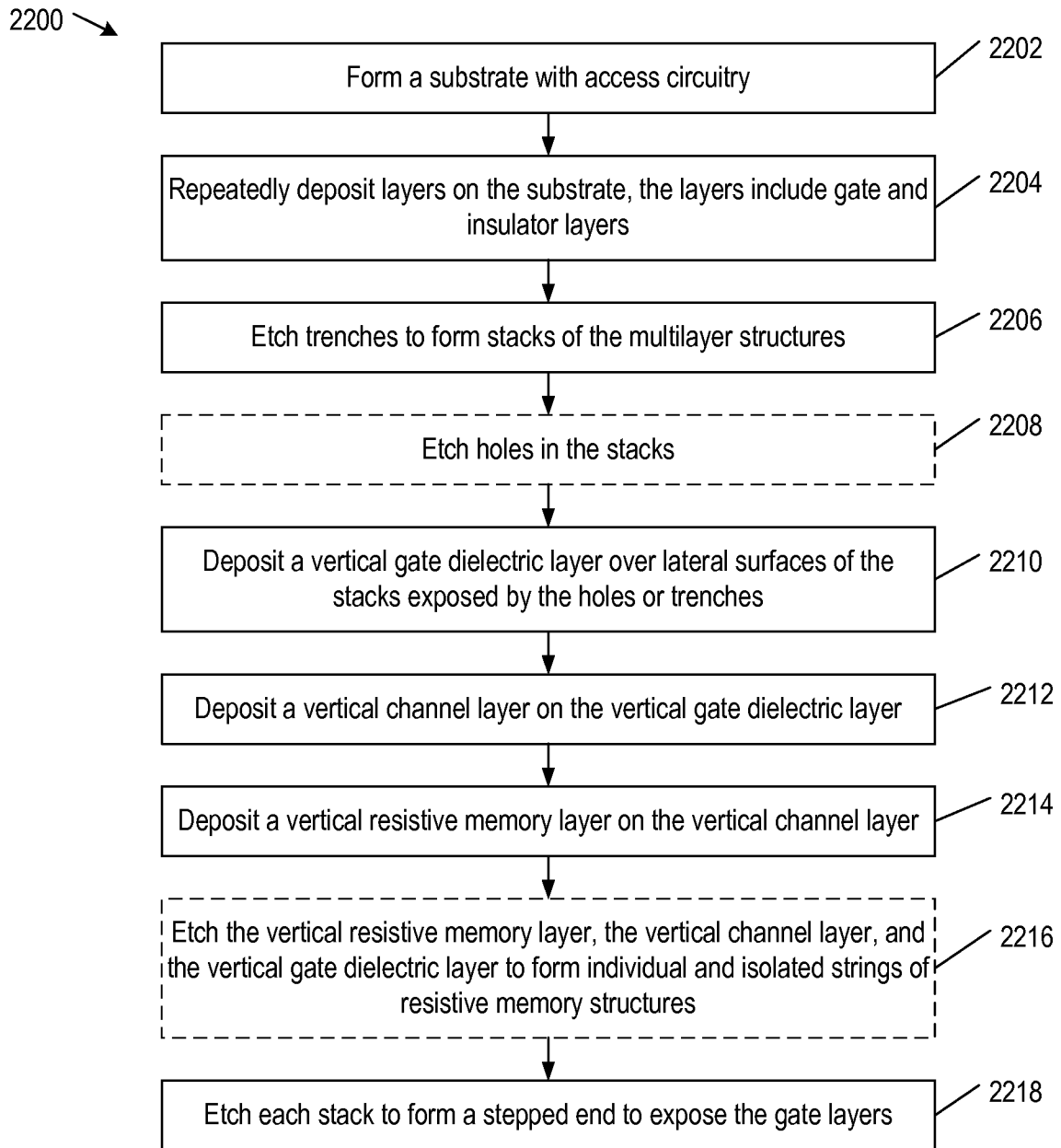


FIG. 22

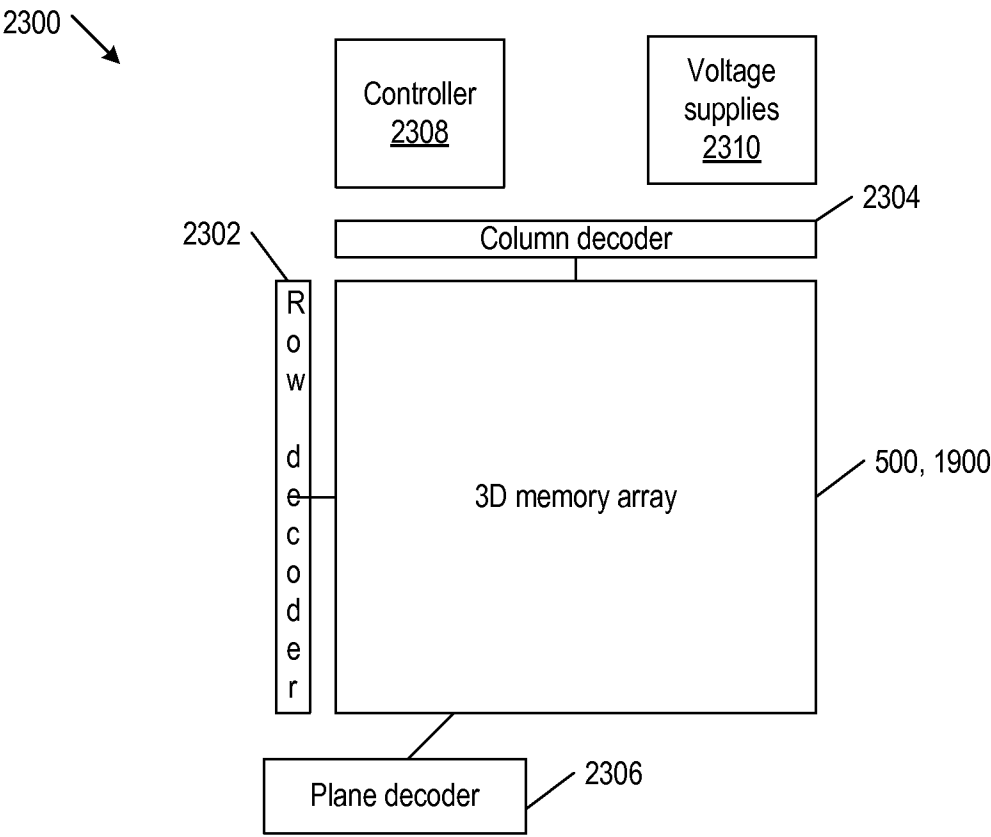


FIG. 23

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/049298**A. CLASSIFICATION OF SUBJECT MATTER****H01L 27/115(2006.01)i, H01L 21/8247(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 27/115; H01L 27/105; H01L 45/00; H01L 21/8247

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: resistive memory, stack, vertical switch, undercut

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2012-248644 A (HITACHI LTD.) 13 December 2012 See abstract, paragraphs [0023]-[0071] and figures 1-16B.	10-11, 13-14
Y		12, 15
A		1-9
Y	US 2008-0149913 A1 (HIROYASU TANAKA et al.) 26 June 2008 See abstract, paragraphs [00088]-[0115] and figures 1-26.	12, 15
A	US 2013-0200331 A1 (TAKAHIRO MORIKAWA et al.) 08 August 2013 See abstract, paragraphs [0011]-[0101] and figures 1A-27.	1-15
A	US 2014-0117304 A1 (NAM KYUN PARK) 01 May 2014 See abstract, paragraphs [0020]-[0043] and figures 1-9.	1-15
A	US 2014-0145137 A1 (HYUNSU JU et al.) 29 May 2014 See abstract, paragraphs [0059]-[0093] and figures 1-4C.	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

29 April 2015 (29.04.2015)

Date of mailing of the international search report

30 April 2015 (30.04.2015)

Name and mailing address of the ISA/KR

International Application Division
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Republic of Korea

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2014/049298

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		US 8829590 B2	09/09/2014
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