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## (54) Raster width regulation circuit.

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## Description

This invention relates to raster width regulation in a television or other video display system.

High resolution video display monitors are used to display computer graphics information in such systems as computer aided design and computer aided manufacturing systems. In such high resolution display systems, which may operate at a line scan frequency which is a multiple of a standard television line frequency, it is desirable to minimize, to the greatest practical extent, display distortion of the video graphics or other information.

One source of display distortion is raster width deflection sensitivity. Line deflection sensitivity depends on the magnitude of the ultor voltage being supplied to the final anode electrode of the picture tube in the display monitor, and depends upon the amplitude of the line scanning current. The amount of electron beam line deflection or throw angle increases with decreasing ultor voltage and with increasing line scanning current amplitude.

Beam current loading of the ultor terminal varies with changes in the information content of the video signal. Bright display areas produce increased beam current loading of the ultor terminal, whereas dark display areas produce reduced beam current loading. Increased beam current loading of the ultor terminal tends to decrease the ultor output voltage, and therefor tends to increase the amount of electron beam line deflection and raster width.

It is a feature of the invention to provide compensation for undesirable raster width variations that tend to produce distortion of the displayed video information. It is another feature of the invention to provide fine or accurate raster width compensation or regulation that satisfies the stringent requirements of a high resolution display system.

In accordance with an aspect of the invention, apparatus for regulating raster width includes a line deflection voltage regulator that is responsive to control signals for developing a first regulated voltage. A line deflection circuit is coupled to the line deflection voltage regulator for generating line scanning current in a line deflection winding. The amplitude of the scanning current is dependent on the first regulated voltage. A high voltage regulator is responsive to control signals for developing a second regulated voltage. A high voltage generator is coupled to the high voltage regulator for generating a ultor output voltage at an ultor terminal. The magnitude of the ultor output voltage is dependent on the second regulated voltage. A high voltage control circuit is coupled in a feedback path between the high voltage generator and the high voltage regulator for developing a first ultor control signal that is representative of the ultor output voltage to regulate the ultor output voltage. A voltage developing circuit is coupled to the feedback path for developing a second ultor control signal that is representative of fluctuations in ultor output voltage. The second control signal is applied to the line deflection voltage regulator to vary the first regulated voltage for providing raster width regulation.

By having a separate high voltage generator to develop the ultor voltage, rather than requiring the line deflection circuit to develop the ultor voltage, beam current loading of the ultor terminal does not produce concurrent direct loading of the line deflection circuit. Undesirable interaction is avoided, between the high voltage generator and the line deflection circuit, that tends to undesirably affect raster width regulation. Furthermore, the provision of a high voltage regulator and a separate line deflection voltage regulator enables separate, relatively independent control of two factors that determine deflection sensitivity, namely, the magnitude of the ultor voltage and the amplitude of the line scanning current. Thus, by supplying the line voltage regulator with a control voltage representative of ultor output voltage fluctuations, the amplitude of the scanning current may be varied to provide accurate raster width regulation to compensate for residual ultor voltage fluctuations that remain uncancelled by operation of the high voltage regulator.

In the Drawing:

The sole FIGURE illustrates a regulated high voltage generator and regulated line deflection circuit with raster width control, embodying the invention.

In the FIGURE, a switched mode power supply regulator 21 generates regulated supply voltages from an unregulated, mains derived voltage $V_{un}$ for providing power to various circuits in a video display monitor. For example, regulator 21 develops a regulated B+ direct voltage for providing power to a high voltage generator 70 and to a line deflection circuit 80. Regulator 21 also develops a regulated voltage $V_1$ for providing power to such circuits as the vertical deflection and display tube driver circuits, not illustrated in the FIGURE, and a regulated supply voltage $V_2$ for providing power to small signal circuits such as the video processing circuits, also not illustrated in the FIGURE.

Line deflection circuit 80 includes a horizontal oscillator 28 providing switching signals S, repeating at the line deflection frequency of, illustratively, 4 fH, where fH is a standard line deflection frequency of, for example, 15.75 kilohertz. Switching signals S are coupled to a driver stage 39 to produce line rate switching of a horizontal output transistor Q1 for generating line scanning current in a line deflection winding $L_H$. Additionally, line deflection circuit 80 includes a damper diode D1, a

deflection retrace capacitor $C_{r1}$ and an S-shaping or trace capacitor $C_s$ coupled in series with line deflection winding $L_H$.

Line deflection winding $L_H$ is coupled to a source of regulated scan supply voltage $V_s$ via the primary winding W1 of a flyback transformer T1. Regulated scan supply voltage $V_s$ is developed from the B+ voltage by a line deflection voltage regulator 60. The average value of the trace voltage developed across trace capacitor $C_s$ is substantially equal to the magnitude of the regulated scan supply voltage $V_s$. Since the peak to peak amplitude of the scanning current is proportional to the average trace voltage being developed by trace capacitor $C_s$, the amplitude of the scanning current is made dependent on the magnitude of the regulated scan supply voltage $V_s$.

The deflection retrace pulse voltage developed across line deflection winding $L_H$ is applied to primary winding W1 of flyback transformer T1 to generate a deflection retrace pulse voltage $V_r$ in a secondary winding W2 of the transformer. Retrace pulse voltage $V_r$ is coupled to horizontal oscillator 28 through terminal A, as is a horizontal sync signal obtained from a source of video signals, not illustrated in the FIGURE. Operation of horizontal oscillator 28 is controlled to synchronize raster line deflection with the raster display of the video content in the video signals.

In accordance with an inventive feature, the function of high voltage generation is separated from the function of line deflection, with high voltage generator 70 being provided with its own power transformer T2. This arrangement eliminates the need for flyback transformer T1 and line deflection circuit 80 to supply power to the picture tube ultor load. Additionally, switched mode power supply regulator 21 is the power source for the other high power monitor load circuits, such as the vertical deflection and display tube driver circuits. Therefore, line deflection circuit 80 does not exhibit undesirable retrace pulse voltage load current modulation that could undesirably produce raster line distortion. No heavy, variable loading occurs on the retrace pulse voltage developed by line deflection winding $L_H$.

High voltage generator 70 comprises a switching power supply, operating on the same pulse principles as line deflection circuit 80, to produce a pulse voltage $V_p$ at the dotted terminal of the primary winding $W_a$ of high voltage transformer T2. The voltage $V_p$ is stepped up by secondary winding $W_b$, and the pulse portion of the voltage is rectified by a diode 24 to generate the DC ultor output voltage at terminal U.

To generate the pulse voltage $V_p$, high voltage generator 70 includes an output switching transistor Q2 switched at, for example, the line deflection frequency by a driver 29 that received the horizontal switching signals S from horizontal oscillator 28. Paralleling output switching transistor Q2 is a damper diode D2, and a resonating capacitor $C_{r2}$ having a function analogous to that of deflection retrace capacitor $C_{r1}$.

High voltage transformer T2 is operated in a flyback converter mode, with the inductance of primary winding $W_a$ serving as the inductance that resonates with capacitor $C_{r2}$ when transistor Q2 is cut off by driver 29. The pulse voltage $V_p$ is generated by a half-cycle resonant oscillation of the resonant circuit formed by winding $W_a$ and capacitor $C_{r2}$. The resonant oscillation is terminated by conduction of damper diode D2. The amplitudes of the pulse voltage $V_p$ and the ultor voltage developed at terminal U are related to the magnitude of the regulated supply voltage $V_{reg}$ developed by a high voltage regulator 50 at an output terminal 23 that is coupled to primary winding $W_a$ of high voltage transformer T2.

High voltage regulator 50 comprises, for example, a series-pass regulator with the collector of a series-pass transistor Q9 coupled to the B+ terminal via a current limiting resistor R1, and with the emitter coupled to output terminal 23 via an overcurrent sampling resistor R2 and an LC filter network 22.

The base and emitter electrodes of an overcurrent limiting transistor Q5 are coupled to respective end terminals of a sampling resistor R2. The collector electrode of transistor Q5 is coupled to the base of transistor Q9.

A controllable current source 30 provides base current to series-pass regulating transistor Q9 for controlling conduction of the transistor under normal operating conditions in accordance with a control signal current $i_{c1}$ flowing from a control input terminal 51. Controllable current source 30 comprises transistors Q3 and Q4 configured as a current mirror, with the base terminals of the current mirror transistors being coupled in common to control terminal 51. The output of controllable source 30 at the collector of current mirror transistor Q4 is coupled to the base of series-pass transistor Q9.

A based current for controlling conduction in series-pass transistor Q9 is supplied from controllable current source 30 in accordance with the value of the control current $i_{c1}$ being sunk by a control transistor Q11. Increasing control current $i_{c1}$, for example, increases the current supplied to the base of series-pass transistor Q9. The conduction of transistor Q9 thereby increases, increasing the amount of current being supplied to output terminal 23.

Excessive current may flow from output terminal 23 into winding $W_a$ of transformer T2, such as may occur under fault operating conditions where,

for example, output switching transistor Q2 becomes a short circuit or where display tube arcing results in excessive current flowing from ultor terminal U. The excessive current flowing from terminal 23 generates a sufficient voltage across sampling resistor R2 to turn on overcurrent limiting transistor Q5. Current from controllable source 30 is shunted away from the base of transistor Q9 by the conduction of transistor Q5 to limit conduction in the series-pass transistor, thereby limiting the amount of current flowing from terminal 23. A zener diode Z1 is coupled between the base and emitter electrodes of series-pass transistor Q9 to prevent an excessive forward biasing voltage from being developed across the base-emitter junction of transistor Q9 during overload conduction of transistor Q5.

To enable high voltage regulator 50 to provide regulation of the ultor voltage at terminal U, control transistor Q11 is a circuit element in a negative feedback path that couples the output of high voltage generator 70, at terminal U, for example, to the control input terminal 51 of high voltage regulator 50. The circuit elements of the feedback path include a voltage divider 90, coupled to ultor terminal U, and a comparator U2 having an inverting input terminal coupled to a junction terminal 91 of voltage divider 90 and having an output terminal coupled to control transistor Q11.

In operation, feedback voltage $V_f$ is applied to the inverting input terminal of comparator U2. Feedback voltage $V_f$ is representative of the ultor voltage being developed at terminal U. When the ultor voltage increases, for example, so does feedback voltage $V_f$. The error voltage $V_{e1}$, developed at the output of comparator U2, decreases, decreasing conduction in control transistor Q11. Ultor control current $i_{c1}$ decreases, decreasing conduction in controllable current source 30 to decrease conduction in series-pass regulator transistor Q9. The regulated supply voltage $V_{reg}$ decreases, decreasing the amplitude of the pulse voltage $V_p$, to thereby decrease the ultor voltage and compensate for the tendency of the ultor voltage to increase.

An adjustable DC control voltage, developed at the wiper arm of an extra-high-tension adjustment potentiometer 42, is coupled to the noninverting input terminal of comparator U2 to adjust the magnitude of the ultor voltage.

Voltage divider 90 includes resistive voltage dividing elements, resistor 25 and resistor 26, that produce the DC and long term average value of the feedback voltage $V_f$ that represents the DC and long term average value of the ultor voltage. Voltage divider junction terminal 91 is DC coupled to the inverting input terminal of comparator U2 via a resistor 41. Thus, changes in the DC and long term average value of the ultor voltage that are sensed by voltage dividing resistors 25 and 26 are preserved in the feedback path as the DC and long term average changes in the error voltage $V_{e1}$ that biases the base of control transistor Q11. Thus, high voltage regulator 50 is capable of responding to changes in the DC level and long term average value changes of the ultor voltage, to vary the regulated supply voltage $V_{reg}$ accordingly, to maintain a constant ultor voltage.

Changes in the long term average value of the ultor voltage may occur due to long term beam current loading of ultor terminal U due to changes in the overall or average brightness of the video information being displayed on the raster. Such overall or average brightness changes occur over the interval of several video field periods or field deflection cycles. If left uncompensated, these long term average value changes in the ultor voltage produce a visually undesirable pulsation of the width of the entire raster.

A second type of raster distortion is one that is caused by short term fluctuations in the ultor voltage. The duration of such short term fluctuations is typically less than one field period or less than one vertical deflection cycle. Such short term fluctuations in the ultor voltage may be caused by short term fluctuations in beam current loading of ultor terminal U when displaying, for example, a stationary display that includes both very bright regions and very dark regions. As the video lines for such a stationary display the displayed within one field, they will vary from lines that display bright video information to lines that display dark video information. These rapid changes in display of video information produce corresponding rapid fluctuations in beam current loading and in ultor voltage over one field interval. The result is that the width of the raster lines within one field also fluctuates in a corresponding manner to distort the display.

In accordance with an inventive feature high voltage regulator 50 is also responsive to the short term fluctuations in ultor output voltage to correct for these fluctuations and maintain a relatively constant ultor voltage. In carrying out this feature, voltage divider 90 includes a capacitor 27 coupled between voltage divider junction terminal 91 and ultor terminal U Short term fluctuations in the ultor voltage are directly coupled, relatively unattenuated, to terminal 91 to develop short term fluctuations in the feedback voltage $V_f$.

The short term fluctuations in the feedback voltage $V_f$ are then coupled to the inverting input terminal of comparator U2 to develop a component of the error voltage $V_{e1}$ at the output of the comparator that enables the control current $i_{c1}$ to provide, as explained later, substantial, not necessarily total, cancellation of the ultor voltage fluctuations at ultor terminal U. The time constant associated with

voltage divider network 90 is matched to the time constant of the RC network 45 coupled between the output and inverting input terminals of comparator U2 to enable the comparator to respond to short term ultor voltage fluctuations while still maintaining stable operation without going into undesirable parasitic oscillation.

In accordance with another aspect of the invention, line deflection voltage regulator 60 is also responsive to the ultor output voltage to vary the regulated scan supply voltage $V_s$ in accordance with the ultor output voltage. Line deflection regulator 60 includes a series-pass transistor Q10 coupled between the regulated B+ terminal and output terminal 67 at which the regulated voltage $V_s$ is developed. Series-pass transistor Q10, and its associated control circuitry, operates in a manner identical to series-pass transistor Q9 of high voltage regulator 50. Thus, line deflection voltage regulator 60 includes a current limiting resistor R3, a current sampling resistor R4, a filter 46, an overcurrent limiting transistor Q8 and associated zener diode Z2, and a controllable current source 40. Current source 40 includes a current mirror-(transistor Q6 with transistor Q7)that supplies base current to series-pass transistor Q10 in accordance with a control signal $i_{c2}$ that flows from a control terminal 62 and that is developed by a control transistor Q12. Conduction in control transistor Q12 is controlled by a error voltage $V_{e2}$ developed at the output of a comparator U1 that in turn is responsive to a control voltage $V_{c2}$ being developed at a control input terminal 61 of regulator 60.

Control input terminal 61 is the summing point for various control signals that are used to regulate the scan supply voltage $V_s$. A feedback voltage $V_{f2}$ is applied to control input terminal 61 via resistor 63 to provide a closed loop negative feedback that maintains a constant deflection retrace pulse amplitude with variations in the frequency of horizontal switching signal S and with residual ripple in the B+ voltage that remains uncorrected by switched mode power supply regulator 21. The feedback voltage $V_{f2}$ is obtained from the retrace pulse voltage $V_r$ that is coupled to a diode 65 via a current limiting resistor 64 and that is then filtered by a capacitor 66.

A second control voltage applied to control input terminal 61 is obtained from a vertical parabola generator 31, of well-known design. Vertical parabola generator 31 supplies a side pincushion correction voltage $V_{pin}$ that is AC coupled by a capacitor 34 via a resistor 37 to terminal 61, after first being divided down in amplitude by voltage dividing resistors 32 and 33. Additional DC bias for the inverting input terminal of comparator U1 is provided by voltage dividing resistors 35 and 36 coupled to a +12V source. The pincushion correction signal $V_{pin}$ produces a vertical rate variation of the scan supply voltage $V_s$ to achieve side pincushion correction of the raster.

To control horizontal width of the raster, an adjustable DC control voltage is developed at the wiper arm of a potentiometer 38 and is coupled to the noninverting input terminal of comparator U1.

In accordance with a feature of the invention, line deflection voltage regulator 60 is made responsive to fluctuations in the ultor output voltage to achieve highly accurate raster width compensation. Depending on the loop gain for the ultor feedback voltage $V_f$ in the feedback path of high voltage regulator 50, some residual ultor voltage error and raster distortion remain uncompensated by high voltage regulator 50. This distortion may be especially objectionable when displaying high resolution computer graphics, for example, where short term beam current loading fluctuations, described previously, produce short term ultor voltage fluctuations.

To correct for the residual distortion, the error voltage $V_{e1}$ developed at the output of comparator U2 of high voltage regulator 50 is AC coupled to control input terminal 61, which is a summing point of line deflection voltage regulator 60, via a variable resistor 43 and a capacitor 44. The DC and long term average changes in the ultor voltage at terminal U establish the DC and long term average value of the error voltage $V_{e1}$. The short term ultor voltage fluctuations establishes a corresponding short term AC fluctuation in the error voltage $V_{e1}$. It is this short term fluctuation that is coupled by resistor 43 and capacitor 44 to control input terminal 61 of line deflection voltage regulator 60.

The regulated scan supply voltage $V_s$ is varied in accordance with these ultor voltage fluctuations in a manner that compensates for the remaining raster distortion produced by the short term fluctuations that remain uncompensated by high voltage regulator 50. The time constant associated with resistor 43 and capacitor 44 is selected to pass on these short term fluctuations to control input terminal 61. The time constant is also matched to the time constant associated with RC network 68 that is coupled between the output and inverting input terminals of comparator U1.

Assume, for example, that the ultor output voltage fluctuation is in the direction to decrease the ultor voltage. This decrease tends to increase the raster width. The accompanying decrease in ultor feedback voltage $V_f$ is coupled to inverting input terminal of comparator U2 to produce an increase in the error voltage $V_{e1}$. The increase in error voltage $V_{e1}$ is coupled to the inverting input terminal of comparator U1 of line deflection voltage regulator 60 to decrease the error voltage $V_{e2}$. The control current $i_{c2}$ thereby decreases, decreasing

conduction in series-pass transistor Q10. The decrease in conduction of series-pass transistor Q10 produces a decrease in the regulated scan supply voltage $V_s$ and therefore a decrease in the amplitude of the line scanning current. The decrease in amplitude of the line scanning current decreases the width of the raster lines as compensation for the tendency of the raster lines to increase with a decrease in ultor voltage.

An advantage of using the output of high voltage regulator comparator U2 as the input to line deflection voltage regulator comparator U1 to provide the mechanism for additional raster width correction, is that the impedances between the output terminal of comparator U2 and the input terminal of comparator U1 may be readily matched and proper signal bias levels may be readily achieved.

An alternative way of obtaining ultor feedback voltage $V_f$ is from a focus electrode voltage that is derived from the resonant pulse voltage being developed at a focus tap terminal F in winding $W_b$ of high voltage transformer T2. The pulse voltage in winding $W_b$ that generates the focus electrode voltage may be used to generate the feedback voltage $V_f$, provided that beam current loading on ultor terminal U produces the same type of ringing and other waveshape distortion of the pulse voltage at tap terminal F as is produced across the entire high voltage secondary winding $W_b$.

It is desirable to use an ultor sense voltage that is directly representative of the ultor voltage, such as ultor feedback voltage $V_f$ that is obtained from junction terminal 91 coupled to ultor terminal U. Such a sense voltage is a direct representation of ultor voltage fluctuations and may be advantageously used to enable line deflection voltage regulator 60 to directly follow such fluctuations.

It is desirable to use such a direct representation sense voltage to permit the amplitude of the line scanning current to track the fluctuations in ultor voltage. Such tracking is necessary to maintain a constant deflection sensitivity. For example, for a relatively small fluctuation, $\delta U$, in the ultor voltage, the change in amplitude $\delta I_p$ of the line scanning current should be directly proportional to the ultor voltage fluctuation $\delta U$ to maintain a constant deflection sensitivity. Changes in the ultor feedback voltage $V_f$ are directly related to the ultor voltage fluctuations. Feedback voltage $V_f$ provides a good sense signal for use by line deflection regulator 60 to produce the necessary changes in scan supply voltage $V_s$ that produce the required changes $\delta I_p$ in the amplitude of the line scanning current.

Using a sampling resistor in the current path of high voltage winding $W_b$ to provide an indirect representation of fluctuations of the ultor voltage U may not provide satisfactory representation because the tracking between the voltage changes across the sampling resistor and the ultor voltage fluctuation $\delta U$ may not be adequate. Such inadequacy may be due in part to the fact that the leakage inductance exhibited by the large number of turns in high voltage winding $W_b$, combined with possibly inadequate filtering by the ultor capacitance, result in an internal generator impedance that causes the ultor voltage to vary in a manner different than that of the current variations in a sampling resistor.

## Claims

1. Apparatus for regulating raster width, comprising:
   a line deflection voltage regulator (60) responsive to control signals for developing a first regulated voltage;
   a line deflection circuit (80) coupled to said line deflection voltage regulator (60) for generating line scanning current in a line deflection winding ($L_H$), the amplitude of said scanning current being dependent on said first regulated voltage;
   a high voltage regulator (50) responsive to control signals for developing a second regulated voltage;
   a high voltage generator (70) coupled to said high voltage regulator (50) for generating an ultor output voltage at an ultor terminal (U), the magnitude of said ultor output voltage being dependent on said second regulated voltage;
   means (U2,Q11) coupled in a feedback path between said high voltage generator (70) and said high voltage regulator (50) for developing a first ultor control signal for said high voltage regulator (50) that is representative of ultor output voltage to regulate said ultor output voltage; and
   means (43,44) coupled to said feedback path for developing a second ultor control signal for said line deflection voltage regulator (60) that is representative of fluctuations in said ultor output voltage to vary said first regulated voltage in accordance therewith for providing raster width regulation.

2. Apparatus according to Claim 1 characterized in that said second ultor control signal is representative of ultor output voltage fluctuations that remain uncancelled by said high voltage regulator (50).

3. Apparatus according to Claim 1 characterized in that said first ultor control signal developing means includes a comparator (U2) having an output ($V_{e1}$) coupled to a control input of said

high voltage regulator (50) and having an input for receiving a feedback voltage representative of said ultor output voltage.

4. Apparatus according to Claim 3 characterized by a resistive voltage divider (25,26) coupled to said ultor terminal (U) for developing said feedback voltage at a junction terminal (91) thereof.

5. Apparatus according to Claim 4 characterized by a capacitance (27) coupled to said ultor terminal (U) and to said junction terminal (91) for enabling said comparator (U2) to respond to relatively rapid fluctuations in said ultor output voltage.

6. Apparatus according to claim 4 or 5 characterized in that said second ultor control signal developing means (43,44) is responsive to the output of said comparator (U2) for developing therefrom said second ultor control signal.

7. Apparatus according to Claim 1 characterized by a third voltage regulator (21) for generating a regulated supply voltage from an unregulated input voltage, said line deflection (60) and high voltage (50) regulators developing their respective regulated voltages from said third voltage regulator (21).

8. Apparatus according to Claim 7 characterized in that said high voltage generator (70) comprises switching means (Q9) coupled to a first winding ($W_a$) of a high voltage transformer (T2), said ultor output voltage being generated from the voltage developed across a second winding ($W_b$) of said transformer (T2).

9. Apparatus according to any preceding claim characterized in that said line deflection circuit (80) is coupled to said line deflection regulator (60) via a second transformer (T1) having a retrace pulse voltage developed therein by said line deflection winding ($L_H$).

10. Apparatus according to Claim 9 characterized by means (64,65,66) for developing a control signal for said line deflection regulator (60) representative of the amplitude of said retrace pulse voltage for varying said first regulated voltage to maintain a regulated retrace pulse voltage.

11. Apparatus according any preceding claim characterized by a vertical rate signal generator (31) for developing a vertical rate control signal for said line deflection voltage regulator (60) to vary said first regulated voltage in a manner that provides side pincushion correction.

**Revendications**

1. Dispositif pour réguler la largeur de mire, comprenant :
un régulateur de tension de déviation de ligne (60) répondant à des signaux de commande pour produire une première tension régulée;
un circuit de déviation de ligne (80) couplé au régulateur de tension de déviation de ligne (60) pour produire un courant de balayage de ligne dans un enroulement de déviation de ligne ($L_H$), l'amplitude du courant de balayage étant dépendante de la première tension régulée;
un régulateur de haute tension (50)répondant aux signaux de commande pour produire une seconde tension régulée;
un générateur de haute tension (70) couplé au régulateur de haute tension (50) pour produire une tension de sortie ultime à une borne ultime (U), la grandeur de la tension de sortie ultime étant dépendante de la seconde tension régulée;
un moyen (U2,Q11) couplé dans un trajet de contre-réaction entre le générateur de haute tension (70) et le régulateur de haute tension-(50) pour produire un premier signal de commande ultime au régulateur de haute tension (50) qui est représentatif de la tension de sortie ultime pour réguler la tension de sortie ultime; et
un moyen (43,44) couplé au trajet de contre-réaction pour produire un second signal de commande ultime au régulateur de tension de déviation de ligne (60) qui est représentatif de fluctuations dans la tension de sortie ultime pour varier la première tension régulée avec celle-ci pour produire la régulation de largeur de mire.

2. Dispositif selon la revendication 1, caractérisé en ce que le second signal de commande ultime précité est représentatif de fluctuations de tension de sortie ultime qui restent non supprimées par le régulateur de haute tension précité (50).

3. Dispositif selon la revendication 1, caractérisé en ce que le moyen précité de production du signal de commande ultime comprend un comparateur (U2) ayant une sortie ($V_{s1}$) couplée à une entrée de commande du régulateur de haute tension (50) précité et ayant une entrée pour recevoir une tension de contre-réaction représentative de la tension de sortie

ultime.

4. Dispositif selon la revendication 3, caractérisé par un diviseur de tension à résistances (25,26) couplé à la borne ultime précitée (U) pour produire la tension de contre-réaction précitée à une borne de jonction (91) de celui-ci.

5. Dispositif selon la revendication 4, caractérisé par un condensateur (27) couplé à la borne ultime précitée (U) et à la borne de jonction précitée (91) pour permettre au comparateur (U2) de répondre à des fluctuations relativement rapides dans la tension de sortie ultime précitée.

6. Dispositif selon la revendication 4 ou 5, caractérisé en ce que le moyen précité de production du second signal de commande ultime (43,44) répond à la sortie du comparateur précité (U2) pour produire de celui-ci le second signal de commande ultime.

7. Dispositif selon la revendication 1, caractérisé par un troisième régulateur de tension (21) pour produire une tension d'alimentation régulée à partir d'une tension d'entrée non régulée, les régulateurs précités de déviation de ligne (60) et de haute tension (50) produisant leurs tensions régulées respectives à partir du troisième régulateur de tension (21).

8. Dispositif selon la revendication 7, caractérisé en ce que le générateur de haute tension précité (70) comprend un moyen de commutation (Q9) couplé à un premier enroulement ($W_a$) d'un transformateur de haute tension (T2), la tension de sortie ultime précitée étant produite à partir de la tension produite à travers un second enroulement ($W_b$) dudit transformateur (T2).

9. Dispositif selon l'une des revendications précédentes, caractérisé en ce que le circuit de déviation de ligne précité (80) est couplé au régulateur de déviation de ligne précité (60) via un second transformateur (T1) ayant une tension d'impulsion de retour produite dans celui-ci par l'enroulement de déviation de ligne ($L_H$).

10. Dispositif selon la revendication 9, caractérisé par un moyen (64,65,66) produisant un signal de commande au régulateur de déviation de ligne précité (60) représentatif de l'amplitude de la tension d'impulsion de retour précitée pour varier la première tension régulée pour maintenir une tension d'impulsion de retour régulée.

11. Dispositif selon l'une des revendications précédentes, caractérisé par un générateur de signaux de fréquence verticale (31) produisant un signal de commande de fréquence verticale au régulateur de tension de déviation de ligne précité (60) pour varier la première tension régulée précitée de manière à produire une correction latérale en coussinet.

## Ansprüche

1. Rasterbreitenregelungsschaltung mit
einem Zeilenablenkspannungsregler (60), der in Abhängigkeit von Steuersignalen eine erste geregelte Spannung erzeugt,
einer mit dem Zeilenablenkspannungsregler (60) gekoppelten Zeilenablenkschaltung (80) zur Erzeugung eines Zeilenablenkstroms in einer Zeilenablenkwicklung ($L_H$), dessen Amplitude von der ersten geregelten Spannung abhängt,
einem Hochspannungsregler (50), der in Abhängigkeit von Steuersignalen eine zweite geregelte Spannung erzeugt,
einem mit dem Hochspannungsregler (50) gekoppelten Hochspannungsgenerator (70) zur Erzeugung einer Anodenausgangsspannung an einem Anodenanschluß (U), deren Größe von der zweiten geregelten Spannung abhängt,
einer in einem Rückkopplungsweg zwischen dem Hochspannungsgenerator (70) und dem Hochspannungsregler (50) liegenden Schaltung (U2,Q11) zur Erzeugung eines ersten Anodenspannungsregelsignals für den Hochspannungsregler (50) als Maß für die Anodenausgangsspannung zu deren Regelung,
und einer in den Rückkopplungsweg eingefügten Schaltung (43,44) zur Erzeugung eines zweiten Anodenspannungsregelsignals für den Zeilenablenkspannungsregler (60), als Maß für Schwankungen der Anodenausgangsspannung zur entsprechenden Änderung der ersten geregelten Spannung im Sinne einer Rasterbreitenregelung.

2. Schaltung nach Anspruch 1, **dadurch gekennzeichnet,** daß das zweite Anodenspannungsregelsignal ein Maß für von dem Hochspannungsregler (50) nicht ausgeregelte Schwankungen der Anodenausgangsspannung ist.

3. Schaltung nach Anspruch 1, **dadurch gekennzeichnet,** daß die das erste Anodenspannungsregelsignal erzeugende Schaltung einen Vergleicher (U2) enthält, dessen Ausgang ($V_{e1}$)

mit einem Steuereingang des Hochspannungsreglers (50) gekoppelt ist und dessen Eingang eine Rückkopplungsspannung zugeführt wird, die ein Maß für die Anodenausgangsspannung ist.

4. Schaltung nach Anspruch 3, **dadurch gekennzeichnet,** daß mit dem Anodenanschluß (U) ein Widerstandspannungsteiler (25,26) gekoppelt ist, an dessen Abgriff (91) die Rückkopplungsspannung verfügbar ist.

5. Schaltung nach Anspruch 4, **dadurch gekennzeichnet,** daß eine Kapazität (27) an den Anodenanschluß (U) und an den Abgriff (91) angeschlossen ist im Sinne einer schnellen Reaktion des Vergleichers (U2) auf relativ schnelle Änderungen der Anodenausgangsspannung.

6. Schaltung nach Anspruch 4 oder 5, **dadurch gekennzeichnet,** daß die das zweite Anodenspannungsregelsignal erzeugende Schaltung (43,44) durch das Ausgangssignal des Vergleichers (U2) zur Erzeugung des zweiten Hochspannungsregelsignals steuerbar ist.

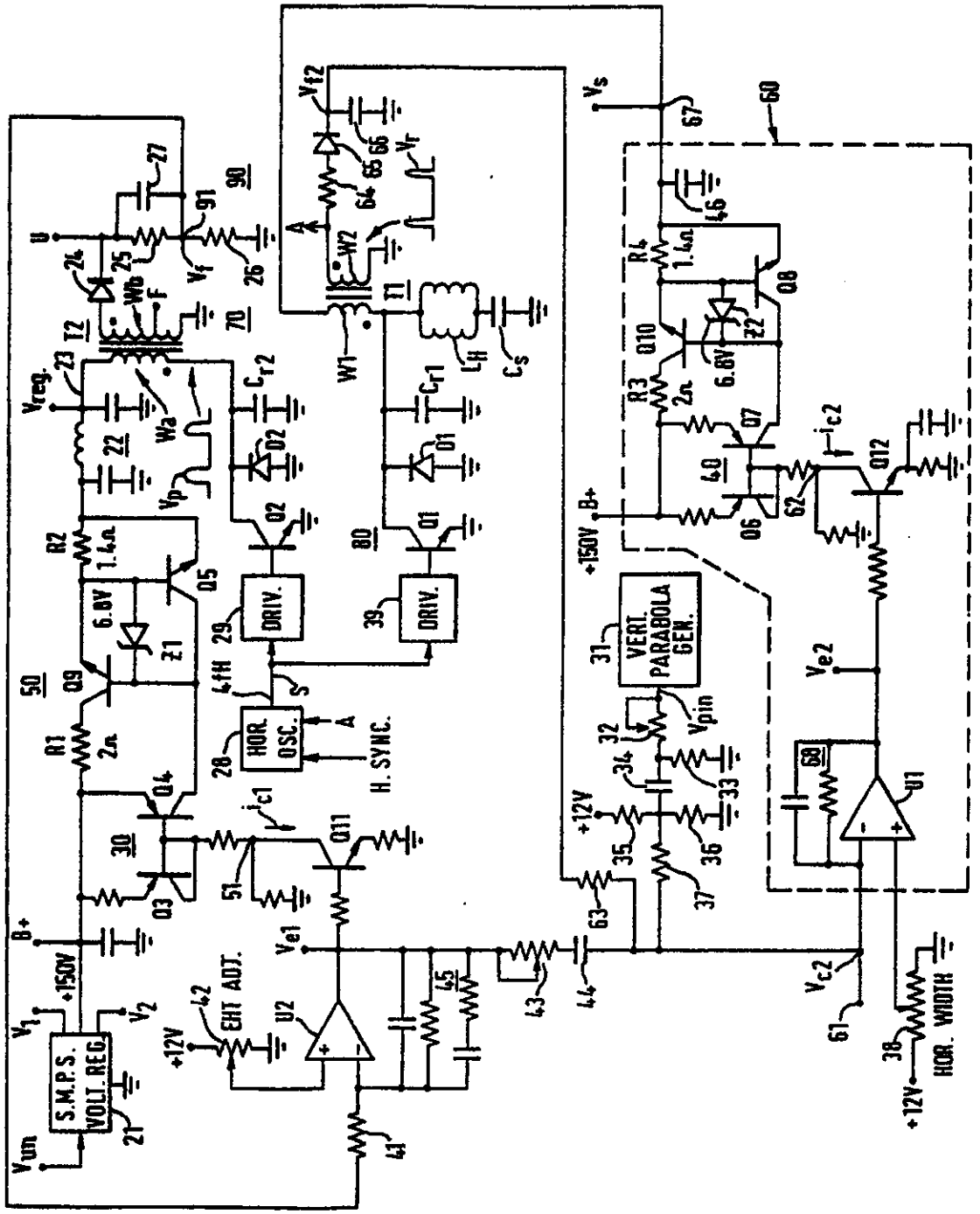
7. Schaltung nach Anspruch 1, **gekennzeichnet durch** einen dritten Spannungsregler (21), der aus einer ungeregelten Eingangsspannung eine geregelte Betriebsspannung ableitet als Versorgungsspannung für den Zeilenablenkspannungsregler (60) und den Hochspannungsregler (50) zur Ableitung von deren jeweiligen geregelten Spannungen.

8. Schaltung nach Anspruch 7, **dadurch gekennzeichnet,** daß der Hochspannungsregler (70) einen Schalter (Q9) aufweist, der mit einer ersten Wicklung ($W_a$) eines Hochspannungstransformators (T2) gekoppelt ist und daß die Anodenausgangsspannung aus der an einer zweiten Wicklung ($W_b$) des Transformators (T2) entstehenden Spannung erzeugt wird.

9. Schaltung nach einem der vorstehenden Ansprüche, **dadurch gekennzeichnet,** daß die Zeilenablenkschaltung (80) mit dem Zeilenablenkspannungsregler (60) über einen zweiten Transformator (T1) gekoppelt ist, in dem von der Zeilenablenkwicklung ($L_H$) eine Rücklaufimpulsspannung entsteht.

10. Schaltung nach Anspruch 9, **gekennzeichnet durch** eine Schaltung (64,65,66) zur Erzeugung eines Steuersignals für den Zeilenablenkspannungsregler (60) als Maß für die Rücklaufimpuls-Spannungsamplitude zur Veränderung der ersten geregelten Spannung im Sinne einer Regelung der Rücklaufimpulsspannung.

11. Schaltung nach einem der vorstehenden Ansprüche, **gekennzeichnet durch** einen Vertikalfrequenzsignalgenerator (31) zur Erzeugung eines vertikalfrequenten Regelsignals für den Zeilenablenkspannungsregler (60) zur Veränderung der ersten geregelten Spannung im Sinne einer Ost-West-Kissenkorrektur.


S.M.P.S. VOLT. REG.
HOR. OSC.
DRIV.
VERT. PARABOLA GEN.
H. SYNC.
EHT ADJ.
HOR. WIDTH
+150V
+12V
B+

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