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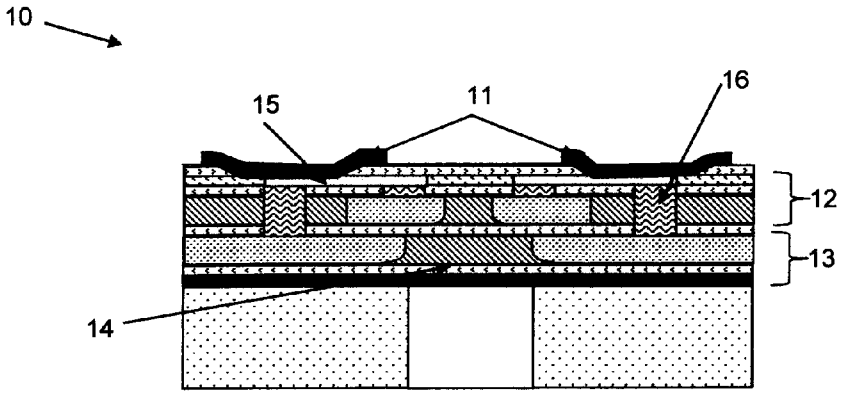

FIG. 1

(57) Abstract: The present invention relates to a sensor system (10). The sensor system comprises at least two contact pads (11), a read out integrated circuit (12), and a sensor device (13). The read out integrated circuit (12) is stacked on top of the sensor device (13), and it (12) is connected to the sensor device (13) through a plurality of vias (16). The at least two contact pads (11) are connected to the read out integrated circuit (12) and the sensor device (13) through a plurality of vias (16) and metal lines (15).

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A SENSOR SYSTEM AND A METHOD FOR FABRICATING THEREOF

FIELD OF INVENTION

The present invention relates to a sensor system and a method for fabricating the sensor system.

BACKGROUND OF THE INVENTION

Field Effect Transistor (FET) based chemical or biological sensor devices are widely used in different field such as medical diagnosis, water treatment system, food processing and the like for detecting chemical and biological compounds.

These sensor devices often require data processing devices such as read out circuit (ROIC) devices in order to produce a useful signal. However, the data processing devices pose challenges to integrate with the sensor devices especially in producing a miniaturized sensor system. Manufacturers typically obviate this problem by arranging a data processing device externally side by side with the sensor device on a planar. The data processing device is connected with the sensor device via wire bonding or through planar integration via metal contact line.

Such integration causes signal losses and leakages as it requires long electrical connection path. Moreover, such integration is dictated by the reduction of the lithography technology when space is limited. In addition, the integration requires packaging to protect the connection and the devices from environment. Separate packaging technologies need to be used for each discrete device due to the differences in the device height, materials, surface treatment and protection requirement.

Hence, in order to address the aforementioned issues, there is a need to provide a sensor system having an integrated sensor device with data processing device.

SUMMARY OF INVENTION

The present invention relates to a sensor system (**10**). The sensor system comprises at least two contact pads (**11**), a read out integrated circuit (**12**), and a

sensor device (**13**). The read out integrated circuit (**12**) is stacked on top of the sensor device (**13**), and it (**12**) is connected to the sensor device (**13**) through a plurality of vias (**16**). The at least two contact pads (**11**) are connected to the read out integrated circuit (**12**) and the sensor device (**13**) through a plurality of vias (**16**) and metal lines (**15**).

Preferably, the sensor system (**10**) is enclosed while having the at least two contact pads (**11**) and a sensing membrane (**14**) of the sensor device (**13**) exposed.

Preferably, the sensor device (**13**) includes a substrate (**20**) on which is provided with a sensing membrane (**14**).

Preferably, the sensor device (**13**) is a Field Effect Transistor (FET) based sensor device.

Preferably, the read out integrated circuit (**41**) is bonded to the sensor device (**42**) through a substrate (**43**).

A method of fabricating a sensor system (**10**) is also provided. The method comprises the steps of fabricating a sensor device (**13**); fabricating a read out integrated circuit (**12**) on top of the sensor device (**13**); and fabricating at least two contact pads (**11**) on top of the read out integrated circuit (**12**).

Preferably, the steps of fabricating the sensor device (**13**) includes the steps of depositing a first silicon nitride layer (**21**) on a substrate (**20**); depositing a silicon dioxide layer (**22**) onto the silicon nitride layer (**21**); depositing a polysilicon layer (**23**) onto the silicon dioxide layer (**22**); depositing a first sacrificial silicon dioxide layer (**24**) onto the polysilicon layer (**23**); depositing a first sacrificial silicon nitride layer (**25**) onto the first sacrificial silicon dioxide layer (**24**); coating and patterning a first resist layer (**26**) onto the first sacrificial silicon nitride layer (**25**); removing a portion of the polysilicon layer (**23**) to produce source/drain implant; removing the first resist layer (**26**); producing a channel implant; removing the first sacrificial layers of silicon dioxide (**24**) and silicon nitride (**25**); depositing a first protective silicon dioxide layer (**27**); coating and patterning a second resist layer (**28**) onto the first protective silicon dioxide layer (**27**); removing exposed portions (**27a**) of the first protective silicon

dioxide layer (**27**); plugging the removed first protective silicon dioxide layer (**16**) with tungsten material (**29**); and removing the second resist layer (**28**).

Preferably, the steps of fabricating the read out integrated circuit (**12**) includes the steps of depositing a first sacrificial silicon dioxide layer onto the sensor device (**13**); depositing a first sacrificial silicon nitride layer (**25**) onto the first sacrificial silicon dioxide layer (**24**); coating and patterning a first resist layer (**26**) onto the first sacrificial silicon nitride layer (**25**); removing a portion of the polysilicon layer (**23**) to produce source/drain implant; removing the first resist layer (**26**); producing a channel implant; removing the first sacrificial layers of silicon dioxide (**24**) and silicon nitride (**25**); depositing a first protective silicon dioxide layer (**27**); coating and patterning a second resist layer (**28**) onto the first protective silicon dioxide layer (**27**); removing exposed portions (**27a**) of the first protective silicon dioxide layer (**27**); plugging the removed first protective silicon dioxide layer (**16**) with tungsten material (**29**); and removing the second resist layer (**28**).

Preferably, the steps of fabricating the at least two contact pads (**11**) includes the steps of: depositing and patterning a second protective silicon dioxide layer (**30**) on top of the read out integrated circuit (**12**); depositing a first metal layer (**31**) onto the patterned second protective silicon dioxide layer (**30**); depositing and patterning a third protective silicon dioxide layer (**32**); depositing a second metal layer (**33**) onto the patterned third protective silicon dioxide layer (**32**); coating and patterning a third resist layer (**34**) onto the second metal layer (**33**); etching exposed portion of the second metal layer (**33**); removing the third resist layer (**34**); and back etching the substrate (**20**) until the first silicon nitride layer (**21**).

Advantageously, the present invention prevents a sensor system from fluid leakage, electrical shortage, and minimize noise signal.

Advantageously, the present invention increases reliability and response time of a sensor system due to shorter interconnections between the read out circuit and sensor device.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

FIG. 1 shows a vertical sectional view of a sensor system (**10**) according to an embodiment of the present invention.

FIGS. 2(a-s) show a method for fabricating the sensor system (**10**) of **FIG. 1**.

FIG. 3 shows a vertical sectional view of a sensor system (**40**) according to another embodiment of the present invention.

DESCRIPTION OF THE PREFFERED EMBODIMENT

A preferred embodiment of the present invention will be described herein below with reference to the accompanying drawings. In the following description, well know functions or constructions are not described in detail since they would obscure the description with unnecessary detail.

Referring now to **FIG. 1**, there is shown a vertical sectional view of a sensor system (**10**) according to an embodiment of the present invention. The sensor system (**10**) comprises of at least two contact pads (**11**), a read-out circuit integrated circuit or ROIC (**12**), and a sensor device (**13**). Preferably, the sensor system (**10**) is packaged and enclosed with a reliable and leak-free material while having the contact pads (**11**) and a sensing membrane (**14**) of the sensor device (**13**) exposed.

The contact pads (**11**) are provided on top of the ROIC (**12**). The contact pads (**11**) allow electrical connectivity of the ROIC (**12**) and sensor device (**13**) to an external circuit. The contact pads (**11**) are suitably made out of any conductive material such as copper, alloy and the like. The contact pads (**11**) are connected to the ROIC (**12**) and sensor device (**13**) through metal lines (**15**) and vias (**16**). The contact pads (**11**) are configured in accordance with the input/output and power requirements of the ROIC (**12**) and sensor device (**13**).

The ROIC (**12**) is stacked on top of the sensor device (**13**) and it is connected to the sensor device (**12**) through a plurality of vias (**16**). The ROIC (**12**) is configured to receive input signals from the sensor device (**13**) and thereon, process this input signals to provide a suitable output. The ROIC (**12**) is an integrated circuit which includes semiconductor devices such as analog to digital converter, amplifiers, transistors, capacitors, resistors and the like.

The sensor device (**13**) includes a substrate (**20**) on which is provided the sensing membrane (**14**) capable for chemical and/or biological sensing. Preferably, the sensor device (**13**) is a Field Effect Transistor (FET) based sensor device. The sensing membrane (**14**) of the sensor device (**13**) is provided at the opposing surface of the ROIC (**12**) and it is exposed for contact with a sample fluid for sensing chemical and/or biological properties. In this regard, the contact pads (**11**) and ROIC (**12**) are not exposed to a fluid region and thus, preventing electrical shortage to occur.

Referring now to **FIGS. 2**, a method of fabricating the sensor system (**10**) of **FIG. 1** is provided. The method of fabricating a sensor system (**10**) generally includes fabricating a sensor device (**13**) which includes the steps as shown in **FIGS. 2a** to **2j**; fabricating a ROIC (**12**) on top of the sensor device (**13**) which includes the steps similar to steps as shown in **FIGS. 2b** to **2k**; and fabricating at least two contact pads (**11**) on top of the ROIC (**12**) which includes the steps as shown in **FIGS. 2l** to **2s**. It should be understood that the method provided include more or less steps or may be performed in the context of a larger processing scheme. Furthermore, the method should not be construed as limiting the order in which the individual steps may be performed.

Firstly, a silicon nitride layer (**21**) is deposited on a substrate (**20**) and thereon, a silicon dioxide layer (**22**) is deposited onto the silicon nitride layer (**21**) as shown in **FIG. 2a**.

Next, a doped polysilicon layer (**23**) is deposited onto the silicon dioxide layer (**22**) as shown in **FIG. 2b**.

In **FIG. 2c**, a first sacrificial silicon dioxide layer (**24**) is deposited onto the doped polysilicon layer (**23**). Thereon, a first sacrificial silicon nitride layer (**25**) is deposited onto the first sacrificial silicon dioxide layer (**24**).

Next, as shown in **FIG. 2d**, a first resist layer (**26**) is coated and patterned onto the first sacrificial silicon nitride layer (**25**) for selective removal of the doped polysilicon layer (**23**).

The doped polysilicon layer (**23**) is selectively removed by means of plasma etching or wet chemical etching using hydrofluoric acid (HF), nitric acid (HNO_3) and water (H_2O) as shown in **FIG. 2e**. The selective removal of the doped polysilicon layer (**23**) produces source/drain implant. Thereon, the first resist layer (**26**) is removed by means of resist stripping using solvents such as acetone, NMP (1-Methyl-2-pyrrolidon) or DMSO (Dimethyl sulfoxide).

Next, as shown in **FIG. 2f**, a channel implant is produced by means of ion implantation of Boron (B), Phosphorus (P) or Arsenic (As).

In **FIG. 2g**, the first sacrificial layers of silicon dioxide (**24**) and silicon nitride (**25**) are removed. The first sacrificial layers of silicon dioxide (**24**) and silicon nitride (**25**) are removed by means of plasma etching with tetrafluoromethane (CF_4), trifluoromethane (CHF_3) or a combination thereof.

Thereon, a first protective silicon dioxide layer (**27**) is deposited as shown in **FIG. 2h**. The first protective silicon dioxide layer (**27**) is then coated with a second resist layer (**28**). The second resist layer (**28**) is patterned and thus, exposing a portion of the first protective silicon dioxide layer (**27**). The exposed portion of the first protective silicon dioxide layer (**27**) is then removed to produce vias (**16**) as shown in **FIG. 2i**.

Next, as shown in **FIG. 2j**, the removed first protective silicon dioxide layer are plugged with tungsten (**29**) and thus, producing the vias (**16**) for the connections of the sensor device (**13**). The second resist layer (**28**) is removed by means of resist stripping using solvents such as acetone, NMP (1-Methyl-2-pyrrolidon) or DMSO (Dimethyl sulfoxide).

The steps as shown in **FIG. 2b** to **FIG. 2j** produce the sensor device and the steps are repeated accordingly for fabricating the ROIC (**12**). **FIG. 2k** shows the fabricated ROIC (**12**) on top of the sensor device (**13**).

After the ROIC (**12**) has been fabricated, a second protective silicon dioxide layer (**30**) is deposited and patterned on top of the ROIC (**12**) as shown in **FIG. 2l**.

Next, as shown in **FIG. 2m**, a first metal layer (**31**) is deposited onto the patterned second protective silicon dioxide layer (**30**). The first metal layer (**31**) is patterned to produce the metal lines (**15**) for connectivity of the vias (**16**) to the contact pads (**11**).

Thereon, a third protective silicon dioxide layer (**32**) is deposited and patterned to form the contact pads (**11**) as shown in **FIG. 2n**. A second metal layer (**33**) is then deposited onto the patterned third protective silicon dioxide layer (**32**) as shown in **FIG. 2o**.

A third resist layer (**34**) is then coated and patterned onto the second metal layer (**33**) for selective removal of the second metal layer (**33**) as shown in **FIG. 2p**. The exposed portion of the second metal layer (**33**) is etched by means of plasma etching using boron trichloride (BCl_3) or wet chemical etching of potassium hydroxide (KOH), sodium hydroxide (NaOH) or phosphoric acid (H3PO4) with nitric acid (HNO3), acetic acid (HAc) and water (H2O), as shown in **FIG. 2q**.

In **FIG. 2r**, the third resist layer (**34**) is removed by means of resist stripping using solvents such as acetone, NMP (1-Methyl-2-pyrrolidon) or DMSO (Dimethyl sulfoxide).

Lastly, the substrate (**20**) is back etched until it reaches the first silicon nitride layer (**21**) and thus, exposing a portion of the first silicon nitride layer (**21**) as shown in **FIG. 2s**. The substrate (**20**) is back etched by means of wet etching or deep reactive-ion etching (DRIE).

Referring now to **FIG. 3**, there is provided a vertical sectional view of a sensor system (**40**) in accordance with another embodiment of the present invention. The sensor system (**40**) includes a read-out circuit integrated circuit or ROIC (**41**) stacked onto a sensor device (**42**). The ROIC (**41**) is bonded to the sensor device (**42**) through a substrate (**43**). Preferably, the substrate (**43**) to bond the ROIC with the sensor device is made out of silicon.

While embodiments of the invention have been illustrated and described, it is not intended that these embodiments illustrated and describe all possible forms of the invention. Rather, the words used in the specifications are words of description rather than limitation and various changes may be made without departing from the scope of the invention.

CLAIMS

1. A sensor system (**10**) comprising:
   a) at least two contact pads (**11**),
   b) read out integrated circuit (**12**), and
   c) a sensor device (**13**);

   characterized in that the read out integrated circuit (**12**) is stacked on top of the sensor device (**13**), and wherein the read out integrated circuit (**12**) is connected to the sensor device (**13**) through a plurality of vias (**16**), and wherein the at least two contact pads (**11**) are connected to the read out integrated circuit (**12**) and the sensor device (**13**) through a plurality of vias (**16**) and metal lines (**15**).

2. A sensor system (**10**) as claimed in claim **1**, wherein the sensor system (**10**) is enclosed while having the at least two contact pads (**11**) and a sensing membrane (**14**) of the sensor device (**13**) exposed.

3. A sensor system (**10**) as claimed in claim **1**, wherein the sensor device (**13**) includes a substrate (**20**) on which is provided with a sensing membrane (**14**)

4. A sensor system (**10**) as claimed in claim **3**, wherein the sensor device (**13**) is a Field Effect Transistor (FET) based sensor device.

5. A sensor system (**40**) as claimed in claim **1**, wherein the read out integrated circuit (**41**) is bonded to the sensor device (**42**) through a substrate (**43**).

6. A method of fabricating a sensor system (**10**) as claimed in claim **1**, comprising the steps of:

   a) fabricating a sensor device (**13**);
   b) fabricating a read out integrated circuit (**12**) on top of the sensor device (**13**); and
   c) fabricating at least two contact pads (**11**) on top of the read out integrated circuit (**12**).

7. A method as claimed in claim **6**, wherein fabricating the sensor device (**13**) comprising the steps of:

a) depositing a silicon nitride layer (**21**) on a substrate (**20**);

b) depositing a silicon dioxide layer (**22**) onto the silicon nitride layer (**21**);

c) depositing a polysilicon layer (**23**) onto the silicon dioxide layer (**22**);

d) depositing a first sacrificial silicon dioxide layer (**24**) onto the polysilicon layer (**23**);

e) depositing a first sacrificial silicon nitride layer (**25**) onto the first sacrificial silicon dioxide layer (**24**);

f) coating and patterning a first resist layer (**26**) onto the first sacrificial silicon nitride layer (**25**);

g) removing a portion of the polysilicon layer (**23**) to produce source/drain implant;

h) removing the first resist layer (**26**);

i) producing a channel implant;

j) removing the first sacrificial layers of silicon dioxide (**24**) and silicon nitride (**25**);

k) depositing a first protective silicon dioxide layer (**27**);

l) coating and patterning a second resist layer (**28**) onto the first protective silicon dioxide layer (**27**);

m) removing exposed portions (**27a**) of the first protective silicon dioxide layer (**27**);

n) plugging the removed first protective silicon dioxide layer (**16**) with tungsten material (**29**); and

o) removing the second resist layer (**28**).

8. A method as claimed in claim **6**, wherein fabricating the read out integrated circuit (**12**) comprising the steps of:

a) depositing a first sacrificial silicon dioxide layer onto the sensor device (**13**);

b) depositing a first sacrificial silicon nitride layer (**25**) onto the first sacrificial silicon dioxide layer (**24**);

c) coating and patterning a first resist layer (**26**) onto the first sacrificial silicon nitride layer (**25**);

d) removing a portion of the polysilicon layer (**23**) to produce source/drain implant;

e) removing the first resist layer (**26**);

f) producing a channel implant;

g) removing the first sacrificial layers of silicon dioxide (**24**) and silicon nitride (**25**);

h) depositing a first protective silicon dioxide layer (**27**);

i) coating and patterning a second resist layer (**28**) onto the first protective silicon dioxide layer (**27**);

j) removing exposed portions (**27a**) of the first protective silicon dioxide layer (**27**);

k) plugging the removed first protective silicon dioxide layer (**16**) with tungsten material (**29**); and

l) removing the second resist layer (**28**).

9. A method as claimed in claim **6**, wherein fabricating the at least two contact pads (**11**) comprising the steps of:

a) depositing and patterning a second protective silicon dioxide layer (**30**) on top of the read out integrated circuit (**12**);

b) depositing a first metal layer (**31**) onto the patterned second protective silicon dioxide layer (**30**);

c) depositing and patterning a third protective silicon dioxide layer (**32**);

d) depositing a second metal layer (**33**) onto the patterned third protective silicon dioxide layer (**32**);

e) coating and patterning a third resist layer (**34**) onto the second metal layer (**33**);

f) etching exposed portion of the second metal layer (**33**);

g) removing the third resist layer (**34**); and

h) back etching the substrate (**20**) until the first silicon nitride layer (**21**).

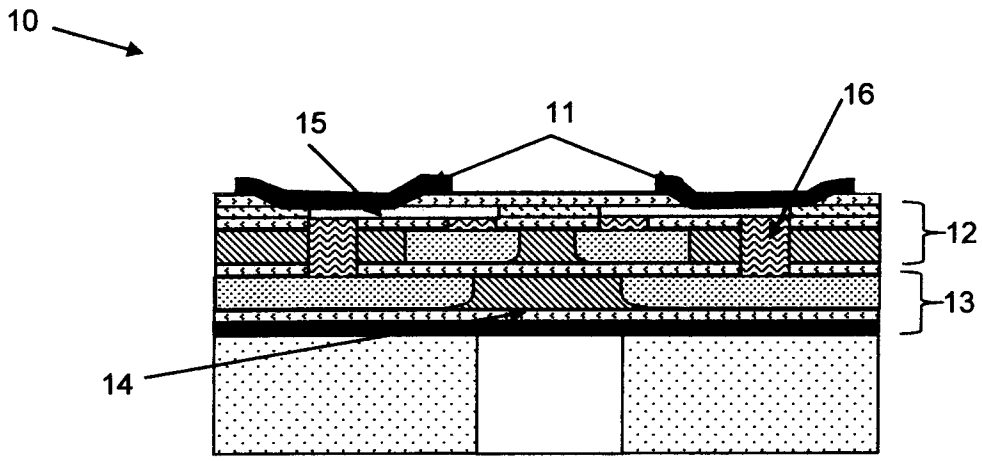

FIG. 1

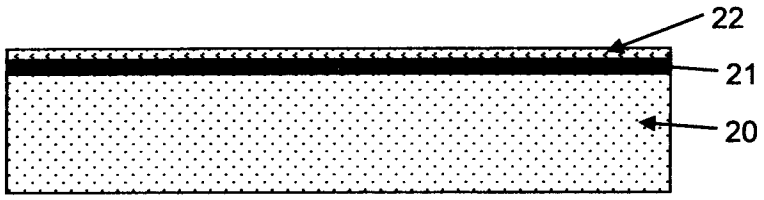

FIG. 2a

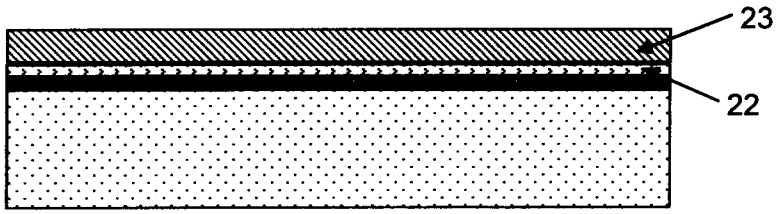

FIG. 2b

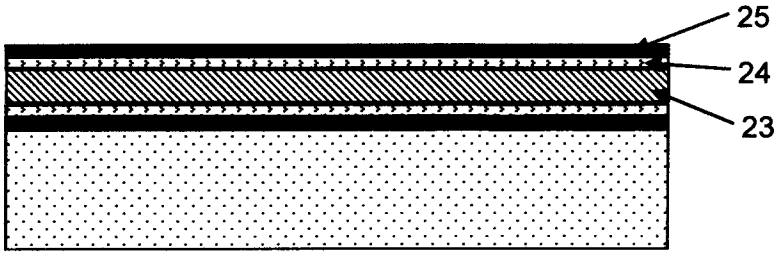

FIG. 2c

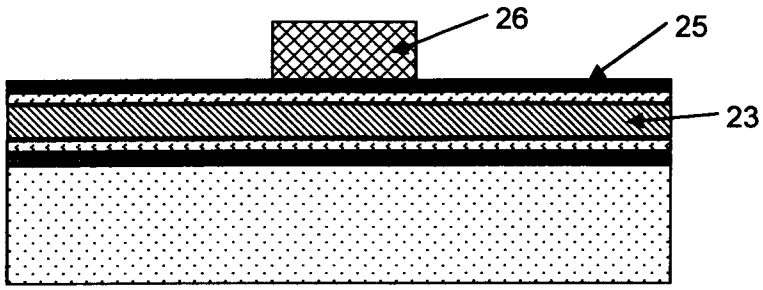

FIG. 2d

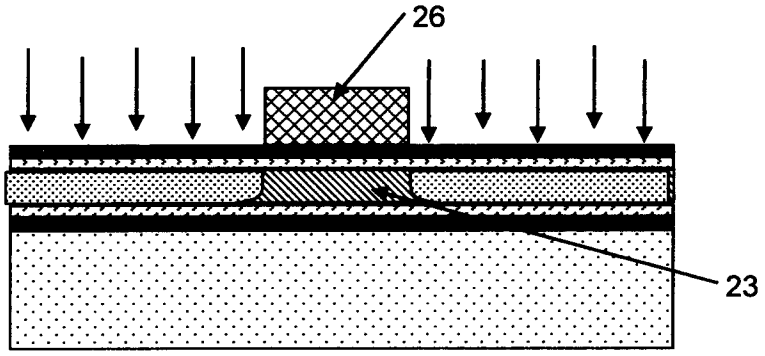

FIG. 2e

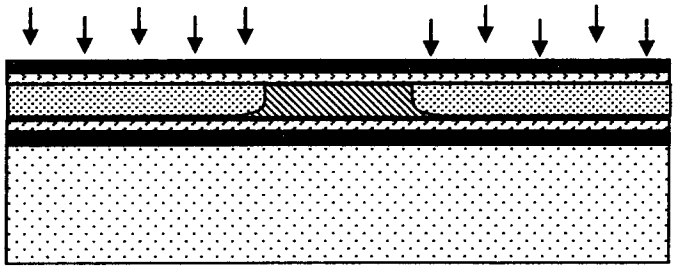

FIG. 2f

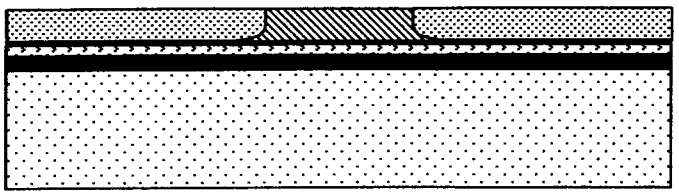

FIG. 2g

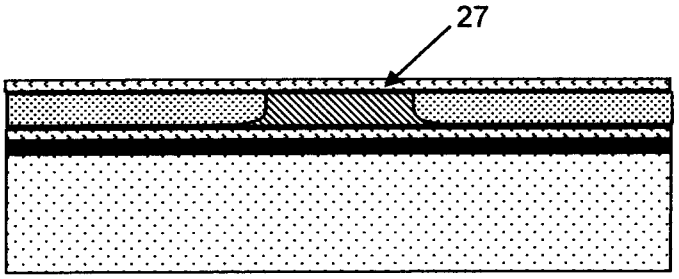

FIG. 2h

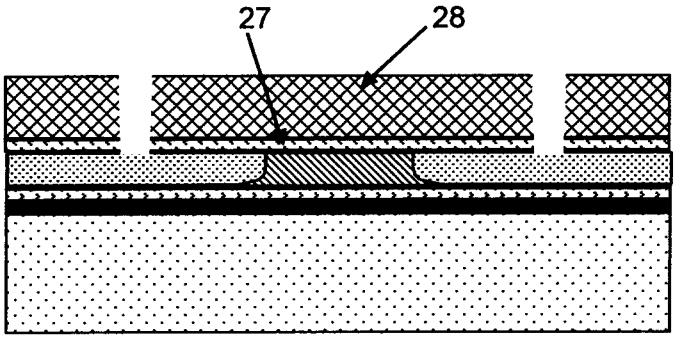

FIG. 2i

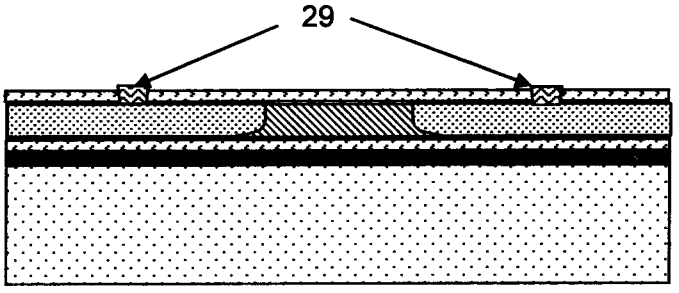

FIG. 2j

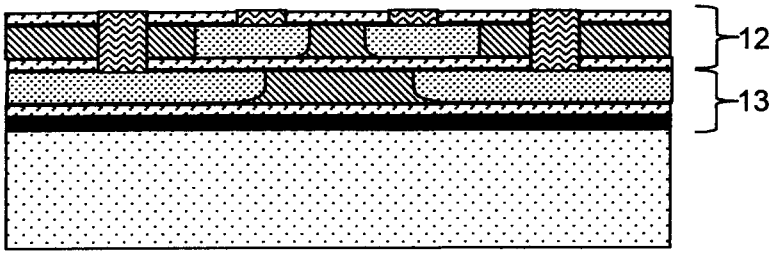

FIG. 2k

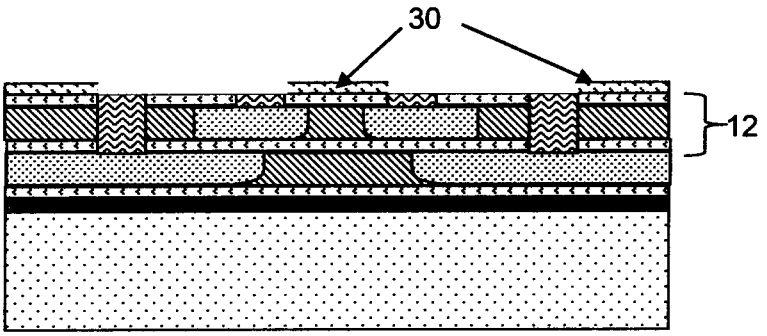

FIG. 2l

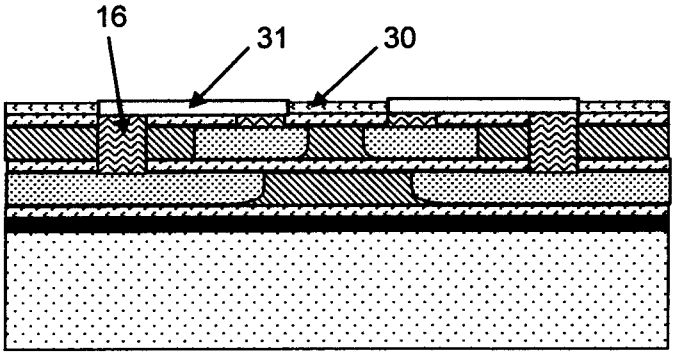

FIG. 2m

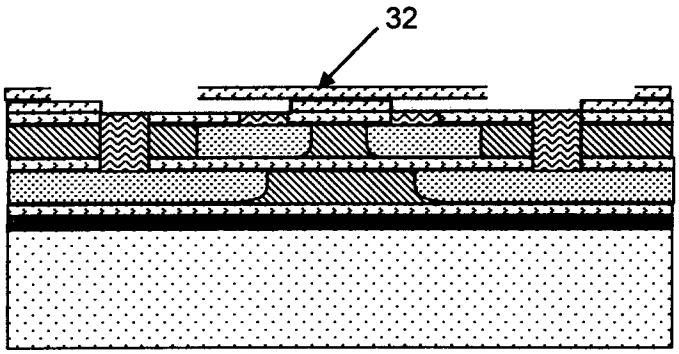

FIG. 2n

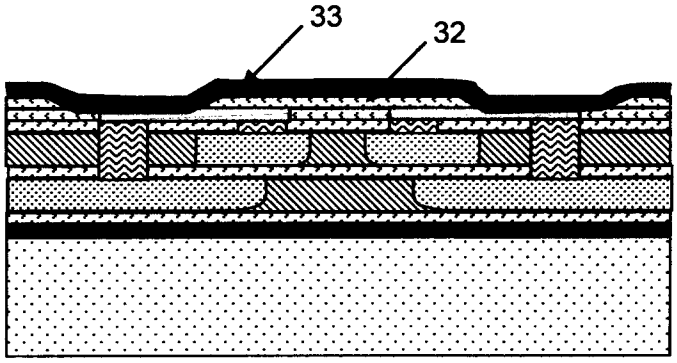

FIG. 2o

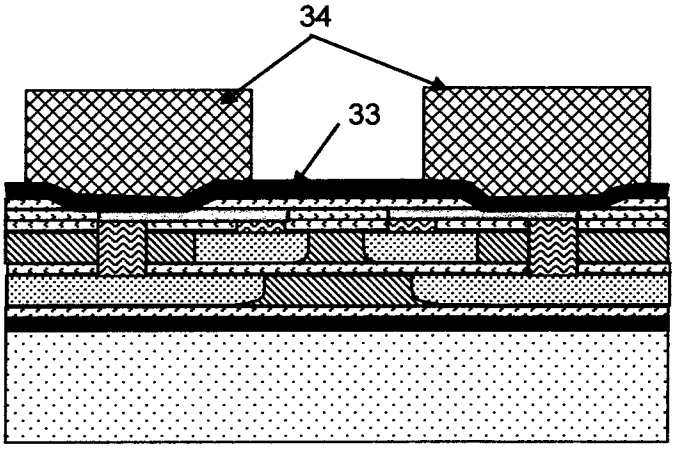

FIG. 2p

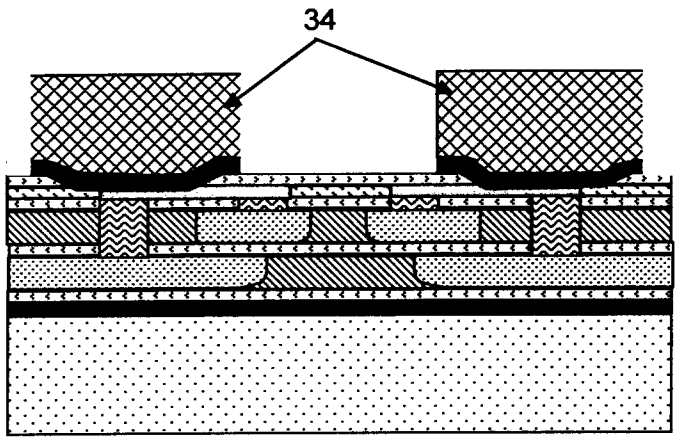

FIG. 2q

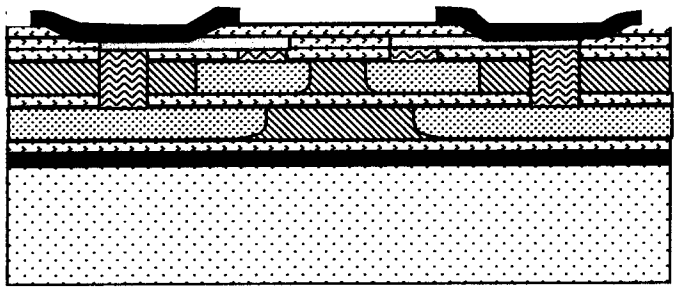

FIG. 2r

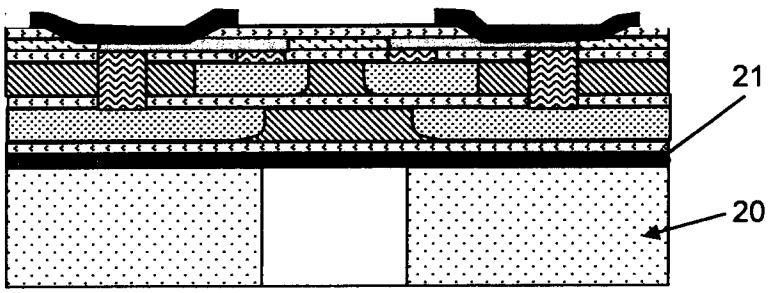

FIG. 2s

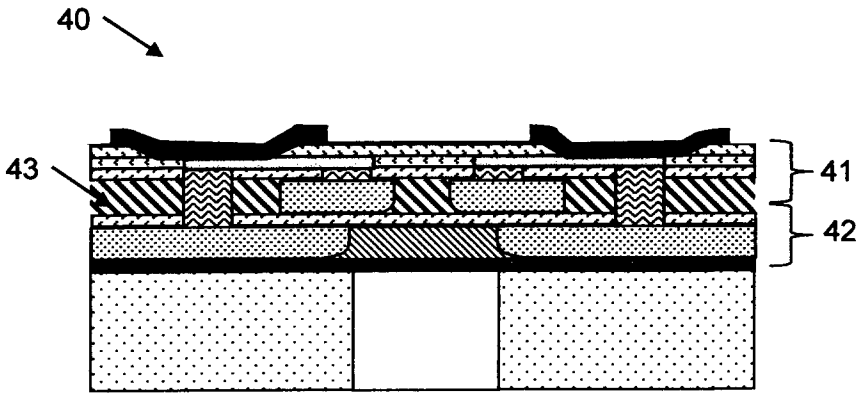

FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/MY2012/000027

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

G01N 27/414 (2006.01) ***H01L 21/77*** (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPODOC & WPI, keywords: detector, sensor, pad, contact, terminal, connect, conduct, electrode, cavity, aperture, groove, open, trench, passage, via, hole, FET, transistor, dice, die, IC, integrated circuit, ROIC, processor, readout circuit, and similar terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2006/0090541 A1 (THEIL) 4 May 2006 Paragraphs 0016-0035, Figs. 1, 3	1-3, 5-6, 8-9 4, 7
Y	WO 1994/022006 A1 (FRAUNHOFER-GESELLSCHAFT ZUR FORDERUNG DER ANGEWANDTEN FORSCHUNG E.V) 29 September 1994 Abstract, description of Figs. 1-5	4, 7
Y	US 5693545 A (CHUNG ET AL.) 2 December 1997 Abstract, column 3, line 2-column 6, line 10	4, 7
Y	US 5077229 A (FORLANI) 31 December 1991 Abstract, column 2, line 27- column 3, line 41	4, 7
A	US 2008/0121946 A1 (YOUN ET AL.) 29 May 2008 Whole document	

☐ Further documents are listed in the continuation of Box C ☒ See patent family annex

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 April 2012	27 April 2012
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. +61 2 6283 7999	Authorized officer **JAYATI RAY** AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No : +61 2 6222 3654

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/MY2012/000027

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member	
US	2006090541	US	7096716
WO	9422006	DE	4308081
US	5693545	NONE	
US	5077229	EP	0363805
US	2008121946	NONE	

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX