



**Fig. 1**

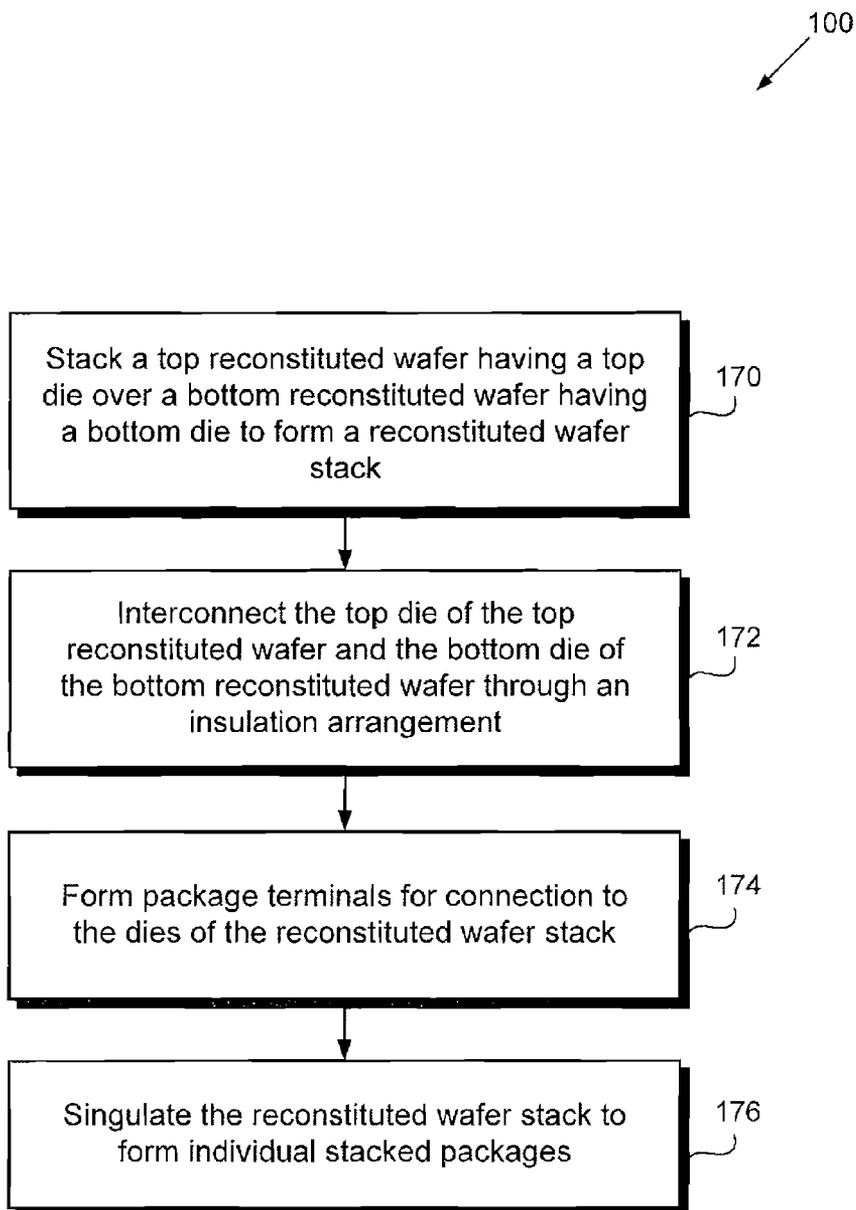


Fig. 2A

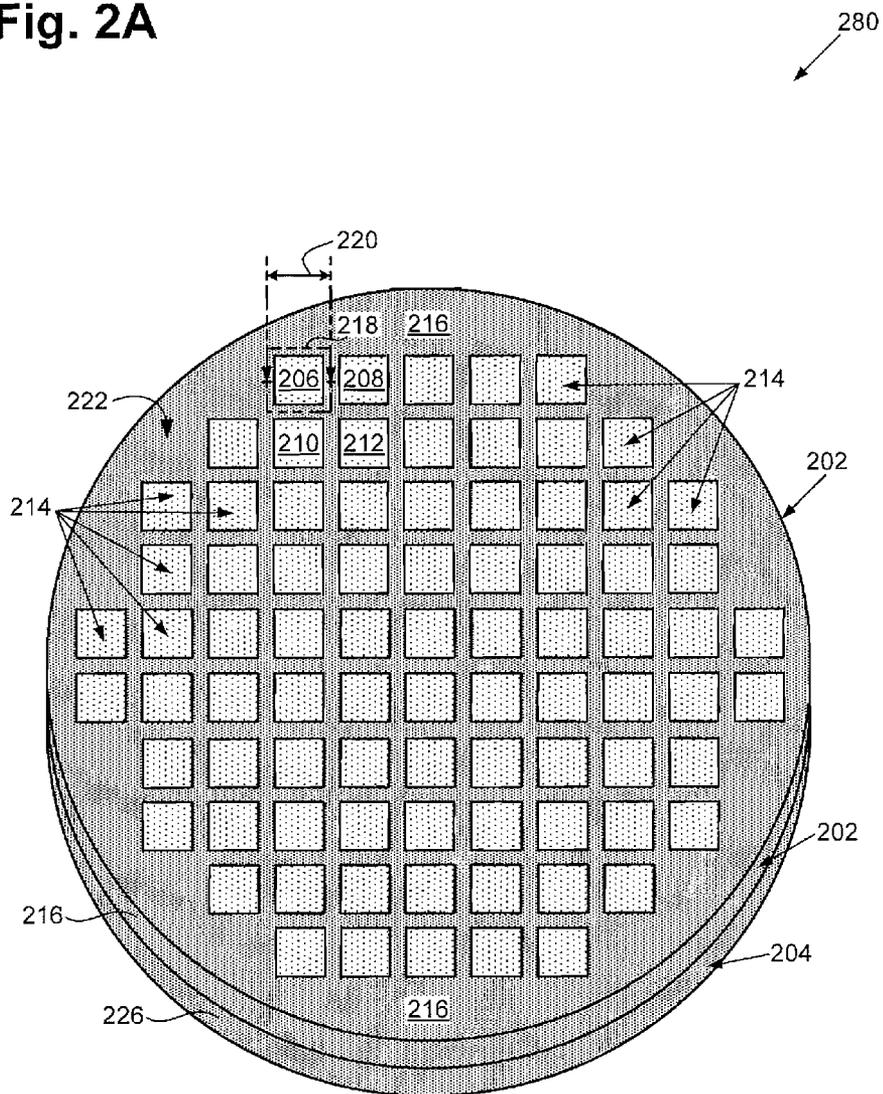


Fig. 2B

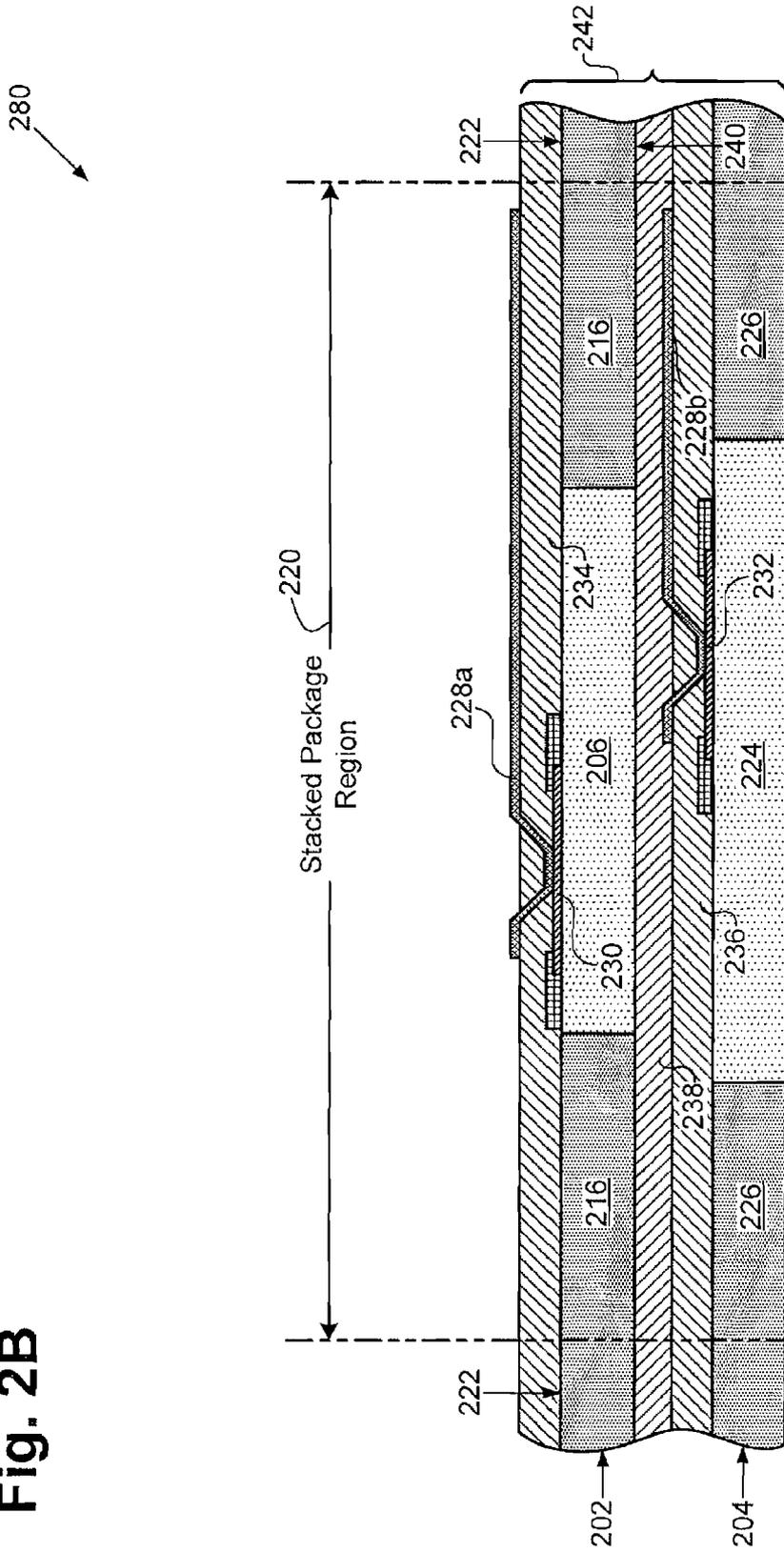


Fig. 2C

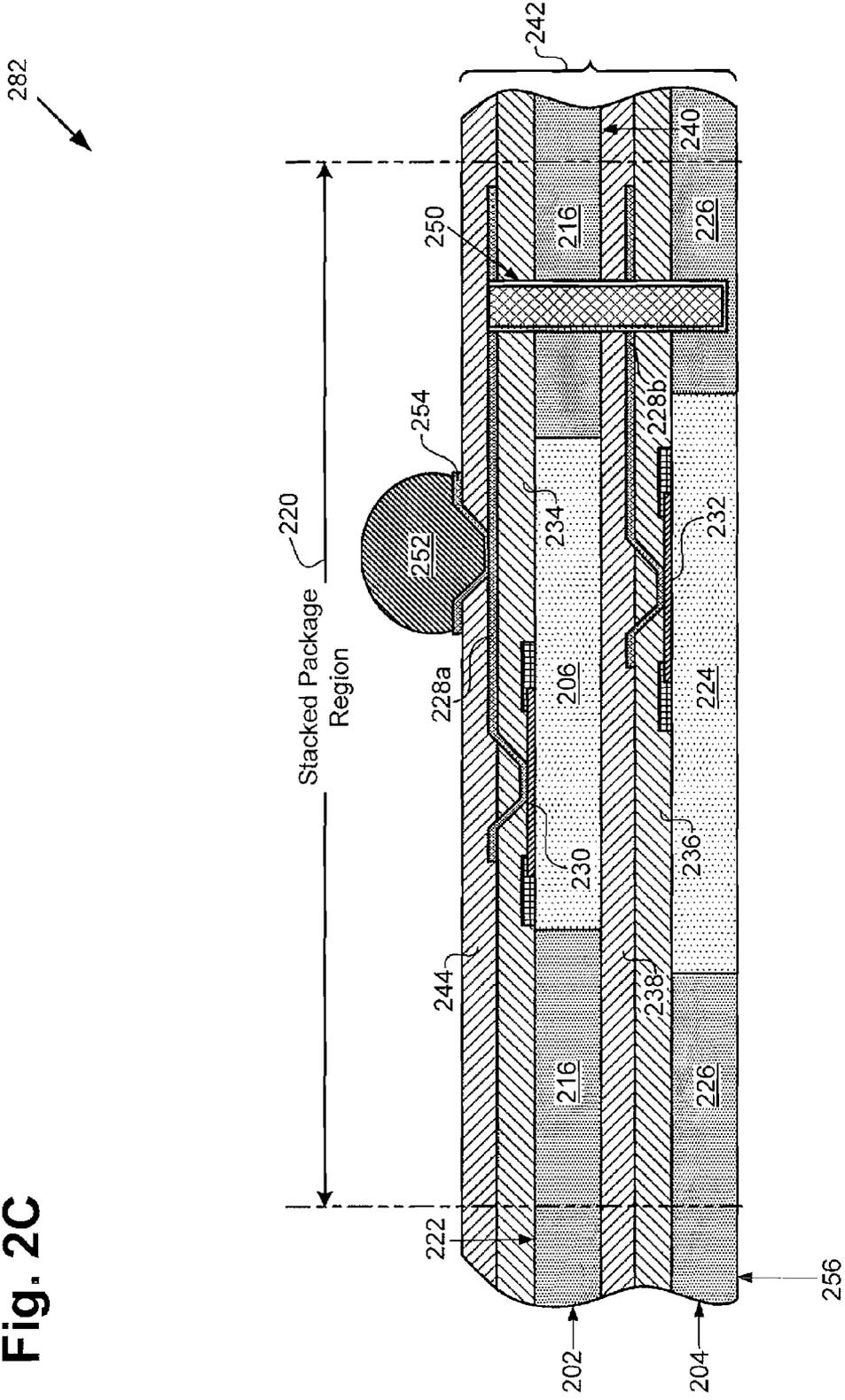


Fig. 2D

284

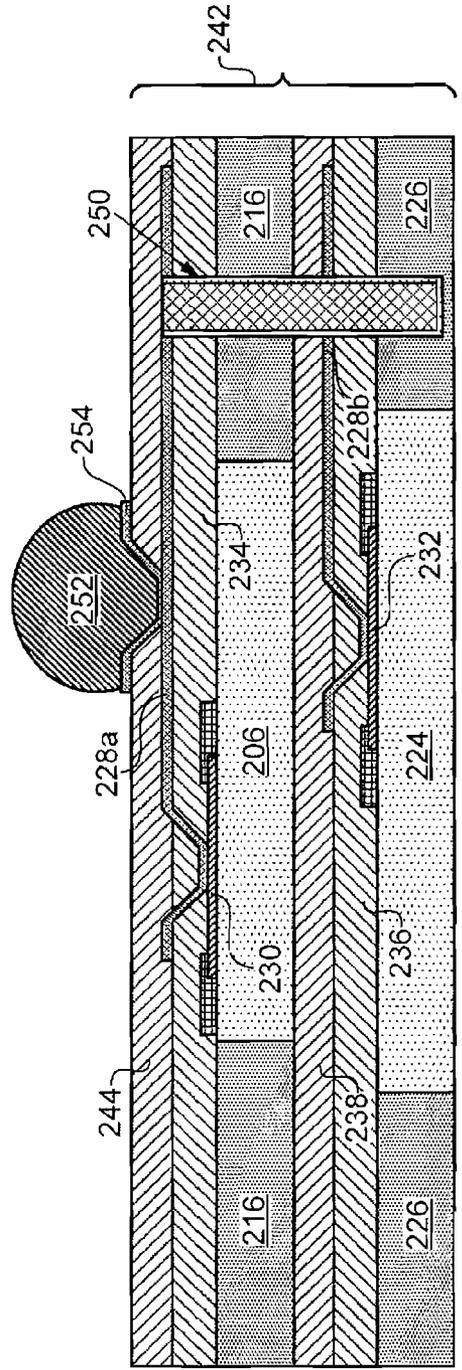
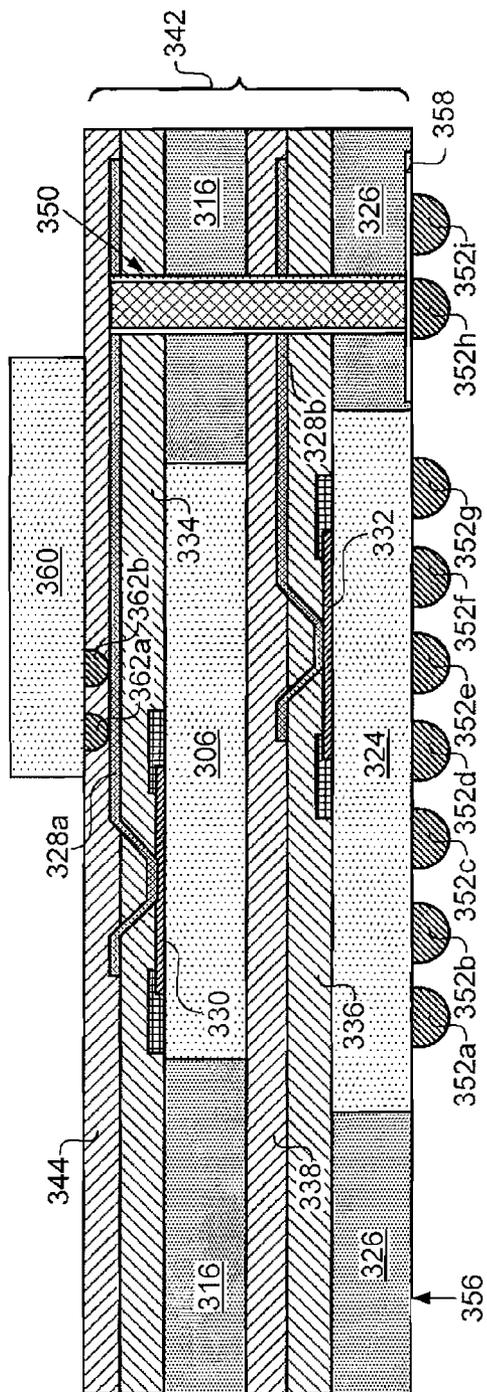


Fig. 3

300



## STACKED PACKAGING USING RECONSTITUTED WAFERS

### BACKGROUND

[0001] Packaging for dies that include, for example, at least one integrated circuit (IC), is continually trending towards reduced package size with increased package density. For example, electronic devices that include these packages, such as cell phones, hands-free headsets, camcorders, cameras, and personal computers, continue to be made smaller. At the same time, these electronic devices increasingly demand higher levels of functionality. However, incorporating higher levels of functionality into these electronic devices tends to increase package size and reduce package density. For example, incorporating higher levels of functionality typically requires additional circuitry and/or dies. The additional circuitry and/or dies can complicate packaging. As one example, among other considerations, the additional circuitry and/or dies may require accommodation of additional input/output (I/O) pads.

[0002] Complications to packaging may be of particular concern in electronic devices, such as portable devices, where component space and layout options for packages are limited. For example, a cell phone may have a form factor that constrains component space in a particular dimension. One approach to coping with limited component space and layout options would be to stack packaged dies to reduce their combined footprint. For example, each of the packaged dies may be housed in a respective package. Then, using package level processes, the respective packages could be stacked on one another and interconnected.

### SUMMARY

[0003] The present disclosure is directed to stacked packaging using reconstituted wafers, substantially as shown in and/or described in connection with at least one of the figures, and as set forth more completely in the claims.

### BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1 presents an exemplary flowchart illustrating a method for manufacturing a stacked package, according to an implementation of the present disclosure.

[0005] FIG. 2A presents an exemplary perspective view of a reconstituted wafer stack, according to an implementation of the present disclosure.

[0006] FIG. 2B presents an exemplary cross-sectional view of a portion of a reconstituted wafer stack, according to an implementation of the present disclosure.

[0007] FIG. 2C presents an exemplary cross-sectional view of a portion of a reconstituted wafer stack, according to an implementation of the present disclosure.

[0008] FIG. 2D presents an exemplary cross-sectional view of a stacked package, according to an implementation of the present disclosure.

[0009] FIG. 3 presents an exemplary cross-sectional view of a stacked package, according to an implementation of the present disclosure.

### DETAILED DESCRIPTION

[0010] The following description contains specific information pertaining to implementations in the present disclosure. One skilled in the art will recognize that the present disclosure may be implemented in a manner different from

that specifically discussed herein. The drawings in the present application and their accompanying detailed description are directed to merely exemplary implementations. Unless noted otherwise, like or corresponding elements among the figures may be indicated by like or corresponding reference numerals. Moreover, the drawings and illustrations in the present application are generally not to scale, and are not intended to correspond to actual relative dimensions.

[0011] FIG. 1 presents exemplary flowchart 100 illustrating a method for manufacturing a stacked package. The approach and technique indicated by flowchart 100 are sufficient to describe at least one implementation of the present disclosure, however, other implementations of the disclosure may utilize approaches and techniques different from those shown in flowchart 100. Furthermore, while flowchart 100 is described with respect to FIGS. 2A, 2B, 2C, & 2D the disclosed inventive concepts are not intended to be limited by specific features shown in FIGS. 2A, 2B, 2C, & 2D.

[0012] Referring now to flowchart 100 of FIG. 1 and FIGS. 2A and 2B, flowchart 100 includes stacking a top reconstituted wafer having a top die over a bottom reconstituted wafer having a bottom die to form a reconstituted wafer stack (action 170 in flowchart 100). FIGS. 2A and 2B show portions of reconstituted wafer stack 280 after action 170, in accordance with implementations of the present disclosure.

[0013] FIG. 2A presents a perspective view of reconstituted wafer stack 280, according to an implementation of the present disclosure. Reconstituted wafer stack 280 includes top reconstituted wafer 202 and bottom reconstituted wafer 204. As shown in FIG. 2A, top reconstituted wafer 202 includes stacked package region 218, which is designated for formation of a stacked package, such as stacked package 284 in FIG. 2D. In FIG. 2A, stacked package region 218 is rectangular and extends completely through reconstituted wafer stack 280. FIG. 2B presents a cross-sectional view of a portion of reconstituted wafer stack 280 along cross-section 220.

[0014] As shown in FIG. 2A, top reconstituted wafer 202 includes top dies 214, of which top dies 206, 208, 210, and 212 are individually labeled, and top molding compound 216 (or more generally "top passivation 216"). FIG. 2A shows top dies 214 being arranged in a grid-like pattern, with each being flanked by top molding compound 216. As shown in FIG. 2A, top molding compound 216 forms a border around and flanks each of top dies 214.

[0015] In one implementation, top dies 214 have been singulated from a same wafer, such as a silicon wafer. In other implementations, at least one of top dies 214 has been singulated from a different wafer than at least another of top dies 214. Furthermore, any or all of top dies 214 can be of substantially identical dimensions with respect to one another (e.g., width, length, thickness), or any dimension can be different. Any of top dies 214 can include an integrated circuit (IC) and/or other electrical components, such as, for example, passive components. In one implementation, each of top dies 214 includes an IC.

[0016] Top reconstituted wafer 202 can be fabricated utilizing various means. In one implementation, top reconstituted wafer 202 is fabricated utilizing embedded wafer level techniques, although in some implementations, other or additional techniques are utilized. In one specific implementation, top dies 214 are placed on an adhesive layer in a grid-like pattern. Top dies 214 are then covered with top molding compound 216 so as to be embedded within top molding compound 216. Subsequently, top molding compound 216 is

thinned to form top reconstituted wafer **202**. In the implementations shown, top molding compound **216** is thinned to reach top dies **214**. However, in other implementations, a layer of top molding compound **216** can remain than covers each of top dies **214**.

**[0017]** Bottom reconstituted wafer **204** can be fabricated by utilizing the same, similar, or different means as top reconstituted wafer **202**. Similar to top dies **214** of top reconstituted wafer **202**, bottom reconstituted wafer **204** includes a plurality of bottom dies, of which bottom die **224** is shown in FIG. **2B**. Furthermore, similar to top dies **214**, the plurality of bottom dies can be arranged in a grid-like pattern, which can be different than the grid-like pattern of top dies **214** (not shown). Also, similar to top dies **214**, bottom molding compound **226** (or more generally “bottom passivation **226**”) forms a border around and flanks each of the plurality of bottom dies.

**[0018]** As shown in FIG. **2B**, in some implementations, top reconstituted wafer **202** has top redistribution layer (top RDL) **228a**. Additionally or instead, in some implementations, bottom reconstituted wafer **204** has bottom redistribution layer (bottom RDL) **228b**. Top RDL **228a** is electrically connected top die **206** and bottom RDL **228b** is electrically connected to bottom die **224**. Top RDL **228a** and bottom RDL **228b** include conductive material, such as copper and route respective top and bottom input and/or output (I/O) pads **230** and **232** of top die **206** and bottom die **224**. Although only top RDL **228a**, bottom RDL **228b**, and top and bottom I/O pads **230** and **232** are shown, top reconstituted wafer **202** and bottom reconstituted wafer **204** each include a plurality of RDLs and I/O pads that are not visible in FIGS. **2A** and **2B**. Furthermore, any of the plurality of RDLs and I/O pads can be on either side of top reconstituted wafer **202** and bottom reconstituted wafer **204** and may include one or multiple levels or layers. As one example, top RDL **228a** and top I/O pad **230** are on top side **222**, but may be on bottom side **240** in some implementations (or may not be present at all).

**[0019]** As shown in FIG. **2B**, top RDL **228a** is on top die passivation **234** (which may also be referred to as “top die RDL passivation **234**”) and bottom RDL **228b** is on bottom die passivation **236** (which may also be referred to as “bottom die RDL passivation **236**”). Also, bottom RDL passivation **238** is on bottom RDL **228b**. Top die passivation **234**, bottom die passivation **236**, and bottom RDL passivation **238** each include dielectric material. For example, in the present implementation, top die passivation **234**, bottom die passivation **236**, and bottom RDL passivation **238** are dielectric polymers. In various implementations, top die passivation **234**, bottom die passivation **236**, and bottom RDL passivation **238** can be the same or different materials than one another.

**[0020]** As shown in FIGS. **2A** and **2B**, top reconstituted wafer **202** having top die **206** is stacked over bottom reconstituted wafer **204** having bottom die **224** to form reconstituted wafer stack **280**. In one implementation, top reconstituted wafer **202** is fabricated separately from bottom reconstituted wafer **204** and top reconstituted wafer **202** is subsequently stacked over bottom reconstituted wafer **204**. In other implementations, top reconstituted wafer **202** is formed over and/or on bottom reconstituted wafer **204**, thereby stacking top reconstituted wafer **202** over bottom reconstituted wafer **204**. While top reconstituted wafer **202** is stacked so that bottom side **240** faces downward, in other implementa-

tions, bottom side **240** can face upward. Also, in some implementations, bottom reconstituted wafer **204** is utilized as a carrier wafer.

**[0021]** In various implementations, any of top RDL **228a**, bottom RDL **228b**, top I/O pad **230**, bottom I/O pad **232**, top die passivation **234**, bottom die passivation **236**, and bottom RDL passivation **238** and/or other features can be formed prior to stacking top reconstituted wafer **202** over bottom reconstituted wafer **204**. In some implementations, at least some of top RDL **228a**, top I/O pad **230**, top die passivation **234**, and/or other features can be formed after stacking top reconstituted wafer **202** over bottom reconstituted wafer **204**.

**[0022]** In various implementations, stacking includes adhering the top reconstituted wafer to the bottom reconstituted wafer using a passivation layer. For example, in the present implementation, stacking includes adhering top reconstituted wafer **202** to bottom reconstituted wafer **204** using bottom RDL passivation **238**. Thus, reconstituted wafer stack **280** can be thin to provide high package density, as in the implementation shown. Referring now to flowchart **100** of FIG. **1** and FIG. **2C**, flowchart **100** includes interconnecting the top die of the top reconstituted wafer and the bottom die of the bottom reconstituted wafer through an insulation arrangement (action **172** in flowchart **100**). FIG. **2C** shows a portion of reconstituted wafer stack **282**, which results from action **172** being performed on reconstituted wafer stack **280**, in accordance with implementations of the present disclosure. In the present implementation, top die **206** of top reconstituted wafer **202** and bottom die **224** of bottom reconstituted wafer **204** are interconnected through insulation arrangement **242**.

**[0023]** In the present implementation, insulation arrangement **242** includes top molding compound **216**, bottom molding compound **226**, top die passivation **234**, bottom die passivation **236**, bottom RDL passivation **238**, and top RDL passivation **244**. However, in other implementations, insulation arrangement **242** can have different constituents and/or additional constituents.

**[0024]** In some implementations, interconnecting comprises forming a conductive via through the insulation arrangement. However, interconnecting can be accomplished in various manners. FIG. **2C** shows conductive via **250** formed through insulation arrangement **242**. Forming conductive via **250** through insulation arrangement **242** can include drilling a hole through at least one of top molding compound **216**, bottom molding compound **226**, top die passivation **234**, bottom die passivation **236**, bottom RDL passivation **238**, and top RDL passivation **244** (although a hole is not drilled through top RDL passivation **244** in the implementation shown). The hole can be drilled, for example, utilizing a mechanical drill, a laser, or other means.

**[0025]** In the present implementation, a hole is drilled through bottom molding compound **226**, top die passivation **234**, bottom die passivation **236**, and bottom RDL passivation **238**, as well as top RDL **228a** and bottom RDL **228b** of reconstituted wafer stack **280** in FIG. **2B**. The hole can subsequently be filled with conductive material to form conductive via **250**, thereby shorting top RDL **228a** and bottom RDL **228b**. Top RDL passivation **244** can later be formed on top RDL **228a**. Top RDL passivation **244** includes dielectric material, such as a dielectric polymer, as one example. It is noted that in various implementations, top RDL passivation **244** and/or other constituents can be formed prior to drilling

the hole and the present disclosure is not limited by the specific implementation shown.

[0026] Thus, as described above, in the present implementation, top die 206 of top reconstituted wafer 202 and bottom die 224 of bottom reconstituted wafer 204 are interconnected by connecting top RDL 228a to bottom RDL 228b. More particularly, top die 206 and bottom die 224 are interconnected by forming conductive via 250 through top RDL 228a and optionally through bottom RDL 228b.

[0027] Referring now to flowchart 100 of FIG. 1 and FIG. 2C, flowchart 100 includes forming package terminals for connection to the top die of the top reconstituted wafer and the bottom die of the bottom reconstituted wafer (action 174 in flowchart 100). For example, FIG. 2C shows reconstituted wafer stack 282, which results from action 174 being performed on reconstituted wafer stack 280, in accordance with implementations of the present disclosure. In the present implementation, package terminal 252 is formed for connection to both top die 206 of top reconstituted wafer 202 and bottom die 224 of bottom reconstituted wafer 204. Package terminal 252 is also formed for connection to both top RDL 228a and bottom RDL 228b.

[0028] In the present implementation, package terminal 252 is formed in top RDL passivation 244 on under bump metallization (UBM) 254 and top RDL 228a. It is noted that UBM 254 is optional. For example, in some implementations, package terminal 252 is formed in top RDL passivation 224 and on top RDL 228a. Also, in the present implementation, package terminal 252 is a solder ball that is part of a ball grid array (BGA). While package terminal 252 is shown as a solder ball, package terminal 252 is exemplary and other types of package terminals can be employed in addition to or instead of a solder ball. In one implementation, for example, a conductive pad is utilized as a package terminal. Also, while only one package terminal is shown, a plurality of package terminals can be formed. For example, reconstituted wafer stack 282 can include, additional package terminals for connection to only one of top die 206 or bottom die 224 or other constituents (not shown). The additional package terminals can be formed concurrently or non-concurrently with package terminal 252, in accordance with various implementations.

[0029] It is noted that while flowchart 100 shows action 174 as being after action 172, in accordance with various implementations, action 174 can occur before, during, and/or after action 172.

[0030] Referring now to flowchart 100 of FIG. 1 and FIGS. 2C and 2D, flowchart 100 includes singulating the reconstituted wafer stack to form individual stacked packages (action 176 in flowchart 100). For example, in the present implementation, reconstituted wafer stack 282 of FIG. 2C is singulated to form stacked package 284. More particularly, reconstituted wafer stack 282 is singulated along stacked package region 218 shown in FIG. 2A. Other individual stacked packages are formed while singulating reconstituted wafer stack 282, which may be substantially similar to or different than stacked package 284.

[0031] While stacked package 284 includes only top die 206 and bottom die 224, in other implementations, stacked package 284 includes more than two dies. For example, stacked package region 218 can include additional dies within top reconstituted wafer 202 and/or bottom reconstituted wafer 204. As one example, top die 208 in FIG. 2A can be within stacked package region 218. Furthermore, the addi-

tional dies can be interconnected with each other, top die 206 and/or bottom die 224 through insulation arrangement 242 utilizing any of RDLs, conductive vias (e.g. conductive via 250), and/or other means. For example, top RDL 228a can interconnect top die 206 and top die 208. Also, while only top reconstituted wafer 202 and bottom reconstituted wafer 204 are shown, stacked package 284 can include dies from other reconstituted wafers. For example, one or more additional reconstituted wafers can be in any of reconstituted wafer stacks 280 and 282. Also, additional RDLs, passivation, and other constituents can be included with the one or more additional reconstituted wafers.

[0032] Furthermore, while only conductive via 250 is shown, more than one conductive via can be utilized to connect dies from different reconstituted wafers. In one implementation, the conductive vias extend through at least top molding compound 216 of insulation arrangement 242. Furthermore, where stacked package 284 includes a die from an additional reconstituted wafer (not shown), a conductive via (or other interconnect) may interconnect the die to only one of or to both of top die 206 and bottom die 224.

[0033] In the present implementation, package terminal 252 and/or other package terminals are formed prior to singulating reconstituted wafer stack 282 to form stacked package 284. However, in other implementations, package terminal 252 and/or other package terminals can be formed after reconstituted wafer stack 282 is singulated. Furthermore, in some implementations, top die 206 and bottom die 224 and/or other dies can be interconnected after singulating reconstituted wafer stack 282.

[0034] However, by forming package terminal 252 and/or other package terminals and interconnecting top die 206 and bottom die 224 and/or other dies prior to singulating reconstituted wafer stack 282, stacked package 284 can be simply and efficiently formed utilizing wafer level and/or panel (e.g. substrate) level processes. For example, in accordance with some implementations, the method illustrated by flowchart 100 is performed utilizing only wafer level and/or panel level processes on top reconstituted wafer 202 and bottom reconstituted wafer 204. Thus, among other advantages, stacked package 284 can be much thinner than packages that could be formed utilizing package level processes.

[0035] As shown in FIG. 2D, stacked package 284 includes top die 206 from top reconstituted wafer 202 situated over bottom die 224 from bottom reconstituted wafer 204. Top die 206 and bottom die 224 are insulated from one another by insulation arrangement 242. Insulation arrangement 242 includes top molding compound 216 that flanks top die 206 and bottom molding compound 226 that flanks bottom die 224, where top molding compound 216 is situated over bottom molding compound 226.

[0036] Top die 206 and bottom die 224 are interconnected through insulation arrangement 242. More particularly, top die 206 and bottom die 224 are interconnected through top molding compound 216. In the present implementation, top die 206 and bottom die 224 are interconnected through conductive via 250, which extends within insulation arrangement 242. Top die 206 has top RDL 228a, and bottom die 224 has bottom RDL 228a that is connected to top RDL 228a through conductive via 250.

[0037] Thus, as described above, top die 206 and bottom die 224 can be interconnected through insulation arrangement 242, effectively and efficiently. For example, insulation arrangement 242 can facilitate interconnection between top

die 206 and bottom die 224 while providing sufficient mechanical support for stacked package 284. Furthermore, top RDL 228a and bottom RDL 228b can be easily interconnected by connecting top RDL 228a to bottom RDL 228b using, for example, conductive via 250 formed through insulation arrangement 242.

[0038] By utilizing RDLs, such as top RDL 228a and bottom RDL 228b, and wafer and/or panel level processes, stacked package 284 can advantageously support higher levels of functionality while accommodating additional circuitry and/or dies without complicating packaging and reducing package density. For example, additional RDLs, I/O pads, and/or dies can easily be incorporated into stacked package 284 as desired without substantially complicating packaging and increasing package density.

[0039] Also, in various implementations, a carrier wafer is utilized to fabricate bottom reconstituted wafer 204 and is utilized as part of stacked package 284. For example, the carrier wafer can be a silicon wafer or a substrate panel that is integrated into stacked package 284. For example, the carrier wafer could be integrated into stacked package 284 as a heat sink. In one implementation, the carrier wafer is a copper leadframe panel.

[0040] Referring now to FIG. 3, FIG. 3 presents a cross-sectional view of stacked package 300, according to an implementation of the present disclosure. Stacked package 300 can be fabricated utilizing the method for manufacturing a stacked package illustrated by flowchart 100. Stacked package 300 includes top die 306, top molding compound 316, bottom die 324, bottom molding compound 326, top RDL 328a, bottom RDL 328b, top I/O pad 330, bottom I/O pad 332, top die passivation 334, bottom die passivation 336, bottom RDL passivation 338, top RDL passivation 344, insulation arrangement 342, and conductive via 350, corresponding respectively to top die 206, top molding compound 216, bottom die 224, bottom molding compound 226, top RDL 228a, bottom RDL 228b, top I/O pad 230, bottom I/O pad 232, top die passivation 234, bottom die passivation 236, bottom RDL passivation 238, top RDL passivation 244, insulation arrangement 242, and conductive via 250 in stacked package 284 of FIG. 2D.

[0041] While stacked package 284 has package terminal 252 on top side 222 of top reconstituted wafer 202, at least one package terminal can be formed on bottom side 256 of bottom reconstituted wafer 204 in addition to or instead of on top side 222. For example, stacked package 300 includes package terminals 352a, 352b, 352c, 352d, 352e, 352f, and 352g on bottom die 324 and bottom side 356. Package terminals 352a, 352b, 352c, 352d, 352e, 352f, and 352g may be only for connection to bottom die 324 or may also or instead be for connection to top die 306 and/or other dies. Stacked package 300 also includes package terminals 352h and 352i on conductive interface 358 and bottom side 356. Like package terminal 252 in FIG. 2C, package terminals 352a, 352b, 352c, 352d, 352e, 352f, 352g, 352h and 352i can be solder balls that are part of a BGA or can be other types of package terminals. While not shown, in some implementations, stacked package 300 has additional solder balls on molding compound 326 for mechanical stability.

[0042] Stacked package 300 also has electrical component 360 connected to top die 306 through top RDL 328a. Electrical component 360 is an individual die in the present implementation, is on top RDL passivation 344, and is connected to top die 306 through top RDL passivation 344 by intercon-

nects 362a and 362b. Electrical component 360 can also be connected to top die 306 through other RDLs and/or other interconnects not shown in FIG. 3. Furthermore, at least one additional individual die can be connected to top die 306 in a same or different manner than individual die 306. In one implementation, electrical component 360 is connected to top die 306 prior to singulating a reconstituted wafer stack to form stacked package 300. In another implementation, electrical component 360 is connected to top die 306 after singulating a reconstituted wafer stack to form stacked package 300 (e.g., after action 176). Furthermore, in some implementations, electrical component 360 is on bottom side 356 of stacked package 300.

[0043] Thus, as described above, implementations of the present disclosure result in a stacked package having a top die from a top reconstituted wafer and a bottom die from a bottom reconstituted wafer. In various implementations, complications in packaging and reduced package density can advantageously be avoided or minimized while still providing for a stacked package that has a high level of functionality. Furthermore, it will be appreciated that implementations of the present disclosure offer significant flexibility in coping with limited component space and layout options.

[0044] From the above description it is manifest that various techniques can be used for implementing the concepts described in the present application without departing from the scope of those concepts. Moreover, while the concepts have been described with specific reference to certain implementations, a person of ordinary skill in the art would recognize that changes can be made in form and detail without departing from the spirit and the scope of those concepts. As such, the described implementations are to be considered in all respects as illustrative and not restrictive. It should also be understood that the present application is not limited to the particular implementations described herein, but many rearrangements, modifications, and substitutions are possible without departing from the scope of the present disclosure.

1. A stacked package comprising:
  - a top die from a top reconstituted wafer situated over a bottom die from a bottom reconstituted wafer;
  - said top die and said bottom die being insulated from one another by an insulation arrangement;
  - said top die and said bottom die being interconnected through said insulation arrangement.
2. The stacked package of claim 1, wherein said top die and said bottom die are interconnected through a conductive via.
3. The stacked package of claim 2, wherein said conductive via extends within said insulation arrangement.
4. The stacked package of claim 1, wherein said top die has a top redistribution layer, and said bottom die has a bottom redistribution layer that is connected to said top redistribution layer.
5. The method of claim 1, wherein said insulation arrangement comprises a top molding compound that flanks said top die and a bottom molding compound that flanks said bottom die.
6. The method of claim 5, wherein said top molding compound is situated over said bottom molding compound.
7. The method of claim 1, wherein said insulation arrangement comprises a top molding compound that flanks said top die, said top die and said bottom die being interconnected through at least said top molding compound.
8. A method for manufacturing a stacked package, said method comprising:

stacking a top reconstituted wafer having a top die over a bottom reconstituted wafer having a bottom die to form a reconstituted wafer stack;

interconnecting said top die of said top reconstituted wafer and said bottom die of said bottom reconstituted wafer through an insulation arrangement;

singulating said reconstituted wafer stack to form said stacked package.

9. The method of claim 8, wherein said interconnecting comprises forming a conductive via through said insulation arrangement.

10. The method of claim 8, wherein said insulation arrangement comprises a top molding compound that flanks said top die of said top reconstituted wafer and a bottom molding compound that flanks said bottom die of said bottom reconstituted wafer.

11. The method of claim 10, wherein said top molding compound is situated over said bottom molding compound.

12. The method of claim 8, further comprising forming a package terminal for connection to said top die of said top reconstituted wafer and said bottom die of said bottom reconstituted wafer prior to said singulating.

13. The method of claim 8, wherein said stacking comprises adhering said top reconstituted wafer to said bottom reconstituted wafer using a passivation layer.

14. A method for manufacturing a stacked package, said method comprising:

stacking a top reconstituted wafer having a top die over a bottom reconstituted wafer having a bottom die to form a reconstituted wafer stack, said top die having a top redistribution layer, and said bottom die having a bottom redistribution layer;

interconnecting said top die of said top reconstituted wafer and said bottom die of said bottom reconstituted wafer by connecting said top redistribution layer to said bottom redistribution layer;

singulating said reconstituted wafer stack to form said stacked package.

15. The method of claim 14, wherein said interconnecting comprises forming a conductive via through said top redistribution layer.

16. The method of claim 14, wherein said interconnecting comprises forming a conductive via through said bottom redistribution layer.

17. The method of claim 14, wherein said interconnecting is through an insulation arrangement.

18. The method of claim 14, further comprising forming a package terminal for connection to said top die and said bottom die prior to said singulating.

19. The method of claim 14, wherein said stacking comprises adhering said top reconstituted wafer to said bottom reconstituted wafer using a passivation layer.

20. The method of claim 19, wherein said passivation layer is a bottom redistribution layer passivation.

\* \* \* \* \*