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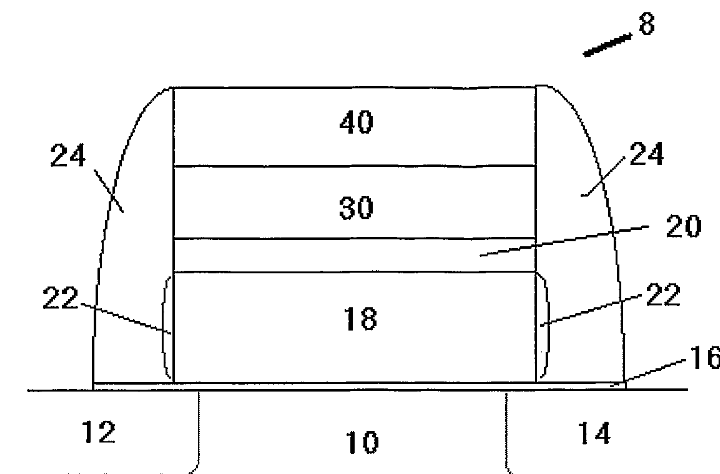
(54) Title: OXIDE-NITRIDE STACK GATE DIELECTRIC



(57) Abstract: A method of making a semiconductor structure comprises forming an oxide layer on a substrate; forming a silicon nitride layer on the oxide layer; annealing the layers in NO; and annealing the layers in ammonia. The equivalent oxide thickness of the oxide layer and the silicon nitride layer together is at most 25 Angstroms.

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— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

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OXIDE-NITRIDE STACK GATE DIELECTRIC AND FORMATION PROCESS

CROSS REFERENCE TO RELATED APPLICATION

This application claims the benefit of U.S. Provisional Application No. 60/506,713 filed 26 September 2003.

BACKGROUND

Modern integrated circuits are constructed with up to several million active devices, such as transistors and capacitors, formed in and on a semiconductor substrate. Interconnections between the active devices are created by providing a plurality of conductive interconnection layers, such as polycrystalline silicon and metal, which are etched to form conductors for carrying signals. The conductive layers and interlayer dielectrics are deposited on the silicon substrate wafer in succession, with each layer being, for example, on the order of 1 micron in thickness.

A gate structure is an element of a transistor. Figure 1 illustrates an example of a gate stack **8**. A semiconductor substrate **10** supports a gate insulating layer **16**, which overlaps doped regions (source/drain regions) in the substrate (**12** and **14**), and the gate insulating layer supports a gate **18**, which is typically polycrystalline silicon. On the gate is a metallic layer **30**. The metallic layer may be separated from the gate by one or more other layers, such as nitrides, oxides, or silicides, illustrated collectively as barrier layer **20**. The metallic layer may in turn support one or more other layers (collectively **40**), such as nitrides, oxides, or silicides. Oxide **22** may be formed on the sides of the gate to protect the gate oxide at the foot of the gate stack; and insulating spacers **24** may be formed on either side of the gate stack. Furthermore, contacts to the source/drain regions in the substrate, and to the gate structure, may be formed.

The continuous scaling of VLSI technologies has demanded a gate dielectric that is scaled down in thickness while maintaining the required leakage performance. Silicon dioxide met these requirements down to a thickness of about 25 Angstroms. Below this thickness it first becomes

marginal for leakage; then the thickness control itself and finally the problem of boron penetration from the polysilicon on the gate oxide into the substrate becomes a very critical issue as the technologies moves to P^+ poly gate for PMOSFETs for better performance. Nitrided SiO_2, in which nitrogen is incorporated (2 to 3%) by annealing the gate oxide in N_2O or NO, has been proposed. This dielectric is robust for boron penetration, due to the fact that nitrided SiO_2 is better for leakage because of the slightly higher dielectric constant. This dielectric can be scaled down to about 22 to 24 Angstroms (physical thickness), below which it fails due to leakage and boron penetration. Since NO annealing also increases the oxide thickness, there is a limit to the amount of nitrogen that can be incorporated for a required thickness. For technology that uses a CD (critical dimension, which corresponds to the width of the gate) of 70 nm and smaller, the gate dielectric thickness should be in the range 14 to 16 Angstroms EOT (equivalent oxide thickness) which cannot be met by nitrided SiO_2. A new material is needed to meet all the requirements.

Current technology uses nitrided SiO_2 which is formed by first growing SiO_2 by dry or wet oxidation and the oxide is typically annealed in NO, at about 850 °C to 900 °C for at least 15 minutes, to incorporate sufficient nitrogen. It is very difficult to scale the thickness below about 18 Angstroms, since the oxidation is too fast and annealing in NO grows significant amounts of oxide. The dielectric is also physically too thin for an EOT of 15 to 16 Angstroms. At this thickness, there is too much tunneling current through the dielectric, resulting in high leakage. The thin dielectric also gives rise to unacceptable boron penetration. Incorporating more nitrogen calls for an increased anneal which would increase the oxide thickness beyond the required limit.

BRIEF SUMMARY

In a first aspect, the present invention is a method of making a semiconductor structure, comprising forming an oxide layer on a substrate; forming a silicon nitride layer on the oxide layer; annealing the layers in NO;

and annealing the layers in ammonia. The equivalent oxide thickness of the oxide layer and the silicon nitride layer together is at most 25 Angstroms.

In a second aspect the present invention is a method of forming a gate dielectric, comprising forming an oxide layer on a substrate; forming a silicon nitride layer on the oxide layer; and annealing the layers in NO and ammonia. The oxide layer has a thickness of 6-10 Angstroms, and the silicon nitride layer has a thickness of 10-30 Angstroms.

In a third aspect, the present invention is a semiconductor structure, comprising a substrate, an oxide layer on the substrate, and a silicon nitride layer on the oxide layer. The oxide layer has a thickness of 6-10 Angstroms, and the silicon nitride layer has a thickness of 10-30 Angstroms.

In a fourth aspect, the present invention is semiconductor structure, comprising a substrate, an oxide layer on the substrate, and a silicon nitride layer on the oxide layer. The oxide layer together with the silicon nitride layer have an equivalent oxide thickness of 12-25 Angstroms.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a gate stack structure.

Figures 2-8 illustrate a method of forming the structure of Figure 9.

Figure 9 shows a gate stack of the present invention.

Figure 10 show the gate stack of Figure 9 after further processing.

Figure 11 shows the details of the gate stack dielectric.

Figure 12 is a graph showing leakage.

DETAILED DESCRIPTION

The present invention makes use of the discovery that a bilayer gate dielectric, with the lower layer being silicon oxide, and the upper being silicon nitride, can be made which has an EOT of preferably 12-25 Angstroms, including 13-15 Angstroms, 14 Angstroms, and 20-25 Angstroms.

The two-part gate dielectric is shown in Figure 11. The gate insulating layer or dielectric layer **102**, is composed of two parts: a silicon oxide layer **104**, and a silicon nitride layer **103**. The gate insulating layer **102** is on the

substrate **100**. The silicon oxide layer preferably has a thickness of 6-10 Angstroms, including 7, 8 and 9 Angstroms. The silicon nitride layer preferably has a thickness of 10-30 Angstroms, including 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 and 24 Angstroms.

5 The oxide layer may be formed in a variety of ways, after removing any native oxide from the substrate using hydrofluoric acid. One method is to use an RCA clean; another method is to rinse the substrate with deionized water containing ozone (O_3), to form an oxide layer having a thickness of about 8 Angstroms; this may be done as the rinse following the removal of the native

10 oxide. In another method, low pressure (100-200 mTorr) oxygen, optionally diluted with nitrogen or another inert gas, is used to thermally grow the oxide layer. In still another method, the oxide layer may be formed by steam oxidation.

Once the oxide is formed, the silicon nitride layer may be formed. This

15 may be done by forming nitrogen rich silicon nitride by LPCVD, using dichlorosilane and ammonia, preferably in a ratio of 1:1000 to 1:3, more preferably 1:100 to 1:33, most preferably 1:33. Alternatively, the silicon nitride layer may be formed from dichlorosilane and ammonia by Atomic Layer Deposition. Once formed, the layer may be annealed in NO at 800-900°C for

20 15-30 minutes; and annealed in ammonia by rapid thermal annealing (RTA) for 30 seconds to 1 minute, or in a furnace for 5-10 minutes. Optionally, nitrogen may be used to dilute the NO and ammonia in either annealing process.

The remainder of the semiconductor structure may be formed as

25 follows.

Referring to Figure 2, the gate insulating layer **102** is on the semiconductor substrate **100**. The semiconductor substrate may be a conventionally known semiconductor material. Examples of semiconductor materials include silicon, gallium arsenide, germanium, gallium nitride,

30 aluminum phosphide, and alloys such as $Si_{1-x}Ge_x$ and $Al_xGa_{1-x}As$, where $0 \leq x \leq 1$. Preferably, the semiconductor substrate is silicon, which may be doped or undoped.

Referring to Figure 3, a gate layer **105** may be formed on the gate insulating layer. The gate layer may contain a variety of semiconducting materials. Typically, a gate layer contains polycrystalline silicon (poly) or amorphous silicon. The gate layer may be doped with one type of dopant (P^+ or N^+), or it may contain both types of dopants in discrete regions. A split gate is a gate layer containing both P^+ and N^+ doping regions.

In the case of a split gate, those regions of the gate that are P^+ doped (such as with B or BF_2^+) are over N^- doped channel regions of the substrate, forming a PMOS device; those regions of the gate that are N^+ doped (such as with As^+ or phosphorus$^+$) are over P^- doped channel regions of the substrate, forming an NMOS device. The P^+ and N^+ doping regions of the gate are separated by a region which is on an isolation region of the substrate. The doping of the regions of the gate is preferably carried out after forming the gate, by masking and doping each region separately, or by an overall doping of the gate with one dopant type, and then masking and doping only one region with the other dopant type (counter doping).

Referring to Figure 4, a barrier layer **115** may optionally be formed on the gate layer. The optional barrier layer may contain a variety of materials, including nitrides, silicides, and oxides, and is preferably a conductive material. For example, the barrier layer may contain refractory silicides and nitrides. Preferably, the barrier layer contains tungsten nitride or silicide.

Referring still to Figure 4, a metallic layer **125** may be formed on the gate layer, or the barrier layer **115**, if it is present. Preferably, the metallic layer has a thickness of 200-600 angstroms, more preferably 300-500 angstroms, most preferably 325-450 angstroms. The metallic layer **125** may contain a variety of metal-containing materials. For example, a metallic layer may contain aluminum, copper, tantalum, titanium, tungsten, or alloys or compounds thereof. Preferably, the metallic layer comprises tungsten or titanium. The metallic layer may be formed, for example, by physical vapor deposition (PVD) of the metal, or by low pressure chemical vapor deposition (LPCVD) of a mixture of a metal halide and hydrogen.

Referring to Figure 5, an etch-stop layer **145** may be formed on the metallic layer by a variety of methods, including chemical vapor deposition (CVD). Preferably, the etch-stop layer is a nitride layer. More preferably, the etch-stop layer is silicon nitride formed by PECVD. The etch-stop layer may vary in composition, so that the top of the etch-stop layer is anti-reflective, for example so that the top of the etch-stop layer is silicon rich silicon nitride, or silicon oxynitride; this layer may also act as a hard mask to protect the etch-stop layer during subsequent etches. Alternatively, a separate anti-reflective layer (ARC) may be formed.

Preferably, the etch-stop layer is formed rapidly at a relatively low temperature. For example, if the gate layer contains both P^+ and N^+ doping regions, diffusion of the dopants may occur if the wafer is maintained at sufficiently high temperatures for a prolonged period of time. Thus, it is desirable that any high temperature processing is performed only for relatively short periods of time. Likewise, it is desirable that any lengthy processing is carried out at relatively low temperatures. Preferably, the etch-stop layer is formed at a temperature of at most 750°C, if the atmosphere is substantially devoid of oxygen, or in a reducing environment (hydrogen rich). Under typical conditions, a temperature of at most 600°C is preferred, at most 450°C is more preferred. A temperature of at least 350°C is preferred, such as 400°C. The depositing of the etch-stop layer is preferably carried out at a temperature and for a time that does not result in substantial diffusion between the P^+ region and the N^+ region in a split gate.

Referring to Figures 6-9, each layer may be patterned to form the gate stack. The patterning may be accomplished, for example, by conventional photolithographic and etching techniques. Referring to Figures 6 and 7, the etch-stop layer may be etched to form a patterned etch-stop layer **150**, for example by forming a patterned photoresist **210** on etch-stop layer **145** (Figure 6) and then etching the exposed portions of the layer. A hydrofluoric acid dip may be used to remove sidewall passivation.

The etch-stop etching may be carried out by exposure to a plasma formed from a mixture of gasses. Preferably, the gasses and plasma

comprise carbon, fluorine and hydrogen. Preferably, the atomic ratio of fluorine:hydrogen is 43:1 to 13:3, more preferably 35:1 to 5:1, most preferably 27:1 to 7:1. Preferably, the mixture of gasses includes CF_4 and CHF_3; preferably the ratio by volume of CF_4 : CHF_3 is 10:1 to 1:3, more preferably 8:1 to 1:2, most preferably 6:1 to 1:1. The gas mixture and plasma may also include other gasses, such as He, Ne or Ar. The pressure during etching is greater than 4 mTorr, preferably at least 10 mTorr, such as 10-80 mTorr, more preferably at least 15 mTorr, such as 15-45 mTorr, most preferably 25-35 mTorr.

The patterned etch-stop layer may be used as a hard mask for the etching of the metallic layer **125** (Figure 7) to form a patterned metallic layer **130** (Figure 8). The patterned etch-stop layer and the patterned metallic layer may be used as a hard mask for the etching of the gate layer **105** (Figure 8) to form patterned gate layer **110** (Figure 9). The gate etching may be carried out by conventional gate etch techniques, for example by exposure to a plasma formed from chlorine, hydrobromic acid and/or oxygen.

The patterned photoresist **210** (Figure 6) may be removed at any stage of the gate stack formation following the etch-stop etch. For example, the patterned photoresist may be removed immediately after the etch-stop etch (as illustrated in Figures 6 and 7), or it may be removed after the etching of the metallic layer or after the gate etching. The removal of the photoresist may be followed by a cleaning procedure to ensure removal of any residual byproduct of the photoresist or of the photoresist removal. For example, the photoresist may be removed by ashing the patterned photoresist to provide a gate stack containing a patterned etch-stop layer (Figure 7). This gate stack without a photoresist layer may then be treated with a cleaning solution to complete the removal and cleaning process. The most preferred cleaning agent contains water, 2-(2 aminoethoxy) ethanol, hydroxylamine, and catechol. An example of a cleaning solution is EKC265tm (EKC, Hayward, CA).

Figure 9 thus illustrates a gate stack **200** which may be formed on a semiconductor wafer. Semiconductor substrate **100** supports a gate

insulating layer **102**, which in turn supports a gate layer **110**. The gate layer supports a metallic layer **130**, which may optionally be separated from the gate layer by barrier layer **120**. The etch-stop layer **150** is on the metallic layer **130**.

5 Further processing of the gate structure may include forming sidewall oxide regions **170** on gate layer **110** and forming spacers **160** (preferably containing nitride) on the sides of the stack. Furthermore, a dielectric layer **180** maybe formed on the etch-stop layer, and contacts or via **190** formed through the dielectric to the substrate, as illustrated in Figure 10. This via 10 may be lined and filled to form a via-contact, for example with TiN and tungsten, respectively. Other processing may include forming contacts to the gate itself.

Other processing may be used to complete formation of semiconductor devices from the semiconductor structure. For example, source/drain regions 15 **12**, **14** may be formed in the substrate, additional dielectric layers may be formed on the substrate, and contacts and metallization layers may be formed on these structures. These additional elements may be formed before, during, or after formation of the gate stack.

The related processing steps, including the etching of the gate stack 20 layers and other steps such as polishing, cleaning, and deposition steps, for use in the present invention are well known to those of ordinary skill in the art, and are also described in Encyclopedia of Chemical Technology, Kirk-Othmer, Volume 14, pp. 677-709 (1995); Semiconductor Device Fundamentals, Robert F. Pierret, Addison-Wesley, 1996; Wolf, Silicon 25 Processing for the VLSI Era, Lattice Press, 1986, 1990, 1995 (vols 1-3, respectively), and Microchip Fabrication 4rd. edition, Peter Van Zant, McGraw-Hill, 2000.

The semiconductor structures of the present invention may be incorporated into a semiconductor device such as an integrated circuit, for 30 example a memory cell such as an SRAM, a DRAM, an EPROM, an EEPROM etc.; a programmable logic device; a data communications device; a clock generation device; etc. Furthermore, any of these semiconductor

devices may be incorporated in an electronic device, for example a computer, an airplane or an automobile.

Using the two-part gate dielectric of the invention shows a Vt (threshold voltage) for a PMOS FET slightly higher than that of SiON (-0.54 vs. -0.46), indicating no boron penetration. Figure 12 is a graph showing leakage on the vertical axis (A/cm^2), and EOT (in Angstroms) on the horizontal axis. In this graph, "THERMAL-NO" represent a device having a thermally grown oxide, followed by annealing in NO; "VTR-NO" is oxide grown thermally in a vertical furnace, followed by annealing in NO; and O/N stack is the two-part gate dielectric of the present invention.

CLAIMS

1. A method of making a semiconductor structure, comprising:
forming an oxide layer on a substrate;
forming a silicon nitride layer on the oxide layer;
5 annealing the layers in NO; and
annealing the layers in ammonia;
wherein the equivalent oxide thickness of the oxide layer and the silicon nitride layer together is at most 25 Angstroms.

2. The method of claim 1, wherein the oxide layer has a thickness
10 of 6-10 Angstroms.

3. The method of claim 1, wherein silicon nitride layer has a thickness of 10-30 Angstroms.

4. The method of claim 1, wherein the forming of the oxide layer comprises rinsing the substrate with deionized water containing ozone.

15 5. The method of claim 1, wherein the forming of the oxide layer comprises steam oxidation

6. The method of claim 1, wherein the forming of the oxide layer comprises thermally growing the oxide layer with oxygen.

7. The method of claim 1, wherein the forming of the silicon nitride
20 layer comprises depositing the silicon nitride by LPCVD.

8. The method of claim 1, wherein the annealing in NO is carried out at a temperature of 800-900°C for 15-30 minutes.

9. The method of claim 1, wherein the annealing in ammonia is carried out by rapid thermal annealing at a temperature of 900°C for 0.5-1
25 minute.

10. The method of claim 1, wherein the annealing in ammonia is carried out in a furnace at a temperature of 900°C for 5-10 minutes.

11. The method of claim 1, wherein the semiconductor structure is a gate dielectric.

5 12. A method of making an electronic device, comprising:
forming a semiconductor device by the method of claim 1, and
forming an electronic device comprising the semiconductor device.

13. A method of making an electronic device, comprising:
10 forming a semiconductor device by the method of claim 12, and
forming an electronic device comprising the semiconductor device.

14. A method of forming a gate dielectric, comprising:
forming an oxide layer on a substrate;
15 forming a silicon nitride layer on the oxide layer; and
annealing the layers in NO and ammonia;
wherein the oxide layer has a thickness of 6-10 Angstroms, and the silicon nitride layer has a thickness of 10-30 Angstroms.

15. A semiconductor structure, comprising:
20 a substrate,
an oxide layer, on the substrate, and
a silicon nitride layer, on the oxide layer,
wherein the oxide layer has a thickness of 6-10 Angstroms, and the silicon nitride layer has a thickness of 10-30 Angstroms.

25 16. The semiconductor structure claim 15, wherein the oxide layer together with the silicon nitride layer have an equivalent oxide thickness of 12-25 Angstroms.

17. The semiconductor structure claim 15, further comprising a polysilicon layer on the silicon nitride layer.

18. The semiconductor structure claim 17, further comprising:
a metallic layer on the polysilicon layer, and
5 an etch-stop layer on the metallic layer.

19. A semiconductor structure, comprising:
a substrate,
an oxide layer, on the substrate, and
a silicon nitride layer, on the oxide layer,
10 wherein the oxide layer together with the silicon nitride layer have an equivalent oxide thickness of 12-25 Angstroms.

20. The semiconductor structure of claim 19, wherein the oxide layer has a thickness of 6-10 Angstroms.

21. The semiconductor structure of claim 19, wherein the silicon
15 nitride layer has a thickness of 10-30 Angstroms.

22. The semiconductor structure claim 19, further comprising a polysilicon layer on the silicon nitride layer.

23. The semiconductor structure claim 22, further comprising:
a metallic layer on the polysilicon layer, and
20 an etch-stop layer on the metallic layer.

24. A semiconductor structure of claim 22, wherein the polysilicon layer is a gate having a width of 45-110 nm.

25. A semiconductor structure of claim 22, wherein the polysilicon layer is a gate having a width of at most 70 nm.

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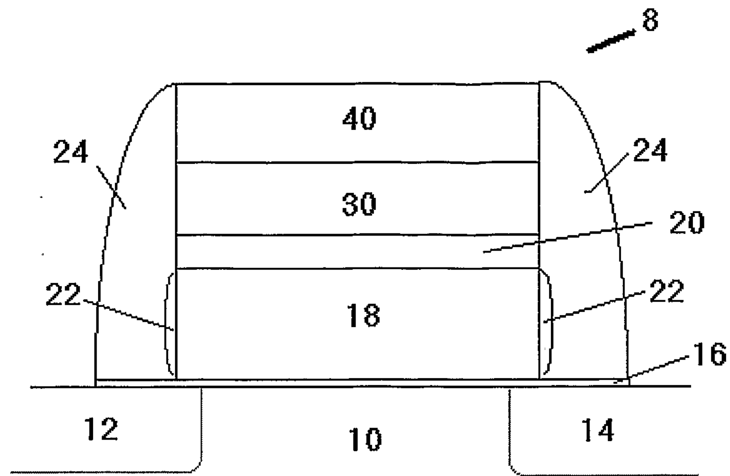

Figure 1

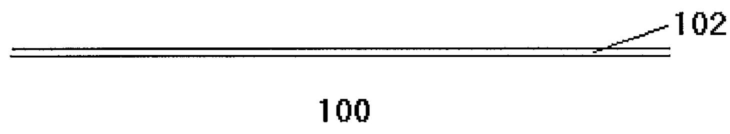

Figure 2

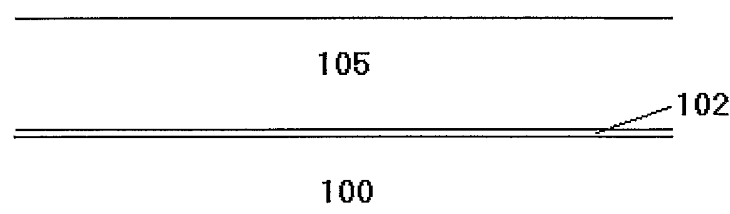

Figure 3

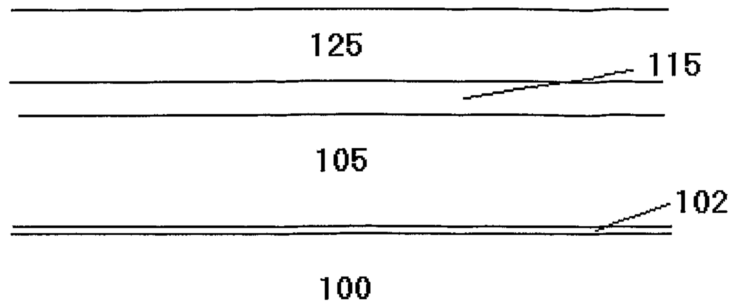

Figure 4

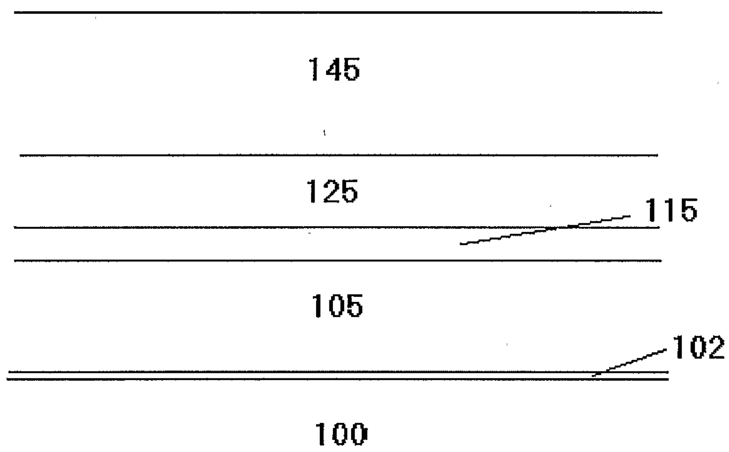

Figure 5

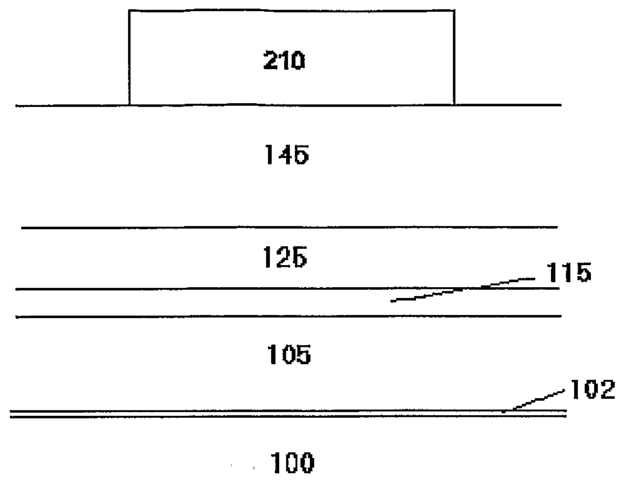

Figure 6

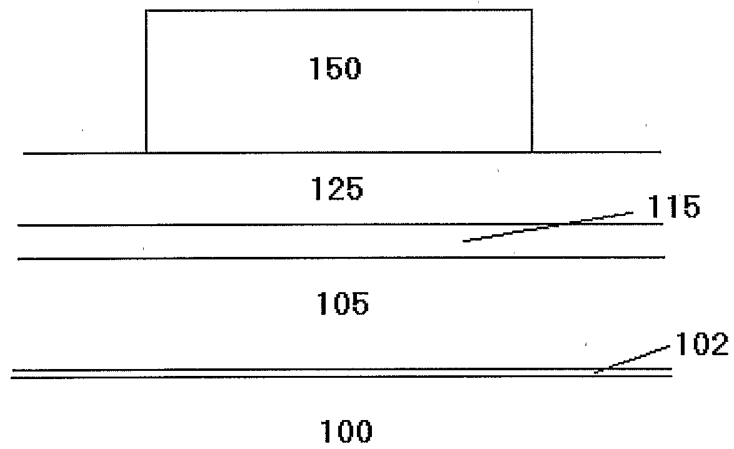

Figure 7

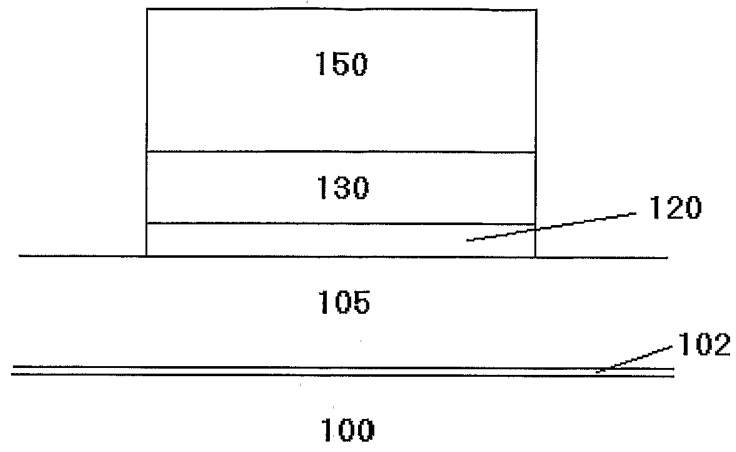

Figure 8

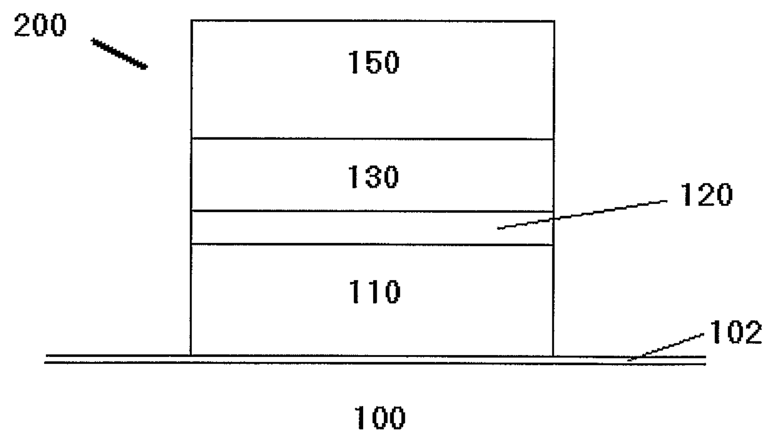

Figure 9

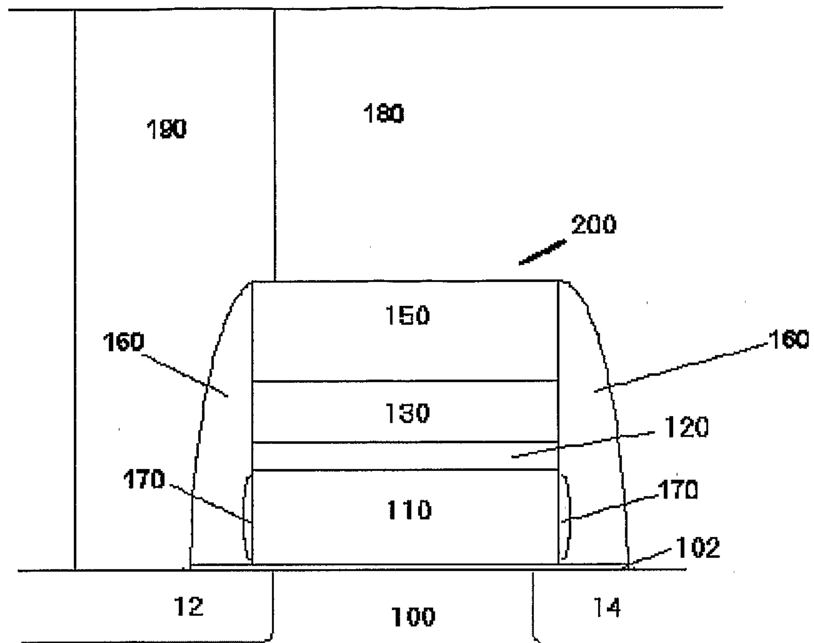

Figure 10

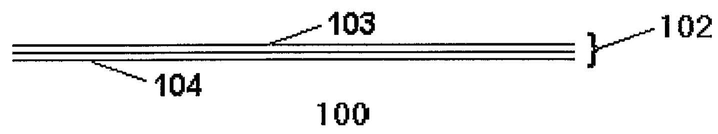

Figure 11

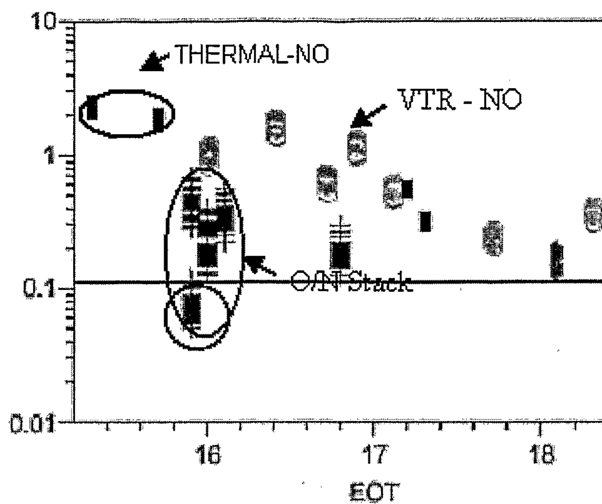

Figure 12

INTERNATIONAL SEARCH REPORT

US2004/031541

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/28 H01L21/314 H01L21/316 H01L21/318 H01L21/324
H01L29/51 H01L21/336

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L C23C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 207 542 B1 (IBOK EFFIONG) 27 March 2001 (2001-03-27) column 1, line 30 - column 2, line 32 column 2, line 60 - column 3, line 36; figures 1-4 column 3, line 46 - line 43	1-3,5, 7-25
Y		4,6

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Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
27 January 2005	07/02/2005

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INTERNATIONAL SEARCH REPORT

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WU Y ET AL: "AGGRESSIVELY SCALED P-CHANNEL MOSFETS WITH STACKED NITRIDE-OXIDE- NITRIDE, N/O/N, GATE DIELECTRICS" ULTRATHIN SIO2 AND HIGH-K MATERIALS FOR ULSI GATE DIELECTRICS. SAN FRANCISCO, CA, APRIL 5 - 8, 1999, MATERIALS RESEARCH SOCIETY SYMPOSIUM PROCEEDINGS. VOL. 567, WARRENDALE, PA : MRS, US, vol. 567, 5 April 1999 (1999-04-05), pages 101-106, XP000897813 ISBN: 0-55899-474-2 page 101 - page 102; figure 1 page 105, last paragraph	15-17, 19-22
Y		6,18, 23-25
A		1-3,7, 11-14

X	KIM B Y ET AL: "Ultra thin (<3 nm) high quality nitride/oxide stack gate dielectrics fabricated by in-situ rapid thermal processing" ELECTRON DEVICES MEETING, 1997. TECHNICAL DIGEST., INTERNATIONAL WASHINGTON, DC, USA 7-10 DEC. 1997, NEW YORK, NY, USA,IEEE, US, 7 December 1997 (1997-12-07), pages 463-466, XP010265547 ISBN: 0-7803-4100-7 the whole document	15-17, 19-22
Y		18,23-25
A		1-3,7-14

Y	US 2002/142500 A1 (FOGLIETTI PIETRO ET AL) 3 October 2002 (2002-10-03) paragraph ‘0037! - paragraph ‘0044!; figure 6 paragraph ‘0011! - paragraph ‘0013! paragraph ‘0037! - paragraph ‘0038!; figure 6 paragraph ‘0041!	4
A		1,2,12, 13

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Information on patent family members

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Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 6207542	B1	27-03-2001	NONE	
US 2002142500	A1	03-10-2002	NONE	