(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
19 February 2009 (19.02.2009)

PCT

(10) International Publication Number
WO 2009/023283 A2

(51) International Patent Classification:
H01L 23/48 (2006.01)

(21) International Application Number:
PCT/US2008/009840

(22) International Filing Date: 15 August 2008 (15.08.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/964,823 15 August 2007 (15.08.2007) US
61/004,308 26 November 2007 (26.11.2007) US

(71) Applicant *(for all designated States except US)*: **TESSERA, INC.** [US/US]; 3099 Orchard Drive, San Jose, CA 95134 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **KWON, Jinsu** [KR/US]; c/o Tessera, Inc., 3099 Orchard Drive, San Jose, CA 95134 (US). **ENDO, Kimitaka** [JP/JP]; C/o Tessera, Inc., 3099 Orchard Drive, San Jose, CA 95134 (US). **MORAN, Sean** [US/US]; C/o Tessera, Inc., 3099 Orchard Drive, San Jose, CA 95134 (US).

(74) Agents: **NEFF, Daryl, K.** et al.; Lerner, David, Littenberg, Krumholz & Mentlik, LLP, 600 South Avenue West, Westfield, NJ 07090 (US).

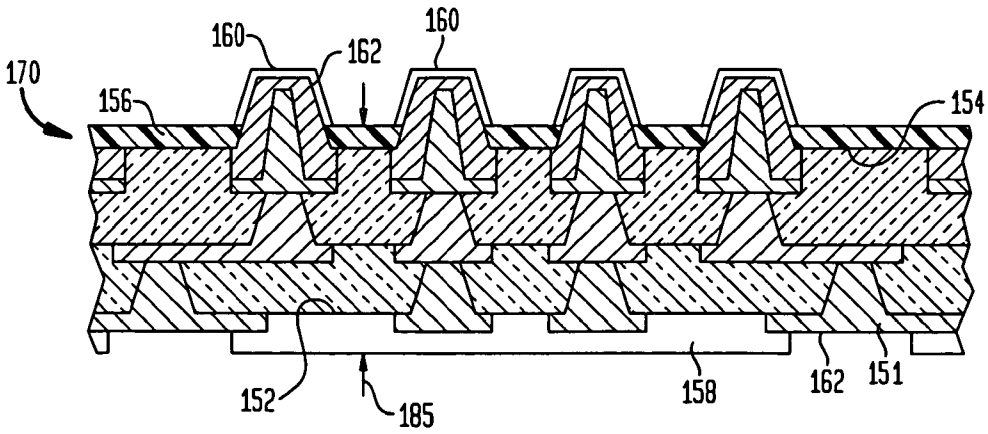
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

(54) **Title:** INTERCONNECTION ELEMENT WITH POSTS FORMED BY PLATING

FIG. 12A



(57) **Abstract:** An interconnection element (170, 190) is provided for conductive interconnection with another element (172) having at least one of microelectronic devices or wiring thereon. The interconnection element includes a dielectric element (187) having a major surface. A plated metal layer (130, 192) including a plurality of exposed metal posts (130) can project outwardly beyond the major surface (176) of the dielectric element. Some of the metal posts can be electrically insulated from each other by the dielectric element (187). The interconnection element typically includes a plurality of terminals (151) in conductive communication with the metal posts. The terminals can be connected through the dielectric element (187) to the metal posts (130). The posts may be defined by plating a metal (122, 124) onto exposed co-planar surfaces of a mandrel (120) and interior surfaces of openings (102) in a mandrel, after which the mandrel can be removed.

WO 2009/023283 A2

INTERCONNECTION ELEMENT WITH POSTS FORMED BY PLATING

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of the filing dates of United States Provisional Applications 60/964,823 (filed August 15, 2007) and 61/004,308 (filed November 26, 2007), the disclosures of which are hereby incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] The subject matter of the present application relates to microelectronic interconnection elements and assemblies and fabrication methods therefor, and more particularly to microelectronic interconnection elements and assemblies having protruding metal posts, especially metal posts defined by plating.

[0003] A current need exists to provide interconnection elements, e.g., chip carriers, package substrates, substrates of multiple chip modules, and other similar elements, for flip-chip interconnection with microelectronic elements having fine-pitch contacts. With traditional technologies such as solder-to-solder interconnections, e.g., arrays of high melting temperature solder bumps, or screen-printing technology, it is becoming increasingly difficult to form conductive bumps of sufficient volume, especially when the pitch of the conductive bumps is smaller than 150 microns.

SUMMARY OF THE INVENTION

[0004] In accordance with an aspect of the invention, an interconnection element, e.g., a package substrate, circuit panel, or other such element, is provided for conductive interconnection with another element having at least one of

microelectronic devices or wiring thereon. The interconnection element can include a sheet-like dielectric element having a major surface. A plated metal layer can be provided thereon which includes a plurality of exposed metal posts projecting outwardly beyond the major surface of the dielectric element. Some or all of the metal posts can be electrically insulated from each other by the dielectric element. The posts can be defined by plating a metal onto exposed co-planar surfaces of a mandrel and interior surfaces of openings in a mandrel and subsequently removing the mandrel. The interconnection element may further include a plurality of terminals in conductive communication with the metal posts. The terminals may be connected through the dielectric element to the metal posts.

[0005] In accordance with one embodiment, the interconnection element may include a plurality of metal wiring traces which extend in at least one direction along the major surface of the dielectric element. One or more of the metal wiring traces can be electrically insulated from the metal posts and one or more of the wiring traces can be conductively connected to the posts. Alternatively, one, some or all of the metal wiring traces can be electrically insulated from the posts. Portions of the dielectric element can be disposed between the at least one metal wiring trace and the adjacent metal posts, for example, in one or more directions along the major surface of the dielectric element for electrically insulating such metal wiring trace from the posts. In another alternative, one, some or all of the metal wiring traces can be conductively connected to the posts. For example, a metal wiring trace can be connected to one of the metal posts adjacent to the trace in a direction along the major surface of the dielectric element.

[0006] In one embodiment, one or more metal wiring traces can be disposed between adjacent ones of the metal posts and insulated from the adjacent metal posts.

[0007] In one embodiment, a portion of the metal layer can extend in a direction along the major surface of the dielectric element and be joined to at least one of the metal posts.

[0008] In one embodiment, the metal layer can be a first metal layer, and the interconnection element includes at least one second metal layer which connects the terminals with the metal posts through the dielectric element. In one embodiment, the second metal layer can be conductively joined to bases of the metal posts.

[0009] In one embodiment, the metal posts can have a height of at least 35 microns from the major surface and a pitch smaller than about 150 microns. Each metal post can be formed with a specific shape, such as, for example, frusto-conical or essentially cylindrical.

[0010] In one embodiment, the interconnection element can be conductively connected to one or more other elements to form an assembly. For example, in one embodiment, a microelectronic assembly can include a packaged microelectronic element in which the metal posts of the interconnection element are conductively interconnected to contacts, e.g., bond pads, of one or more microelectronic elements such as a bare semiconductor chip having an integrated circuit thereon or a packaged semiconductor chip including a semiconductor chip and a package having terminals other than the bond pads of the chip. A semiconductor chip can be mounted to the interconnection element in a "face-down" or "flip-chip" orientation with the front face of the chip facing the interconnection element. Alternatively, the semiconductor chip can be mounted in a "face-up" orientation with the front face of the chip facing

away from the interconnection element. In one example, a microelectronic element is mounted in a face-down orientation with the interconnection element. The microelectronic element may include a plurality of exposed contacts having a pitch, wherein the metal posts have a pitch matching the pitch of the contacts and the metal posts are conductively joined to the contacts.

[0011] In a particular embodiment, the metal layer of the interconnection element includes an inner metal layer adjacent to the dielectric element and an outer metal layer overlying the inner metal layer. The inner metal layer can be formed, for example, by plating a metal onto the outer metal layer. In one example, the outer metal layer may include nickel and the inner metal layer includes copper.

[0012] In one embodiment, a microelectronic assembly or package may include an interconnection element and a microelectronic element having a plurality of exposed contacts arranged at a pitch. In such assembly, the metal posts of the interconnection element can have a pitch matching the pitch of the contacts, with the metal posts being joined to the contacts.

[0013] In accordance with an aspect of the invention, a method is provided for fabricating an interconnection element, wherein the interconnection element can have raised conductive posts for conductive interconnection with another element having at least one of microelectronic devices or wiring thereon. In such method, conductive posts can be formed within a plurality of holes of a first element. In one example, each conductive post can include a metal liner lining walls of the holes. Terminals of the interconnection element can be formed which are in conductive communication with the conductive posts. The terminals may be connected to the conductive posts through structure extending through a dielectric layer. The conductive posts can then be caused

to project outwardly beyond a major surface of the interconnection element, such as by partially or fully removing the first element. The first element or portion thereof can be removed after forming the terminals, for example. In one example, the first is removed by etching the first element selectively relative to a metal liner of each conductive post which lines walls of the holes in the first element.

[0014] In one embodiment, the first element may include a first metal and the metal liner can include a second metal. The second metal may be such that it resists attack by an etchant used to selectively etch the first element.

[0015] In one embodiment, the step of forming metal posts can include forming a second metal layer in contact with the metal liner within the holes. In a particular embodiment, the metal liner within the holes can be formed by processing including plating. The second metal layer can be formed by steps including plating. In one embodiment, the second metal layer may fill the holes.

[0016] The second metal layer may include the first metal. The first metal can be copper, for example, and the metal liner may include nickel, for example.

[0017] In one embodiment, the first element can include a metal sheet which consists essentially of copper and the holes can have a pitch less than about 150 microns. The first element can be formed by laser drilling through holes in a metal sheet and joining a carrier to a face of the metal sheet to cover the through holes. The first element can be formed, for example, by mechanically forming through holes in a metal sheet and joining a carrier to a face of the metal sheet to cover the through holes.

[0018] In a particular embodiment, the metal or conductive posts can frusto-conical shape. In one

embodiment, the metal or conductive posts can have cylindrical shape.

[0019] In accordance with an aspect of the invention, a method is provided for fabricating an interconnection element. In accordance with such method, conductive posts can be formed within a plurality of blind holes of a first element which includes a first metal. Each conductive post can have a liner including a second metal lining the holes and a layer including a third metal contacting the liner within the holes, the second metal being resistant to attack by an etchant which attacks the first metal. A plurality of terminals can be formed such that the terminals are exposed at a bottom surface of a dielectric layer and are in conductive communication with the conductive posts. At least a portion of the first element can be removed using the etchant to cause at least portions of the conductive posts to protrude beyond the surface of the dielectric layer. In one embodiment, this can be done after the posts and terminals are formed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] FIG. 1 is a fragmentary sectional view (through line 1-1 of FIG. 2) illustrating a preliminary stage in a method of fabricating an interconnection element in accordance with one embodiment.

[0021] FIG. 2 is a fragmentary plan view corresponding to the sectional view illustrated in FIG. 1 in a method of fabricating an interconnection element in accordance with one embodiment.

[0022] FIGS. 3 through 12A are fragmentary sectional views illustrating a series of stages subsequent to the stage illustrated in FIG. 1 in a method of fabricating an interconnection element in accordance with one embodiment.

[0023] FIG. 12B is a fragmentary plan view corresponding to FIG. 12A of an interconnection element in accordance with one embodiment.

[0024] FIG. 13A is a fragmentary sectional view of an interconnection element in accordance with one embodiment, as externally interconnected with other elements.

[0025] FIG. 13B is a fragmentary sectional view of an interconnection element in accordance with a variation of the embodiment illustrated in FIG. 12 and 13A.

[0026] FIGS. 14 through 17 are fragmentary sectional views illustrating a series of stages in a method of fabricating an interconnection element in accordance with a variation of the embodiment illustrated in FIGS. 1 through 12.

[0027] FIGS. 18 through 25 are fragmentary sectional views illustrating a series of stages in a method of fabricating an interconnection element in accordance with one embodiment.

DETAILED DESCRIPTION

[0028] In accordance with an embodiment, a method is described herein for fabricating an interconnection element having raised conductive posts formed by plating, the posts usable to conductively connect the interconnection element to another element such as a microelectronic element or a wiring element, such as a circuit panel. As discussed herein, through use of an interconnection element having protruding conductive posts, interconnection can be provided to microelectronic elements or other elements having arrays of exposed contacts. In a particular example, the conductive posts of an interconnection element described herein can connect to contacts of a microelectronic element which are arranged at a fine pitch, for example, at a pitch less than 150 microns as measured center-to-center.

[0029] As illustrated in FIG. 1, an element 100 (shown in fragmentary sectional view) is patterned to form a plurality of through holes 102 extending between a top surface 104 of the element and a bottom surface 106 remote from the top surface. The element 100 has a thickness 108 between the top and bottom surfaces which can range from a few tens of microns to a few hundred microns. The thickness 108 typically is uniform over the area 103 defined by the top surface of the element 100, as shown in FIG. 2 (plan view). The element can be conductive, or can incorporate a nonconductive or semi-conductive element. In one example, the element is a sheet or foil which consists essentially of metal. For example, the element can be a foil consisting essentially of copper.

[0030] The through holes 102 (FIGS. 1-2) can be formed by optical ablation or mechanically, among other possible methods. For example, the through holes can be formed by drilling using a laser such as an ultraviolet wavelength (UV) YAG laser, i.e., one made from yttrium aluminum garnet (YAG) which typically is doped with neodymium or other dopant. Holes produced by such UV YAG laser have walls 109 which are nearly vertical, i.e., at relatively small angles to the vertical direction, where "vertical" is defined by a normal angle to the top surface 104. Thus, the walls 109 slant inward such that the width 110 of the through holes becomes smaller in the direction from the top surface towards the bottom surface.

[0031] Through holes in an element having a thickness 108 of 70 microns can be drilled to widths 110, such as 50 microns, and can be arranged at a pitch 112, such as 60 microns. Of course, through holes having greater widths and pitch or smaller widths and pitch can be attained within such element.

[0032] After forming the through holes, the bottom surface 106 of the element 100 then is joined to a major surface 114 of a carrier 116 to form a structure 120 as shown in FIG. 3. Carrier 116 may consist essentially of a metal sheet or other element having a conductive major surface 114 aligned with the bottom ends 118 of the through holes, for example. When the element 100 and carrier 116 both consist essentially of copper, they can be joined together by pressing the surfaces 106, 112 (FIG. 1) together at a joining temperature of approximately 350 degrees Celsius. Typically, the top surface 114 of the carrier 116 is a planar surface when joined to a planar bottom surface 106 of the element 100 such that bottom ends 118 of the through holes 102 become closed off by the carrier 116, as illustrated in FIG. 3. The structure formed by combining element 100 with the carrier 116 is a conductive mandrel 118 on which a set of conductive posts will be formed by plating in subsequent processing.

[0033] As illustrated in FIG. 4, a first metal layer 122 can be electroplated onto the conductive mandrel 118 so as to form a metal liner 122. Alternatively, the metal liner 122 can be formed by using a metal laminate (patterned or unpatterned), electroless plating, chemical vapor deposition (CVD) or physical vapor deposition (PVD) (sputtering), among others. The first metal layer can consist essentially of a metal which is not attacked by an etchant that attacks the underlying metal of the conductive mandrel 118. For example, when the conductive mandrel 118 consists essentially of copper, the first metal can include or consist essentially of a metal such as nickel. Such nickel layer is plated or deposited to a sub-micron thickness or to a thickness of a few microns, for example, 3 microns. Etchants are known which can be used to etch copper features while selectively preserving nickel features with which they come in contact.

The importance of the type of metal used in the first metal layer will become apparent from the description of subsequent processing below.

[0034] As illustrated in FIG. 5, a second metal layer 124 is placed onto the first metal layer 122. The second metal layer overlies the metal liner 122 and fills the remaining space within the holes 102. The placement of the second metal layer can be done using techniques like those described above. In one example, an electroplating process is used. An electroplating process typically results in the second metal layer also overlying the top surface 104 of the mandrel. In a particular embodiment, the second metal layer includes or consists essentially of copper.

[0035] FIG. 6 illustrates a stage of processing after patterning the first and second metal layers into individual separate conductive posts 130. The first and second metal layers can be patterned, for example, by photolithographically patterning a resist layer overlying the metal layers and etching each metal layer, in turn, using an etchant appropriate therefor.

[0036] Subsequently, as illustrated in FIG. 7, a dielectric layer 132 is formed such that it overlies the exposed bases 133 of the conductive posts 130. The dielectric layer can be formed by any suitable method such as by pressing or laminating a partially cured layer thereto, with or without the application of heat, or can be formed using a flowable dielectric material which optionally may be hardened or densified through subsequent treatment such as heating.

[0037] Thereafter, as illustrated in FIG. 8, the dielectric layer 132 is patterned to form openings 134 extending downward from a top surface 140 of the dielectric layer 130 to expose at least portions of the conductive posts. The openings 134 are formed in alignment, e.g., in

axial alignment, with the conductive posts 130. In one example, the dielectric layer 132 can be patterned by photolithographically patterning openings in a resist layer (not shown) atop the dielectric layer, followed by etching the dielectric layer through the openings in the resist layer. Alternatively, the openings can be formed by laser drilling with a CO2 laser or excimer laser, for example.

[0038] Thereafter, as illustrated in FIG. 9, a third metal layer is placed onto the structure to form conductive vias 136 filling the holes, as well as a metal layer 142 extending along the top surface 140. In one example, the third metal is electroplated onto the structure. The third metal layer can consist essentially of copper. A seed layer may be first formed on the dielectric layer prior to plating the third metal layer thereon. FIG. 9 illustrates the third metal layer after subsequent patterning to form individual traces 138 extending along the top surface.

[0039] Subsequently, as illustrated in FIG. 10, a second dielectric layer 144 is formed and holes are patterned therein. A fourth metal layer then is electroplated thereon to fill the holes in the second dielectric layer, forming second conductive vias 146 and traces 150 of a second metal layer 148 atop the dielectric layer 144. The second dielectric layer 144 can be formed and patterned in similar manner to the first dielectric layer 132 and the fourth metal layer can be formed and patterned in similar manner to the third metal layer. In one example, the fourth metal layer consists essentially of copper. Through such processing, the structure now includes two wiring layers 142, 146 at different levels which are conductively interconnected by conductive vias 146. Each of the wiring layers 142, 146 may include metal lines or metal traces 138, 148 which are oriented in the same direction or in different directions from each other. In this way, metal lines 138

can be used to conductively connect the vias 136 and metal lines 150 can be used to connect vias 146. Wiring layer 148 may also include conductive pads 151 overlying some of the vias 146.

[0040] Thereafter, as illustrated in FIG. 11, the conductive mandrel is removed from the structure. For example, the conductive mandrel 118 can be a sacrificial structure which is removed by selectively etching the material of the mandrel so as to preserve the material of the metal liner 122 within the holes. In a particular example, the mandrel can be a sacrificial element made from a material such as copper, which can be etched selectively in relation to a material of the metal liner 122, e.g., nickel.

[0041] To remove the mandrel in this way, exposed surfaces of the second metal layer 148 can be covered temporarily by a protective layer and an etchant applied to selectively attack the material of the mandrel 118 until the metal liner 122 becomes exposed as an outer layer of conductive posts 130. During such etching process, a major surface (bottom surface 152) of the dielectric layer 132 also becomes exposed. As a result, the conductive posts now project outwardly beyond the exposed bottom surface 152 of the dielectric layer 132. The resulting conductive posts may have different possible shapes. For example, the posts may have frusto-conical shape, of which tips 160 can be flat or essentially flat. Alternatively, the posts may be cylindrical in shape. Other shapes are also possible, which may include posts which are elongated in a horizontal direction, i.e., in a direction parallel to the major surface 152 of the dielectric element, such that the posts may appear as rails protruding from the dielectric element 132.

[0042] The conductive posts extend a height 164 from an exposed major surface 152 of the dielectric layer. In one embodiment, the height can range from a few tens of microns to a few hundred microns, depending on the depth of the holes 102 within the mandrel 118 (FIG. 3) used to form the conductive posts. The pitch 166, defined as the distance between centers of adjacent conductive posts, can range upwards from several tens of microns. The conductive posts at the bases thereof have width 168 which can range upwards from a few tens of microns. At tips 160, the conductive posts can have width 161 which may be the same, nearly the same, or somewhat smaller than the width 168 at the base of the conductive posts. In a particular example, the height 164 of each post is approximately 70 microns, the width 168 at the base is approximately 60 microns, and the width 161 at the tip of approximately 50 microns is nearly the same as the base width 168. In such example, the pitch 166 can range upwards from 80 microns, for example, a pitch of 100 microns.

[0043] Through fabrication of the conductive posts using mandrel 118 having holes of regular height 108 (Fig. 3), the tips of the conductive posts can be made co-planar to facilitate joining of the conductive posts with co-planar features of another conductive element. Moreover, through use of a mandrel 118 conductive posts 130 can be produced which have broad tips having the same width or nearly the same width as the bases of the posts. These features can be beneficial when joining the conductive posts to lands, conductive pads or conductive bumps of another microelectronic element, e.g., a semiconductor chip having devices thereon, or a wiring element, e.g., a circuit panel.

[0044] In subsequent processing, as illustrated in FIG. 12A, solder masks 156, 156 may be formed overlying each of the bottom and major surfaces 152, 152 of the dielectric

layer. The view shown in FIG. 12 is inverted in relation to that shown in FIG. 11. Optionally, a finish metal layer 162 such as gold or other metal may be applied to exposed tips 160 of the posts and terminals 151 exposed within openings in solder mask 158.

[0045] The interconnection element 170 (FIG. 12A) can be relatively thin, having a sheet-like dielectric element 187 formed by the combination of dielectric layers 132 and 144 with a thickness 185 from as little as a few tens of microns. The dielectric element typically has lateral dimensions in directions along its major surface 176 (in a direction of the pitch 166 of posts and a second direction transverse thereto) which range upwards from a few millimeters to one hundred millimeters or more. The dielectric element can be flexible, rigid or semi-rigid, depending upon its thickness and the elastic modulus of the dielectric material or materials from which it is fabricated.

[0046] As shown in plan view in FIG. 12B, the posts 130 project above major surface 176 and are typically are laid out in a grid pattern corresponding with a land grid array ("LGA") or ball grid array ("BGA") exposed at the surface of a microelectronic element. Alternatively, the posts 130 can be laid out in a plurality of rows or in a perimeter or radial layout arrangement.

[0047] FIG. 13A illustrates the interconnection element 170 as joined in flip-chip manner with contacts 174 exposed at a major surface 175 of a microelectronic element 172, e.g., a semiconductor chip having active devices, passive devices or both active and passive devices thereon. The interconnection element may function as a fan-out element with features 138 carrying signals, voltages and ground to and from the microelectronic element to locations beyond edges of the microelectronic element.

[0048] In one example, the interconnection element can function as a package substrate or chip carrier in a package including the microelectronic element and interconnection element. Thus, in a particular embodiment, the contacts 174 of the chip have a pitch 195 in a left-right direction shown in FIG. 13 and the metal posts 130, 128a have a pitch 196 which matches the pitch 195 of the chip contacts 174.

[0049] Alternatively, the interconnection element can function as a carrier to which a plurality of microelectronic elements and optionally other circuit elements, e.g., integrated or discrete passive devices or discrete active devices or combination thereof are directly connected.

[0050] The tips 160 of the conductive posts, which project outwardly beyond an exposed surface 176 of the solder mask at the upper face of the interconnection element 170, are joined to corresponding conductive pads 174 of the microelectronic element. As illustrated in FIG. 13A, the posts of the interconnection element can be joined directly to the conductive pads, such as through a diffusion bond formed between a finish metal at the tips 160 of the posts, e.g., gold, and another metal present in the conductive pads and the posts. Alternatively, the posts can be joined to the microelectronic element through a fusible metal such as a solder, tin or a eutectic composition, the fusible metal wetting the posts and the pads to form wetted or soldered joints. For example, the fusible metal can be provided in form of solder bumps (not shown), exposed at a surface 175 of the microelectronic element, the bumps being provided on conductive pads 174 having suitable under bump metal structures. In another example, solder masses or tin carried on the tips 160 of the conductive posts can form part of the joints.

[0051] The conductive posts 130, which are solid metal structures throughout, have relatively high current-carrying capacity, making the interconnection element suitable for interconnection with microelectronic elements, i.e., chips having high current density. Elements typically included within a processor such as microprocessors, co-processors, logic chips, and the like, have high current density and typically also have high interconnect density (high numbers of relatively fine pitch pads 174). The high current-carrying capacity of the solid metal posts 130 of interconnection element 170 make them suitable for interconnection with such chips. The formation of the metal posts by plating within openings of a mandrel allows one to form metal posts which have frusto-conical shape, essentially cylindrical shape, or other shape as needed.

[0052] At a lower face 178 of the interconnection element, terminals 151 can be joined to corresponding terminals 182 of a circuit panel, wiring element, packaged microelectronic element or other conductive element. For example, as illustrated in FIG. 13A, the terminals 151 can be joined to terminals 182 of a circuit panel 184 via conductive masses 180. In one example, the conductive masses 180 can include a fusible metal such as solder, tin or a eutectic composition.

[0053] In a variation of the above embodiment, processing which forms the second dielectric layer and fourth metal layer as described above with reference to FIG. 10 is omitted. In such case, the resulting interconnection element does not include the second dielectric layer. Terminals of the interconnection element are formed using the metal features 138 (FIG. 9) of the third metal layer. Such interconnection element may function as a chip carrier to provide fan-out as described above.

[0054] FIG. 13B illustrates an interconnection element 190 in accordance with a variation of the embodiment illustrated in FIGS. 12A-B. As seen in FIG. 13B, traces 192, 192a, 192b extend in at least one direction along a major surface 193 of the dielectric layer 194. For example, the traces 192, 192a, 192b can extend in the same directions 173 to which the posts depicted in FIG. 13B are aligned. Alternatively, the traces 192, 192a, 192b can extend in a direction along the major surface of the dielectric layer 194 which is transverse to the direction in which the posts are aligned. For example, the traces 192, 192a, 192b can be disposed in a direction into and out of the plane in which the interconnect element is depicted in FIG. 12A.

[0055] Some traces, e.g., trace 192a, can be disposed between adjacent conductive posts 130a and can be electrically insulated therefrom by the dielectric element including dielectric layer 132. Although not shown specifically in FIG. 13B, a plurality of traces 192a can be disposed between adjacent ones of the metal posts. As depicted in FIG. 13B, traces 192, 192a can be electrically insulated from the metal posts. Alternatively, a trace can be conductively connected to one or more metal posts, in such manner as trace 192b is shown connected with post 130b. In another example, traces 192, 192b shown at edges of FIG. 13B can extend in directions 173 and be connected to other metal posts (not shown) which are disposed at locations along the major surface of the dielectric layer 194 beyond edges 171 of the view depicted in FIG. 13B. Alternatively or in addition thereto, traces 192, 192a, 192b can be extend in a direction transverse to the plane of the drawing of FIG. 12A and be insulated from or connected to metal posts (not shown) which are beyond the view.

[0056] The traces 192 including traces 192a, 192b can be formed simultaneously with the posts 130 when the posts 130

are plated onto surfaces of the openings 102, e.g., recesses in the mandrel 118 and then separated by subsequent patterning, e.g., etching in accordance with a masking layer, as described above with reference to FIGS. 5-6.

[0057] In another variation, although not specifically depicted in FIG. 13B, traces along the surface of the dielectric element need not be conductively connected to any of the conductive posts.

[0058] FIGS. 14 through 17 illustrate a method of forming an interconnection element in accordance with a variation of the above-described embodiment. This embodiment varies from that described above in that the second metal layer 224 may not have sufficient thickness to fill the holes 102 in the mandrel 118. For example, a thin conductive layer 224 consisting essentially of copper and having a thickness of a few microns or a few tens of microns can be electroplated onto the metal liner 222. A thin copper layer having a thickness of one to two microns or up to a few tens of microns can be formed, for example, by electroplating copper onto a metal liner 222 consisting essentially of nickel. FIG. 15 illustrates the structure after patterning the second metal layer 224 and metal liner 222 to form conductive posts 230. The metal layers can be patterned in a manner such as described above with reference to FIG. 6.

[0059] Subsequently, as shown in FIG. 16, a dielectric layer 232 is formed which covers the conductive posts 230, in a manner similar to that described above (FIG. 7). The dielectric layer 232 may or may not extend inward into interior volumes enclosed by the metal layers of the posts 230. As shown in FIG. 16, dielectric material may partially or fully occupy the interior volume enclosed by the metal layers 222, 222 within each post.

[0060] In the stage of processing illustrated in FIG. 17, holes 234 are formed in the dielectric layer 232 in axial

alignment with the conductive posts 230, by processing such as that described above (FIG. 8), e.g., with photolithography or laser drilling, for example. As a result of such processing, the dielectric material can be removed from the interior volumes 236 of the conductive posts. The dielectric material is fully removed from interior volumes of the posts as shown in FIG. 17. Thereafter, processing continues in a manner as described above with reference to FIG. 9, except that when the third metal layer 142 is formed, interior volumes of the conductive posts are also filled in the process. Thereafter, steps are performed to complete the interconnection element, as described above with reference to FIGS. 10-12.

[0061] Alternatively, at the stage of processing illustrated in FIG. 17, the dielectric material may be only partially removed, such that at least portions of the second metal layer 224 of the conductive posts are exposed. However, some dielectric material may remain within the interior volumes of the posts. Then, the electroplating step (FIG. 9) may fill the interior volumes of the posts only partially, i.e., only to the extent that the interior volumes are not occupied by dielectric material.

[0062] In another variation of the above-described embodiment, a relatively thin second metal layer 324 (FIG. 18) is formed on the metal liner 322, in like manner to that described above with reference to FIG. 14. Thereafter, the second metal layer and metal liner are patterned to form conductive posts 330 (FIG. 19) interconnected by second metal features 331, e.g., traces, metal lines or other metal features extending along a top surface 104 of the mandrel 118.

[0063] After forming a dielectric layer 332 thereon (FIG. 20), holes 334 (FIG. 21) are formed in the dielectric

layer 332 in axial alignment with the second metal features 331 such that at least portions of the second metal features 331 are exposed within the holes. A third relatively thin metal layer 342 (FIG. 22) can then be electroplated onto the structure, which may be preceded by the formation of a seed layer. During the electroplating process, the exposed second metal features 331 serve to provide conductive interconnection to the conductive mandrel 118. The third metal layer 342 can have a thickness ranging from one or two microns and up.

[0064] As further illustrated in FIG. 23, the third metal layer can be patterned into individual third metal features 338, e.g., lines, traces, pads or other features conductively connected to the second metal layer below. Some of the metal lines formed thereby extend in directions over the first dielectric layer 332 but may not be conductively connected to the third metal features 331 of the second metal layer. Thereafter, a second dielectric layer 344 can be formed over the first dielectric layer 332 and the third metal features 338 thereon, after which the second dielectric layer 344 is patterned to form holes 346 in axial alignment with the third metal features 338 such that the metal features 338 are exposed within holes 346. A fourth metal layer then is electroplated thereon and patterned to form fourth metal features 348 conductively connected with the third metal features 338.

[0065] FIG. 24 illustrates the structure 350 after removal of the mandrel, which can be done as described above with reference to FIG. 11. FIG. 25 illustrates a resulting interconnection element 370, after forming solder masks 356 and 356 and a finish metal layer 362 thereon as described above with reference to FIG. 12. As seen in FIG. 25, the interconnection element 370 includes metal posts 330 having plated metal layers 322, 322 that do not fill the entire

volumes of the posts. Instead, a dielectric material may fill interior volumes of the posts. The metal posts 330 are interconnected by way of the second, third and fourth metal features 331, 336 and 346 to terminals 351 exposed at a major surface 378 of the interconnection element 370 opposite from the conductive posts.

[0066] The conductive posts 330 of interconnection element 370, which are not solid metal structures throughout, have somewhat lower current-carrying capacity than the above-described interconnection element 170 (FIG. 12). It may be possible to produce the interconnection element 370 at lower cost, if the conductive posts and other metal features therein can be plated in less time than the time required to make the comparable metal posts, vias and metal features of interconnection element 170 (FIG. 12). The lower current-carrying capacity of interconnection element 370 may also be better suited to certain types of chips which have lower current density, such as, for example, memory chips.

[0067] Although the invention herein has been described with reference to particular embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present invention. It is therefore to be understood that numerous modifications may be made to the illustrative embodiments and that other arrangements may be devised without departing from the spirit and scope of the present invention as defined by the appended claims.

CLAIMS

1. An interconnection element for conductive interconnection with another element having at least one of microelectronic devices or wiring thereon, comprising:

a dielectric element having a major surface;

a plated metal layer including a plurality of exposed metal posts projecting outwardly beyond the major surface of the dielectric element, at least some of the metal posts electrically insulated from each other by the dielectric element, the posts being defined by plating a metal onto exposed co-planar surfaces of a mandrel and interior surfaces of openings in a mandrel and subsequently removing the mandrel; and

a plurality of terminals in conductive communication with the metal posts, the terminals being connected through the dielectric element to the metal posts.

2. An interconnection element as claimed in claim 1, wherein the metal layer includes a plurality of metal wiring traces extending in at least one direction along the major surface of the dielectric element, at least some of the metal wiring traces being electrically insulated from the metal posts.

3. An interconnection element as claimed in claim 1, wherein one or more metal wiring traces are disposed between adjacent ones of the metal posts and is insulated from the adjacent metal posts.

4. An interconnection element as claimed in claim 1, wherein at least a portion of the metal layer extends in a direction along the major surface of the dielectric element and is joined to at least one of the metal posts.

5. An interconnection element as claimed in claim 1, wherein portions of the dielectric element are disposed between the at least one metal wiring trace and the adjacent metal posts.

6. An interconnection element as claimed in claim 2, wherein at least one of the metal wiring traces is connected to an adjacent one of the metal posts.

7. An interconnection element as claimed in claim 1, wherein the metal layer is a first metal layer and at least one second metal layer connects the terminals with the metal posts through the dielectric element.

8. An interconnection element as claimed in claim 7, wherein the second metal layer is conductively joined to bases of the metal posts.

9. An interconnection element as claimed in claim 1, wherein the metal posts have a height of at least 35 microns from the major surface and a pitch smaller than about 150 microns.

10. An interconnection element as claimed in claim 1, wherein each metal post has frusto-conical shape.

11. An interconnection element as claimed in claim 1, wherein each metal post has essentially cylindrical shape.

12. A packaged microelectronic element including the interconnection element as claimed in claim 1, and a microelectronic element including a plurality of exposed contacts having a pitch, wherein the metal posts have a pitch matching the pitch of the contacts, the metal posts being conductively joined to the contacts.

13. An interconnection element as claimed in claim 1, wherein the metal layer includes an inner metal layer adjacent to the dielectric element and an outer metal layer overlying the inner metal layer.

14. An interconnection element as claimed in claim 13, wherein the inner metal layer is formed by plating a metal onto the outer metal layer.

15. An interconnection element as claimed in claim 14, wherein the outer metal layer includes nickel and the inner metal layer includes copper.

16. A packaged microelectronic element including the interconnection element as claimed in claim 1 and a microelectronic element including a plurality of exposed contacts having a pitch, wherein the metal posts have a pitch matching the pitch of the contacts, the metal posts being joined to the contacts.

17. A method of fabricating an interconnection element having raised conductive posts for conductive interconnection with another element having at least one of microelectronic devices or wiring thereon, comprising:

a) forming conductive posts within a plurality of holes of a first element, each conductive post including at least a metal liner lining walls of the holes;

b) forming terminals in conductive communication with the conductive posts, the terminals being connected through a dielectric layer to the conductive posts; and

c) causing the conductive posts to project outwardly beyond a major surface of the interconnection element.

18. The method as claimed in claim 17, wherein the conductive posts are caused to project outwardly by removing at least a portion of the first element after forming the terminals.

19. The method as claimed in claim 18, wherein the first element is removed by etching the first element selectively relative to the metal liner.

20. The method as claimed in claim 19, wherein the first element includes a first metal and the metal liner includes a second metal, the second metal resisting attack by an etchant used to selectively etch the first element.

21. The method as claimed in claim 20, wherein step (a) includes forming a second metal layer in contact with the metal liner within the holes.

22. The method as claimed in claim 21, further comprising forming the metal liner by processing including plating.

23. The method as claimed in claimed in claim 21, wherein the step of forming the second metal layer includes plating.

24. The method as claimed in claim 23, wherein the second metal layer fills the holes.

25. The method as claimed in claim 21, wherein the second metal layer includes the first metal.

26. The method as claimed in claim 25, wherein the first metal is copper and the metal liner includes nickel.

27. The method as claimed in claim 17, wherein the first element includes a metal sheet consisting essentially of copper and the holes have a pitch less than about 150 microns.

28. The method as claimed in claim 27, wherein the first element is formed by laser drilling through holes in a metal sheet and joining a carrier to a face of the metal sheet to cover the through holes.

29. The method as claimed in claim 27, wherein the first element is formed by mechanically forming through holes in a metal sheet and joining a carrier to a face of the metal sheet to cover the through holes.

30. The method as claimed in claim 27, wherein the conductive posts have frusto-conical shape.

31. The method as claimed in claim 27, wherein conductive posts have cylindrical shape.

32. A method of fabricating an interconnection element, comprising:

a) forming conductive posts within a plurality of blind holes of a first element including a first metal, each conductive post having a liner including a second metal lining the holes and a layer including a third metal

contacting the liner within the holes, the second metal being resistant to attack by an etchant which attacks the first metal;

b) forming terminals exposed at a bottom surface of a dielectric layer, the terminals being in conductive communication with the conductive posts; and

c) selectively removing at least a portion of the first element using the etchant to cause at least portions of the conductive posts to protrude beyond the surface of the dielectric layer.

FIG. 1

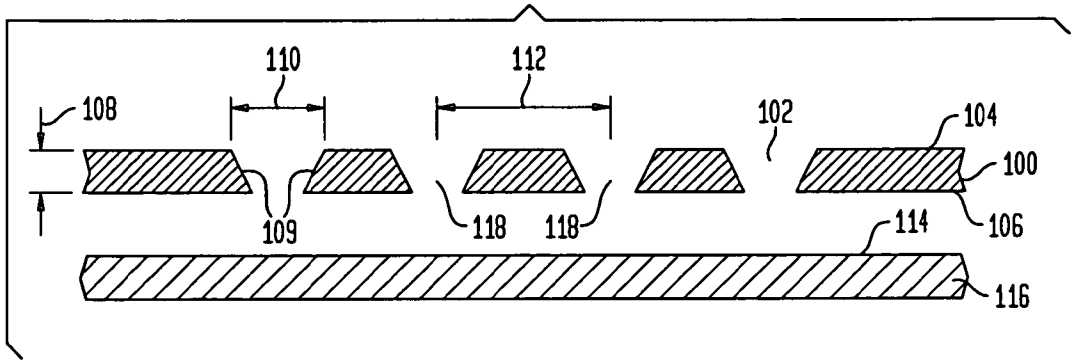

110
112
108
102
104
100
109
118
118
114
106
116

FIG. 2

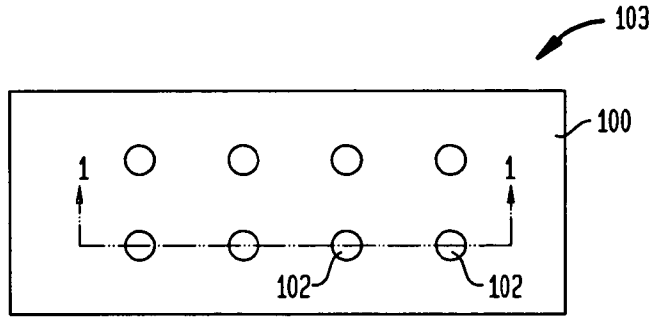

103
100
1
1
102
102

FIG. 3

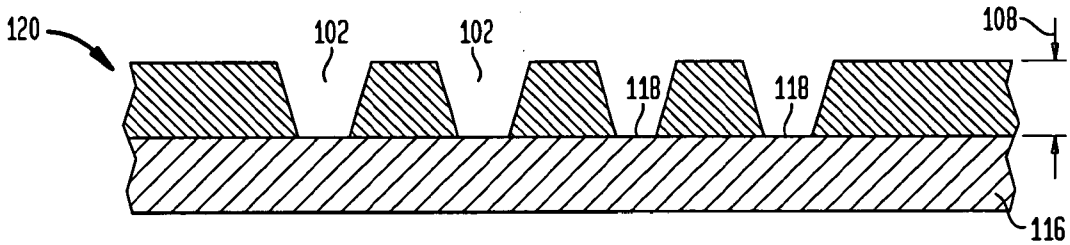


FIG. 4

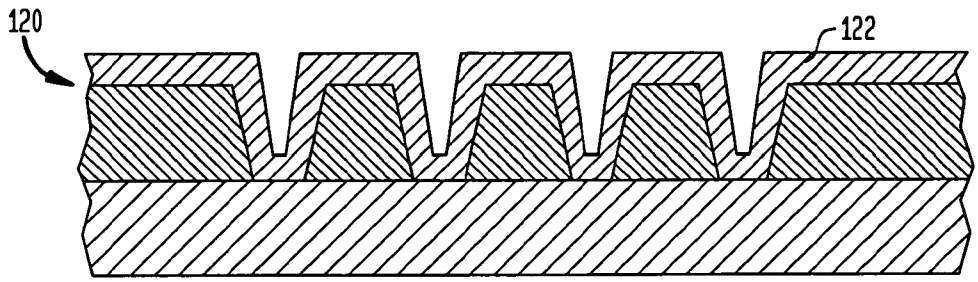


FIG. 5

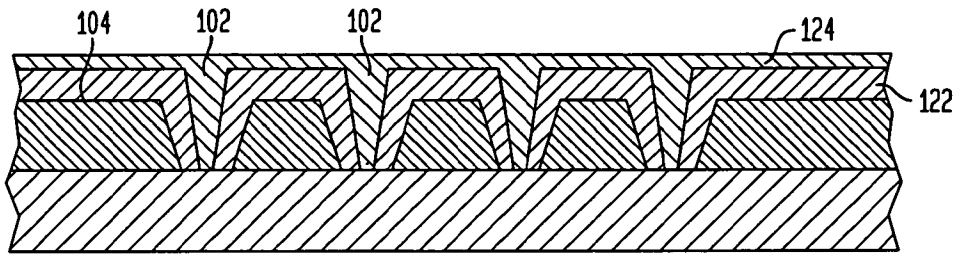


FIG. 6

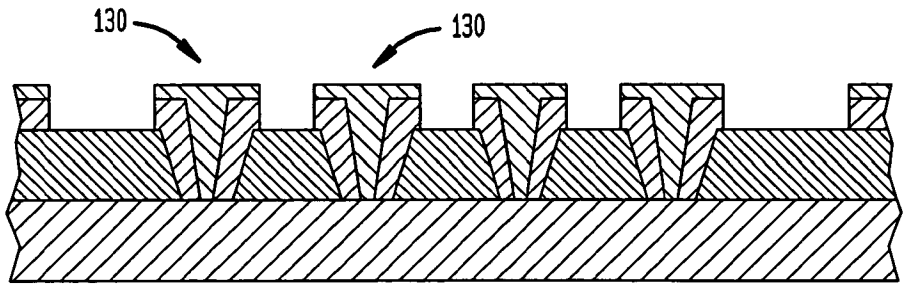


FIG. 7

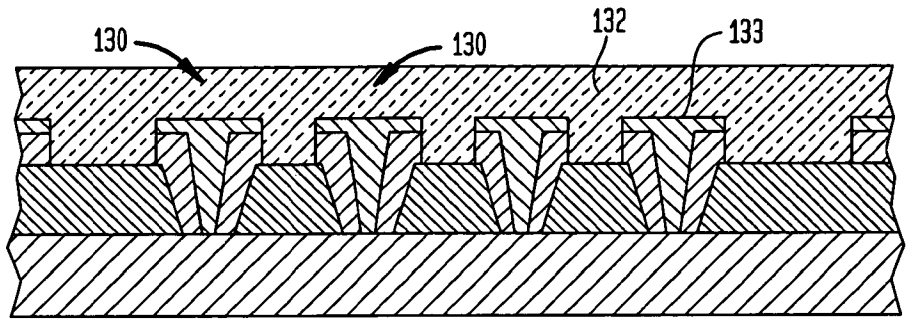


FIG. 8

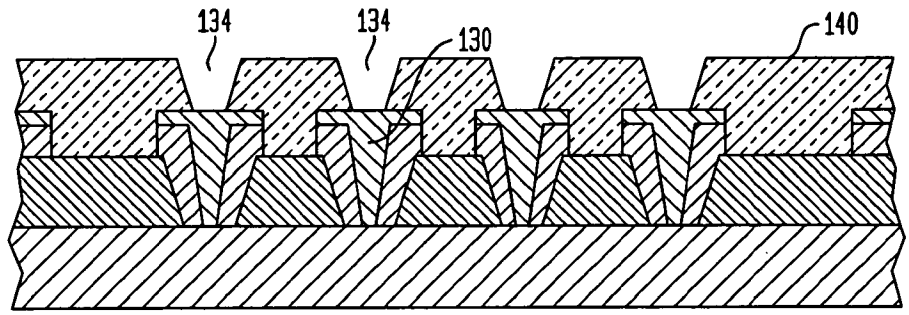


FIG. 9

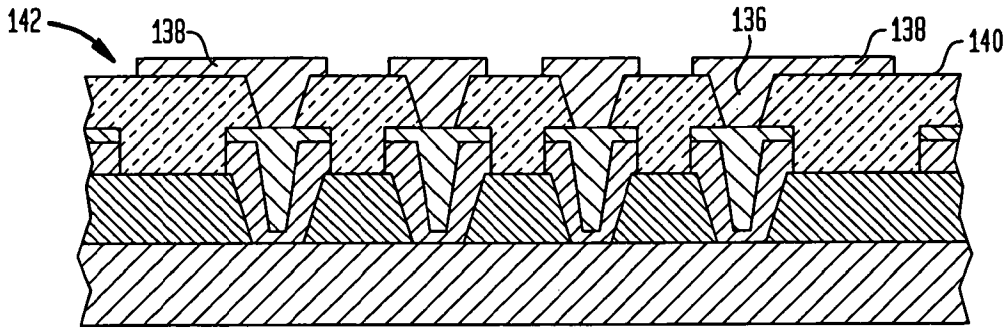


FIG. 10

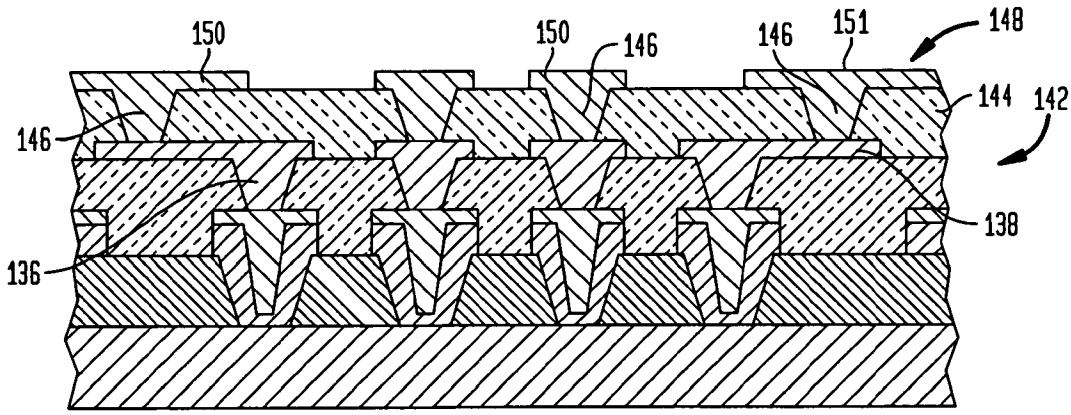


FIG. 11

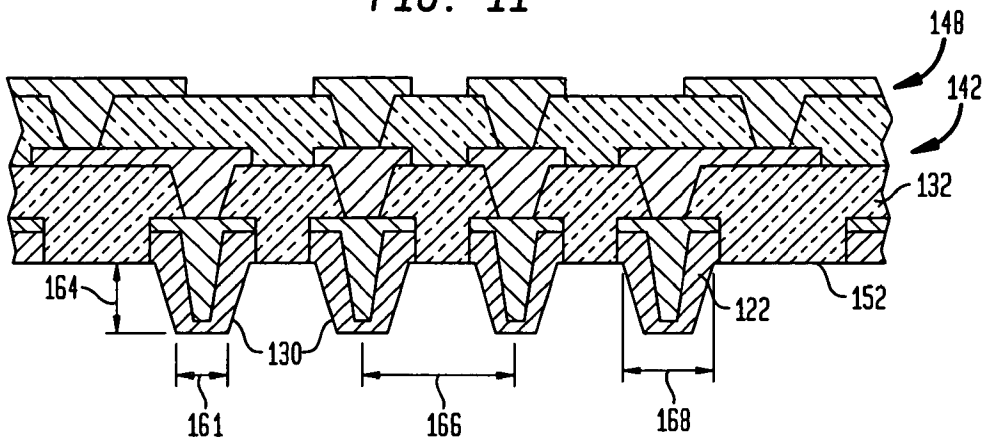


FIG. 12A

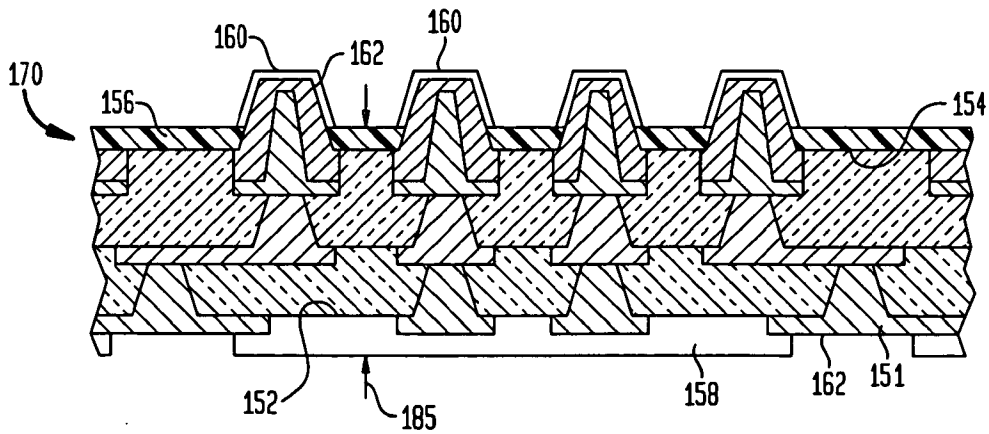


FIG. 12B

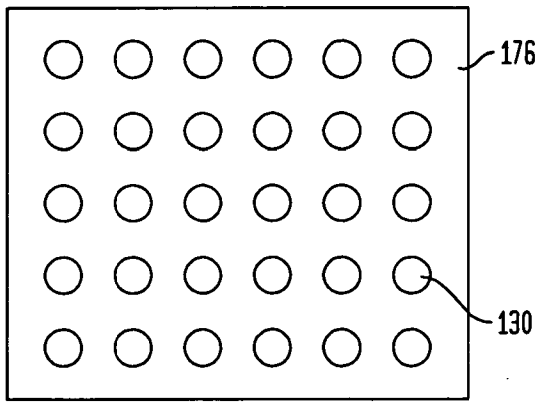


FIG. 13A

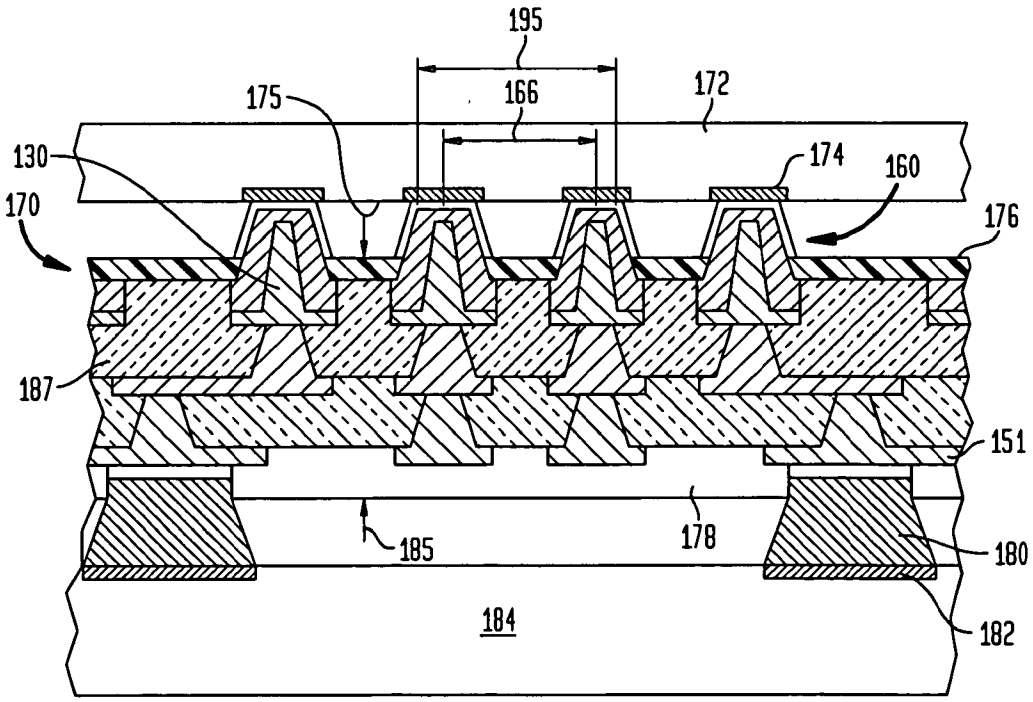


FIG. 13B

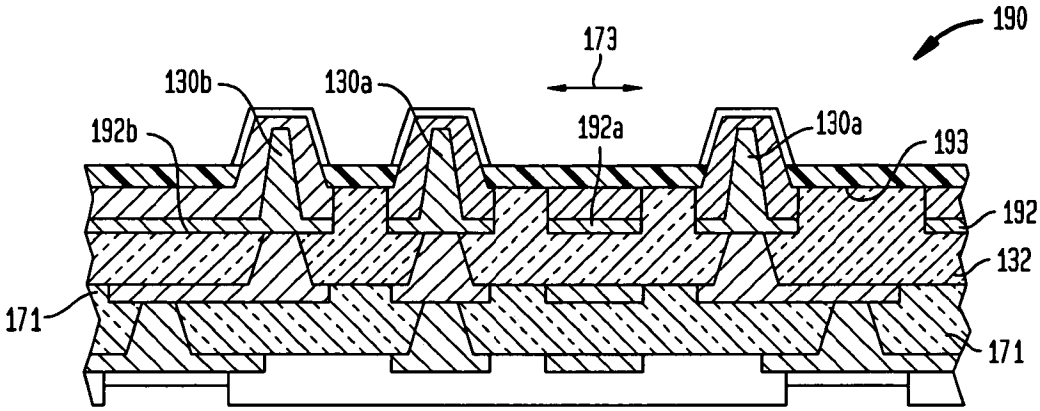


FIG. 14

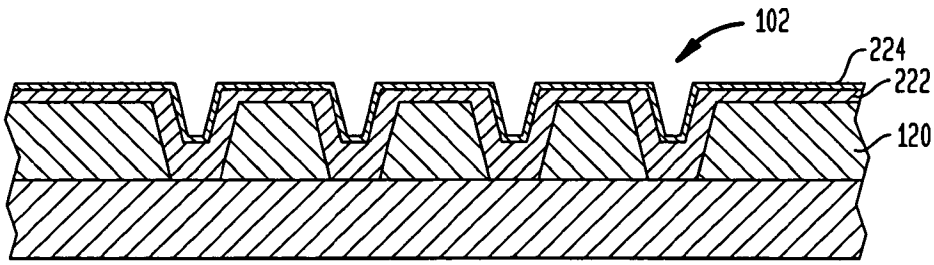


FIG. 15

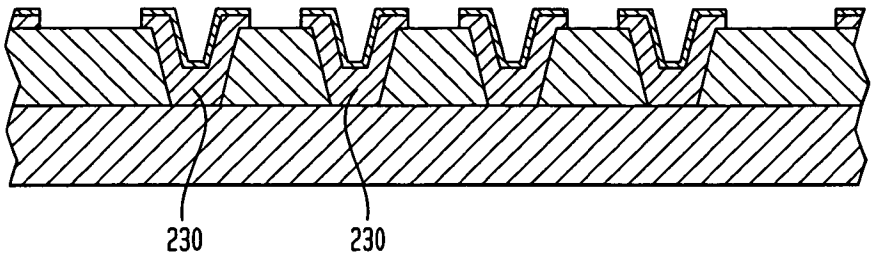


FIG. 16

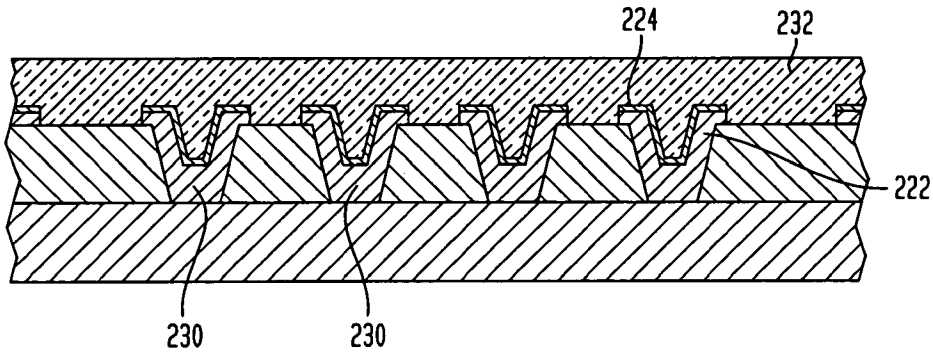


FIG. 17

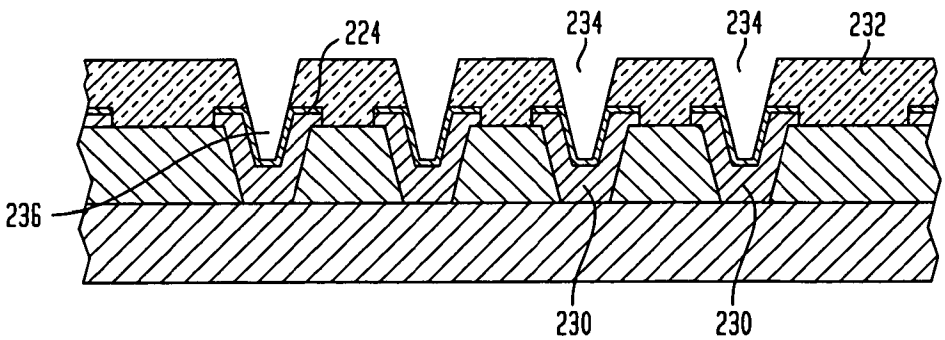


FIG. 18

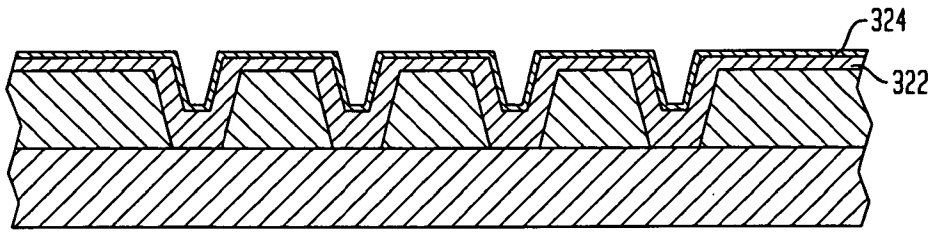


FIG. 19

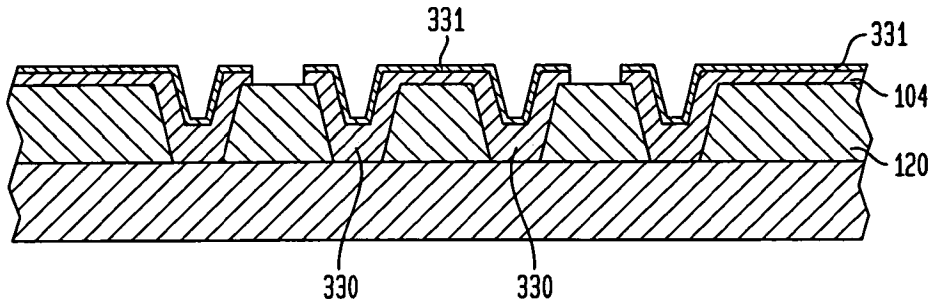


FIG. 20

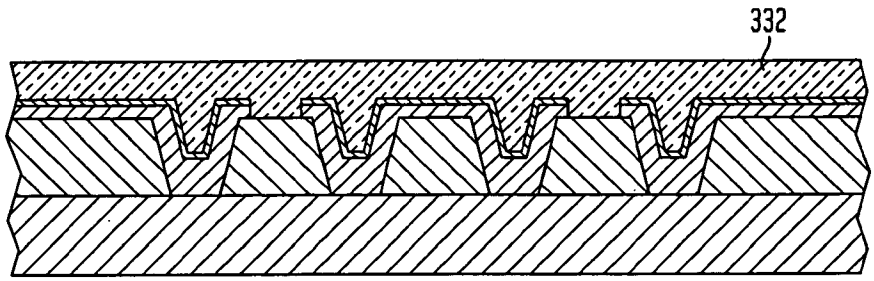


FIG. 21

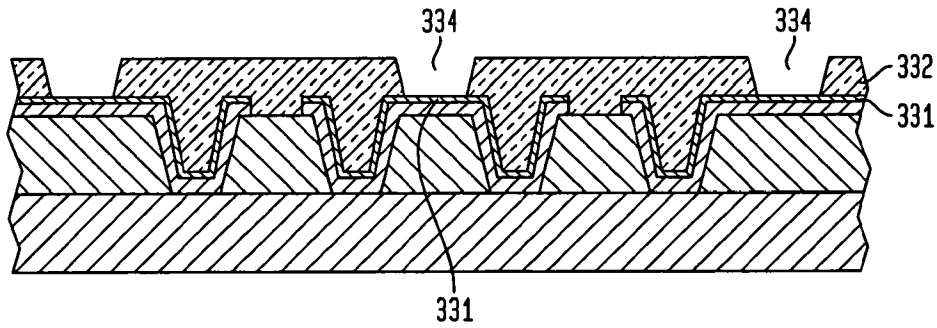


FIG. 22

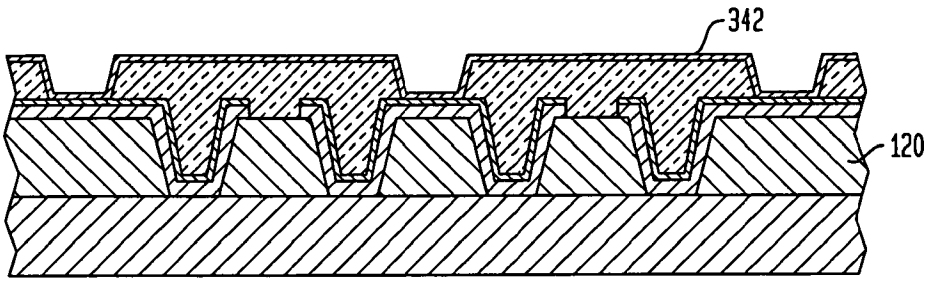


FIG. 23

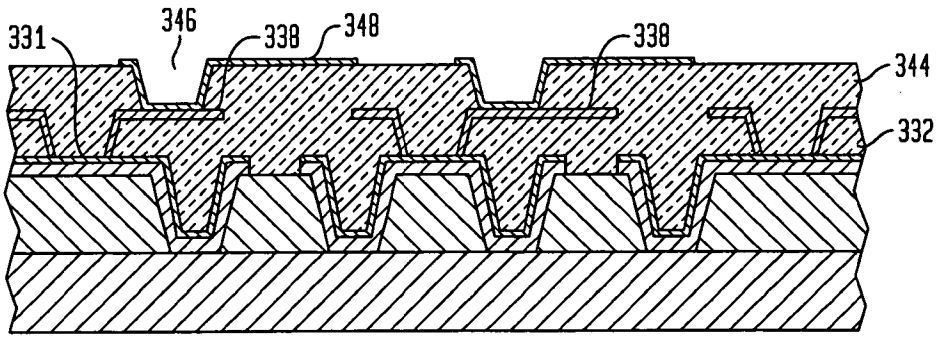


FIG. 24

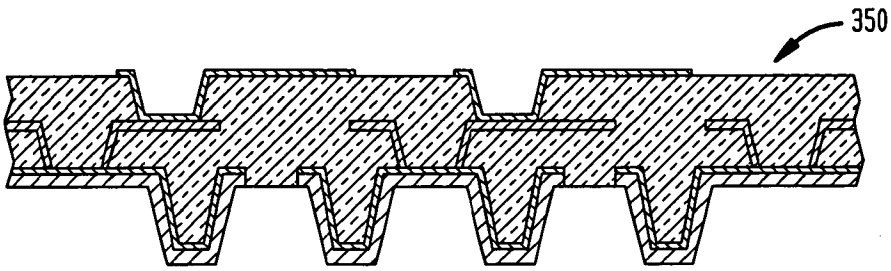
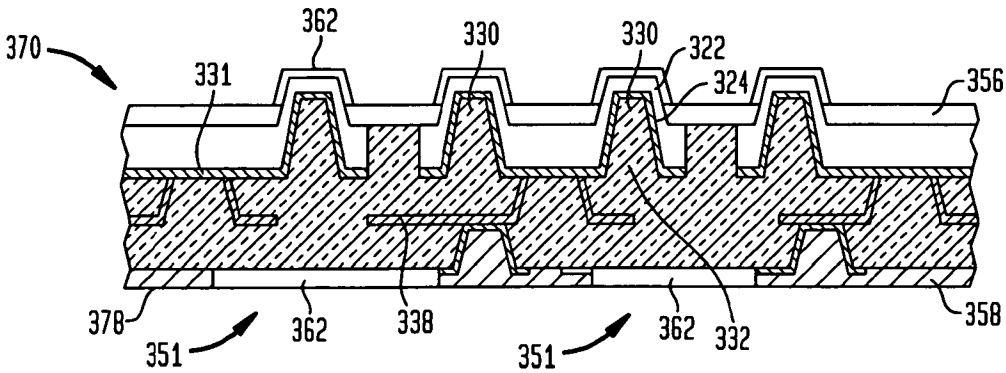

350

FIG. 25


370
362
330
330
322
324
331
356
378
351
362
338
351
362
332
358