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Semiconductor memory device

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(73) Proprietor
Hitachi Ltd.,
5—1, Marunouchi 1-chome
Chiyoda-ku
Tokyo
Japan

(72) Inventor
Nobuyoshi Tanimura

(74) Agent and/or
Address for Service
Mewburn Ellis & Co.,
2/3 Cursitor Street
London EC4A EC4A 1BQ

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GB 1469231
GB 1380776
GB 1272551

(58) Field of search
G4A

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FIG. 1

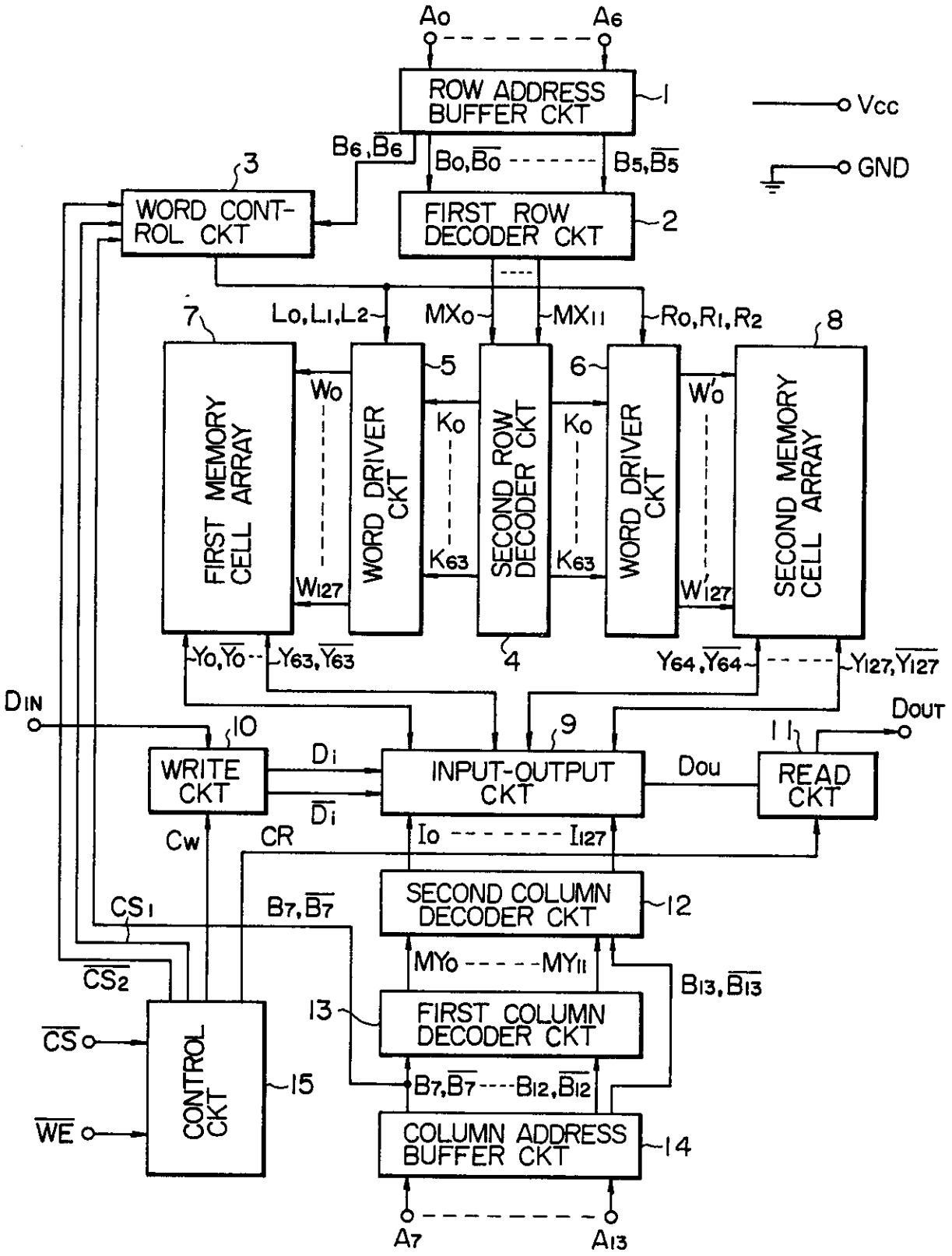

A0
A6
ROW ADDRESS BUFFER CKT
1
Vcc
GND
B6, B̄6
B0, B̄0
B5, B̄5
3
WORD CONTROL CKT
FIRST ROW DECODER CKT
2
7
L0, L1, L2
MX0
MX11
R0, R1, R2
8
FIRST MEMORY CELL ARRAY
W0
W127
WORD DRIVER CKT
5
K0
K63
SECOND ROW DECODER CKT
4
6
WORD DRIVER CKT
W'0
W'127
SECOND MEMORY CELL ARRAY
Y0, Ȳ0
Y63, Ȳ63
Y64, Ȳ64
Y127, Ȳ127
DIN
DOUT
10
WRITE CKT
Di
D̄i
9
INPUT-OUTPUT CKT
Dou
11
READ CKT
Cw
CR
I0
I127
CS1
B7, B̄7
SECOND COLUMN DECODER CKT
12
CS2
MY0
MY11
B13, B̄13
13
FIRST COLUMN DECODER CKT
CS̄
WĒ
CONTROL CKT
15
B7, B̄7
B12, B̄12
COLUMN ADDRESS BUFFER CKT
14
A7
A13

FIG. 2

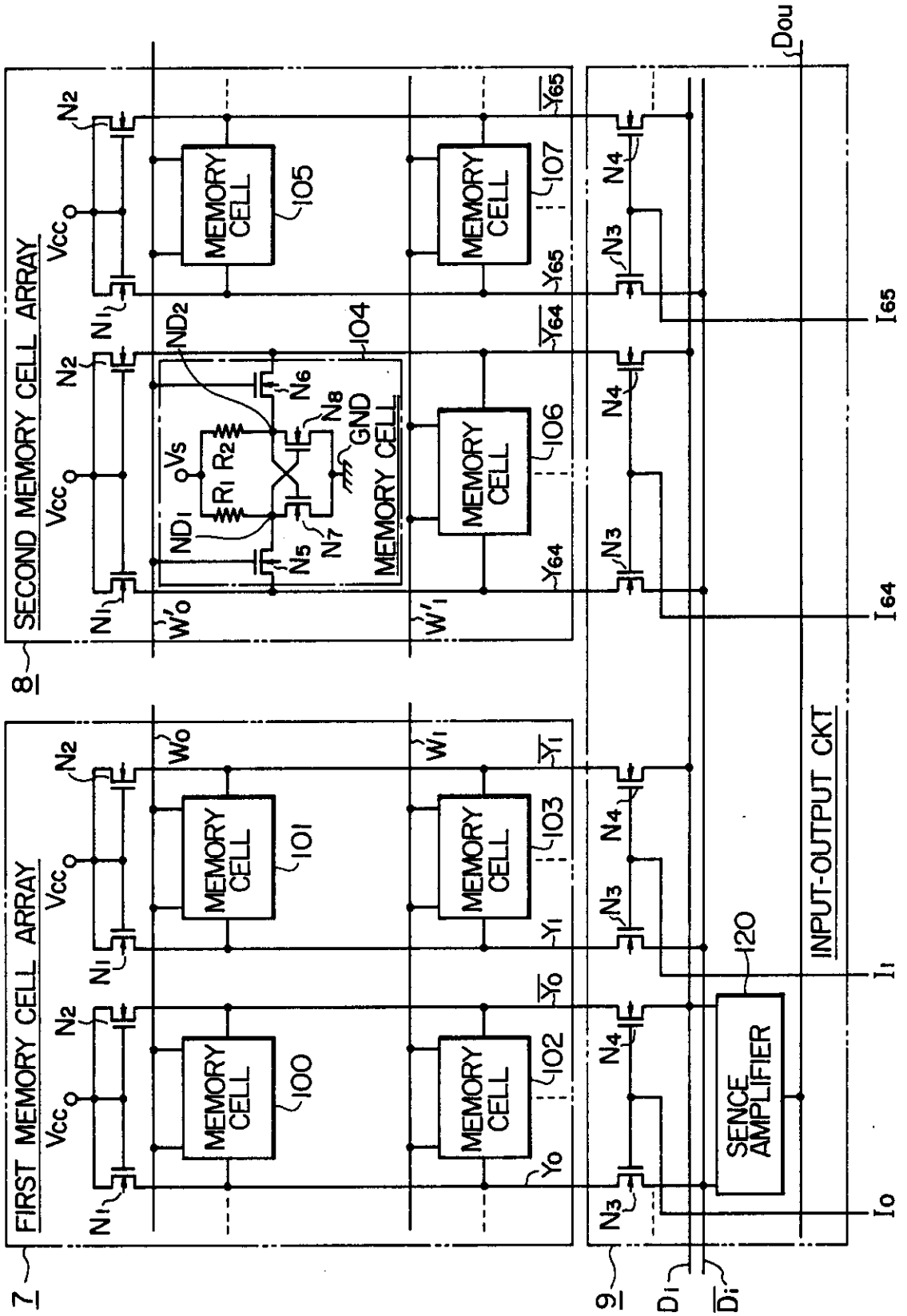

FIRST MEMORY CELL ARRAY
SECOND MEMORY CELL ARRAY
MEMORY CELL
SENCE AMPLIFIER
INPUT-OUTPUT CKT
Vcc
GND
Vs
Dou
100
101
102
103
104
105
106
107
120
7
8
9

FIG. 3A

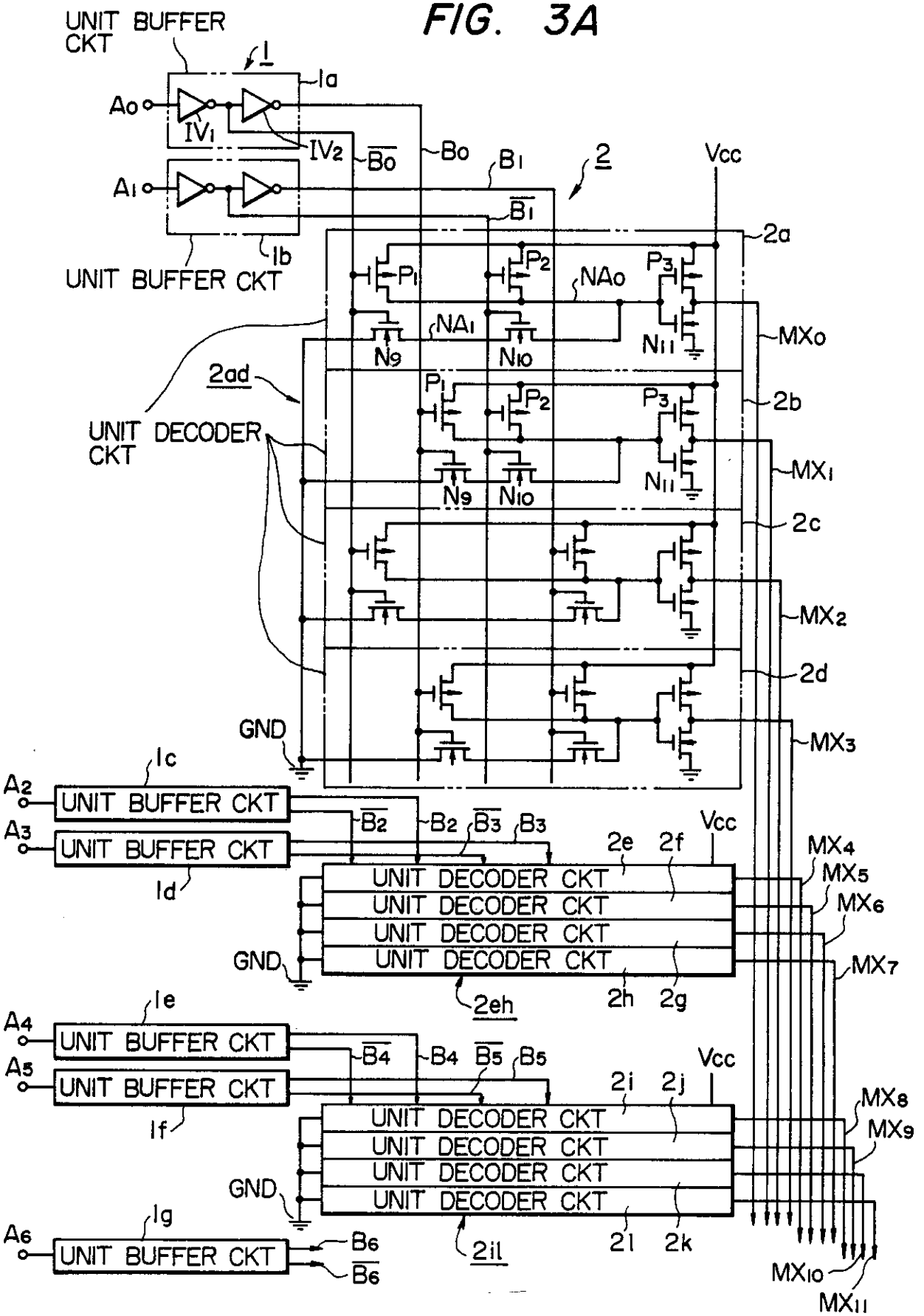

UNIT BUFFER CKT
1
1a
Ao
IV1
IV2
Bo
Bo
B1
2
Vcc
A1
B1
1b
UNIT BUFFER CKT
2a
P1
P2
NAo
P3
NA1
N9
N10
N11
MXo
2ad
UNIT DECODER CKT
2b
MX1
2c
MX2
2d
GND
MX3
1c
A2
UNIT BUFFER CKT
B2
B2
B3
B3
Vcc
A3
UNIT BUFFER CKT
1d
2e
2f
MX4
MX5
MX6
UNIT DECODER CKT
UNIT DECODER CKT
UNIT DECODER CKT
UNIT DECODER CKT
GND
MX7
2eh
2h
2g
1e
A4
UNIT BUFFER CKT
B4
B4
B5
B5
Vcc
A5
UNIT BUFFER CKT
1f
2i
2j
MX8
MX9
UNIT DECODER CKT
UNIT DECODER CKT
UNIT DECODER CKT
UNIT DECODER CKT
GND
1g
A6
UNIT BUFFER CKT
B6
B6
2il
2l
2k
MX10
MX11

FIG. 3B

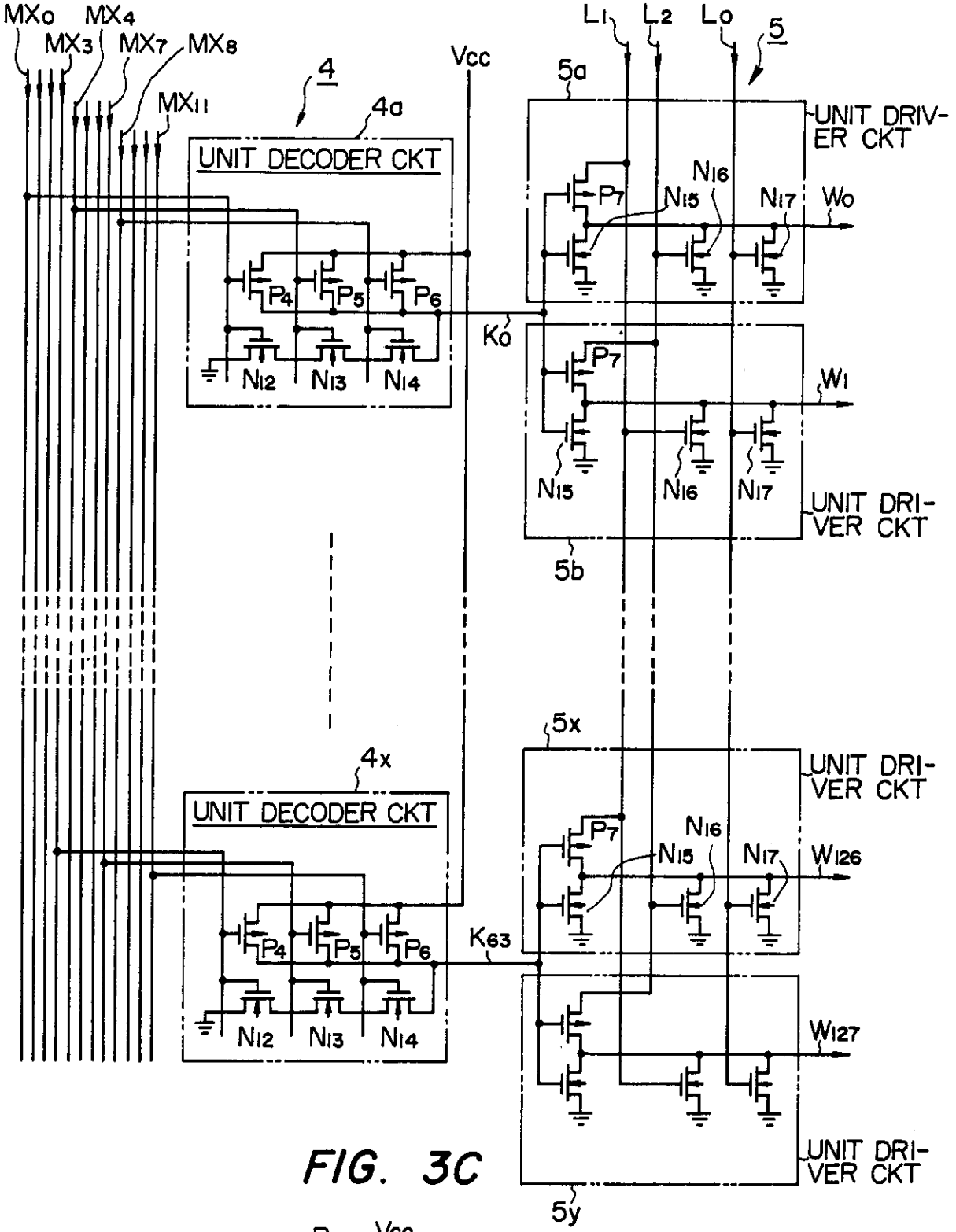

MXo
MX4
MX3
MX7
MX8
MX11
4
4a
UNIT DECODER CKT
Vcc
L1
L2
Lo
5
5a
UNIT DRIV-ER CKT
P7
N16
N15
N17
Wo
P4
P5
P6
Ko
N12
N13
N14
W1
5b
UNIT DRI-VER CKT
4x
5x
K63
W126
W127
5y

FIG. 3C

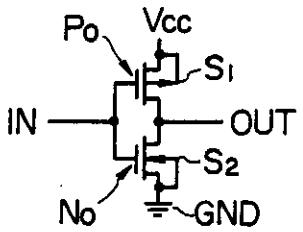

Po
Vcc
S1
IN
OUT
S2
No
GND

FIG. 4A

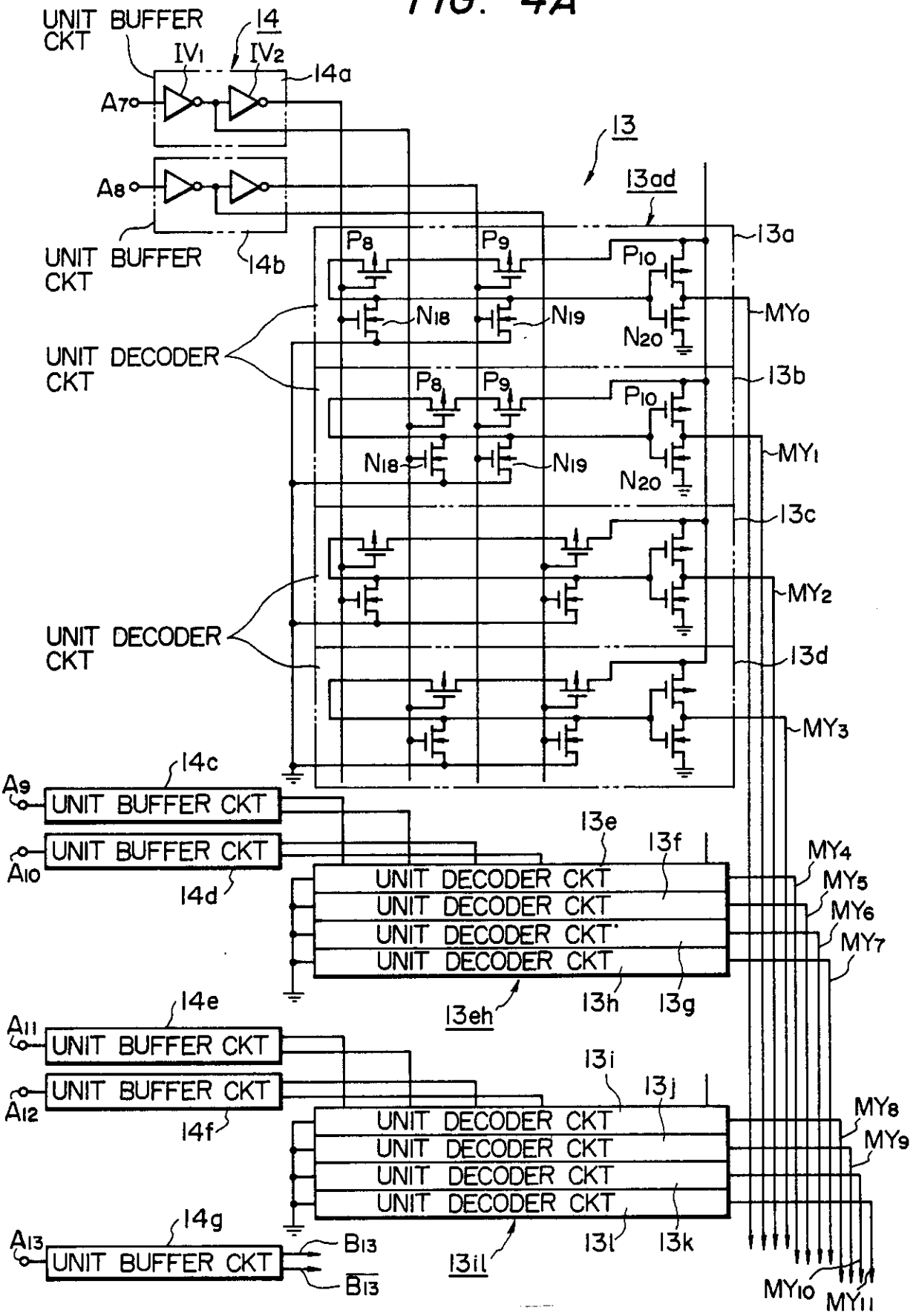

UNIT BUFFER CKT
14
IV1
IV2
14a
A7
A8
UNIT BUFFER CKT
14b
13
13ad
13a
P8
P9
P10
N18
N19
N20
MY0
UNIT DECODER CKT
13b
MY1
13c
MY2
UNIT DECODER CKT
13d
MY3
14c
A9
UNIT BUFFER CKT
A10
UNIT BUFFER CKT
14d
13e
13f
UNIT DECODER CKT
UNIT DECODER CKT
UNIT DECODER CKT
UNIT DECODER CKT
MY4
MY5
MY6
MY7
13eh
13h
13g
14e
A11
UNIT BUFFER CKT
A12
UNIT BUFFER CKT
14f
13i
13j
UNIT DECODER CKT
UNIT DECODER CKT
UNIT DECODER CKT
UNIT DECODER CKT
MY8
MY9
14g
A13
UNIT BUFFER CKT
B13
B13
13il
13l
13k
MY10
MY11

FIG. 4B

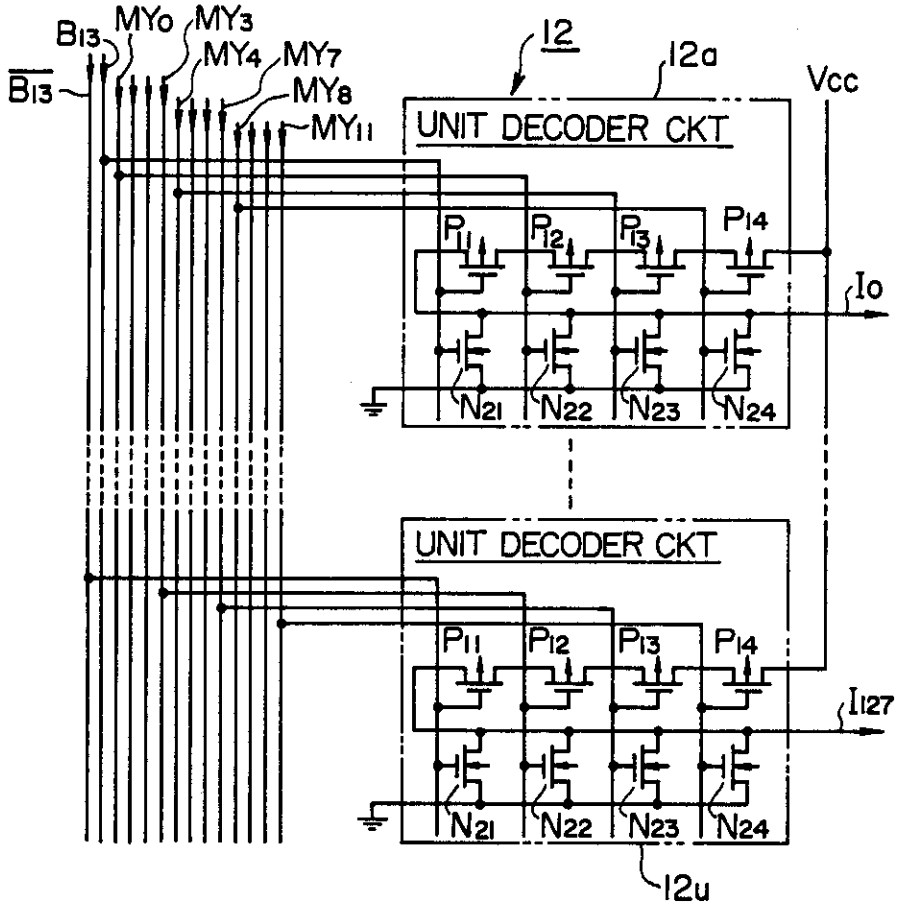

B13
B13
MY0
MY3
MY4
MY7
MY8
MY11
12
12a
Vcc
UNIT DECODER CKT
P11
P12
P13
P14
Io
N21
N22
N23
N24
UNIT DECODER CKT
P11
P12
P13
P14
I127
N21
N22
N23
N24
12u

FIG. 4C

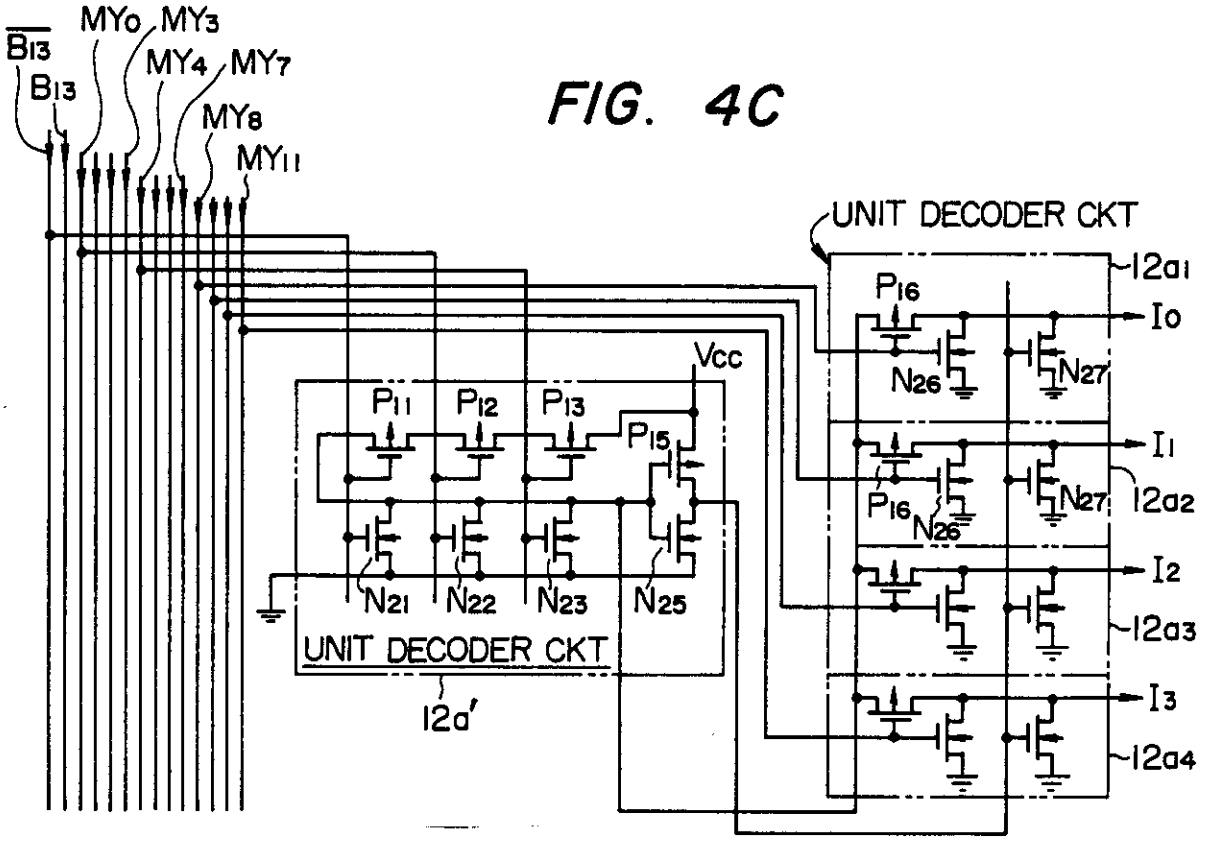

B13
B13
MY0
MY3
MY4
MY7
MY8
MY11
UNIT DECODER CKT
12a1
P16
Io
N26
N27
Vcc
P11
P12
P13
P15
I1
P16
N26
N27
12a2
N21
N22
N23
N25
I2
UNIT DECODER CKT
12a'
12a3
I3
12a4

FIG. 5

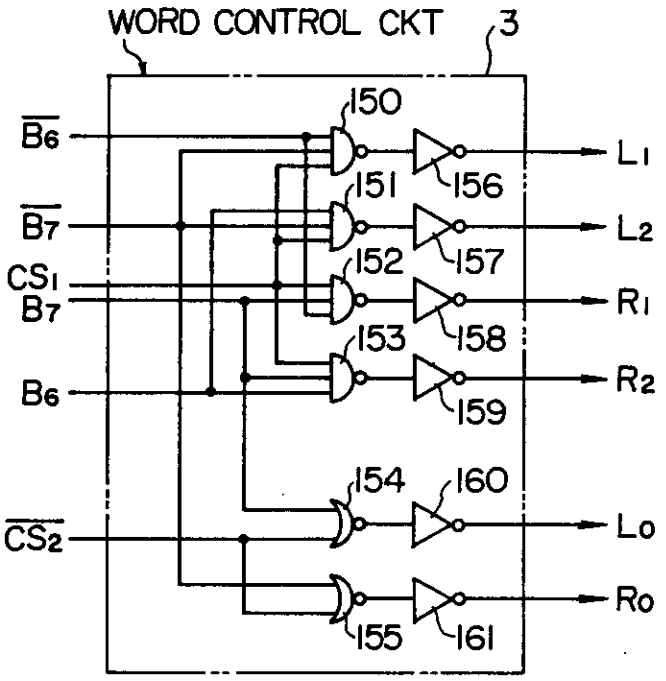

WORD CONTROL CKT
3
150
151
152
153
154
155
156
157
158
159
160
161
$\overline{B_6}$
$\overline{B_7}$
CS_1
B_7
B_6
$\overline{CS_2}$
L_1
L_2
R_1
R_2
L_0
R_0

FIG. 6

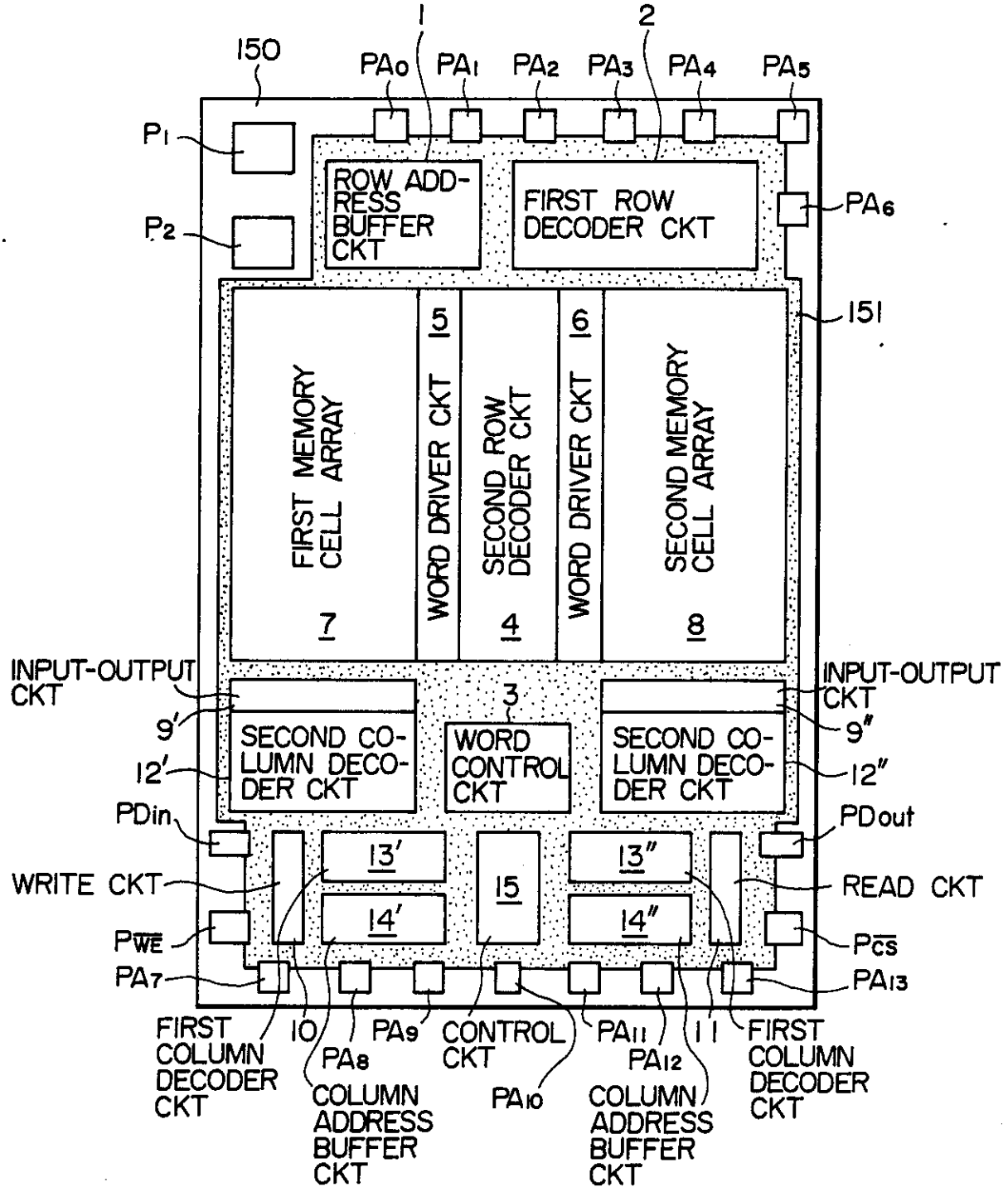

150
1
2
PA0
PA1
PA2
PA3
PA4
PA5
P1
P2
ROW ADDRESS BUFFER CKT
FIRST ROW DECODER CKT
PA6
151
FIRST MEMORY CELL ARRAY
7
5
WORD DRIVER CKT
SECOND ROW DECODER CKT
4
6
WORD DRIVER CKT
SECOND MEMORY CELL ARRAY
8
INPUT-OUTPUT CKT
9'
12'
SECOND COLUMN DECODER CKT
3
WORD CONTROL CKT
SECOND COLUMN DECODER CKT
INPUT-OUTPUT CKT
9"
12"
PDin
PDout
WRITE CKT
13'
14'
15
13"
14"
READ CKT
PWE
PCS
PA7
PA13
FIRST COLUMN DECODER CKT
10
PA8
PA9
CONTROL CKT
PA10
PA11
PA12
11
FIRST COLUMN DECODER CKT
COLUMN ADDRESS BUFFER CKT
COLUMN ADDRESS BUFFER CKT

FIG. 7A

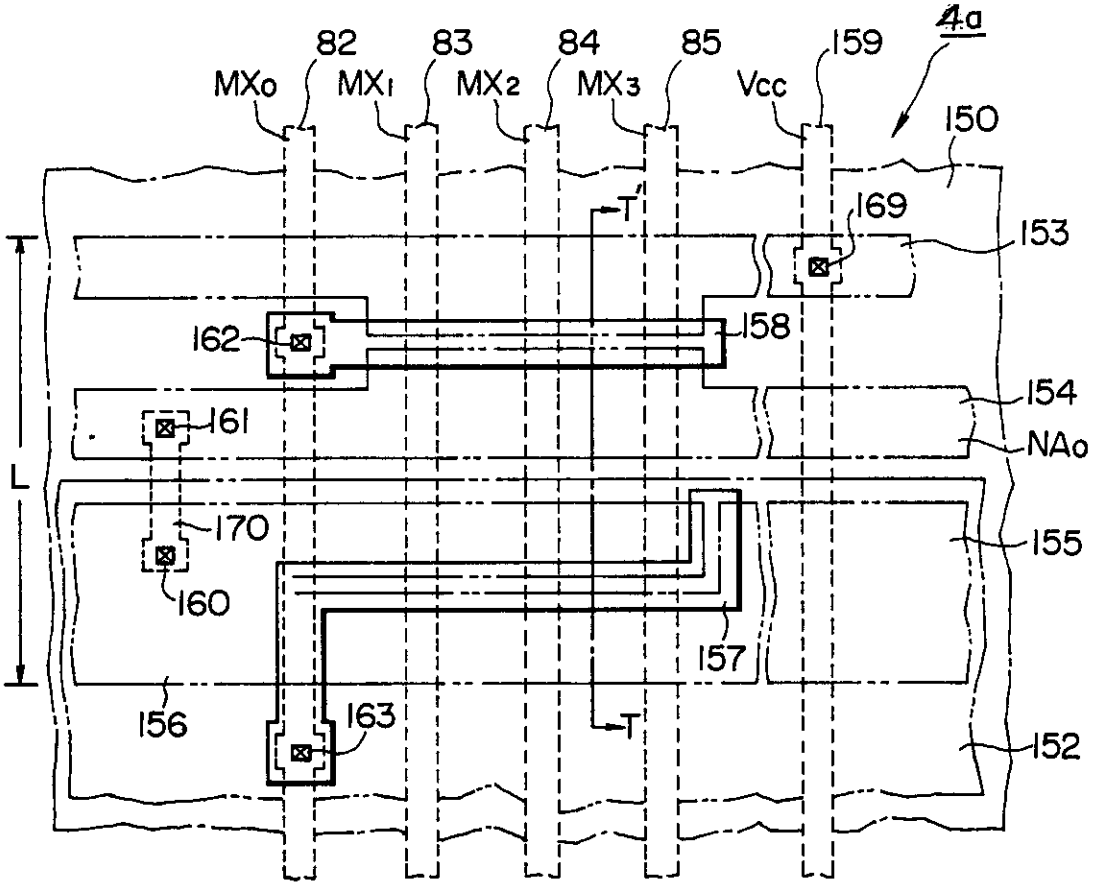

82
83
84
85
159
4a
MXo
MX1
MX2
MX3
Vcc
150
T'
169
153
162
158
154
161
NAo
L
170
155
160
157
156
163
T
152

FIG. 7B

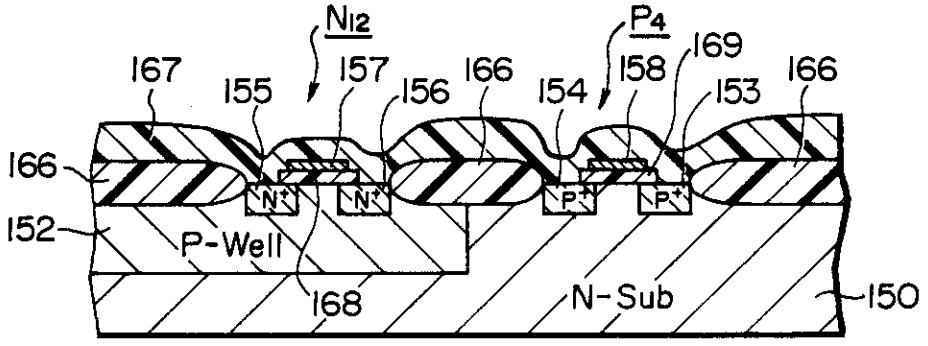

N12
P4
167
155
157
156
166
154
158
169
153
166
166
N+
N+
P+
P+
152
P-Well
168
N-Sub
150

FIG. 8A

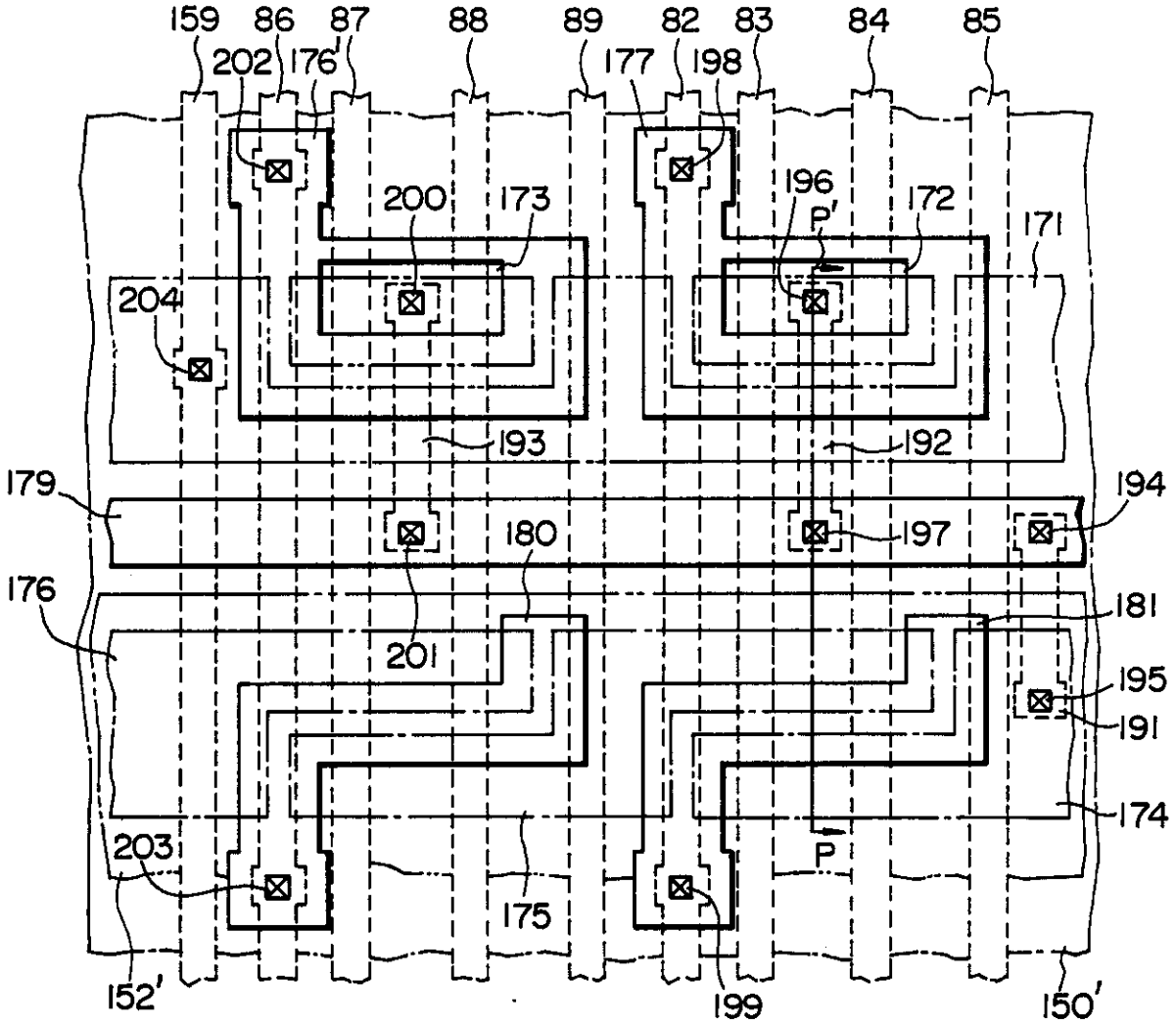

159
86
87
88
89
82
83
84
85
202
176'
177
198
200
173
196
P'
172
171
204
193
192
179
194
180
197
176
181
201
195
191
174
203
P
175
152'
199
150'

FIG. 8B

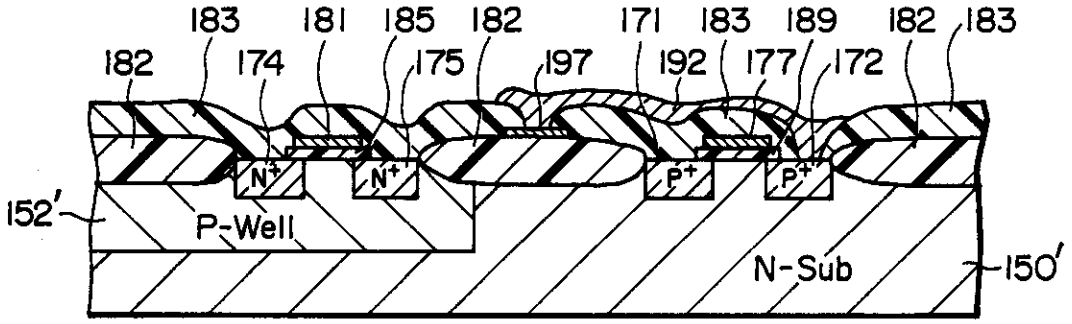

183
181
185
182
171
183
189
182
183
182
174
175
197
192
177
172
N+
N+
P+
P+
152'
P-Well
N-Sub
150'

FIG. 9A

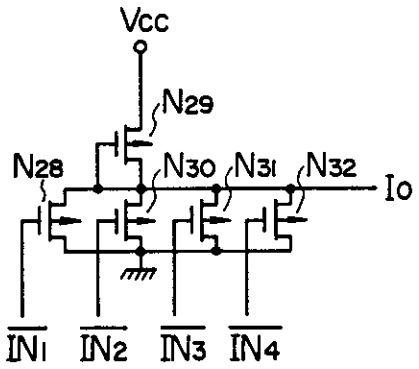


FIG. 9B

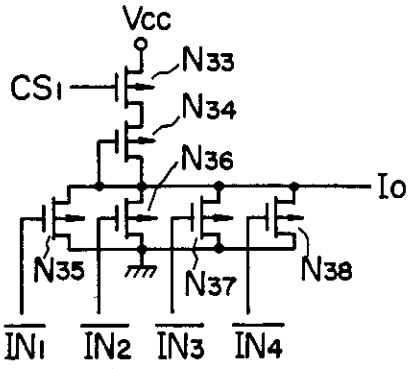


FIG. 9C

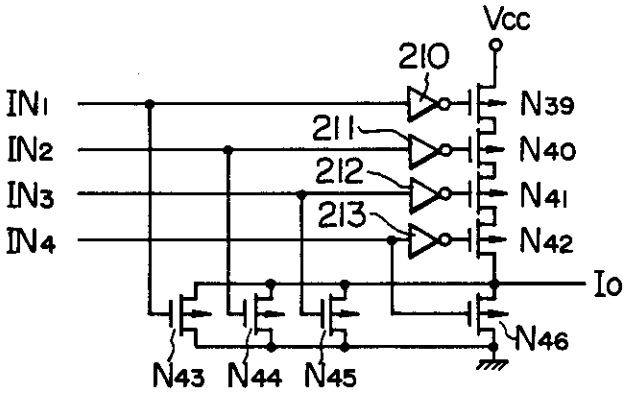


FIG. 10A

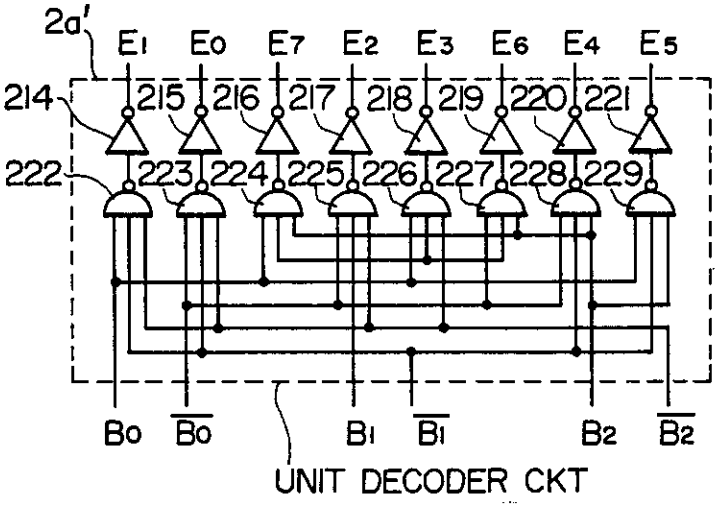
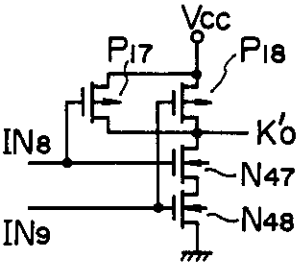


FIG. 10B



"Semiconductor Memory Device".

The present invention relates to a semiconductor memory circuit device (hereinafter referred to as a "memory"), and more particularly to a memory constructed of complementary insulated gate field effect transistors.

In a memory, one of a plurality of memory circuits (hereinafter referred to as "memory cells" or "cells") can be selected on the basis of an output signal of an address decoder circuit.

Usually, the address decoder circuit includes switching elements (for example, insulated gate field effect transistors which shall hereinafter be referred to as "FETs") which are connected in series or in parallel and which are respectively controlled "on" or "off" by address signals.

When the memory is designed to have a large capacity, address signals of an increased number of bits are required. In correspondence with the address signals,

the number of the switching elements connected in series or in parallel within the address decoder circuit is increased.

In this respect, the switching elements cause stray capacitances to various nodes of the circuit and have unnegligible operating resistances in themselves. Therefore, the address decoder circuit including the increased number of switching elements as above stated has its operating speed limited seriously.

The plurality of memory cells constructed as the semiconductor integrated circuit are usually arranged on a substrate such as semiconductor substrate in the shape of a matrix. Unit decoder circuits which constitute the address decoder circuit are arranged in correspondence with the memory cell rows or columns in the matrix arrangement.

In order to effectively utilize the surface of the semiconductor substrate, the unit decoder circuits have to be arranged at pitches corresponding to the pitches of the memory cell rows or memory cell columns.

Nevertheless, the unit decoder circuits including the increased number of switching elements are difficult to arrange at the pitches referred to above.

The increase in the number of switching elements

as above stated signifies also an increase in the area of element regions on the substrate.

The address decoder circuit can be constructed of complementary insulated gate field effect transistors (hereinafter referred to as "complementary FETs) with a view to lowering the power dissipation by reducing the operating current thereof.

However, the address decoder circuit to be constructed of the complementary FETs requires a much larger number of switching elements in comparison with an address decoder circuit as is constructed of only FETs of the single channel type. It is therefore desirable that the operating speed, the pitch, and the area as above stated are especially considered for the address decoder circuit which is constructed of the complementary FETs.

According to one aspect of the present invention there is provided a semiconductor memory circuit device including:

(a) a memory cell array comprising a plurality of memory cells arranged in rows and columns;

(b) first means for receiving input row address signals, each of which comprises a predetermined number of bits, said first receiving means providing an output of at least first partial row address signals, each of which comprises a portion of said predetermined number of bits of a corresponding input row address signal;

(c) a first row decoder circuit comprising a plurality of first unit row decoders, each of which receives said first partial row address signals from said first receiving means and provides intermediate first decoded signals of said first partial address signals, each of said first unit row decoders consisting of a NAND circuit;

(d) a plurality of first inverters;

(e) a second row decoder circuit comprising a plurality of second unit row decoders, each of which selectively receives said first intermediate decoded signals through said first inverters and provides an output decoded signal for selecting a row from said memory cell array, each of said second unit row decoders consisting of a NAND circuit;

(f) a word driver circuit connected between the output of said second row decoder circuit and said memory cell array;

(g) second means for receiving input column address signals, each of which comprises a predetermined number of bits, said second receiving means providing an output of at least first partial column address signals, each of which comprises a portion of said predetermined number of bits of a corresponding input column address signal;

(h) a first column decoder circuit comprising a plurality of first unit column decoders, each of which receives said first partial column address signals from said second receiving means and provides second intermediate decoded signals of said first partial column address signals, each of said first unit column decoders consisting of a NOR circuit;

(i) a plurality of second inverters; and

(j) a second column decoder circuit comprising a plurality of second unit column decoders, each of which selectively receives said second intermediate decoded signals through said second inverters and provides output decoded signals for selecting a column of said memory array, each of said second unit column decoders consisting of a NOR circuit.

According to a second aspect of the present invention there is provided a semiconductor memory circuit device including:

(a) a memory cell array comprising a plurality of memory cells arranged in rows and columns;

(b) first means for receiving input row address signals, each of which comprises a predetermined number of bits, said first receiving means providing an output of row address signals;

(c) a row decoder circuit which receives said row address signals from said first receiving means and provides output decoded signals for selecting a row from said memory cell array, said row decoder circuit consisting of a plurality of NAND circuits;

(d) a word driver circuit connected between the output of said row decoder circuit and said memory array;

(e) second means for receiving input column address signals, each of which comprises a predetermined number of bits, said second receiving means providing an output of column address signals; and

(f) a column decoder circuit which receives said column address signals from said second receiving means and provides output decoded signals for selecting a column of said memory array, said column decoder circuit consisting of a plurality of NOR circuits.

The present invention will now be described in greater detail by way of examples with reference to the accompanying drawings, wherein:-

Figure 1 is a block diagram of one preferred form of semiconductor memory device;

Figure 2 is a circuit diagram of memory cell arrays and input/output circuits of the memory device shown in Figure 1,

Figure 3A is a circuit diagram of the row address buffer circuit and the first row decoder circuit;

Figure 3B is a circuit diagram of the second row decoder circuit and a word drive circuit;

and;

Figure 3C is a circuit diagram of the inverter circuit, all being parts of the memory device shown in Figure 1;

Figure 4A is the column address buffer circuit and the first column decoder circuit;

Figures 4B and 4C are circuit diagrams each showing the second column decoder circuit, all being parts of the memory device shown in Figure 1;

Figure 5 is a circuit diagram of the word

control circuit of the memory device shown in Figure 1;

Figure 6 is a layout diagram on the substrate of the semiconductor memory device shown in Figure 1;

Figure 7A is a plan view of the circuit elements which constitute a decoder circuit;

Figure 7B is a sectional view of the substrate taken along the line T - T' in Figure 7A;

Figure 8A is a plan view of circuit elements which constitute another decoder circuit;

Figure 8B is a sectional view of the substrate taken along the line P - P' in Figure 8A;

Figures 9A, 9B and 9C are circuit diagrams each showing alternative forms of the second decoder circuit;

Figure 10A is a circuit diagram of an alternative form of the first decoder circuit; and

Figure 10B is a circuit diagram of yet a further form of the second decoder circuit.

Referring first to Figure 1, the semiconductor memory device includes: row and column address buffer circuits 1 and 14 respectively; first row and column decoder circuits 2 and 13 respectively; second row and column decoder circuits 4 and 12 respectively; word driver circuits 5 and 6; first and second memory cell arrays 7 and 8 respectively; and a word control circuit 3.

The respective circuit blocks referred to above will be described in greater detail later with reference to Figures 2 to 6. The memory circuit also includes an input/output circuit 9, a write circuit 10, a read circuit 11, and a control circuit 15.

The control circuit 15 receives a chip select signal and a write control signal at a chip select terminal $\overline{CS}$ and a write control terminal $\overline{WE}$ respectively, and thereby provide terminals CS_1 and $\overline{CS}_2$, C_W and C_R with control signals for controlling the operations of the word control circuit 3, the write circuit 10 and the read circuit 11 respectively.

In order to establish a memory capacity of 16 kilobits, each of the memory cell arrays 7 and 8 is constructed of 8,192 static memory cells. In practice it consists of 8,192 bits arranged into a matrix of 128 rows and 64 columns.

Each memory cell is constructed so as to have select terminals and data input/output terminals as shown in Figure 2.

The respective select terminals of a plurality of memory cells arranged in an identical row are connected in common to one word line, whilst the respective data input/output terminals of a plurality

of memory cells arranged in an identical column are connected in common to data lines.

Accordingly, each of the memory cell arrays 7 and 8 has 128 word lines and 64 pairs of data lines.

The word lines W_0 to W_{127} of the memory cell array 7 are selected by the word driver circuit 5, whilst the word lines W_0' to W_{127}' of the memory cell array 8 are selected by the word driver circuit 6.

The data line pairs Y_0, $\overline{Y_0}$ to Y_{63}, $\overline{Y_{63}}$ and Y_{64}, $\overline{Y_{64}}$ to Y_{127}, $\overline{Y_{127}}$ of the respective memory cell arrays 7 and 8 are selected by the input/output circuit 9.

Address signals for selecting the word lines W_0 to W_{127} and W_0' to W_{127}' are supplied to terminals A_0 to A_6 of the row address buffer circuit 1, whilst address signals for selecting the data line pairs, Y_0, $\overline{Y_0}$ to Y_{127}, $\overline{Y_{127}}$ are supplied to terminals A_7 to A_{13} of the column address buffer circuit 14.

The row address buffer circuit 1 receives the address signals of 7 bits supplied to the terminals A_0 to A_6 (hereinbelow, written in the manner of address signals A_0 to A_6), and thereby outputs non-inverted address signals B_0 to B_6 and inverted address signals $\overline{B_0}$ to $\overline{B_6}$.

Amongst the 7-bit address signals provided from the row address buffer circuit 1, the address signals of

6 bits, or B_0, $\overline{B_0}$ to B_5, $\overline{B_5}$ are supplied to the first row decoder circuit 2, and the address signal of the remaining 1 bit, or B_6, $\overline{B_6}$ is supplied to the word control circuit 3.

The first decoder circuit 2 receives the address signals B_0, $\overline{B_0}$ to B_5, $\overline{B_5}$ and thereby provides decoded signals MX_0 to MX_{11}.

The decoded signals MX_0 to MX_{11} are made signals which are respectively obtained by the combinations of specified ones among the 6-bit address signals B_0, $\overline{B_0}$ to B_5, $\overline{B_5}$.

For example, the address signals B_0, $\overline{B_0}$ to B_5, $\overline{B_5}$ are divided by means of the first decoder circuit 2 into three groups each consisting of 2 bits, and they are decoded in group unit.

The decoded signals MX_0 to MX_{11} are called "intermediate signals" because they are signals obtained at an intermediate stage in the course of finally obtaining decoded signals which are in one-to-one correspondence with the states of the address signals B_0, $\overline{B_0}$ to B_5, $\overline{B_5}$.

The second row decoder circuit 4 receives the intermediate signals delivered from the first row decoder circuit 2, and thereby provides decoded signals K_0 to K_{63}.

The respective decoded signals K_0 to K_{63} are in

one-to-one correspondence with the states of the 6 bits of the address signals B_0, $\overline{B_0}$ to B_5, $\overline{B_5}$.

Since each of the intermediate signals MX_0 to MX_{11} is formed by the logical operation of the 2-bit address signals as described above, each of the decoded signals K_0 to K_{63} can be formed by decoding 3 bits amongst the 12-bit intermediate signals.

The decoded signals K_0 to K_{63} delivered from the second row decoder circuit 4 are supplied to the word driver circuits 5 and 6. The word driver circuits 5 and 6 are controlled by the word control circuit 3.

The word control circuit 3 receives the address signals B_6 and $\overline{B_6}$ delivered from the address buffer circuit 1, the control signals CS_1 and $\overline{CS_2}$ delivered from the control circuit 15, and address signals B_7 and $\overline{B_7}$ delivered from the address buffer circuit 14, and thereby provides control signals L_0, L_1 and L_2 to be supplied to the word driver circuit 5, and control signals R_0, R_1 and R_2 to be supplied to the word drive circuit 6.

The word driver circuit 5 is constructed so as to provide word signals for selecting the 128 word lines of the memory cell array 7 on the basis of the 64-bit decoded signals provided from the second row decoder circuit 4 and the control signals provided from the word

control circuit 3.

Similarly, the word drive circuit 6 is constructed so as to deliver 128 word signals to the word lines W_0' to W_{127}' under the control of the control of the control signals R_0, R_1 and R_2.

In the case where a single decoder circuit is used instead of the above described first and second decoder circuits, each of unit decoder circuits which constitute the single decoder circuit must decode the 6-bit address signals B_0, $\overline{B_0}$ to B_5, $\overline{B_5}$.

In contrast, in the case of the construction shown in Figure 1, each of the unit decoder circuits which constitute the first decoder circuit 2 may decode only 2-bit address signals, and each of the unit decoder circuits which constitute the second decoder circuit 4 may decode only the 3-bit intermediate signals as stated above.

Thus, the number of switching elements to be incorporated in a section extending from the address signal input terminals to the input end of the word drive circuit can be reduced. In addition, the number of all the switching elements which constitute the first and second decoder circuits can be reduced.

In the case where the address signals are

substantially decoded by the word driver circuits 5 and 6 as in Figure 1, the number of the unit decoder circuits which constitute the second decoder circuit 4 can be made smaller with respect to the number of the word lines of the memory cell arrays 7 and 8.

The column address buffer circuit 14 is constructed similarly to the row address buffer circuit 1, and responds to the input address signals A_7 to A_{13} to provide non-inverted address signals B_7 to B_{13} and inverted address signals $\overline{B_7}$ to $\overline{B_{13}}$.

The first column decoder circuit 13 receives the address signals of 6 bits, or B_7 to B_{12} and $\overline{B_7}$ to $\overline{B_{12}}$ amongst the address signals of 7 bits, and provides intermediate signals MY_0 to MY_{11} on the basis of these address signals.

The second column decoder circuit 12 receives the intermediate signals MY_0 to MY_{11} and the address signals B_{13} and $\overline{B_{13}}$, and provides decoded signals I_0 to I_{127}.

The decoded signals I_0 to I_{127} have one signal which corresponds to the address signals B_7 to B_{13} and and $\overline{B_7}$ to $\overline{B_{13}}$, at a high level and the others at a low level.

The input/output circuit 9 includes a pair of

common data lines, and column select circuits (not shown) which are connected between the common data lines and the data lines of the memory cell arrays 7 and 8 and which are respectively controlled "on" or "off" by the output signals I_0 to I_{127} of the second column decoder circuit 12. If necessary, the input/output circuit 9 may further include a sense amplifier (not shown) which receives signals from the common data lines.

The write circuit 10 has a non-inverting output terminal D_i and an inverting output terminal $\overline{D_i}$ which are coupled to the common data lines of the input/output circuit 9.

The write circuit 10 has its operation controlled by the control signal C_W. When the control signal C_W is at a writing operation level, the write circuit 10 provides the output terminals D_i and $\overline{D_i}$ with a non-inverted signal and an inverted signal corresponding to a signal applied to an input terminal D_{in}, respectively. When the control signal C_W is at a non-writing operation level, the output terminals D_i and $\overline{D_i}$ are brought into floating states.

The read circuit 11 has its operation controlled by the control signal C_R. When the control signal C_R is at a reading operation level, the read circuit 11

provides a signal corresponding to an output signal from the input/output circuit 9. When the control signal C_R is at a non-reading operation level, and output terminal of the read circuit 11 is brought into a floating state.

The word lines of the memory cell arrays 7 and 8 are selected by the word driver circuits 5 and 6, and the data lines thereof are selected by the input/output circuit 9.

Accordingly, only one memory cell in the memory cell array 7 or 8 as selected through the word line and the data line is coupled to the common data line within the input/output circuit 9.

During the process of reading information, the signal level of the common data line as determined by the stored information of the selected memory cell is amplified by the sense amplifier within the input/output circuit 9, and an output signal from the sense amplifier is read out by the read circuit 11.

During the process of writing information, the signal level of the common data line within the input/output circuit 9 is determined by the write circuit 10, and the signal of the common data line is supplied to the memory cell through the selected data line. As a result, a signal provided from the write circuit 10 is

stored in the selected memory cell.

The various circuit blocks above mentioned are formed on a single semiconductor substrate by known semiconductor integrated circuit techniques.

In that case, the terminals A_0 to A_{13}, D_{in}, D_{out}, $\overline{CS}$ and $\overline{WE}$ and power supply terminals V_{CC} and GND are formed as external terminals of a semiconductor integrated circuit device (IC).

Examples of specific circuits used in the respective circuit blocks will now be described in greater detail.

The semiconductor memory circuit described above is especially suited to a memory constructed of complementary FETs. Accordingly, the circuits which are described hereinafter are mainly constructed of complementary FETs.

Referring now to Figure 2, the memory cell arrays 7 and 8 include memory cells in the matrix arrangement 100 to 103, and 104 to 107; word lines W_0 and W_1, and W_0' and W_1'; pairs of data lines Y_0, $\overline{Y_0}$ and Y_1, $\overline{Y_1}$, and Y_{64}, $\overline{Y_{64}}$ and Y_{65}, $\overline{Y_{65}}$; and FETs N_1 and N_2 for data line loads; respectively.

All the memory cells have the same construction. As illustrated in detail with respect to the memory cell

104, each memory cell comprises N-channel type FETs N_7 and N_8, load resistors R_1 and R_2 which are formed by high-resistivity polycrystalline silicon layers, the FETs and the resistors constituting a flip-flop circuit, and N-channel type FETs N_5 and N_6 for transfer.

The memory cell employing load resistances which are formed by the high-resistivity polycrystalline silicon layers can be formed on a relatively small area on the semiconductor substrate in comparison with the memory cell which consists of complementary FETs. Each memory cell can be made to have a sufficiently low power dissipation by designing the load resistors to have high resistance values. The memory cells comprise single channel type FETs as stated above in spite of the fact that the other circuits to be described later comprise complementary FETs.

The gate electrodes of the transfer FETs N_5 and N_6 constitute the select terminals of the memory cell. The output electrode of each of the transfer FETs N_5 and N_6 constitutes the input or output terminal of the memory cell.

As shown in the memory cell arrays 7 and 8, the select terminals of the memory cells which are arranged in an identical row are connected in common to

one word line, and the respective pairs of input/output terminals of the memory cells which are arranged in an identical column are connected to one pair of data lines.

Each data line is connected to the source electrode of the N-channel type FET N_1 or N_2, the gate and drain electrodes of which are connected to the power supply terminal V_{CC}.

The input/output circuit 9 includes N-channel type FETs N_3 and N_4 which constitute the column select circuits, the common data lines D_i and $\overline{D_i}$, the sense amplifier 120 and the output line D_{OU}.

The respective data line pairs of the memory cell arrays 7 and 8 are coupled to the common data lines D_i and $\overline{D_i}$ through the corresponding FETs N_3 and N_4.

The gate electrodes of the FETs N_3 and N_4, which are connected in common and which correspond to each data line pair are coupled to the corresponding output terminal of the second decoder circuit 12 (see Figure 1).

The common data lines D_i and $\overline{D_i}$ are connected to a pair of input terminals of the preamplifier 120 and the pair of output terminals of the write circuit 10 (see Figure 1).

An output terminal of the sense amplifier 120 is connected to the output line D_{OU}.

In the memory cell arrays 7 and 8, each word line is selected by the high level of the signal because the transfer FETs in the memory cell are of the N-channel type. Each data line pair is selected by the high level of the signal delivered from the second decoder circuit 12.

Referring now to Figure 3A, the address buffer circuit 11 includes unit buffer circuits 1a to 1g which correspond to the terminals A_0 to A_6 respectively. As shown with respect to the unit buffer circuit 1a, each unit buffer circuit comprises two inverter circuits IV_1 and IV_2 which are connected in cascade.

As shown in Figure 3C, each of the inverter circuit IV_1 and IV_2 comprises a P-channel type FET P_0 and an N-channel type FET N_0, the drain electrodes of which are connected in common to an output terminal OUT and the gate electrodes of which are connected in common to an input terminal IN. Although no illustration is or will be made in Figure 2 and the succeeding drawings for the sake of clarity, as shown in Figure 3C, the body gate S_1 of the P-channel type FET P_0 is connected to the power supply terminal V_{CC} and the body gate S_2 of the N-channel type FET N_0 is connected to the other power supply terminal GND.

The first decoder circuit 2 comprises unit decoder

circuits 2a to 2l each of which receives divided partial address signals of 2 bits in order to provide the intermediate signal.

Every four of the unit decoder circuits constitute one group of circuits in correspondence with the partial address signals. The groups of unit decoder circuits 2ad to 2il are identical to one another. Accordingly, in Figure 3A, only the circuit arrangement of the group of unit decoder circuits 2ad is shown in detail.

In the group of unit decoder circuits 2ad, the unit decoder circuit 2a comprises a complementary type NAND circuit which consists of P-channel type FETs P_1 and P_2 and N-channel type FETs N_9 and N_{10}, and a complementary type inverter circuit which consists of a P-channel type FET P_3 and an N-channel type FET N_{11} and which receives an output signal of the NAND circuit.

In the case where at least one of output signals $\overline{B_0}$ and $\overline{B_1}$ of the unit buffer circuits 1a and 1b is at the low level, at least one of the P-channel type FETs P_1 and P_2 connected in parallel is brought into its "on" state and at least one of the N-channel type FETs N_9 and N_{10} connected in series is brought into its "off" state, so that the output signal of the NAND circuit is

at the high level.

When both the signals $\overline{B_0}$ and $\overline{B_1}$ are at the high level, the output signal of the NAND circuit is at the low level. The inverter circuit provides a signal inverted with respect to the output signal of the NAND circuit.

In the NAND circuit, the varying rate of its output signal is limited by stray capacitances (not shown) existing between nodes NA_0 and NA_1 of the circuit and the earth point of the circuit and the "on" resistances of the respective FETs. Whereas the P-channel type FETs P_1 and P_2 are connected in parallel, the N-channel type FETs N_9 and N_{10} are connected in series, so that the rate of fall of the output signal is substantially limited as compared with the rate of rise. As shown, only the two N-channel FETs are connected in series as stated above, so that the rate of fall of the output signal can be made comparatively high.

In similar manner to the unit decoder circuit 2a, each of the unit decoder circuits 2b to 2d comprises a NAND circuit and an inverter circuit of the complementary type.

The unit decoder circuits 2a to 2d provide the intermediate signals MX_0 to MX_3 satisfying the following expressions (1) to (4) in response to the signals B_0, $\overline{B_0}$,

B_1 and $\overline{B_1}$ formed on the basis of the partial address signals A_0 and A_1, respectively:

$$MX_0 = \overline{B_0} \cdot \overline{B_1} \quad \ldots\ldots\ldots (1)$$

$$MX_1 = B_0 \cdot \overline{B_1} \quad \ldots\ldots\ldots (2)$$

$$MX_2 = \overline{B_0} \cdot B_1 \quad \ldots\ldots\ldots (3)$$

$$MX_3 = B_0 \cdot B_1 \quad \ldots\ldots\ldots (4)$$

In similar manner, the unit decoder circuits 2e to 2h, and 2i to 2l provide the intermediate signals MX_4 to MX_7, and MX_8 to MX_{11} on the basis of the partial address signals, respectively.

Each group of unit decoder circuits responds to the four signals from the two unit buffer circuits, to provide the same number of intermediate signals.

In the case where, as described above, the address signals are divided into the partial address signals each consisting of 2 bits and are decoded every partial address signal, the number of the unit decoder circuits can be made comparatively small. The number of types of the intermediate signals to be supplied to the second decoder circuit 4 can be reduced accordingly.

Referring to Figure 3B, the second decoder circuit 4 comprises 64 unit decoder circuits 4a to 4x, whilst the word drive circuit 5 comprises 128 unit drive circuits

5a to 5y.

The Unit decoder circuits 4a to 4x are all identical to one another. Each of the unit decoder circuits 4a to 4x comprises a complementary NAND circuit which consists of P-channel type FETs P_4 to P_6 and N-channel type FETs N_{12} to N_{14}.

Each of the unit decoder circuits 4a to 4x has three input terminals. The input terminal which is connected to the gate electrodes of the pair of FETs P_4 to N_{12}, is supplied with one of the intermediate signals MX_0 to MX_3, the input terminal which is connected to the gate electrodes of the pair of FETs P_5 and N_{13} is supplied with one of the intermediate signals MX_4 to MX_7, and the input terminal which is connected to the gate electrode of the remaining pair of FETs P_6 and N_{14} is supplied with one of the intermediate signals MX_8 to MX_{11}.

The unit decoder circuits 4a to 4x are constructed so as to selectively receive the three types of intermediate signals, and are thereby brought into one-to-one correspondence with the respective states of the 6-bit address signals (A_0 to A_5).

For example, the unit decoder circuit 4a is constructed so as to receive the intermediate signals MX_0, MX_4 and MX_8, whereby when all the 6-bit address

signals A_0 to A_5 are at the low level, this unit decoder circuit responds in order to provide a signal K_0 at the low level.

Owing to circuit connections as shown in the figure, the output signal of each of the unit decoder circuits 4a to 4x is supplied to the corresponding two unit driver circuits.

Each unit driver circuit also receives control signals L_0 to L_2 from the word control circuit 3.

The control signal L_0 is brought into the low level in response to the situation that the control signal $\overline{CS_2}$ provided from the control circuit has been brought to the low level in correspondence with the low level of the chip select signal $\overline{CS}$ and that the signal B_7 provided from the address buffer circuit 14 has been brought to the low level. The control signal L_1 is brought into the high level when the control signal CS_1 provided from the control circuit 15 has been brought to the high level in response to the low level of the chip select signal $\overline{CS}$ and the signals $\overline{B_6}$ and $\overline{B_7}$ provided from the address buffer circuits 1 and 13 have also been brought to the high level. The control signal L_2 is brought into the high level when the control signal CS_1 has been brought to the high level and the signals B_6

and $\overline{B_7}$ have also been brought to the high level.

In Figure 3B, the respective unit driver circuits 5a to 5y are operated by the outputs of the corresponding unit decoder circuits 4a to 4x when the chip select signal $\overline{CS}$ and the column address signal B_7 are at the low level.

One of the pair of unit driver circuits 5a and 5b is operated substantially by the row address signal $\overline{B_6}$ or B_6.

By way of example, in the case where the output signal K_0 of the unit decoder circuit 4a is at the low level in correspondence with the low level of the address signals A_0 to A_5 as stated above, if the row address signal $\overline{B_6}$ is at the high level, the control signal L_1 is brought to the high level and the control signal L_2 to the low level in response to the signal $\overline{B_6}$. The unit driver circuit 5a provides a word signal W_0 at the high level because a FET P_7 is brought into its "on" state and FETs N_{15} to N_{17} are brought into their "off" states. The unit driver circuit 5b provides a word signal W_1 at the low level because the control signal L_2 is brought to the low level and the FET N_{16} is brought into its "on" state.

On the other hand, if the row address signal B_6

is brought to the high level, the word signal W_1 of the unit driver circuit 5b is brought to the high level in response thereto.

As illustrated in Figure 1, the output signals of the second decoder circuit 4 are supplied to the word driver circuits 5 and 6 in common. Although not shown, the construction of the word driver circuit 6 for the memory cell array 8 is similar to that of the word driver circuit 5.

The word driver circuit 5 is operated by the output signal of the second decoder circuit 4 when the chip select signal $\overline{CS}$ and the column address signal B_7 are at the low level as stated above. On the other hand, the word driver circuit 6 is operated by the output signal of the second decoder circuit 4 when the column address signal $\overline{B_7}$ is at the low level and the chip select signal $\overline{CS}$ is at the low level. The column address signal $\overline{B_7}$ is the phase-inverted signal of the column address signal B_7. Accordingly, in correspondence with the level of the column address signal B_7, the word driver circuit 5 or the word driver circuit 6 is operated by the output signal of the second decoder circuit 4. Therefore, the word lines of the memory cell arrays 7 and 8 can be selected through the address signals A_0 to A_6 by means of the single common

second decoder circuit 4 which is associated with these memory cell arrays 7 and 8.

Owing to the construction, the number of the unit decoder circuits in the second decoder circuit can be reduced by half with respect to the number of word signals required in the memory cell arrays.

In each of the unit decoder circuits constituting the second decoder circuit, the number of the FETs in series connection which act as a limit to the operating speed of the circuit is reduced as in the case of the unit decoder circuit of the first decoder circuit.

In Figure 3A, each of the complementary type inverter circuits IV_1 and IV_2 constituting the unit buffer circuit is allowed to drive only two pairs of FETs. Therefore, the inverter circuits IV_1 and IV_2 can be constructed so as to drive comparatively light loads.

Similarly , each of the unit decoder circuits constituting the first decoder circuit may drive a comparatively small number of pairs of FETs constituting the second decoder circuit.

As a result, the circuits in Figures 3A and 3B can be made comparatively small in size and can be operated at high speed.

Referring now to Figure 4A, the address buffer circuit 14 comprises unit buffer circuits 14a to 14g. In similar manner to the unit buffer circuit shown in Figure 3A, each of the unit buffer circuits consists of complementary type inverter circuits IV_1 and IV_2 connected in series.

As shown, the first column decoder circuit 13 comprises twelve unit decoder circuits 13a to 13l.

The unit decoder circuits 13a to 13l have constructions similar to one another. Each unit decoder circuit 13a to 13l comprises a complementary type NOR circuit consisting of P-channel type FETs P_8 and P_9 and N-channel type FETs N_{18} and N_{19}, and a complementary type inverter circuit which comprises a P-channel type FET P_{10} and an N-channel type FET N_{20} and which receives an output signal from the NOR circuit.

The unit decoder circuits 13a to 13d constitute a first group of unit decoder circuits 13ad, and they provide the intermediate signals MY_0 to MY_3 responsive to partial address signals A_7 and A_8 of 2 bits respectively.

Owing to a circuit arrangement as shown in the figure, the intermediate signals MY_0 to MY_3 fulfill relations of the following expressions (5) to (8) respectively:

$$MY_0 = \overline{B_7} + \overline{B_8} \quad \ldots\ldots (5)$$

$$MY_1 = B_7 + \overline{B_8} \quad \ldots\ldots (6)$$

$$MY_2 = \overline{B_7} + B_8 \quad \ldots\ldots (7)$$

$$MY_3 = B_7 + B_8 \quad \ldots\ldots (8)$$

Similarly, groups of unit decoder circuits 13 eh and 13 il provide the intermediate signals MY_4 to MY_7, and MY_8 to MY_{11} in response to the partial address signals respectively.

The respective intermediate signals MY_0 to MY_{11} and output signals B_{13} and $\overline{B_{13}}$ of the unit buffer circuit 14g are supplied to the second column decoder circuit 12 in Figure 4B.

The second decoder circuit 12 comprises 128 unit decoder circuits 12a to 12u.

As shown in Figure 4B, each of the unit decoder circuits 12a to 12u comprises a complementary NOR circuit which consists of P-channel type FETs P_{11} to P_{14} and N-channel type FETs N_{21} to N_{24}.

The unit decoder circuits 12a to 12u are respectively supplied with four types of signals which consist of one signal selected from the signals B_{13} and $\overline{B_{13}}$, one signal selected from the intermediate signals MY_0 to MY_3, one signal selected from the intermediate signals MY_4 to MY_7 and one signal selected from the intermediate

signals MY_8 to MY_{11}.

As stated above, the data line of the memory cell array is selected by the signal at the high level from the second decoder circuit 12.

Accordingly, the four types of signals to be supplied to the respective unit decoder circuits are selected so that signals from desired unit decoder circuits may be brought to the high level in one-to-one correspondence with desired combinations of the levels of the respective input address signals A_7 to A_{12}.

For example, the unit decoder circuit 12a provides a data line select signal I_0 at the high level when all the signals MY_0, MY_4, MY_8 and B_{13} have been brought to the low level, that is, when all the address signals A_7 to A_{13} have been brought to the low level.

By means of the first decoder circuit 13, the number of FETs of the second decoder circuit 12 can be reduced and the operating speed of the second decoder circuit 12 can be increased for the same reasons as given in the case of the decoders shown in Figures 3A and 3B.

In contrast, in the case where the first decoder circuit 13 is not provided, one pair of P-channel type FET and N-channel type FET are required for each input address signal in the unit decoder circuit in the second decoder

circuit. Accordingly, the unit decoder circuit requires as many as 7 pairs of FETs, i.e. 14 FETs for the input address signals A_7 to A_{13}.

In this example, the input address signal A_{13} has no input address signal to be combined therewith. For this reason, the address signals B_{13} and $\overline{B_{13}}$ generated on the basis of the input address signal A_{13} are transmitted to the second decoder circuit as described above. Thus, the number of input lines necessary for the second decoder circuit 12 may be fourteen. This number is equal to the number of input lines of the decoder circuit at the time when the first decoder circuit 13 is not provided.

Instead of the above measure, the 3 bits of the input address signals A_{11}, A_{12} and A_{13} could be used as partial address signals and be decoded in order to constitute the intermediate signals which are supplied to the second decoder circuit. In this way, the number of FETs in each of the unit decoder circuits constituting the second decoder circuit can be reduced by 2.

The reduction of the number of the FETs of the second decoder circuit as above described results in reducing the number of P-channel type FETs which are connected between the power supply terminal V_{CC} and the output in the second decoder circuit. Accordingly, in such a case

where all the P-channel type FETs P_{11} to P_{14} are brought into their "on" states, the "on" resistances of the FETs existing between the power supply V_{CC} and the output node decrease. In consequence, the drivability of the second decoder circuit for its load increases, and/the time taken to change the signal from the low level to the high level can be reduced.

Moreover, the number of gate electrodes of the FETs to be connected to the input lines of the second decoder circuit 12 becomes 64, which is one half of the number of gate electrodes of the FETs to be connected to the lines of the decoder in the case where the first decoder 13 is not provided. In other words, the load on the first decoder is reduced. Accordingly, the operating speed of the first decoder circuit can be increased. In addition, since the load on each buffer circuit is only the first decoder circuit, the operating speed thereof can be increased.

Referring now to Figure 5, the word control circuit 3 comprises NANDs 150 to 153, NORs 154 to 155, and inverters 156 to 161. Each of the circuits consists of complementary FETs.

The control signals L_0 and R_0 which are provided from the word control circuit 3 are generated in order to

select either the first memory cell array 7 or the second memory cell array 8 as described above. Accordingly, while either memory cell array is selected by the control signals, the other memory cell array is non-selected. This eliminates the increase of power dissipation in the non-selected memory cell array.

In the memory cell arrays 7 and 8, the load FETs N_1 and N_2 are connected to the respective data lines as shown in Figure 2. The load FETs have relatively low impedances as compared with the resistances within the memory cells.

In the case where, in the memory cell array having no memory cell to be selected, the word line has been brought to the high level, the transfer FETs N_5 and N_6 of the memory cell are brought into the "on" states by the high level of this word line.

As a result, a comparatively large current is caused to flow to the FET N_7 or N_8 of the memory cell through the load FET N_1 or N_2 and the transfer FET N_5 or N_6.

All the word lines in the memory cell array which includes no memory cell to be selected are kept intact at the low level by the control signal L_0 or R_0. Accordingly, the current as above stated is inhibited from

flowing to the memory cell in this memory cell array, so that an increase in the power dissipation is prevented.

The respective circuits can be formed on a single substrate in an arrangement which makes the size of the substrate smaller.

Figure 6 shows patterns of the respective circuit blocks which are formed on a single semiconductor substrate 150. The second decoder circuit 4 is formed on substantially the central part of the surface of the substrate 150. The word driver circuits 5 and 6 are formed holding the second decoder circuit 4 therebetween, and the first memory cell array 7 and the second memory cell array 8 are formed holding them therebetween.

The second decoder circuit 12 is divided into parts 12' and 12", which are respectively formed on the lower sides of the first memory cell array 7 and the second memory cell array 8. The input/output circuit 9 is similarly divided into parts 9' and 9", which are respectively formed between the first memory cell array 7 and the second decoder circuit 12' and between the second memory cell array 8 and the second decoder circuit 12".

The first decoder circuit 13 and the address buffer circuit 14 are similarly divided into parts 13' and 13" and parts 14' and 14", respectively. As shown,

they are formed in those peripheral parts on the surface of the substrate 150 which are spaced from the first and second memory cell arrays 7 and 8 and the second decoder circuit parts 12' and 12". Also the address buffer circuit 1 and the first decoder circuit 2 are formed in those peripheral parts on the surface of the substrate 150 which are spaced from the first and second memory cell arrays 7 and 8, the second decoder circuit 4 and the word driver circuits 5 and 6.

Also the word control circuit 3, the control circuit 15, the write circuit 10 and the read circuit 11 are formed in peripheral parts on the surface of the substrate 150.

Bonding pads PA_0 to PA_{13} for connecting the terminals to receive the input address signals A_0 to A_{13}, to terminals outside the circuit device are arranged in the marginal parts on the surface of the substrate 150. Similarly, bonding pads P_1, P_2, $P\overline{WE}$, $P\overline{CS}$, PD_{in}, PD_{out} for connecting the terminals to receive the voltages, the control signals $\overline{WE}$ and $\overline{CS}$ and the input signal D_{in}, the terminal to provide the signal D_{out}, to terminals outside the circuit device are arranged in the marginal parts on the surface of the substrate 150.

The interconnections between the various circuits and the various bonding pads are made in an interconnection region 151 which is shown stippled.

It is desirable in order to reduce the occupying area of the memory to make the repeated dimensions in the direction of the columns equal to one another, i.e. the pitch of the plurality of cells constituting the memory cell array 7 or 8, the pitch of the unit driver circuits in the driver circuit corresponding to the cells, and the pitch of the unit decoder circuits in the second decoder circuit 4 corresponding to the unit driver circuits. If the pitches of the three constituents are different, interconnections for connecting them will bend, and an increased area will be required for the semiconductor substrate on account of the bent parts. It is therefore necessary to make the respective pitches equal as described above.

By contrasting each memory cell of a comparatively small number of elements of comparatively small size, the pitch of the plurality of memory cells can be made comparatively small.

The unit driver circuits constituting the word driver circuit, and the unit decoder circuits constituting the second decoder circuit include comparatively large numbers of elements of comparatively large size. The

elements and interconnections which constitute the unit driver circuits and the unit decoder circuits are usually arranged so as to conform with the pitch of the memory cells.

The second decoder circuit can be formed at a comparatively small lateral dimension because the number of the elements thereof is reduced as mentioned above.

The memory cell arrays, the word drive circuits and the second decoder circuit are integrated at high density in the memory as stated above, with the result that there is insufficient area available to arrange another circuit such as a peripheral circuit amongst them.

In contrast, comparatively large vacant areas are left amongst the peripheral circuits and near the bonding pads which are arranged around the above referred to circuits.

The first decoder circuit is arranged in the peripheral parts of the substrate 150 as shown. As stated above, this first decoder circuit can be divided into several groups of unit decoder circuits each decoding the 2-bit partial address signals. It can accordingly be arranged by effectively utilizing the peripheral vacant area of the substrate 150, which permits the size of the semiconductor substrate to be reduced.

Figure 7A is a plan view of circuit elements which constitute the unit decoder circuit 4a of the second decoder circuit 4. Figure 7B is a sectional view of part of the semiconductor substrate taken along the line T - T' in Figure 7A. On account of limited space, Figure 7A shows only the P-channel type FET P_6 and the N-channel type FET N_{14} in the unit decoder circuit 4a.

Formed on the substrate 150 are the following : a P-type well region 152; P-type semiconductor regions 153 and 154; N-type semiconductor regions 155 and 156; aluminium interconnection layers 82 to 85 and 159 and 170; conductive polycrystalline silicon layers 157 and 158; and contact holes 160 to 164 for electrically connecting the aluminium interconnection layers and the conductive polycrystalline silicon layers or the aluminium interconnection layers and the semiconductor regions.

The P-channel type FET P_6 consists of the P-type regions 153 and 154 as the source and drain regions thereof and the polycrystalline silicon layer 158 as the gate electrode thereof, whilst the N-channel type FET N_{14} consists of the N-type regions 155 and 156 as the source and drain regions thereof and the polycrystalline silicon 157 as the gate electrode thereof. The P-type region layer 154 is also used as the drain regions of the FETs P_4 and P_5 though this is not shown in Figures 7A and 7B.

The aluminium interconnection layers 82 to 85 are respectively supplied with the intermediate signals MX_0 to MX_3 from the unit decoder circuits 2a to 2d in Figure 3A. The aluminium interconnection layer 82 is connected to the gate electrode 158 of the FET P_6 through the contact hole 162, and is further connected to the gate electrode 157 of the FET N_{14} through the contact hole 163.

The aluminium interconnection layer 159 is connected to the P-type region 153 through the contact hole 164. This aluminium interconnection layer 159 functions to supply the voltage V_{CC} to one output electrode of the P-channel type FET P_6.

The aluminium interconnection layer 170 is connected to the P-type region 154 through the contact hole 161, and is further connected to the N-type region 156 through the contact hole 160. The output signal K_0 is derived through this aluminium interconnection layer 170.

The vertical dimension (pitch) of the unit decoder circuit is represented by L in Figure 7A. It is made equal to the pitch of the plurality of cells in the memory array.

As shown in Figure 7B, the substrate 150 also includes thick insulating films 166 and 167, and gate oxide films 169 and 168 of the P-channel type FET P_6 and the N-channel type FET N_{14} respectively.

In the case where the capacity of the memory is increased by reducing the dimensions of the cells, it is possible to reduce the dimensions of the second decoder circuit in conformity with the cells as stated above. Thus, the area of a chip can be effectively used. The number of FETs which constitute the second decoder circuit can thus be reduced. Consequently, the area per element of the FETs to constitute the second decoder circuit can be increased in correspondence with the occupying area of the reduced FETs.

By increasing the area of the element in this manner, the "on" resistance of the particular FET can be lowered. It is accordingly possible to further raise the operating speeds of the second decoder circuits explained with reference to Figures 3B and 4B.

Figure 8A is a plan view of another unit decoder circuit whilst Figure 8B is a sectional view of a part of the semiconductor substrate taken along the line P - P' in Figure 8A. On account of limited space, Figure 8A only shows the P-channel type FETs P_5 and P_6 and the N-channel

type FETs N_{13} and N_{14}.

Formed on a substrate 150' are the following : a P-type well 152'; P-type semiconductor regions 171, N-type semiconductor regions 174, 175 and 176; 172 and 173;/ Aluminium interconnection layers 82 to 89, 159, 191, 192 and 193; and conductive polycrystalline silicon layers 176', 177 and 179.

The FET P_6 consists of the P-type semiconductor regions 171 and 172 and the conductive polycrystalline silicon layer 177, whilst the FET P_5 consists of the P-type semiconductor regions 171 and 173 and the conductive polycrystalline silicon layer 176'. The FET N_{14} consists of the N-type semiconductor regions 174 and 175 and a conductive polycrystalline silicon layer 181, whilst the FET N_{13} consists of the N-type semiconductor regions 175 and 176 and a conductive polycrystalline silicon layer 180. The aluminium interconnection layer 86 is connected to the layer 176' constituting the gate electrode of the FET P_5 through a contact hole 202, and is further connected to the layer 180 constituting the gate electrode of the FET N_{13} through a contact hole 203. The aluminium interconnection layer 82 is connected to the layer 177 constituting the gate electrode of the FET P_6 through a contact hole 198, and is further connected to the layer

181 constituting the gate electrode of the FET N_{14} through a contact hole 199.

The aluminium interconnection layer 159 is connected to the P-type semiconductor region 171 through a contact hole 204. This aluminium interconnection layer is provided in order to supply the voltage V_{CC} to the P-type semiconductor region 171 which forms one output electrode of each of the FETs P_6 and P_5.

The aluminium interconnection layer 193 serves to electrically connect the P-type semiconductor region 173 forming the other output electrode of the FET P_5, to the conductive polycrystalline silicon layer 179. It is connected to the P-type region 173 and the polycrystalline silicon layer 179 through contact holes 200 and 201 respectively.

The aluminium interconnection layer 192 serves to electrically connect the P-type region 172 forming the other output electrode of the FET P_6, to the polycrystalline silicon layer 179. It is connected to the P-type region 172 and the polycrystalline silicon layer 179 through contact holes 196 and 197 respectively.

The aluminium interconnection layer 191 serves to electrically connect the N-type region 174 and the polycrystalline silicon layer 179. It is connected

to the polycrystalline silicon layer 179 and the N-type region 174 through contact holes 194 and 195 respectively.

The output signal K_0 of the unit decoder circuit is taken from the polycrystalline silicon layer 179.

The substrate 150' also includes as shown in Figure 8B, thick oxide films 182 and 183, the gate oxide film 189 of the FET P_6, and the gate oxide film 185 of the FET N_{14}.

In a modified form, the unit decoder circuit 12 shown in Figure 4B can be replaced with the combination as shown in Figure 4C between a unit decoder circuit 12a' and a unit decoder circuit comprising four sections 12a1 to 12a4, each of which receives an output signal of the unit decoder circuit 12a' and the intermediate signals MY_8 to MY_{11}. In the case of Figure 4C, circuits such as 12a1 can be reduced to one quarter of those shown in Figure 4B.

The various circuits stated above may well consist only of FETs of the single channel type as shown in the alternative form of unit decoder circuit shown in Figure 9A. The unit decoder circuit shown therein consists of N-channel type FETs N_{28} to N_{32}. Thus, the number of elements which constitute the unit decoder circuit can be still further reduced as compared with

the circuit employing complementary FETs.

A further form of unit decoder circuit is shown in Figure 9B which consists of N-channel type FETs N_{33} to N_{38}. In this case, the FET N_{33} is controlled "on" or "off" by the control signal CS_1 from the control circuit 15. It is therefore possible to prevent the unit decoder circuit from dissipating power during the non-selection of the memory.

Yet another form of a unit decoder circuit is shown in Figure 9C which consists of N-channel type FETs N_{39} to N_{46} and inverter circuits 210 to 213. In this case, the power dissipation in the second decoder circuit is reduced by the use of the inverter circuits.

In each of the foregoing alternative forms, the four address signals corresponding to the two input address signals are decoded in the unit decoder circuit of the first decoder circuit, and the intermediate signals obtained by the decoding are decoded again in the unit decoder circuit of the second decoder circuit.

It is also allowed, however, that three or more input address signals are set, that six or more address signals corresponding thereto are decoded in the unit decoder circuit of the first decoder circuit, and that the intermediate signals thus obtained are further

decoded in the unit decoder circuit of the second decoder circuit. In this way, the number of FETs which constitute the second decoder circuit can be further reduced.

By way of example, when the above construction is applied to the input address signals A_0, A_1 and A_2 in the foregoing embodiment, the number of FETs which constitute the unit decoder circuit of the second decoder circuit can be made 4.

In this case, the unit decoder circuit of the first decoder circuit becomes a logic circuit as shown in Figure 10A.

This unit decoder circuit 2a' comprises NAND circuits 222 to 229 and inverter circuits 214 to 221. It receives address signals B_0 to B_2 and $\overline{B_0}$ to $\overline{B_2}$ generated on the basis of the input address signals from the address buffer circuit 1, and provides decoded intermediate signals E_0 to E_7.

When such unit decoder circuit 2a' is used, the unit decoder circuit of the second decoder circuit is designed in accordance with the circuit as shown in Figure 10B.

This unit decoder circuit comprises P-channel type FETs P_{17} and P_{18} and N-channel type FETs N_{47} and N_{48}. The unit decoder circuit has only two inputs. As the input IN_8, for example, any one of the intermediate signals E_0 to E_7 may be applied. Thus, the single unit decoder circuit of the second decoder circuit requires only two FETs with respect to the input address signals A_0, A_1 and A_2, which means that the number of elements of the second decoder circuit can be further reduced.

In all the above described embodiments, the memory used employs cells of the static type. The memory circuit may equally employ cells of the dynamic type. The effects in this case are the same as those in the various embodiments described above.

CLAIMS:

1. A semiconductor memory circuit device including:

(a) a memory cell array comprising a plurality of memory cells arranged in rows and columns;

(b) first means for receiving input row address signals, each of which comprises a predetermined number of bits, said first receiving means providing an output of at least first partial row address signals, each of which comprises a portion of said predetermined number of bits of a corresponding input row address signal;

(c) a first row decoder circuit comprising a plurality of first unit row decoders, each of which receives said first partial row address signals from said first receiving means and provides intermediate first decoded signals of said first partial address signals, each of said first unit row decoders consisting of a NAND circuit;

(d) a plurality of first inverters;

(e) a second row decoder circuit comprising a plurality of second unit row decoders, each of which selectively receives said first intermediate decoded signals through said first inverters and provides an output decoded signal for selecting a row from said memory cell array, each of said second unit row decoders consisting of a NAND circuit;

(f) a word driver circuit connected between the output of said second row decoder circuit and said memory cell array;

(g) second means for receiving input column address signals, each of which comprises a predetermined number of bits, said second receiving means providing an output of at least first partial column address signals, each of which comprises a portion of said predetermined number of bits of a corresponding input column address signal;

(h) a first column decoder circuit comprising a plurality of first unit column decoders, each of which receives said first partial column address signals from said second receiving means and provides second intermediate decoded signals of said first partial column address signals, each of said first unit column decoders consisting of a NOR circuit;

(i) a plurality of second inverters; and

(j) a second column decoder circuit comprising a plurality of second unit column decoders, each of which selectively receives said second intermediate decoded signals through said second inverters and provides output decoded signals for selecting a column of said memory array, each of said second unit column decoders consisting of a NOR circuit.

2. A semiconductor memory circuit device according to claim 1, wherein each of said unit first row decoders and unit first column decoders is responsive to two bits of said first partial row address signals and first partial column address signals, respectively.

3. A semiconductor memory circuit device according to claim 2, wherein for 2-bit input signals made up of bits B_{XO}, B_{X1}, $\overline{B_{XO}}$ and $\overline{B_{X1}}$, each of said unit first row decoders provides intermediate decoded output signals of

$$MX_O = \overline{B_{XO}} \cdot \overline{B_{X1}}$$

$$MX_1 = B_{XO} \cdot \overline{BX_1}$$

$$MX_2 = \overline{B_{XO}} \cdot B_{X1}$$

$$MX_3 = B_{XO} \cdot B_{X1}$$

and wherein for input signals made up of bits B_{YO}, B_{Y1}, $\overline{B_{YO}}$ and $\overline{B_{Y1}}$, each of said first column unit decoders provides intermediate decoded output signals of :

$$MY_O = \overline{B_{YO}} \cdot \overline{B_{Y1}}$$

$$MY_1 = B_{YO} \cdot \overline{B_{Y1}}$$

$$MY_2 = \overline{B_{YO}} \cdot B_{Y1}$$

$$MY_3 = B_{YO} \cdot B_{Y1}.$$

4. A semiconductor memory circuit device according to claim 1, wherein said first receiving means provides an additional output of second partial row address signals, each of which comprises a different portion of said predetermined number of bits of said corresponding input row address signals than said first partial row address signals, and further including a word control circuit coupled between said first receiving means and said word driver circuit, wherein said word control circuit receives said second partial row address signals and controls said word driver circuit in accordance with said second partial row address signals to provide word signals for selecting rows from said memory array.

5. A semiconductor memory circuit device according to claim 4, wherein said word driver comprises a plurality of unit driver circuits, and wherein the pitch in a column direction between individual memory cells in said memory array is equal to the pitch in a column direction between the unit decoder circuits in said second row decoder and the pitch in a column direction between unit driver circuits in said word driver circuit.

6. A semiconductor memory circuit device according to claim 1, wherein each of said first and second unit row decoders comprises a complementary NAND circuit, and each of said first and second unit column decoders comprises a complementary NOR circuit.

7. A semiconductor memory circuit device according to claim 6, wherein said word driver circuit comprises a plurality of complementary type unit driver circuits, each of said unit driver circuits including a first FET of first conductivity type having a source connected to an output of said word control circuit, a drain connected to said memory cell array and gate connected to the output of said second row decoder circuit, and a second FET of second conductivity type having a source connected to a reference potential point, a drain connected to the drain of said first FET, and a gate commonly connected to the gate of said first FET.

8. A semiconductor memory circuit device according to claim 7, wherein each of the outputs of said second unit row decoders is connected to at least two unit driver circuits.

9. A semiconductor memory circuit device including:

(a) a memory cell array comprising a plurality of memory cells arranged in rows and columns;

(b) first means for receiving input row address signals, each of which comprises a predetermined number of bits, said first receiving means providing an output of row address signals;

(c) a row decoder circuit which receives said row address signals from said first receiving means and provides output decoded signals for selecting a row from said memory cell array, said row decoder circuit consisting of a plurality of NAND circuits;

(d) a word driver circuit connected between the output of said row decoder circuit and said memory array;

(e) second means for receiving input column address signals, each of which comprises a predetermined number of bits, said second receiving means providing an output of column address signals; and

(f) a column decoder circuit which receives said column address signals from said second receiving means and provides output decoded signals for selecting a column of said memory array, said column decoder circuit consisting of a plurality of NOR circuits.

10. A semiconductor memory circuit device constructed and arranged to operate substantially as herein described with reference to and as illustrated in Figures 1 to 7, or Figures 1 to 7 as modified by any one of Figures 8 to 10 of the accompanying drawings.

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HITACHI, LTD., 5-1 Marunouchi 1-chome, Chiyoda-ku, Tokyo, Japan, a corporation organised under the laws of Japan,

NOBUYOSHI TANIMURA, 1-22-7-402, Naka-machi, Musashino-shi, Tokyo, Japan.

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Address for Service:

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