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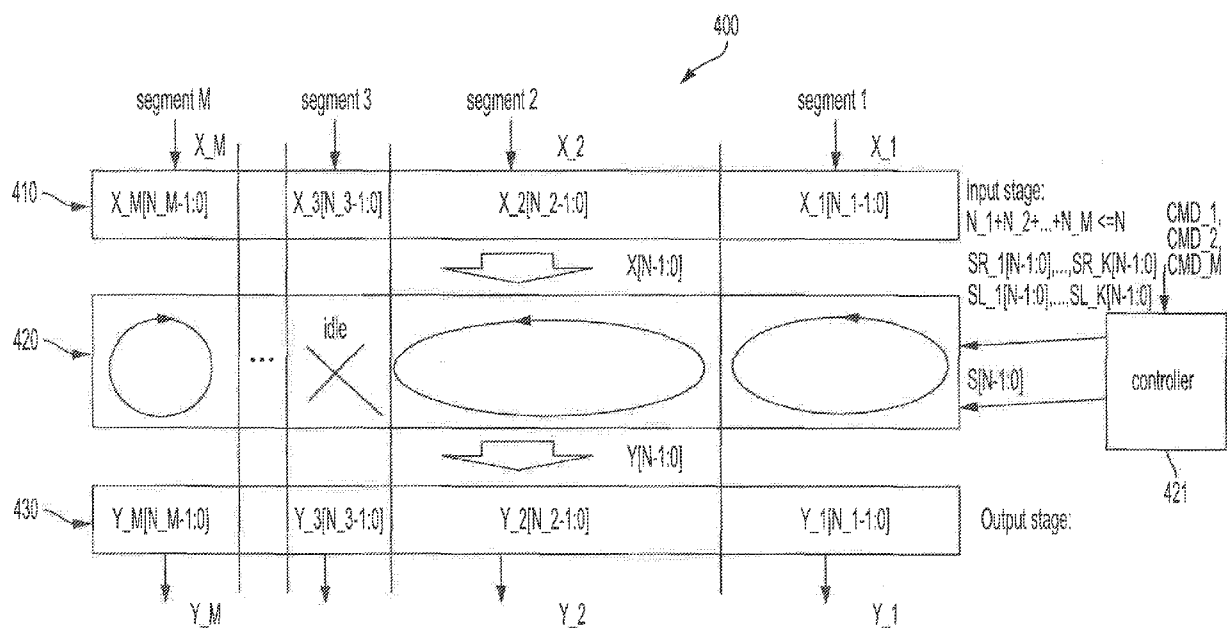


FIG. 4B

(57) Abstract: Systems and methods that provide reconfigurable shifter configurations supporting multiple instruction, multiple data (MIMD) are described. Shifters (400) implemented support multiple data shifts with respect to an instance of data shifting, wherein multiple individual different data shifts are implemented at a time in parallel. Reconfigurable segmented scalable shifters (400), in addition being reconfigurable for scalability in supporting data shifting with respect to various bit lengths of data, are configured to support data shifting of differing bit lengths in parallel. The data shifters (400) implement segmentation for facilitating data shifting with respect to differing bit lengths. Different data shift commands may be provided with respect to each such segment, thereby facilitating multiple data shifts in parallel with respect to various bit lengths of data. Reconfigurable segmented scalable shifter configurations provide for fully reconfigurable data width and shift command of each message of input data.



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## RECONFIGURABLE SEGMENTED SCALABLE SHIFTER

### CROSS-REFERENCE TO RELATED APPLICATIONS

**[0001]** The present application is related to commonly assigned U.S. patent application number [HKAP.P0132US.10010543350], entitled “PARALLEL LDPC DECODER,” filed concurrently herewith, the disclosure of which is hereby incorporated by reference herein in its entirety as if fully set forth below for all applicable purposes.

### TECHNICAL FIELD

**[0002]** The present invention relates generally to data shifting and, more specifically, to reconfigurable shifters.

### BACKGROUND OF THE INVENTION

**[0003]** A shifter is often an important element in digital signal processing. For example, shifters are used for a variety of applications such as channel decoder (e.g. 5G Quasi-Cyclic Low-Density Parity Check (QC-LDPC) decoder), Arithmetic Logic Unit (ALU) of CPU, Coordinate Rotation Digital Computer (CORDIC) processor, data encryption (e.g. Rijndael algorithm), etc.

**[0004]** There are three main types of data shifting as may be provided using shifters. FIGURE 1 shows bit shift examples for an eight-bit ALU for arithmetic shift, logical shift, and cyclic shift types of data shifting. The data shifting type examples of FIGURE 1 illustrated data shifting for both left and right shifts.

**[0005]** It can be appreciated from the examples shown in FIGURE 1 that data shifting provided by a shifter involves more than simply shifting data bits to the left or right. For example, in implementing an arithmetic shift, the input is a signed number (e.g., in the illustrated 8-bit example, bit [7] is a sign-bit) and a sign bit is inserted as the leftmost bit when the bits are shifted to the right. Alternatively, a “0” bit is inserted as the rightmost bit when the bits are shifted to the left in implementing an arithmetic shift. In implementing a logical shift, a “0” bit is inserted as the rightmost bit when the bits are shifted to the left and as the leftmost bit when the bits are shifted to the right. In implementing a cyclic shift, a bit leftmost bit is inserted as the rightmost bit when the bits are shifted to the left and a rightmost bit is inserted as the leftmost bit when the bits are shifted to the right. Accordingly, circuitry configured for implementing data shifting can be somewhat complicated, particularly if configured to accommodate multiple types of data shifting.

**[0006]** Traditional shifters support a single shifting command with respect to an instance of data shifting. For example, a common configuration of a traditional shifter is the single instruction, single data (SISD) implementation illustrated in FIGURE 2A. In operation of a SISD shifter, a single shift command (CMD) is provided with respect to input data (X, such as may comprise bits [7:0] of the eight-bit examples of FIGURE 1) for implementing a data shift and generating corresponding output data (Y, such as may comprise bits [7:0] shifted in accordance with CMD). Another common configuration of a traditional shifter is the single instruction, multiple data (SIMD) implementation illustrated in FIGURE 2B. In operation of a SIMD shifter, a single shift command (CMD) is provided with respect to multiple input data (X<sub>1</sub>, X<sub>2</sub>, . . . X<sub>M</sub>, such as may each comprise bits [7:0] of the eight-bit examples of FIGURE 1) for implementing a same data shift with respect to each such input and generating corresponding output data (Y<sub>1</sub>, Y<sub>2</sub>, . . . Y<sub>M</sub>, such as may each comprise bits [7:0] shifted in accordance with CMD). Such traditional shifters do not support multiple data shift commands allowing individual, multiple different data shifting to be implemented in parallel (e.g., providing different data shifts with respect to multiple input data, such as each of X<sub>1</sub>, X<sub>2</sub>, . . . X<sub>M</sub>).

**[0007]** Reconfigurable scalable shifter configurations have been implemented to accommodate data shifting with respect to data of different bit sizes. FIGURE 3 illustrates scalable operation of a typical reconfigurable shifter implementation for an example in which the shifter accommodates up to eight-bit data shifting and an instance of data shifting involves five-bit data. Logic circuitry of such traditional reconfigurable scalable shifters is designed based

on the longest bit length of input data that the shifter can handle. In operation, portions of the logic circuitry are idle when processing input data with shorter bit lengths. For example, as shown in FIGURE 3, although the shifter is reconfigurable to accommodate data shifting with respect to less than the full complement of data bits supported by the shifter, that portion of the shifter not needed for data shifting with respect to the scaled-down input remains idle during the particular instance of data shifting (e.g., circuitry with respect to data bit positions [7:5] remain idle while circuitry with respect to data bit positions [4:0] perform shifting with respect to 5-bit input data). It can be readily appreciated that hardware resources in the shifter may be appreciably underutilized as the bit length of input data varies depending on the applications.

**[0008]** Specific examples of prior shifter configurations may be found in U.S. patent numbers 9,537,510 and 8,713,399. The shifters of U.S. patent number 9,537,510 provide implementations in which multiple shifter stages cooperate to provide SISD configurations supporting variable shift values with respect to input data of M bits. The shifters therein do not, however, support parallel segmented data with variable size. The shifters of U.S. patent number 8,713,399 provide implementations in which SIMD configurations support data shifts with respect to multiple input data of pre-determined data sizes. For example, a same shift command is implemented for providing data shifting with respect to a group of three input messages (i.e.,  $n=3$ ), a group of six input messages (i.e.,  $n=6$ ), or a group of nine input messages (i.e.,  $n=9$ ). The shifters therein do not, however, support all possible data size values, and instead support only the pre-determined data sizes. Moreover, the same data shift is implemented with respect to each input message of a group.

#### BRIEF SUMMARY OF THE INVENTION

**[0009]** The present invention is directed to systems and methods provide reconfigurable shifter configurations supporting multiple instruction, multiple data (MIMD). Shifters implemented according to embodiments of the invention support multiple data shifts with respect to an instance of data shifting, wherein multiple individual different data shifts are implemented at a time in parallel. In operation according to embodiments, multiple data shift commands may be utilized such that a plurality of data (e.g., each message of the input data) can have an individual shifting command to thereby implement different data shifting with respect to each such data.

**[0010]** MIMD shifters implemented according to embodiments of the present invention provide reconfigurable segmented scalable shifter configurations. Reconfigurable segmented scalable shifters of embodiments, in addition being reconfigurable for scalability in supporting data shifting with respect to various bit lengths of data, are configured to support data shifting of differing bit lengths in parallel. For example, messages of differing bit lengths may be provided individual data shifting in parallel. Accordingly, inputs of a reconfigurable segmented scalable shifter of embodiments may comprise a mix of inputs of different sizes.

**[0011]** The data shifters of embodiments implement segmentation for facilitating data shifting with respect to differing bit lengths. For example, one or more messages from input data may be provided data shifting in each segment of a reconfigurable segmented scalable shifter. In operation according to embodiments, the segmentation of a reconfigurable segmented scalable shifter utilizes an otherwise idle portion of logic for data shifting of other input data. Different data shift commands may be provided with respect to each such segment, thereby facilitating multiple data shifts in parallel with respect to various bit lengths of data.

**[0012]** Reconfigurable segmented scalable shifter configurations provide for fully reconfigurable data width and shift command of each message of input data. For example, shifters of embodiments are reconfigurable with respect to a number of segments (M) (e.g.,  $1 \leq M \leq N$ ), a size of each segment ( $N_m$ ) (e.g.,  $N \geq N_m \geq 2$ ), a shift value of each segment (S) ( $0 \leq S \leq N$ ), a shift direction (D) of each segment (e.g., D is left or right), and/or a shift type (T) of each segment (e.g., T is logical, arithmetic, or cyclic). Such reconfigurable segmented scalable shifters in accordance with concepts of the present invention provide flexible and efficient utilization of hardware for parallel processing data input of various bit lengths.

**[0013]** The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims. The novel features which are believed to be characteristic of the invention, both as to its organization and method of operation, together with further objects and advantages will be better understood from the following description when considered in connection with the accompanying figures. It is to be expressly understood, however, that each of the figures is provided for the purpose of illustration and description only and is not intended as a definition of the limits of the present invention.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0014]** For a more complete understanding of the present disclosure, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

**[0015]** FIGURE 1 shows data shifting type examples for both left and right data shifts;

**[0016]** FIGURES 2A and 2B show single instruction shifters of the prior art;

**[0017]** FIGURE 3 shows scalable operation of a typical reconfigurable shifter implementation of the prior art;

**[0018]** FIGURES 4A and 4B show multiple instruction multiple data implementations of a reconfigurable segmented scalable shifter according to embodiments of the invention;

**[0019]** FIGURE 5A shows a reconfigurable segmented scalable shifter implementing a single segment providing cyclic data shifting in accordance with embodiments of the invention;

**[0020]** FIGURES 5B-5D show details with respect to a logarithmic shifter configuration of a reconfigurable segmented scalable shifter embodiment of FIGURE 5A;

**[0021]** FIGURE 6 shows an output stage configured to merge results of a right shifter portion and left shifter portion to provide cyclic shift results according to embodiments of the invention;

**[0022]** FIGURE 7 shows a reconfigurable segmented scalable shifter implementing two segments providing cyclic data shifting in accordance with embodiments of the invention;

**[0023]** FIGURE 8 shows an example of a shifter stage to a logarithmic shifter configuration according to embodiments of the invention;

**[0024]** FIGURE 9 shows a reconfigurable segmented scalable shifter implementing two segments providing right arithmetic data shifting in accordance with embodiments of the invention;

**[0025]** FIGURE 10 shows an output stage configured to replace shifter results with sign bits to provide arithmetic shift results according to embodiments of the invention;

**[0026]** FIGURE 11 shows a reconfigurable segmented scalable shifter implementing two segments providing left arithmetic data shifting in accordance with embodiments of the invention;

**[0027]** FIGURE 12 shows an output stage configured to replace shifter results with 0 to provide arithmetic shift results according to embodiments of the invention;

**[0028]** FIGURE 13 shows a reconfigurable segmented scalable shifter implementing two segments providing right logical data shifting in accordance with embodiments of the invention;

**[0029]** FIGURE 14 shows an output stage configured to replace shifter results with 0 to provide logical shift results according to embodiments of the invention;

**[0030]** FIGURE 15 shows a reconfigurable segmented scalable shifter implementing two segments providing left logical data shifting in accordance with embodiments of the invention;

**[0031]** FIGURE 16 shows details of a reconfigurable segmented scalable shifter according to embodiments of the invention;

**[0032]** FIGURES 17A-17F show a configuration of controllable data path elements as may be utilized in an output stage of a reconfigurable segmented scalable shifter supporting cyclic shifts, arithmetic shifts, and logical shifts according to embodiments of the invention;

**[0033]** FIGURE 18 shows a sectioned shifter stage configuration of a reconfigurable segmented scalable shifter of embodiments of the invention;

**[0034]** FIGURE 19 shows details of a reconfigurable segmented scalable shifter implementing sections according to embodiments of the invention; and

**[0035]** FIGURE 20 shows an output stage configured to merge results of a right shifter portion and left shifter portion to provide cyclic shift results according to embodiments of the invention.

#### DETAILED DESCRIPTION OF THE INVENTION

**[0036]** FIGURE 4A shows reconfigurable segmented scalable shifter 400 of embodiments of the invention. Reconfigurable segmented scalable shifter 400 provides a reconfigurable shifter configuration supporting multiple instruction, multiple data (MIMD). In particular, input data (X) supplied to reconfigurable segmented scalable shifter 400 comprises a number of messages (M), shown as messages X<sub>1</sub>, X<sub>2</sub>, . . . X<sub>M</sub>, wherein multiple individual different data shifts may be implemented at a time in parallel with respect to these messages to provide output data (Y) comprising M messages, shown as messages Y<sub>1</sub>, Y<sub>2</sub>, . . . Y<sub>M</sub>, having shifted data. Accordingly, multiple data shift commands (e.g., CMD<sub>1</sub>, CMD<sub>2</sub>, . . . CMD<sub>M</sub>) are shown in association with the messages of the input data. In operation according to embodiments, each message of the input data (e.g., X<sub>1</sub>, X<sub>2</sub>, . . . X<sub>M</sub>) may have an individual shift implemented with respect thereto in accordance with a corresponding one of the data shift commands (e.g., CMD<sub>1</sub>→X<sub>1</sub>, CMD<sub>2</sub>→X<sub>2</sub>, . . . CMD<sub>M</sub>→X<sub>M</sub>) to thereby facilitate different data shifting with respect to each output message (e.g., Y<sub>1</sub>, Y<sub>2</sub>, . . . Y<sub>M</sub>).

**[0037]** The segmentation configuration implemented according to the embodiments of reconfigurable segmented scalable shifter 400 facilitates utilizing idle portion of logic for the shift of additional input data. FIGURE 4B shows additional detail with respect to reconfigurable segmented scalable shifter 400, including the segmentation configuration thereof, in accordance with embodiments of the invention. In particular, reconfigurable segmented scalable shifter 400 shown in FIGURE 4B includes input stage 410, shifter stage 420, and output stage 430 implementing a segmentation configuration.

**[0038]** Input stage 410 may, for example, comprise configurable memory elements (e.g., random access memory (RAM), flash memory, magnetic memory, optical memory, etc.) and/or controllable data paths (e.g., controllable data path elements) suitable for storage of the data of messages input to reconfigurable segmented scalable shifter 400 for which shifting is provided and for controllably associating such data with reconfigurable segments of shifter stage 420. As will be better understood from the discussion which follows, input stage 410 is utilized to associate the one or more messages (e.g., X<sub>1</sub>, X<sub>2</sub>, . . . X<sub>M</sub>) of the input data (X) with corresponding segments of shifter stage

420. For example, in the illustrated embodiment, the input data (X) includes messages  $X_1, X_2, X_3, \dots, X_M$ , wherein input stage 410 facilitates correspondence of the  $N_1$  number of bits of message  $X_1$  (e.g., bits 0 to  $N_1-1$  of message  $X_1$ ) to segment 1 of shifter stage 420, correspondence of the  $N_2$  number of bits of message  $X_2$  (e.g., bits 0 to  $N_2-1$  of message  $X_2$ ) to segment 2 of shifter stage 420, correspondence of the  $N_3$  number of bits of message  $X_3$  (e.g., bits 0 to  $N_3-1$  of message  $X_3$ ) to segment 3 of shifter stage 420, and correspondence of the  $N_M$  number of bits of message  $X_M$  (e.g., bits 0 to  $N_M-1$  of message  $X_M$ ) to segment M of shifter stage 420.

**[0039]** Shifter stage 420 may, for example, comprise controllable data path elements (e.g., multiplexers and associated control elements) suitable for implementing data shifts. Such data path elements of embodiments may implement various shifter architectures, such as logarithmic shifter configurations, barrel shifter configurations, combinational shifter configurations, etc. As will be better understood from the discussion below, shifter stage 420 provides reconfigurable, scalable segments that are utilized in implementing data shifting in parallel with respect to multiple messages of input data. Controller 421 of shifter stage 420 is shown in the illustrated embodiment for providing individual shifting commands to the segments of shifter stage 420 in accordance with data shift commands (e.g.,  $CMD_1, CMD_2, \dots, CMD_M$ ) provided in association with the input data (e.g.,  $X = X_1, X_2, X_3, \dots, X_M$ ). Data shifting is independently provided by segments (e.g., left cyclic by segment 1, left cyclic by segment 2, and right cyclic by segment M) of shifter stage 420 in accordance with the respective data shift commands to thereby implement multiple individual different data shifts at a time in parallel.

**[0040]** It should be appreciated that, although implementation of cyclic shifts are illustrated in the example of FIGURE 4B, embodiments may implement various data shifting types (e.g., arithmetic shift, logical shift, and/or cyclic shift), whether by all segments or in various different combinations by the segments. Moreover, one or more segments may be configured so as to provide no data shifting operation in any instance of data shifting by reconfigurable segmented scalable shifter 400. For example, segment 3 shown in the exemplary embodiment of FIGURE 4B is unused for data shifting (e.g., idle or configured to pass data bits straight through without shifting) in the data shifting instance illustrated. Such unused segments may, for example, be used in situations where the messages ( $X_1, X_2, \dots, X_M$ ) of the input data (X) comprise fewer bits in the aggregate than are accommodated by the particular implementation of reconfigurable segmented scalable shifter 400. The location of such unused segments may be anywhere within the reconfigurable segmented scalable shifter of embodiments, such as to conveniently accommodate various message lengths, to facilitate a segment starting with the least significant bit (LSB) of a respective message, etc., as will be better understood from the discussion which follows.

**[0041]** Reconfigurable segmented scalable shifter 400 of embodiments is configured to be reconfigurable with respect to data width and/or shift command of each message of input data. For example, as shown in further detail below, shifter stage 420 of embodiments is reconfigurable with respect to the number of segments (M) (e.g.,  $1 \leq M \leq N$ ), the size of each segment ( $N_m$ ) (e.g.,  $N \geq N_m \geq 2$ ), the shift value (S) of each segment ( $S_m$ ) ( $0 \leq S_m \leq N$ ), the shift direction (D) of each segment ( $D_m$ ) (e.g.,  $D_m$  is left or right), and/or the shift type (T) of each segment ( $T_m$ ) (e.g.,  $T_m$  is logical, arithmetic, or cyclic), any or all of which may be controlled by controller 421. The individual data shift commands (e.g.,  $CMD_1, CMD_2, \dots, CMD_M$ ) provided to reconfigurable segmented scalable shifter 400 (e.g., to controller 421) of embodiments may include various such information (e.g., the size of the respective segment ( $N_m$ ), the shift value of the respective segment ( $S_m$ ), the shift direction of the respective segment ( $D_m$ ), the shift type of the respective segment ( $T_m$ ), etc.). Additionally or alternatively, one or more general data shift commands (e.g., CMD, not shown in the illustrated embodiment) including various such information (e.g., the number of segments (M), the size of each segment ( $N_m$ ), a globally applicable shift value (S), a globally applicable shift direction (D), a globally applicable shift type (T), etc.) may be provided to reconfigurable segmented scalable shifter 400 (e.g., to controller 421) of embodiments for controlling aspects generally applicable to the shifter and/or segments thereof.

**[0042]** Output stage 430 may, for example, comprise configurable memory elements (e.g., RAM, flash memory, magnetic memory, optical memory, etc.) and/or controllable data paths (e.g., controllable data path elements) suitable for controllably associating reconfigurable segments of shifter stage 420 with messages of output data for storage of the shifted data of the messages for which shifting is provided. As will be better understood from the

discussion which follows, output stage 430 is utilized to associate segments of shifter stage 420 with the one or more messages (e.g.,  $Y_1, Y_2, \dots, Y_M$ ) of the output data (Y). For example, in the illustrated embodiment, the output data (Y) includes messages  $Y_1, Y_2, Y_3, \dots, Y_M$ , wherein output stage 410 facilitates correspondence of the  $N_1$  number of the shifted bits of message  $Y_1$  (e.g., bits 0 to  $N_1-1$  of message  $Y_1$ ) to segment 1 of shifter stage 420, correspondence of the  $N_2$  number of shifted bits of message  $Y_2$  (e.g., bits 0 to  $N_2-1$  of message  $Y_2$ ) to segment 2 of shifter stage 420, correspondence of the  $N_3$  number of un-shifted bits of message  $Y_3$  (e.g., bits 0 to  $N_3-1$  of message  $Y_3$ ) to segment 3 (idle in this illustrated example) of shifter stage 420, and correspondence of the  $N_M$  number of shifted bits of message  $Y_M$  (e.g., bits 0 to  $N_M-1$  of message  $Y_M$ ) to segment M of shifter stage 420.

**[0043]** In order to aid in understanding concepts of the present invention, example shifter embodiments are described below with reference to logarithmic shifter configurations providing data shifting using 3 stage architectures with respect to input/output data having bit lengths of 8 bits, it should be appreciated that these are exemplary implementations and are not limiting with respect to the present invention. Embodiments of a reconfigurable segmented scalable shifter may, for example, be implemented using logarithmic shifter configurations, barrel shifter configurations, combinational shifter configurations, or combinations thereof. The 8 bit reconfigurable segmented scalable shifter examples are provided for simplicity, and it is expected that reconfigurable segmented scalable shifters in accordance with embodiments of the invention will be implemented to accommodate significantly larger data inputs (e.g., 384 data inputs for a 5G QC-LDPC decoder implementation). Likewise, although examples of segmentation providing configurations having a small number of segments (e.g.  $M=1$  or  $M=2$ ) are provided for simplifying the concepts discussed, embodiments of a reconfigurable segmented scalable shifter may accommodate a wide range of segmentation configurations having various segment sizes (e.g., segments ranging from 2 to 384 bits, having segment sizes from 384 to 2 for the above mentioned 5G QC-LDPC decoder implementation).

**[0044]** FIGURE 5A shows an exemplary embodiment of reconfigurable segmented scalable shifter 400 implemented in a relatively simple configuration helpful for understanding the concepts of the present invention. Reconfigurable segmented scalable shifter 400 of the embodiment of FIGURE 5A is configured as an 8 bit single segment implementation providing a 3 bit cyclic shift to the right (e.g., shifter size  $N=8$ , number of segments  $M=1$ , segment 1 size  $N_1=8$ , segment 1 shift value  $S_1=3$ , segment 1 shift direction  $D_1=Right$ , and segment 1 shift type  $T_1=Cyclic$ ).

**[0045]** The input data (X) comprises 8 bits in the illustrated example. Accordingly, the input data may be represented as  $X[7:0]$ , wherein  $X[7:0]=\{X[7], X[6], X[5], X[4], X[3], X[2], X[1], X[0]\}$ . Correspondingly, the output data may be represented as  $Y[7:0]$ , wherein  $Y[7:0]=\{Y[7], Y[6], Y[5], Y[4], Y[3], Y[2], Y[1], Y[0]\}$ . As mentioned above, the number of segments (M) is 1 in this example. Accordingly,  $X_1[7:0]=X[7:0]$  and  $Y_1[7:0]=Y[7:0]$ , where  $X_1[7:0]$  is the input data of segment 1 and  $Y_1[7:0]$  is the output data of segment 1.

**[0046]** As shown in FIGURES 5B-5D, the reconfigurable segmented scalable shifter of FIGURE 5A may be implemented using a logarithmic shifter configuration. The number of stages of the logarithmic shifter is  $K=\lceil \log_2(N) \rceil$ . In the exemplary embodiment  $N=8$ , and thus  $K=\log_2(8)=3$ . The 3 stages of a logarithmic shifter are shown in the right shift portion of shifter stage 420 shown in FIGURE 5B, wherein  $YR_1[7:0]$  = output of stage 1,  $YR_2[7:0]$  = output of stage 2, and  $YR_3[7:0]$  = output of stage 3.

**[0047]** The stages of the logarithmic shifter implement log increasing shifts at each stage (e.g., shift 1 bit at stage 1, shift 2 bits at stage 2, shift 4 bits at stage 4). The shifts provided by the stages may be controllably combined to provide a range of shift values from 0 (e.g., pass data bits straight through without shifting) through the combined total shift values of all stages (e.g.,  $1+2+4=7$  in the 3 stage example). In the example of the illustrated embodiment, the segment 1 shift value  $S_1=3$  and the segment 1 shift direction  $D_1=Right$ . This may be represented as a shift right command for segment 1 of  $SR1=3$ , which may be provided in a 3 bit binary coded decimal (BCD) representation as 3'b011. It should be appreciated that the 3 bits of the BCD shift command representation correspond to the operation of the 3 stages in performing the desired data shift. In particular, in the BCD representation the LSB (1 in this example) corresponds to the shift of stage 1 being selected (stage 1 providing shift right 1 bit), the middle bit (1 in this example)

corresponds to the shift of stage 2 being selected (stage 2 providing shift right 2 bits), and the most significant bit (MSB) (0 in this example) corresponds to the shift of stage 3 not being selected (stage 3 passing data bits straight through without providing shift right 4 bits) to thereby provide 3 bit right shift.

**[0048]** Control signals may be provided with respect to each stage of the shifter to implement the foregoing commands with respect to any instance of data shifting. For example, as shown in FIGURE 5C, a data shift for any particular bit at the various stages of the shifter may be implemented using a multiplexer architecture. In particular, an instance of multiplexer 501 may be disposed at the path junctions of each stage (e.g., junctions of path 0 and path 1, path 1 and path 2, path 2 and path 3, path 3 and path 4, path 4 and path 5, path 5 and path 6, and path 6 and path 7 in stage 1, junctions of path 0 and path 2, path 1 and path 3, path 2 and path 4, path 3 and path 5, path 4 and path 6, and path 5 and path 7 in stage 2, junctions of path 0 and path 4, path 1 and path 5, path 2 and path 6, and path 3 and path 7 in stage 3 of right shift portion 521 (FIGURE 5D) and junctions of path 1 and path 0, path 2 and path 1, path 3 and path 2, path 4 and path 3, path 5 and path 4, path 6 and path 5, and path 7 and path 6 in stage 1, junctions of path 2 and path 0, path 3 and path 1, path 4 and path 2, path 5 and path 3, path 6 and path 4, and path 7 and path 5 in stage 2, junctions of path 4 and path 0, and path 5 and path 1, path 6 and path 2, path 7 and path 3 in stage 3 of left shift portion 522) and provided with a control signal to select output of either shifted data or passing data straight through.

**[0049]** As illustrated in FIGURE 5C, embodiments in accordance with the foregoing provide  $SR\_k[n]$  as the control signal of stage  $k$ , path  $n$ . Accordingly,  $SR\_1[7:0]$  = control signals for the paths of right shift stage 1,  $SR\_2[7:0]$  = control signals for the paths of right shift stage 2, and  $SR\_3[7:0]$  = control signals for the paths of right shift stage 3 in the 3 stages of the right shift portion of shifter stage 420 shown in FIGURE 5B. If the control signal of a path is "0", the data will propagate along the same path to next stage. However, if the control signal of the path is "1", the data of the other path coupled to the multiplexer will propagate along that path to the next stage. Accordingly, in the above described example where  $SR1 = 3 = 3'b011$ , the control signals for the stages of the shifter may be represented as  $SR\_1[7:0] = 1111\_1111$  (stage 1),  $SR\_2[7:0] = 1111\_1111$  (stage 2), and  $SR\_3[7:0] = 0000\_0000$  (stage 3). Implementing the data shifts in accordance with these control signals to provide 3 bit right shift of  $X[3]$  to  $Y[0]$ ,  $X[4]$  to  $Y[1]$ ,  $X[5]$  to  $Y[2]$ ,  $X[6]$  to  $Y[3]$ , and  $X[7]$  to  $Y[4]$  is illustrated in the bolded paths of right shift portion 521 shown in FIGURE 5D.

**[0050]** As previously mentioned, reconfigurable segmented scalable shifter 400 of FIGURE 5A is configured as an 8 bit single segment implementation providing a 3 bit cyclic shift to the right. The right shift portion of shifter stage 420 shown in FIGURE 5B, however, does not provide paths for implementing the cyclic aspect of the data shift (e.g., to route data from  $X[2]$  to  $Y[7]$ , from  $X[1]$  to  $Y[6]$ , and from  $X[0]$  to  $Y[5]$ ). Accordingly, embodiments implement another shifter portion in shifter stage 420 for this purpose.

**[0051]** FIGURE 5D shows right shift portion 521 and left shift portion 522 of shifter stage 420. In accordance with embodiments of the invention, in a right cyclic shift operation, right shift portion 521 may provide right data shifts and left shift portion 522 may be utilized for implementing the cyclic aspect of the data shift. Similarly, in a left cyclic shift operation, left shift portion 522 may provide left data shifts and right shift portion 521 may be utilized for implementing the cyclic aspect of the data shift. Moreover, as will be better understood from the discussion which follows, right shift portion 521 may provide right shifts in right arithmetic shift and right logical shift operations. Similarly, left shift portion 522 may provide left shifts in left arithmetic shift and left logical shift operations.

**[0052]** Continuing with the 3 bit cyclic shift to the right of the example, right shift portion 521 provides the 3 bit shift to the right to appropriately route data from  $X[3]$  to  $Y[0]$ , from  $X[4]$  to  $Y[1]$ , from  $X[5]$  to  $Y[2]$ , from  $X[6]$  to  $Y[3]$ , and from  $X[7]$  to  $Y[4]$ , as shown in FIGURE 5D. However, right shift portion 521 does not appropriately route data from  $X[2]$  to  $Y[7]$ , from  $X[1]$  to  $Y[6]$ , and from  $X[0]$  to  $Y[5]$  for the 3 bit cyclic shift to the right. This cyclic aspect of the data shift may be implemented as a left shift of the particular input data. The left shift needed for the particular right cyclic shift being implemented may be computed from the segment size and segment shift value (e.g., shift left command equals segment size minus right shift value). In the above example,  $SL1 = N\_1 - S\_1 = 8 - 3 = 5$ , wherein  $SL$  is the segment 1 shift left command,  $N\_1$  is the segment 1 segment size, and  $S\_1$  is the segment 1 shift value. This may

be represented as a shift left command for segment 1 of  $SL1=5$ , which may be provided in a 3 bit BCD representation as  $3'b101$ .

**[0053]** Similar to the control signals provided with respect to the right shift portion, embodiments in accordance with the foregoing provide  $SL_k[n]$  as the control signal of stage  $k$ , path  $n$ . Accordingly,  $SL_1[7:0]$  = control signals for the paths of left shift stage 1,  $SL_2[7:0]$  = control signals for the paths of left shift stage 2, and  $SL_3[7:0]$  = control signals for the paths of left shift stage 3 in the 3 stages of the left shift portion of shifter stage 420 shown in FIGURE 5D. Accordingly, in the above described example where  $SL1 = 5 = 3'b101$ , the control signals for the stages of the shifter may be represented as  $SL_1[7:0] = 1111\_1111$  (stage 1),  $SL_2[7:0] = 0000\_0000$  (stage 2), and  $SL_3[7:0] = 1111\_1111$  (stage 3). Implementing the data shifts in accordance with these control signals to provide 5 bit left shift of  $X[2]$  to  $Y[7]$ ,  $X[1]$  to  $Y[6]$ , and  $X[0]$  to  $Y[5]$  to implement the cyclic aspect of the 3 bit right cyclic shift is illustrated in the bolded paths of left shift portion 522 shown in FIGURE 5D.

**[0054]** It should be understood that both selections (i.e., dashed line for the path of selection value of 0, and solid line for the path of selection value of 1) of the selectable shifter paths are shown in the illustrations of FIGURES 5B and 5D for all outputs of all stages (i.e.,  $YR_3[7:0]$ ,  $YR_2[7:0]$ ,  $YR_1[7:0]$ ) to show the various possible paths that may be selected using the aforementioned control signals. In FIGURE 5B, for example, one output of stage 1  $YR_1[0]$  has two sources  $X[1]$  and  $X[0]$ , wherein if the selection value is 0 the source from  $X[0]$  will be selected but if the selection value is 1 the source from  $X[1]$  will be selected. The bold lines overlaying the illustrated possible selectable paths in FIGURE 5D illustrate the finally selected path contributing to the final output of the shifter in the example given above.

**[0055]** Output stage 430 of embodiments operates to merge the results of right shifter portion 521 and left shifter portion 522 to provide the cyclic shift results. For example, output stage 430 may comprise instances of multiplexer 602 disposed at the corresponding outputs of each path of right shift portion 521 and left shift portion 522 (e.g., path 0 of both portions, path 1 of both portions, path 2 of both portions, path 3 of both portions, path 4 of both portions, path 5 of both portions, path 6 of both portions, and path 7 of both portions) and provided with a control signal to select output of either right shifted data or left shifted data, as shown in FIGURE 6. The merging of the shifter results may be controlled by an output selection control signal  $S[i]$ , wherein  $S[i] = 1$  for  $i \geq SL1$ , where  $i = \{0, 1, \dots, 7\}$ ,  $SL1 = N\_1 - S\_1$ . It can be appreciated that the data of  $Y[7:0]$  (i.e.,  $Y[7]$ ,  $Y[6]$ ,  $Y[5]$ ,  $Y[4]$ ,  $Y[3]$ ,  $Y[2]$ ,  $Y[1]$ ,  $Y[0]$ ) as stored and/or output by output stage 430 in this example corresponds to the 3 bit cyclic shift to the right illustrated in FIGURE 5A.

**[0056]** Although the foregoing example is described with reference to implementing a right data shift, the concepts are readily applicable to a left data shift. For example, the roles of the right shift portion and left shift portion of the reconfigurable segmented scalable shifter exemplary embodiment may be reversed (i.e., switching the right shift portion for the left shift portion and vice versa) in order to implement a left cyclic shift.

**[0057]** As previously mentioned, reconfigurable segmented scalable shifter 400 of the example of FIGURES 5A-5D provides a relatively simple configuration in which only 1 segment ( $M=1$ ) is provided in order to aid in understanding the concepts of the present invention. In operation according to embodiments of the invention, the data paths within the same segment all share the same control signal value (i.e., the data paths of a segment are controlled to implement the same data shift). Accordingly, in the above example the control signal of all 8 paths within a particular stage are the same (e.g., for right shift stage 1 all control signal values are 1 or  $SR_1[7:0] = 1111\_1111$ , for right shift stage 2 all control signal values are 1 or  $SR_2[7:0] = 1111\_1111$ , for right shift stage 3 all control signal values are 0 or  $SR_3[7:0] = 0000\_0000$ , for left shift stage 1 all control signal values are 1 or  $SL_1[7:0] = 1111\_1111$ , for left shift stage 2 all control signal values are 0 or  $SL_2[7:0] = 0000\_0000$ , and for left shift stage 3 all control signals are 1 or  $SL_3[7:0] = 1111\_1111$ ). It should be appreciated, however, that the foregoing example reconfigurable segmented scalable shifter provides individual control signals for each path, facilitating independent control for segmentation according to embodiments of the invention. In contrast, only 1 control signal is provided for all paths of a traditional

shifter implementation. Accordingly, such traditional shifters are unable to support the segmentation of embodiments of the present invention.

**[0058]** To better illustrate the segmentation facilitated by embodiments of a reconfigurable segmented scalable shifter of the present invention, attention is directed to reconfigurable segmented scalable shifter 400 of FIGURE 7 implemented in a 2 segment (M=2) configuration. In particular, FIGURE 7 shows reconfigurable segmented scalable shifter 400 configured as an 8 bit 2 segment implementation wherein segment 1 provides a 3 bit cyclic shift to the right and segment 2 provides a 2 bit cyclic shift to the right (e.g., shifter size N=8, number of segments M=2, segment 1 size N<sub>1</sub>=5, segment 1 shift value S<sub>1</sub>=3, segment 1 shift direction D<sub>1</sub>=Right, and segment 1 shift type T<sub>1</sub>=Cyclic, segment 2 size N<sub>2</sub>=3, segment 2 shift value S<sub>2</sub>=2, segment 2 shift direction D<sub>2</sub>=Right, and segment 2 shift type T<sub>2</sub>=Cyclic).

**[0059]** It should be appreciated that, although the example of FIGURE 7 shows a configuration in which both segments implement a same type of shift (e.g., cyclic) and a shift in the same direction (e.g., right), there is no limitation with respect to such a configuration according to embodiments of the invention. For example, a reconfigurable segmented scalable shifter of embodiments may be configured to provide different sizes of segments, different shift directions by the segments, different shift values by the segments, and/or different types of shifts by the segments.

**[0060]** As with the example of FIGURE 5A, the input data (X) of the example of FIGURE 7 comprises 8 bits, wherein the input data may be represented as X[7:0] (e.g., X[7:0]={X[7], X[6], X[5], X[4], X[3], X[2], X[1], X[0]}) and the output data may be represented as Y[7:0] (e.g., Y[7:0]={Y[7], Y[6], Y[5], Y[4], Y[3], Y[2], Y[1], Y[0]}). In the example of FIGURE 7, however, the number of segments (M) is 2, wherein segment 1 comprises 5 bits and segment 2 comprises 3 bits such that X<sub>1</sub>[4:0] is the input of segment 1 and X<sub>2</sub>[2:0] is the input of segment 2, and Y<sub>1</sub>[4:0] is the output data of segment 1 and Y<sub>2</sub>[2:0] is the output data of segment 2. Accordingly, X[7:0]={X[7], X[6], X[5], X[4], X[3], X[2], X[1], X[0]}={X<sub>2</sub>[2:0], X<sub>1</sub>[4:0]}, wherein X<sub>1</sub>[4:0]={X[4], X[3], X[2], X[1], X[0]} and X<sub>2</sub>[2:0]={X[7], X[6], X[5]}. Similarly, Y[7:0]={Y[7], Y[6], Y[5], Y[4], Y[3], Y[2], Y[1], Y[0]}={Y<sub>2</sub>[2:0], Y<sub>1</sub>[4:0]}, wherein Y<sub>1</sub>[4:0]={Y[4], Y[3], Y[2], Y[1], Y[0]}, and Y<sub>2</sub>[2:0]={Y[7], Y[6], Y[5]}.

**[0061]** FIGURE 8 shows an example of a shifter stage, as may be utilized in an embodiment of the reconfigurable segmented scalable shifter of FIGURE 7, implemented using a logarithmic shifter configuration. The number of stages of the logarithmic shifter is K=ceil[log<sub>2</sub>(N)], wherein in the exemplary embodiment N=8, and thus K=log<sub>2</sub>(8)=3, as discussed above. The 3 stages of a logarithmic shifter are shown in right shift portion 521 and left shift portion 522 of shifter stage 420 illustrated in FIGURE 8, wherein YR<sub>1</sub>[7:0] = output of stage 1 of the right shift portion, YR<sub>2</sub>[7:0] = output of stage 2 of the right shift portion, YR<sub>3</sub>[7:0] = output of stage 3 of the right shift portion, YL<sub>1</sub>[7:0] = output of stage 1 of the left shift portion, YL<sub>2</sub>[7:0] = output of stage 2 of the left shift portion, and YL<sub>3</sub>[7:0] = output of stage 3 of the left shift portion.

**[0062]** As discussed in detail in the previous example, embodiments of reconfigurable segmented scalable shifters may provide SR<sub>k</sub>[n] as the control signal of stage k, path n. Accordingly, SR<sub>1</sub>[7:0] = control signals for the paths of right shift stage 1, SR<sub>2</sub>[7:0] = control signals for the paths of right shift stage 2, and SR<sub>3</sub>[7:0] = control signals for the paths of right shift stage 3 in the 3 stages of the right shift portion of shifter stage 420 shown in FIGURE 8. Correspondingly, SL<sub>1</sub>[7:0] = control signals for the paths of left shift stage 1, SL<sub>2</sub>[7:0] = control signals for the paths of left shift stage 2, and SL<sub>3</sub>[7:0] = control signals for the paths of left shift stage 3 in the 3 stages of the left shift portion of shifter stage 420 shown in FIGURE 8. If the control signal of a path is "0", the data will propagate along the same path to next stage. However, if the control signal of the path is "1", the data of the other path coupled to the multiplexer will propagate along that path to the next stage.

**[0063]** In this segmented example, SR1 = 3 = 3'b011 (i.e., segment 1 shift value S<sub>1</sub>=3 and segment 1 shift direction D<sub>1</sub>=Right) and SR2 = 2 = 3'b010 (i.e., segment 2 shift value S<sub>2</sub>=2, segment 2 shift direction D<sub>2</sub>=Right). This segmented example provides cyclic shifts, and thus left data shifting is utilized to provide the cyclic

aspect of the data shift. In this example,  $SL_1 = 5 - 3 = 2 = 3'b010$  (i.e., segment 1 size  $N_1=5$ , segment 1 shift value  $S_1=3$ , and segment 1 shift type  $T_1=Cyclic$ ) and  $SL_2 = 3 - 2 = 1 = 3'b001$  (i.e., segment 2 size  $N_2=3$ , segment 2 shift value  $S_2=2$ , and segment 2 shift type  $T_2=Cyclic$ ). The control signals for the stages of the segmented shifter may be represented as  $SR_1[7:0] = 0001\_1111$  (stage 1),  $SR_2[7:0] = 1111\_1111$  (stage 2), and  $SR_3[7:0] = 0000\_0000$  (stage 3) for the right shift portion and  $SL_1[7:0] = 1110\_0000$  (stage 1),  $SL_2[7:0] = 0001\_1111$  (stage 2), and  $SL_3[7:0] = 0000\_0000$  (stage 3) for the left shift portion. It can be appreciated that segmented data shifting is provided for the 5 bits of segment 1 by the right most 5 bits of each of the foregoing control signals, and for the 3 bits of segment 2 by the left most 3 bits of each of the foregoing control signals. Implementing the data shifts in accordance with the shift right control signals ( $SR_1$ ,  $SR_2$ , and  $SR_3$ ) provides 3 bit right shift of  $X[3]$  to  $Y[0]$  and  $X[4]$  to  $Y[1]$  for segment 1 and 2 bit right shift of  $X[7]$  to  $Y[5]$  for segment 2 as illustrated by the bolded paths of right shift portion 521 of FIGURE 8. Correspondingly, implementing the data shifts in accordance with the shift left control signals ( $SL_1$ ,  $SL_2$ , and  $SL_3$ ) provides 2 bit left shift of  $X[0]$  to  $Y[2]$ ,  $X[1]$  to  $Y[3]$  and  $X[2]$  to  $Y[4]$  for the cyclic aspect of segment 1 and 1 bit left shift of  $X[5]$  to  $Y[6]$  and  $X[6]$  to  $Y[7]$  for the cyclic aspect of segment 2 as illustrated by the bolded paths of right shift portion 521 of FIGURE 8.

**[0064]** In the illustration of FIGURE 8, the un-selected paths of the selectable shifter paths are not shown, and that only the selected path for each output of each stage are shown, wherein the bold lines illustrate the finally selected path contributing to the final output of the shifter in the example given above. It should be appreciated that the illustration of FIGURE 8, having the un-selected paths not shown, is in contrast to the illustration in FIGURE 5D where both selections (i.e., dashed line for the path of selection value of 0, and solid line for the path of selection value of 1) of the selectable shift paths are shown with the finally selected path contributing to the final output of the shifter.

**[0065]** As previously described, output stage 430 of embodiments operates to merge the results of right shifter portion 521 and left shifter portion 522 to provide the cyclic shift results, such as through the use of instances of multiplexer 602 as shown in FIGURE 6. The merging of the shifter results in this segmented example may be controlled by an output selection control signal  $S[i]$ , wherein :  $S[i] = 1$  for  $i \geq SL_1$ , where  $i = \{0, 1, \dots, 4\}$ ,  $SL_1 = N_1 - S_1$  (segment 1) and  $S[i] = 1$  for  $i \geq SL_2 + 5$ , where  $i = \{5, 6, 7\}$ ,  $SL_2 = N_2 - S_2$  (segment 2). It can be appreciated that the data of  $Y[7:0]$  (i.e.,  $Y[7]$ ,  $Y[6]$ ,  $Y[5]$ ,  $Y[4]$ ,  $Y[3]$ ,  $Y[2]$ ,  $Y[1]$ ,  $Y[0]$ ) as stored and/or output by output stage 430 in this example corresponds to the 3 bit cyclic shift to the right of segment 1 and the 2 bit cyclic shift to the right of segment 2 illustrated in FIGURE 7.

**[0066]** Although the above example is described with reference to implementing a right data shift, the concepts are readily applicable to a left data shift. For example, the roles of the right shift portion and left shift portion of the reconfigurable segmented scalable shifter exemplary embodiment may be reversed (i.e., switching the right shift portion for the left shift portion and vice versa) in order to implement a left cyclic shift.

**[0067]** Further, although the two examples above are described with reference to implementing cyclic shifts, the concepts are readily applicable to other types of data shifting. For example, arithmetic shifts and/or logical shifts may be implemented using the exemplary reconfigurable segmented scalable shifter architecture. Accordingly, FIGURES 9 and 11 show examples of implementing arithmetic shifts using the exemplary reconfigurable segmented scalable shifter architecture and FIGURES 13 and 15 show examples of implementing logical shifts using the exemplary reconfigurable segmented scalable shifter architecture.

**[0068]** Referring first to FIGURE 9, an example of segmented arithmetic data shifting is shown. In particular, FIGURE 9 shows reconfigurable segmented scalable shifter 400 configured as an 8 bit 2 segment implementation wherein segment 1 provides a 3 bit arithmetic shift to the right and segment 2 provides a 2 bit arithmetic shift to the right (e.g., shifter size  $N=8$ , number of segments  $M=2$ , segment 1 size  $N_1=5$ , segment 1 shift value  $S_1=3$ , segment 1 shift direction  $D_1=Right$ , and segment 1 shift type  $T_1=Arithmetic$ , segment 2 size  $N_2=3$ , segment 2 shift value  $S_2=2$ , segment 2 shift direction  $D_2=Right$ , and segment 2 shift type  $T_2=Arithmetic$ ). It should be appreciated that, although the example of FIGURE 9 shows a configuration in which both segments implement a same type of shift

(e.g., arithmetic) and a shift in the same direction (e.g., right), there is no limitation with respect to such a configuration according to embodiments of the invention.

**[0069]** As with the previous examples, the input data (X) of the example of FIGURE 9 comprises 8 bits, wherein the input data may be represented as X[7:0] (e.g., X[7:0]={X[7], X[6], X[5], X[4], X[3], X[2], X[1], X[0]}) and the output data may be represented as Y[7:0] (e.g., Y[7:0]={Y[7], Y[6], Y[5], Y[4], Y[3], Y[2], Y[1], Y[0]}). In the example of FIGURE 9, the number of segments (M) is 2, wherein segment 1 comprises 5 bits and segment 2 comprises 3 bits such that X<sub>1</sub>[4:0] is the input of segment 1 and X<sub>2</sub>[2:0] is the input of segment 2, and Y<sub>1</sub>[4:0] is the output data of segment 1 and Y<sub>2</sub>[2:0] is the output data of segment 2. Accordingly, X[7:0]={X[7], X[6], X[5], X[4], X[3], X[2], X[1], X[0]}={X<sub>2</sub>[2:0], X<sub>1</sub>[4:0]}, wherein X<sub>1</sub>[4:0]={X[4], X[3], X[2], X[1], X[0]} and X<sub>2</sub>[2:0]={X[7], X[6], X[5]}. Similarly, Y[7:0]={Y[7], Y[6], Y[5], Y[4], Y[3], Y[2], Y[1], Y[0]}={Y<sub>2</sub>[2:0], Y<sub>1</sub>[4:0]}, wherein Y<sub>1</sub>[4:0]={Y[4], Y[3], Y[2], Y[1], Y[0]}, and Y<sub>2</sub>[2:0]={Y[7], Y[6], Y[5]}.

**[0070]** FIGURE 8 shows an example of a shifter stage, as may be utilized in an embodiment of the reconfigurable segmented scalable shifter of FIGURE 9, implemented using a logarithmic shifter configuration. The number of stages of the logarithmic shifter is  $K=\lceil \log_2(N) \rceil$ , wherein in the exemplary embodiment  $N=8$ , and thus  $K=\log_2(8)=3$ , as discussed above. The 3 stages of a logarithmic shifter are shown in right shift portion 521 of shifter stage 420 illustrated in FIGURE 8, wherein YR<sub>1</sub>[7:0] = output of stage 1 of the right shift portion, YR<sub>2</sub>[7:0] = output of stage 2 of the right shift portion, and YR<sub>3</sub>[7:0] = output of stage 3 of the right shift portion. It should be noted that left shift portion 522 of shifter stage 420 shown in FIGURE 8 is not utilized in the example of FIGURE 9 in light of the functionality of the left shift portion not being needed to implement the right arithmetic shift.

**[0071]** As previously discussed, embodiments of reconfigurable segmented scalable shifters may provide SR<sub>k</sub>[n] as the right shift portion control signal of stage k, path n. Accordingly, SR<sub>1</sub>[7:0] = control signals for the paths of right shift stage 1, SR<sub>2</sub>[7:0] = control signals for the paths of right shift stage 2, and SR<sub>3</sub>[7:0] = control signals for the paths of right shift stage 3 in the 3 stages of the right shift portion of shifter stage 420 shown in FIGURE 8. If the control signal of a path is “0”, the data will propagate along the same path to next stage. However, if the control signal of the path is “1”, the data of the other path coupled to the multiplexer will propagate along that path to the next stage. The left shift portion control signal SL<sub>k</sub>[n] is unneeded in this example and may be any value (i.e., “don’t care”).

**[0072]** In this segmented example, SR<sub>1</sub> = 3 = 3'b011 (i.e., segment 1 shift value S<sub>1</sub>=3 and segment 1 shift direction D<sub>1</sub>=Right) and SR<sub>2</sub> = 2 = 3'b010 (i.e., segment 2 shift value S<sub>2</sub>=2, segment 2 shift direction D<sub>2</sub>=Right). The control signals for the stages of the segmented shifter may be represented as SR<sub>1</sub>[7:0] = 0001\_1111 (stage 1), SR<sub>2</sub>[7:0] = 1111\_1111 (stage 2), and SR<sub>3</sub>[7:0] = 0000\_0000 (stage 3) for the right shift portion. It can be appreciated that segmented data shifting is provided for the 5 bits of segment 1 by the right most 5 bits of each of the foregoing control signals, and for the 3 bits of segment 2 by the left most 3 bits of the foregoing control signals. Implementing the data shifts in accordance with the shift right control signals (SR<sub>1</sub>, SR<sub>2</sub>, and SR<sub>3</sub>) provides 3 bit right shift of X[3] to Y[0] and X[4] to Y[1] for segment 1 and 2 bit right shift of X[7] to Y[5] for segment 2 as illustrated by the bolded paths of right shift portion 521 of FIGURE 8.

**[0073]** The segmented reconfigurable segmented scalable shifter configuration of this example provides arithmetic shifts and thus, although the bits actually shifted (e.g., the outputs of path 0 and path 1 for segment 1 and path 5 for segment 2, as shown by the circled stage 3 outputs in right shift portion 521 of FIGURE 8), a sign bit (e.g., sign-bit X[7] for segment 2 and sign bit X[4] for segment 1) is inserted as the leftmost bit for each right shift operation (e.g., the outputs of path 2, path 3, and path 4 for segment 1 and path 6 and path 7 for segment 2, as shown by the circled stage 3 outputs in left shift portion 522 of FIGURE 8). The data output positions tied to a respective sign bit X[N] may be determined according to YL<sub>K</sub>[N-1:0], wherein the data bit for YL<sub>K</sub> is replaced with the respective sign bit, rather than the output of the left shift portion as in the previous cyclic shift examples, for merging with the output of the right shift portion. Accordingly, output stage 430 of embodiments operates to merge the results of right shifter portion 521 and the sign bit for respective segments to provide the arithmetic shift results, such as through the use of instances of multiplexer 1003 as shown in FIGURE 10. The merging of the shifter results and sign bits in this segmented example may be

controlled by an output selection control signal  $S[i]$ , wherein :  $S[i] = 1$  for  $i \geq SL1$ ,  $i = \{0, 1, \dots, 4\}$ ,  $SL1 = N_1 - S_1$  (segment 1) and  $S[i] = 1$  for  $i \geq SL2+5$ ,  $i = \{5, 6, 7\}$ ,  $SL2 = N_2 - S_2$  (segment 2). It can be appreciated that the data of  $Y[7:0]$  (i.e.,  $Y[7]$ ,  $Y[6]$ ,  $Y[5]$ ,  $Y[4]$ ,  $Y[3]$ ,  $Y[2]$ ,  $Y[1]$ ,  $Y[0]$ ) as stored and/or output by output stage 430 in this example corresponds to the 3 bit arithmetic shift to the right of segment 1 and the 2 bit arithmetic shift to the right of segment 2 illustrated in FIGURE 9.

**[0074]** Referring now to FIGURE 11, another example of segmented arithmetic data shifting is shown. In particular, FIGURE 11 shows reconfigurable segmented scalable shifter 400 configured as an 8 bit 2 segment implementation wherein segment 1 provides a 2 bit arithmetic shift to the left and segment 2 provides a 1 bit arithmetic shift to the left (e.g., shifter size  $N=8$ , number of segments  $M=2$ , segment 1 size  $N_1=5$ , segment 1 shift value  $S_1=2$ , segment 1 shift direction  $D_1=Left$ , and segment 1 shift type  $T_1=Arithmetic$ , segment 2 size  $N_2=3$ , segment 2 shift value  $S_2=1$ , segment 2 shift direction  $D_2=Left$ , and segment 2 shift type  $T_2=Arithmetic$ ). It should be appreciated that, although the example of FIGURE 11 shows a configuration in which both segments implement a same type of shift (e.g., arithmetic) and a shift in the same direction (e.g., left), there is no limitation with respect to such a configuration according to embodiments of the invention.

**[0075]** As with the previous examples, the input data ( $X$ ) of the example of FIGURE 11 comprises 8 bits, wherein the input data may be represented as  $X[7:0]$  (e.g.,  $X[7:0] = \{X[7], X[6], X[5], X[4], X[3], X[2], X[1], X[0]\}$ ) and the output data may be represented as  $Y[7:0]$  (e.g.,  $Y[7:0] = \{Y[7], Y[6], Y[5], Y[4], Y[3], Y[2], Y[1], Y[0]\}$ ). In the example of FIGURE 11, the number of segments ( $M$ ) is 2, wherein segment 1 comprises 5 bits and segment 2 comprises 3 bits such that  $X_1[4:0]$  is the input of segment 1 and  $X_2[2:0]$  is the input of segment 2, and  $Y_1[4:0]$  is the output data of segment 1 and  $Y_2[2:0]$  is the output data of segment 2. Accordingly,  $X[7:0] = \{X[7], X[6], X[5], X[4], X[3], X[2], X[1], X[0]\} = \{X_2[2:0], X_1[4:0]\}$ , wherein  $X_1[4:0] = \{X[4], X[3], X[2], X[1], X[0]\}$  and  $X_2[2:0] = \{X[7], X[6], X[5]\}$ . Similarly,  $Y[7:0] = \{Y[7], Y[6], Y[5], Y[4], Y[3], Y[2], Y[1], Y[0]\} = \{Y_2[2:0], Y_1[4:0]\}$ , wherein  $Y_1[4:0] = \{Y[4], Y[3], Y[2], Y[1], Y[0]\}$ , and  $Y_2[2:0] = \{Y[7], Y[6], Y[5]\}$ .

**[0076]** FIGURE 8 shows an example of a shifter stage, as may be utilized in an embodiment of the reconfigurable segmented scalable shifter of FIGURE 11, implemented using a logarithmic shifter configuration. The number of stages of the logarithmic shifter is  $K = \lceil \log_2(N) \rceil$ , wherein in the exemplary embodiment  $N=8$ , and thus  $K = \log_2(8) = 3$ , as discussed above. The 3 stages of a logarithmic shifter are shown in left shift portion 522 of shifter stage 420 illustrated in FIGURE 8, wherein  $YL_1[7:0]$  = output of stage 1 of the left shift portion,  $YL_2[7:0]$  = output of stage 2 of the left shift portion, and  $YL_3[7:0]$  = output of stage 3 of the left shift portion. It should be noted that right shift portion 521 of shifter stage 420 shown in FIGURE 8 is not utilized in the example of FIGURE 11 in light of the functionality of the right shift portion not being needed to implement the left arithmetic shift.

**[0077]** As previously discussed, embodiments of reconfigurable segmented scalable shifters may provide  $SL_k[n]$  as the left shift portion control signal of stage  $k$ , path  $n$ . Accordingly,  $SL_1[7:0]$  = control signals for the paths of left shift stage 1,  $SL_2[7:0]$  = control signals for the paths of left shift stage 2, and  $SL_3[7:0]$  = control signals for the paths of left shift stage 3 in the 3 stages of the left shift portion of shifter stage 420 shown in FIGURE 8. If the control signal of a path is "0", the data will propagate along the same path to next stage. However, if the control signal of the path is "1", the data of the other path coupled to the multiplexer will propagate along that path to the next stage. The right shift portion control signal  $SR_k[n]$  is unneeded in this example and may be any value (i.e., "don't care").

**[0078]** In this segmented example,  $SL1 = 2 = 3'b010$  (i.e., segment 1 shift value  $S_1=2$  and segment 1 shift direction  $D_1=Left$ ) and  $SL2 = 1 = 3'b001$  (i.e., segment 2 shift value  $S_2=1$ , segment 2 shift direction  $D_2=Left$ ). The control signals for the stages of the segmented shifter may be represented as  $SL_1[7:0] = 1110\_0000$  (stage 1),  $SL_2[7:0] = 0001\_1111$  (stage 2), and  $SL_3[7:0] = 0000\_0000$  (stage 3) for the left shift portion. It can be appreciated that segmented data shifting is provided for the 5 bits of segment 1 by the right most 5 bits of each of the foregoing control signals, and for the 3 bits of segment 2 by the left most 3 bits of the foregoing control signals. Implementing the data shifts in accordance with the shift left control signals ( $SL_1$ ,  $SL_2$ , and  $SL_3$ ) provides 2 bit left shift of  $X[0]$  to

Y[2], X[1] to Y[3], and X[2] to Y[4] for segment 1 and 1 bit left shift of X[5] to Y[6] and X[6] to Y[7] for segment 2 as illustrated by the bolded paths of left shift portion 522 of FIGURE 8.

**[0079]** The segmented reconfigurable segmented scalable shifter configuration of this example provides arithmetic shifts and thus, although the bits actually shifted (e.g., the outputs of path 2, path 3, and path 4 for segment 1 and path 6 and path 7 for segment 2, as shown by the circled stage 3 outputs in left shift portion 522 of FIGURE 8), 0 is inserted as the rightmost bit for each left shift operation (e.g., the outputs of path 0 and path 1 for segment 1 and path 5 for segment 2, as shown by the circled stage 3 outputs in right shift portion 521 of FIGURE 8). The data output positions tied to 0 may be determined according to  $YR\_K[N-1:0]$ , wherein the data bit for  $YR\_K$  is replaced with 0, rather than the output of the left shift portion as in the previous cyclic shift examples, for merging with the output of the left shift portion. Accordingly, output stage 430 of embodiments operates to merge the results of left shifter portion 522 and 0 to provide the arithmetic shift results, such as through the use of instances of multiplexer 1204 as shown in FIGURE 12. The merging of the shifter results and 0 in this segmented example may be controlled by an output selection control signal  $S[i]$ , wherein:  $S[i] = 1$  for  $i \geq SL1$ ,  $i = \{0, 1, \dots, 4\}$ ,  $SL1 = S\_1$  (segment 1) and  $S[i] = 1$  for  $i \geq SL2+5$ ,  $i = \{5, 6, 7\}$ ,  $SL2 = S\_2$  (segment 2). It can be appreciated that the data of  $Y[7:0]$  (i.e.,  $Y[7]$ ,  $Y[6]$ ,  $Y[5]$ ,  $Y[4]$ ,  $Y[3]$ ,  $Y[2]$ ,  $Y[1]$ ,  $Y[0]$ ) as stored and/or output by output stage 430 in this example corresponds to the 2 bit arithmetic shift to the left of segment 1 and the 1 bit arithmetic shift to the left of segment 2 illustrated in FIGURE 11.

**[0080]** Having described examples of cyclic and arithmetic shifters, reference is now made to FIGURE 13 for an example implementing a logical shift using the exemplary reconfigurable segmented scalable shifter architecture. In particular, FIGURE 13 shows reconfigurable segmented scalable shifter 400 configured as an 8 bit 2 segment implementation wherein segment 1 provides a 3 bit logical shift to the right and segment 2 provides a 2 bit logical shift to the right (e.g., shifter size  $N=8$ , number of segments  $M=2$ , segment 1 size  $N\_1=5$ , segment 1 shift value  $S\_1=3$ , segment 1 shift direction  $D\_1=Right$ , and segment 1 shift type  $T\_1=Logical$ , segment 2 size  $N\_2=3$ , segment 2 shift value  $S\_2=2$ , segment 2 shift direction  $D\_2=Right$ , and segment 2 shift type  $T\_2=Logical$ ). It should be appreciated that, although the example of FIGURE 13 shows a configuration in which both segments implement a same type of shift (e.g., logical) and a shift in the same direction (e.g., right), there is no limitation with respect to such a configuration according to embodiments of the invention.

**[0081]** As with the previous examples, the input data (X) of the example of FIGURE 13 comprises 8 bits, wherein the input data may be represented as  $X[7:0]$  (e.g.,  $X[7:0] = \{X[7], X[6], X[5], X[4], X[3], X[2], X[1], X[0]\}$ ) and the output data may be represented as  $Y[7:0]$  (e.g.,  $Y[7:0] = \{Y[7], Y[6], Y[5], Y[4], Y[3], Y[2], Y[1], Y[0]\}$ ). In the example of FIGURE 13, the number of segments (M) is 2, wherein segment 1 comprises 5 bits and segment 2 comprises 3 bits such that  $X\_1[4:0]$  is the input of segment 1 and  $X\_2[2:0]$  is the input of segment 2, and  $Y\_1[4:0]$  is the output data of segment 1 and  $Y\_2[2:0]$  is the output data of segment 2. Accordingly,  $X[7:0] = \{X[7], X[6], X[5], X[4], X[3], X[2], X[1], X[0]\} = \{X\_2[2:0], X\_1[4:0]\}$ , wherein  $X\_1[4:0] = \{X[4], X[3], X[2], X[1], X[0]\}$  and  $X\_2[2:0] = \{X[7], X[6], X[5]\}$ . Similarly,  $Y[7:0] = \{Y[7], Y[6], Y[5], Y[4], Y[3], Y[2], Y[1], Y[0]\} = \{Y\_2[2:0], Y\_1[4:0]\}$ , wherein  $Y\_1[4:0] = \{Y[4], Y[3], Y[2], Y[1], Y[0]\}$ , and  $Y\_2[2:0] = \{Y[7], Y[6], Y[5]\}$ .

**[0082]** FIGURE 8 shows an example of a shifter stage, as may be utilized in an embodiment of the reconfigurable segmented scalable shifter of FIGURE 13, implemented using a logarithmic shifter configuration. The number of stages of the logarithmic shifter is  $K = \lceil \log_2(N) \rceil$ , wherein in the exemplary embodiment  $N=8$ , and thus  $K = \log_2(8) = 3$ , as discussed above. The 3 stages of a logarithmic shifter are shown in right shift portion 521 of shifter stage 420 illustrated in FIGURE 8, wherein  $YR\_1[7:0]$  = output of stage 1 of the right shift portion,  $YR\_2[7:0]$  = output of stage 2 of the right shift portion, and  $YR\_3[7:0]$  = output of stage 3 of the right shift portion. It should be noted that left shift portion 522 of shifter stage 420 shown in FIGURE 8 is not utilized in the example of FIGURE 13 in light of the functionality of the left shift portion not being needed to implement the right logical shift.

**[0083]** As previously discussed, embodiments of reconfigurable segmented scalable shifters may provide  $SR\_k[n]$  as the right shift portion control signal of stage k, path n. Accordingly,  $SR\_1[7:0]$  = control signals for the paths of right shift stage 1,  $SR\_2[7:0]$  = control signals for the paths of right shift stage 2, and  $SR\_3[7:0]$  = control

signals for the paths of right shift stage 3 in the 3 stages of the right shift portion of shifter stage 420 shown in FIGURE 8. If the control signal of a path is “0”, the data will propagate along the same path to next stage. However, if the control signal of the path is “1”, the data of the other path coupled to the multiplexer will propagate along that path to the next stage. The left shift portion control signal  $SL\_k[n]$  is unneeded in this example and may be any value (i.e., “don’t care”).

**[0084]** In this segmented example,  $SR1 = 3 = 3'b011$  (i.e., segment 1 shift value  $S\_1=3$  and segment 1 shift direction  $D\_1=Right$ ) and  $SR2 = 2 = 2'b010$  (i.e., segment 2 shift value  $S\_2=2$ , segment 2 shift direction  $D\_2=Right$ ). The control signals for the stages of the segmented shifter may be represented as  $SR\_1[7:0] = 0001\_1111$  (stage 1),  $SR\_2[7:0] = 1111\_1111$  (stage 2), and  $SR\_3[7:0] = 0000\_0000$  (stage 3) for the right shift portion. It can be appreciated that segmented data shifting is provided for the 5 bits of segment 1 by the right most 5 bits of each of the foregoing control signals, and for the 3 bits of segment 2 by the left most 3 bits of the foregoing control signals. Implementing the data shifts in accordance with the shift right control signals ( $SR\_1$ ,  $SR\_2$ , and  $SR\_3$ ) provides 3 bit right shift of  $X[3]$  to  $Y[0]$  and  $X[4]$  to  $Y[1]$  for segment 1 and 2 bit right shift of  $X[7]$  to  $Y[5]$  for segment 2 as illustrated by the bolded paths of right shift portion 521 of FIGURE 8.

**[0085]** The segmented reconfigurable segmented scalable shifter configuration of this example provides logical shifts and thus, although the bits actually shifted (e.g., the outputs of path 0 and path 1 for segment 1 and path 5 for segment 2, as shown by the circled stage 3 outputs in right shift portion 521 of FIGURE 8), a 0 is inserted as the leftmost bit for each right shift operation (e.g., the outputs of path 2, path 3, and path 4 for segment 1 and path 6 and path 7 for segment 2, as shown by the circled stage 3 outputs in left shift portion 522 of FIGURE 8). The data output positions tied to 0 may be determined according to  $YL\_K[N-1:0]$ , wherein the data bit for  $YL\_K$  is replaced with 0, rather than the output of the left shift portion as in the previous cyclic shift examples, for merging with the output of the right shift portion. Accordingly, output stage 430 of embodiments operates to merge the results of right shifter portion 521 and 0 for respective segments to provide the logical shift results, such as through the use of instances of multiplexer 1405 as shown in FIGURE 14. The merging of the shifter results and 0 in this segmented example may be controlled by an output selection control signal  $S[i]$ , wherein :  $S[i] = 1$  for  $i \geq SL1$ ,  $i = \{0, 1, \dots, 4\}$ ,  $SL1 = N\_1 - S\_1$  (segment 1) and  $S[i] = 1$  for  $i \geq SL2+5$ ,  $i = \{5, 6, 7\}$ ,  $SL2 = N\_2 - S\_2$  (segment 2). It can be appreciated that the data of  $Y[7:0]$  (i.e.,  $Y[7]$ ,  $Y[6]$ ,  $Y[5]$ ,  $Y[4]$ ,  $Y[3]$ ,  $Y[2]$ ,  $Y[1]$ ,  $Y[0]$ ) as stored and/or output by output stage 430 in this example corresponds to the 3 bit logical shift to the right of segment 1 and the 2 bit logical shift to the right of segment 2 illustrated in FIGURE 13.

**[0086]** Referring now to FIGURE 15, another example of segmented logical data shifting is shown. In particular, FIGURE 15 shows reconfigurable segmented scalable shifter 400 configured as an 8 bit 2 segment implementation wherein segment 1 provides a 2 bit logical shift to the left and segment 2 provides a 1 bit logical shift to the left (e.g., shifter size  $N=8$ , number of segments  $M=2$ , segment 1 size  $N\_1=5$ , segment 1 shift value  $S\_1=2$ , segment 1 shift direction  $D\_1=Left$ , and segment 1 shift type  $T\_1=Logical$ , segment 2 size  $N\_2=3$ , segment 2 shift value  $S\_2=1$ , segment 2 shift direction  $D\_2=Left$ , and segment 2 shift type  $T\_2=Logical$ ). It should be appreciated that, although the example of FIGURE 15 shows a configuration in which both segments implement a same type of shift (e.g., logical) and a shift in the same direction (e.g., left), there is no limitation with respect to such a configuration according to embodiments of the invention.

**[0087]** As with the previous examples, the input data ( $X$ ) of the example of FIGURE 15 comprises 8 bits, wherein the input data may be represented as  $X[7:0]$  (e.g.,  $X[7:0] = \{X[7], X[6], X[5], X[4], X[3], X[2], X[1], X[0]\}$ ) and the output data may be represented as  $Y[7:0]$  (e.g.,  $Y[7:0] = \{Y[7], Y[6], Y[5], Y[4], Y[3], Y[2], Y[1], Y[0]\}$ ). In the example of FIGURE 15, the number of segments ( $M$ ) is 2, wherein segment 1 comprises 5 bits and segment 2 comprises 3 bits such that  $X\_1[4:0]$  is the input of segment 1 and  $X\_2[2:0]$  is the input of segment 2, and  $Y\_1[4:0]$  is the output data of segment 1 and  $Y\_2[2:0]$  is the output data of segment 2. Accordingly,  $X[7:0] = \{X[7], X[6], X[5], X[4], X[3], X[2], X[1], X[0]\} = \{X\_2[2:0], X\_1[4:0]\}$ , wherein  $X\_1[4:0] = \{X[4], X[3], X[2], X[1], X[0]\}$  and  $X\_2[2:0] = \{X[7], X[6], X[5]\}$ . Similarly,  $Y[7:0] = \{Y[7], Y[6], Y[5], Y[4], Y[3], Y[2], Y[1], Y[0]\} = \{Y\_2[2:0], Y\_1[4:0]\}$ , wherein  $Y\_1[4:0] = \{Y[4], Y[3], Y[2], Y[1], Y[0]\}$ , and  $Y\_2[2:0] = \{Y[7], Y[6], Y[5]\}$ .

**[0088]** FIGURE 8 shows an example of a shifter stage, as may be utilized in an embodiment of the reconfigurable segmented scalable shifter of FIGURE 15, implemented using a logarithmic shifter configuration. The number of stages of the logarithmic shifter is  $K = \lceil \log_2(N) \rceil$ , wherein in the exemplary embodiment  $N=8$ , and thus  $K = \log_2(8) = 3$ , as discussed above. The 3 stages of a logarithmic shifter are shown in left shift portion 522 of shifter stage 420 illustrated in FIGURE 8, wherein  $YL\_1[7:0]$  = output of stage 1 of the left shift portion,  $YL\_2[7:0]$  = output of stage 2 of the left shift portion, and  $YL\_3[7:0]$  = output of stage 3 of the left shift portion. It should be noted that right shift portion 521 of shifter stage 420 shown in FIGURE 8 is not utilized in the example of FIGURE 15 in light of the functionality of the right shift portion not being needed to implement the left logical shift.

**[0089]** As previously discussed, embodiments of reconfigurable segmented scalable shifters may provide  $SL\_k[n]$  as the left shift portion control signal of stage  $k$ , path  $n$ . Accordingly,  $SL\_1[7:0]$  = control signals for the paths of left shift stage 1,  $SL\_2[7:0]$  = control signals for the paths of left shift stage 2, and  $SL\_3[7:0]$  = control signals for the paths of left shift stage 3 in the 3 stages of the left shift portion of shifter stage 420 shown in FIGURE 8. If the control signal of a path is “0”, the data will propagate along the same path to next stage. However, if the control signal of the path is “1”, the data of the other path coupled to the multiplexer will propagate along that path to the next stage. The right shift portion control signal  $SR\_k[n]$  is unneeded in this example and may be any value (i.e., “don’t care”).

**[0090]** In this segmented example,  $SL1 = 2 = 3'b010$  (i.e., segment 1 shift value  $S\_1=2$  and segment 1 shift direction  $D\_1=Left$ ) and  $SL2 = 1 = 3'b001$  (i.e., segment 2 shift value  $S\_2=1$ , segment 2 shift direction  $D\_2=Left$ ). The control signals for the stages of the segmented shifter may be represented as  $SL\_1[7:0] = 1110\_0000$  (stage 1),  $SL\_2[7:0] = 0001\_1111$  (stage 2), and  $SL\_3[7:0] = 0000\_0000$  (stage 3) for the left shift portion. It can be appreciated that segmented data shifting is provided for the 5 bits of segment 1 by the right most 5 bits of each of the foregoing control signals, and for the 3 bits of segment 2 by the left most 3 bits of the foregoing control signals. Implementing the data shifts in accordance with the shift left control signals ( $SL\_1$ ,  $SL\_2$ , and  $SL\_3$ ) provides 2 bit left shift of  $X[0]$  to  $Y[2]$ ,  $X[1]$  to  $Y[3]$ , and  $X[2]$  to  $Y[4]$  for segment 1 and 1 bit left shift of  $X[5]$  to  $Y[6]$  and  $X[6]$  to  $Y[7]$  for segment 2 as illustrated by the bolded paths of left shift portion 522 of FIGURE 8.

**[0091]** The segmented reconfigurable segmented scalable shifter configuration of this example provides logical shifts and thus, although the bits actually shifted (e.g., the outputs of path 2, path 3, and path 4 for segment 1 and path 6 and path 7 for segment 2, as shown by the circled stage 3 outputs in left shift portion 522 of FIGURE 8), 0 is inserted as the rightmost bit for each left shift operation (e.g., the outputs of path 0 and path 1 for segment 1 and path 5 for segment 2, as shown by the circled stage 3 outputs in right shift portion 521 of FIGURE 8). The data output positions tied to 0 may be determined according to  $YR\_K[N-1:0]$ , wherein the data bit for  $YR\_K$  is replaced with 0, rather than the output of the left shift portion as in the previous cyclic shift examples, for merging with the output of the left shift portion. Accordingly, output stage 430 of embodiments operates to merge the results of left shifter portion 522 and 0 to provide the arithmetic shift results, such as through the use of instances of multiplexer 1204 as shown in FIGURE 12. The merging of the shifter results and 0 in this segmented example may be controlled by an output selection control signal  $S[i]$ , wherein :  $S[i] = 1$  for  $i \geq SL1$ ,  $i = \{0, 1, \dots, 4\}$ ,  $SL1 = S\_1$  (segment 1) and  $S[i] = 1$  for  $i \geq SL2+5$ ,  $i = \{5, 6, 7\}$ ,  $SL2 = S\_2$  (segment 2). It can be appreciated that the data of  $Y[7:0]$  (i.e.,  $Y[7]$ ,  $Y[6]$ ,  $Y[5]$ ,  $Y[4]$ ,  $Y[3]$ ,  $Y[2]$ ,  $Y[1]$ ,  $Y[0]$ ) as stored and/or output by output stage 430 in this example corresponds to the 2 bit arithmetic shift to the left of segment 1 and the 1 bit arithmetic shift to the left of segment 2 illustrated in FIGURE 15.

**[0092]** FIGURE 16 shows details of an embodiment of reconfigurable segmented scalable shifter 400 as may be configured to provide data shifting in accordance with examples discussed above. In particular, reconfigurable segmented scalable shifter 400 of FIGURE 16 illustrates an 8 bit shifter configuration in which input stage 410 is configured to provide input data to both right shifter portion 521 and left shifter portion 522 of shifter stage 420 to thereby facilitate accommodation of reconfigurable shifter operation to support various types of data shifting (e.g., cyclic shifts, arithmetic shifts, and/or logical shifts, as shown in the above examples). Shifter stage 420 of FIGURE 16 includes an array of multiplexers 501 disposed in 3 stages of a logarithmic shifter configuration and responsive to control signals (e.g.,  $SR$  and/or  $SL$  control signals, as shown in the above examples) provided by controller 421 to facilitate reconfigurable data shifting operation. In order to simplify reconfigurable segmented scalable shifter 400 as shown in

FIGURE 16, output stage 430 is shown in a cyclic shift implementation configuration. That is output stage 430 of the illustrated embodiment includes an array of multiplexers 602 responsive to control signals (e.g.,  $S[i]$  output selection control signals, as shown in the above examples) provided by controller 421 to facilitate merging the results of right shifter portion 521 and left shifter portion 522 to provide cyclic shift results.

**[0093]** It should be readily understood from the above cyclic shift, arithmetic shift, and logical shift examples that the logic of shifter stage 420 may support each of these data shift types where output stage 430 is adapted to merge outputs of the right shift portion and left shift portion (e.g., cyclic shift), tie certain outputs to a sign-bit (e.g., right arithmetic shift), and tie certain outputs to 0 (e.g., left arithmetic shift and logical shift) as appropriate (e.g., based upon shift type and/or shift direction). FIGURE 17A shows a configuration of controllable data path elements as may be utilized in output stage 430 to facilitate embodiments of reconfigurable segmented scalable shifter 400 supporting arithmetic shifts. An instance of the multiplexer circuit of FIGURE 17A may, for example, be utilized in place of each of multiplexers 602 shown in output stage 430 to provide an output stage configuration supporting cyclic shifts, arithmetic shifts, and logical shifts (e.g., to control merging of data from shifter stage 420 and/or replacing particular bits with a respective sign bit or 0, as appropriate to the shift type being implemented). Controller 421 may accordingly provide output selection control signals  $S[i]$  for the particular shift type being implemented, as shown in the examples above. As shown in FIGURES 17B-17F, the shifters of the configuration of FIGURE 17A may be controlled to provide cyclic shifts (FIGURE 17B), arithmetic shifts (FIGURES 17C and 17D), and logical shifts (FIGURES 17E and 17F).

**[0094]** As can be seen from the above examples, reconfigurable segmented scalable shifter 400 of embodiments is reconfigurable for scalability in supporting data shifting with respect to various bit lengths of data and supports data shifting of differing bit lengths in parallel. For example, shifters of embodiments are reconfigurable with respect to a number of segments ( $M$ ) (e.g.,  $1 \leq M \leq N$ ), a size of each segment ( $N_m$ ) (e.g.,  $N \geq N_m \geq 1$ ), a shift value of each segment ( $S$ ) ( $1 \leq S \leq N$ ), a shift direction ( $D$ ) of each segment (e.g.,  $D$  is left or right), and/or a shift type ( $T$ ) of each segment (e.g.,  $T$  is logical, arithmetic, or cyclic). In the examples of reconfigurable segmented scalable shifter 400 discussed above, segmentation is implemented for data shifting with respect to differing bit lengths, wherein individual data shift control is provided with respect to each path of a data shifter stage to implement different data shift commands for the segments and control multiple data shifts in parallel. Embodiments of a reconfigurable segmented scalable shifter in accordance with the concepts herein may be implemented to accommodate relatively large data widths (e.g.,  $N=384$  for a 5G QC-LDPC decoder implementation). Accordingly, the control signal structure may become relatively complicated as configurations of a reconfigurable segmented scalable shifter are scaled up for such implementations. Embodiments may thus implement a less complicated shifter stage configuration which nevertheless is reconfigurable for scalability in supporting data shifting with respect to various bit lengths of data and supports data shifting of differing bit lengths in parallel.

**[0095]** FIGURE 18 illustrates a sectioned shifter stage configuration which is readily scalable to accommodate large data widths. Shifter stage 420 shown in FIGURE 18 implements a sectioned configuration in which each of the left shift and right shift portions (either one of which is represented in the illustration) are divided into multiple sections, wherein the data paths of each section share the same control signals. For example, the shifter may be divided into a plurality of sections of equal data widths, different data widths, or a combination thereof where, although each section may be controlled individually to provide different data shifting (e.g., direction and/or shift value), all data of a section controlled together for same data shifting (e.g., direction and shift value). Such configurations may, for example, provide a satisfactory tradeoff between the number of segments and hardware cost.

**[0096]** Segmentation for data shifting with respect to differing bit lengths may be implemented by configuring a group of one or more sections for each segment, wherein the group of sections for a particular segment provides an aggregate data width equal to or greater than the data width of the segment. Accordingly, one or more messages of various data widths from input data may be provided data shifting in each segment as hosted by a respective group of one or more sections, wherein the messages may be provided individual data shifting in parallel through appropriately controlling the sections for each segment.

**[0097]** The number of sections (Se) and the section data width (W) are preferably related to the shifter data width (N) so that the total data width is sectioned (e.g.,  $N = Se * W$ ). In the exemplary embodiment of shifter stage 420 shown in FIGURE 18, the shifter data width  $N=384$ , the number of sections  $Se = 24$ , and the data width of each section  $W = 16$  (e.g.,  $384=24*16$ ). M number of segments may be hosted by various groups of sections of shifter section 420, wherein the number of segments is less than or equal to the shifter data width (e.g.,  $1 \leq M \leq N$ ) and the aggregate size of the segments is less than or equal to the shifter data width (e.g.,  $N_1+N_2+\dots+N_M \leq N$ ).

**[0098]** In accordance with embodiments of the invention, a segment is aligned with the LSB of a first section of the corresponding group of sections and any portion of the aggregate data width of the group of sections which exceeds the corresponding section bit width remains unused at the MSB end of the last section of the group of sections. This configuration is illustrated in FIGURE 18, wherein M segments (e.g., segment 1, segment 2, . . . segment M) of different data widths are hosted by corresponding groups of sections of shifter stage 420.

**[0099]** As shown in the example of FIGURE 18, the  $N_1$  number of bits of message  $X_1$  is less than the section data width W (e.g.,  $N_1=10$  and  $W=16$ ), and thus the group of sections hosting segment 1 comprises section 1, wherein the LSB of message  $X_1$  aligns with the LSB position of section 1 and a portion of the data width of section 1 greater than the number of bits of message  $X_1$  remains unused (e.g.,  $(1*16)-10=6$  unused bits). Each shifter data path of section 1 of embodiments is controlled using same control signals. Thus a single instance of control signals is used to provide data shifting for segment 1 (e.g., as opposed to 10 separate data shift path control signals as may be implemented by examples shown above).

**[00100]** In contrast to exemplary message  $X_1$ , the  $N_2$  number of bits of message  $X_2$  is greater than the section data width W (e.g.,  $N_2=38$  and  $W=16$ ), and thus the group of sections hosting segment 2 comprises section 2, section 3, and section 4 (e.g.,  $CEILING.MATH(38/16)=3$  sections), wherein the LSB of message  $X_2$  aligns with the LSB position of section 2 (the first section of the segment) and a portion of the aggregate data width of the sections greater than the number of bits of message  $X_2$  remains unused in section 4 (the last section hosting the segment) (e.g.,  $(3*16)-38=10$  unused bits). Each shifter data path of section 2 of embodiments is controlled using same control signals, each shifter data path of section 3 of embodiments is controlled using same control signals, and each shifter data path of section 4 of embodiments is controlled using same control signals. Thus 3 instances of control signals (e.g., an instance of control signals for each section hosting the segment) are used to provide data shifting for segment 2 (e.g., as opposed to 38 separate data shift path control signals as may be implemented by examples shown above).

**[00101]** The  $N_M$  number of bits of message  $X_M$  is an integer multiple of the section data width W (e.g.,  $N_M=32$  and  $W=16$ ), and thus the group of sections hosting segment M comprises section  $Se-2$  and section  $Se-1$  (e.g.,  $CEILING.MATH(32/16)=2$  sections), wherein the LSB of message  $X_M$  aligns with the LSB position of section  $Se-2$  (the first section of the segment) and the MSB of message  $X_M$  aligns with the MSB position of section  $Se-1$  (the last section hosting the segment) (e.g.,  $(2*16)-32=0$  unused bits). Each shifter data path of section  $Se-2$  of embodiments is controlled using same control signals and each shifter data path of section  $Se-1$  of embodiments is controlled using same control signals. Thus 2 instances of control signals (e.g., an instance of control signals for each section hosting the segment) are used to provide data shifting for segment M (e.g., as opposed to 32 separate data shift path control signals as may be implemented by examples shown above).

**[00102]** FIGURE 19 shows an example of a shifter stage, as may be utilized in a sectioned embodiment of the reconfigurable segmented scalable shifter of FIGURE 18, implemented using a logarithmic shifter configuration. The data width of the shifter illustrated in FIGURE 19 is 16, wherein 4 sections of 4 bits are implemented (e.g.,  $N=16$ ,  $Se=4$ , and  $W=4$ ). The number of stages of the logarithmic shifter is  $K=ceil[\log_2(N)]$ , wherein in the exemplary embodiment  $N=16$ , and thus  $K=log_2(8)=4$ . The 4 stages of a logarithmic shifter are shown in right shift portion 1921 and left shift portion 1922 of shifter stage 420 illustrated in FIGURE 19, wherein  $YR_1[15:0]$  = output of stage 1 of the right shift portion,  $YR_2[15:0]$  = output of stage 2 of the right shift portion,  $YR_3[15:0]$  = output of stage 3 of the right shift portion,  $YR_4[15:0]$  = output of stage 4 of the right shift portion,  $YL_1[15:0]$  = output of stage 1 of the left shift

portion, YL\_2[15:0] = output of stage 2 of the left shift portion, YL\_3[15:0] = output of stage 3 of the left shift portion, and YL\_4[15:0] = output of stage 4 of the left shift portion.

**[00103]** In the embodiment shown in FIGURE 19, shifter stage 420 is configured as a 16 bit, 4 section, 3 segment implementation wherein segment 1 provides a 4 bit right cyclic shift with respect to a 7 bit message using section 1 and section 2, segment 2 provides a 2 bit right cyclic shift with respect to a 4 bit message using section 3, and segment 3 provides a 1 bit right cyclic shift with respect to a 3 bit message using section 4 (e.g., shifter size  $N=16$ , number of sections  $Se=4$ , section data width  $W=4$ , number of segments  $M=3$ , segment 1 size  $N_1=7$ , segment 1 shift value  $S_1=4$ , segment 1 shift direction  $D_1=Right$ , segment 1 shift type  $T_1=Cyclic$ , and segment 1 section group = [section 1, section 2], segment 2 size  $N_2=4$ , segment 2 shift value  $S_2=2$ , segment 2 shift direction  $D_2=Right$ , segment 2 shift type  $T_2=Cyclic$ ), and segment 2 section group = [section 3], and segment 3 size  $N_3=3$ , segment 3 shift value  $S_3=1$ , segment 3 shift direction  $D_3=Right$ , segment 3 shift type  $T_3=Cyclic$ ), and segment 3 section group = [section 4]).

**[00104]** It should be appreciated that, although the example of FIGURE 19 shows a configuration in which each segment implements a same type of shift (e.g., cyclic) and a shift in the same direction (e.g., right), there is no limitation with respect to such a configuration according to embodiments of the invention. For example, a reconfigurable segmented scalable shifter of embodiments may be configured to provide different sizes of segments, different shift directions by the segments, different shift values by the segments, and/or different types of shifts by the segments.

**[00105]** The input data (X) of the example of FIGURE 19 comprises 16 bits, wherein the input data may be represented as  $X[15:0]$  (e.g.,  $X[15:0]=\{X[15], X[14], \dots, X[0]\}$ ) and the output data may be represented as  $Y[15:0]$  (e.g.,  $Y[15:0]=\{Y[15], Y[14], \dots, Y[0]\}$ ). In the example of FIGURE 19 the number of segments (M) is 3, wherein segment 1 comprises 7 bits, segment 2 comprises 4 bits, and segment 3 comprises 3 bits such that  $X_1[6:0]$  is the input of segment 1,  $X_2[3:0]$  is the input of segment 2, and  $X_3[2:0]$  is the input of segment 3, and  $Y_1[6:0]$  is the output data of segment 1,  $Y_2[3:0]$  is the output data of segment 2, and  $Y_3[2:0]$  is the output data of segment 3. The section group hosting segment 1 is section 1 and section 2, the section group hosting segment 2 is section 3, and the section group hosting segment 3 is section 4. Accordingly, implementing offsets for the segment and section mapping (e.g., offset\_m: offset\_4, 3, 2, 1, N-m:  $N_4, 3, 2, 1$ , wherein offset\_m is the value of the beginning path  $i$  of each segment),  $X_1[6:0]=\{X[6], X[5], X[4], X[3], X[2], X[1], X[0]\}$ ,  $X_2[3:0]=\{X[11], X[10], X[9], X[8]\}$ , and  $X_3[2:0]=\{X[14], X[13], X[12]\}$ . Similarly, again implementing offsets for the segment and section mapping,  $Y_1[6:0]=\{Y[6], Y[5], Y[4], Y[3], Y[2], Y[1], Y[0]\}$ ,  $Y_2[3:0]=\{Y[11], Y[10], Y[9], Y[8]\}$  and  $Y_3[2:0]=\{Y[14], Y[13], Y[12]\}$ .

**[00106]** In this segmented example,  $SR1 = 4 = 4'b0100$  (i.e., segment 1 shift value  $S_1=4$  and segment 1 shift direction  $D_1=Right$ ),  $SR2 = 2 = 4'b0010$  (i.e., segment 2 shift value  $S_2=2$ , segment 2 shift direction  $D_2=Right$ ), and  $SR3 = 1 = 4'b0001$  (i.e., segment 3 shift value  $S_3=1$ , segment 3 shift direction  $D_3=Right$ ). This segmented example provides cyclic shifts, and thus left data shifting is utilized to provide the cyclic aspect of the data shift. In this example,  $SL1 = 7 - 4 = 3 = 4'b0011$  (i.e., segment 1 size  $N_1=7$ , segment 1 shift value  $S_1=3$ , and segment 1 shift type  $T_1=Cyclic$ ),  $SL2 = 4 - 2 = 2 = 4'b0010$  (i.e., segment 2 size  $N_2=4$ , segment 2 shift value  $S_2=2$ , and segment 2 shift type  $T_2=Cyclic$ ), and  $SL3 = 3 - 1 = 2 = 4'b0010$  (i.e., segment 3 size  $N_3=3$ , segment 3 shift value  $S_3=1$ , and segment 3 shift type  $T_3=Cyclic$ ). Using the individual data shifter path control of the previous examples, the control signals for the stages of the segmented shifter may be represented as  $SR_1[15:0] = 1111\_0000\_0000\_0000$  (stage 1),  $SR_2[15:0] = 0000\_1111\_0000\_0000$  (stage 2),  $SR_3[15:0] = 0000\_0000\_1111\_1111$  (stage 3), and  $SR_4[15:0] = 0000\_0000\_0000\_0000$  (stage 4) for the right shift portion and  $SL_1[15:0] = 0000\_0000\_1111\_1111$  (stage 1),  $SL_2[15:0] = 1111\_1111\_1111\_1111$  (stage 2),  $SL_3[15:0] = 0000\_0000\_0000\_0000$  (stage 3), and  $SL_4[15:0] = 0000\_0000\_0000\_0000$  for the left shift portion.

**[00107]** This embodiment, however, implements grouping by sections and thus the control signals may be simplified to  $SRG_1[3:0]=1000$  (stage 1),  $SRG_2[3:0]=0100$  (stage 2),  $SRG_3[3:0]=0011$  (stage 3), and  $SRG_4[3:0]=0000$  (stage 4) for the right shift portion and  $SLG_1[3:0]=0011$  (stage 1),  $SLG_2[3:0]=1111$  (stage 2),

SLG\_3[3:0]=0000 (stage 3), and [3:0]=0000 (stage 4) for the left shift portion. It can be appreciated that segmented data shifting is provided for the 7 bits of segment 1 served by section 1 and section 2 by the right most 2 bits of each of the foregoing control signals, for the 4 bits of segment 2 served by section 3 by the third from the right bit of each of the foregoing control signals, and for the 3 bits of segment 3 served by section 4 by the left most bit of each of the foregoing control signals.

**[00108]** Output stage 430 of embodiments operates to merge the results of right shifter portion 1921 and left shifter portion 1922 to provide the cyclic shift results, wherein the unused portion any section is discarded. Accordingly, output stage 430 may comprise instances of multiplexer 602 disposed at the corresponding outputs of each path of right shift portion 1921 and left shift portion 1922 and provided with a control signal to select output of either right shifted data or left shifted data, as shown in the version of output stage 430 FIGURE 20 scaled for the 16 data width of shifter stage 420 of FIGURE 19. The merging of the shifter results may be controlled by an output selection control signal  $S[i]$ , wherein  $S[i] = 1$  if  $(SL + \text{offset}_m) \geq SL$ . Although not shown in order to simplify the illustration, it should be appreciated that output stage 430 of this embodiment may include a configuration of controllable data path elements corresponding to that of FIGURE 17A to facilitate embodiments of reconfigurable segmented scalable shifter 400 supporting cyclic shifts, arithmetic shifts, and logical shifts.

**[00109]** Although the example of FIGURES 18 and 19 shows reconfigurable segmented scalable shifters configured for the data width or size of the input data (e.g., segment 1 input  $X_1$ , segment 2 input  $X_2$ , and segment 3 input  $X_3$  of FIGURE 19) being different, it should be appreciated that the data width or size of all input data may be the same (e.g., segment 1 input  $X_1$  data width = segment 2 input  $X_2$  data width = segment 3 input  $X_3$  data width) according to embodiments of the invention. In accordance with some embodiments configured for the same data width of all input data, the control signals of every stage for all sections of a shifter stage may be the same (e.g., where the same shift is provided with respect to each input message) or the size of the control signals of every stage for all sections of a shifter stage may be the same, although the control signals themselves may differ, (e.g., where different shifts are provided with respect to some or all input messages).

**[00110]** It should be appreciated that, although the sections of the example sectioned reconfigurable segmented scalable configuration of FIGURES 18 and 19 comprise a same data width, embodiments may comprise sections of different data widths. For example, each of section 1 through section Se of FIGURE 18 may be of different data widths. As another example, some sections of section 1 through section Se may be of different data widths while other sections of section 1 through section Se may be of the same data width.

**[00111]** As can be appreciated from the above described example, sectioned embodiments of a reconfigurable segmented scalable shifter may combine a plurality of successive sections to form a data shifter for accommodating data widths larger than the individual sections. Such reconfigurable segmented scalable shifter configurations provide for fully reconfigurable data width and shift command of each message of input data for flexible and efficient utilization of hardware for parallel processing data input of various bit lengths.

**[00112]** Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

## CLAIMS

What is claimed is:

1. A reconfigurable segmented scalable shifter comprising:  
a shifter stage having N-bit data input, N-bit data output, and control signal input, wherein the shifter stage is configured to implement different data shifts for multiple data segments of the N-bit data input in parallel in response to a plurality of individual shifting commands of a control signal, and  
a controller coupled to the control signal input of the shifter stage, wherein the controller is configured to provide the plurality of individual shifting commands to the shifter stage, wherein each shifting command of the plurality of individual shifting commands implements a different data shift of the different data shifts for the multiple data segments of the N-bit data input, and wherein the different data shifts implemented by the shifter stage in accordance with the plurality of individual shifting commands provide shifted N-bit data at the N-bit data output having the different data shifts for the multiple data segments.
2. The reconfigurable segmented scalable shifter of claim 1, wherein the plurality of individual shifting commands include a control signal for individually controlling each data path of the shifter stage.
3. The reconfigurable segmented scalable shifter of claim 1, wherein data paths of the shifter stage are subdivided into a plurality of sections each including a plurality of data paths, wherein the plurality of individual shifting commands include a control signal for individually controlling each section of the plurality of sections, and wherein each data path of the plurality of data paths of a section is controlled by a same control signal of the plurality of individual shifting commands.
4. The reconfigurable segmented scalable shifter of claim 3, wherein the plurality of sections comprises S number of sections, wherein a data width of each section is W-bits, and wherein  $N=S*W$ .
5. The reconfigurable segmented scalable shifter of claim 4, wherein each data segment of the multiple data segments starts from a least significant bit (LSB) of a section.
6. The reconfigurable segmented scalable shifter of claim 3, wherein two or more sections of the plurality of sections have a different data width with respect to each other.
7. The reconfigurable segmented scalable shifter of claim 1, wherein the shifter stage comprises a shifter architecture selected from the group consisting of a logarithmic shifter configuration, a barrel shifter configuration, and a combinational shifter configuration.
8. The reconfigurable segmented scalable shifter of claim 1, wherein the multiple different data shifts implemented in parallel include different data shifts selected from the group consisting of different data shift direction for a first segment and a second segment of the multiple data segments, different shift type for the first segment and the second segment, and different shift value for the first segment and the second segment.
9. The reconfigurable segmented scalable shifter of claim 8, wherein the first segment and second segment have different data widths.
10. The reconfigurable segmented scalable shifter of claim 1, wherein each segment of the multiple data segments has a same data width.

11. The reconfigurable segmented scalable shifter of claim 1, further comprising:  
an N-bit data output stage coupled to the N-bit data output of the shifter stage, wherein the N-bit data output stage is configured to select data for output based upon data shifting types of the multiple different data shifts.
12. The reconfigurable segmented scalable shifter of claim 11, wherein the data shifting types are selected from the group consisting of arithmetic shift, logical shift, and cyclic shift.
13. The reconfigurable segmented scalable shifter of claim 11, wherein each individual shifting command of the plurality of individual shifting commands of the control signal includes a shift value signal and an output selection signal, wherein the shift value for an individual shifting command specifies an amount of shift provided by the shifter stage for a respective data shift of the multiple different data shifts, and wherein the output selection signal selects data for output corresponding to a data shifting type for the respective data shift of the multiple different data shifts.
14. The reconfigurable segmented scalable shifter of claim 11, wherein the output selection signal controls the output stage to select a sign bit for output instead of an output of the shifter stage when the data shift type is an arithmetic shift and the shift direction is right, to select a 0 bit value for output instead of an output of the shifter stage when the data shift type is an arithmetic shift and the shift direction is left, to select a 0 bit value for output instead of an output of the shifter stage when the data shift type is a logical shift and the shift direction is right, and to select a 0 bit value for output instead of an output of the shifter stage when the data shift type is a logical shift and the shift direction is left.
15. The reconfigurable segmented scalable shifter of claim 13, wherein the shifter stage comprises:  
a right shift portion, wherein the shift value signal for each individual shifting command of the plurality of individual shifting commands includes a right shift value to control a right shift aspect of the right shift portion for a respective data shift of the multiple different data shifts; and  
a left shift portion, wherein the shift value signal for each individual shifting command of the plurality of individual shifting commands includes a left shift value to control a left shift aspect of the left shift portion for a respective data shift of the multiple different data shifts.
16. The reconfigurable segmented scalable shifter of claim 15, wherein the right shift portion and the left shift portion each has K stages, where  $K = \text{ceiling}(\log_2(N))$ .
17. The reconfigurable segmented scalable shifter of claim 15, further comprising:  
an N-bit data input stage coupled to the N-bit data input of the shifter stage, wherein the N-bit data input stage is configured to provide N-bit input data comprising the multiple data segments to both the right shift portion and the left shift portion of the shifter stage.
18. A method comprising:  
providing, by a controller coupled to a control signal input of a shifter stage of a reconfigurable segmented scalable shifter, a control signal having a plurality of individual shifting commands each controlling a different data shift of different data shifts for multiple data segments of N-bit data input to the shifter stage; and  
implementing, by the shifter stage in response to the control signal, different data shifts for the multiple data segments of the N-bit data input in parallel.
19. The method of claim 18, wherein the plurality of individual shifting commands include a control signal for individually controlling each data path of the shifter stage.

20. The method of claim 18, wherein data paths of the shifter stage are subdivided into a plurality of sections each including a plurality of data paths, wherein the plurality of individual shifting commands include a control signal for individually controlling each section of the plurality of sections, and wherein each data path of the plurality of data paths of a section is controlled by a same control signal of the plurality of individual shifting commands.

21. The method of claim 20, wherein the plurality of sections comprises S number of sections, wherein a data width of each section is W-bits, and wherein  $N=S*W$ .

22. The method of claim 21, wherein each data segment of the multiple data segments starts from a least significant bit (LSB) of a section.

23. The method of claim 20, wherein two or more sections of the plurality of sections have a different data width with respect to each other.

24. The method of claim 18, wherein the multiple different data shifts implemented in parallel include different data shifts selected from the group consisting of different data shift direction for a first segment and a second segment of the multiple data segments, different shift type for the first segment and the second segment, and different shift value for the first segment and the second segment.

25. The method of claim 24, wherein the first segment and second segment have different data widths.

26. The method of claim 18, wherein each segment of the multiple data segments has a same data width.

27. The method of claim 18, further comprising:  
selecting, by an N-bit data output stage coupled to the shifter stage, data for output based upon data shifting types of the multiple different data shifts.

28. The method of claim 27, wherein each individual shifting command of the plurality of individual shifting commands of the control signal includes a shift value signal and an output selection signal, wherein the shift value for an individual shifting command specifies an amount of shift provided by the shifter stage for a respective data shift of the multiple different data shifts, and wherein the output selection signal selects data for output corresponding to a data shifting type for the respective data shift of the multiple different data shifts.

29. The method of claim 27, wherein the output selection signal controls the output stage to select a sign bit for output instead of an output of the shifter stage when the data shift type is an arithmetic shift and the shift direction is right, to select a 0 bit value for output instead of an output of the shifter stage when the data shift type is an arithmetic shift and the shift direction is left, to select a 0 bit value for output instead of an output of the shifter stage when the data shift type is a logical shift and the shift direction is right, and to select a 0 bit value for output instead of an output of the shifter stage when the data shift type is a logical shift and the shift direction is left.

30. The method of claim 28, further comprising:  
providing, by an N-bit data input stage coupled to the shifter stage, N-bit input data comprising the multiple data segments to both a right shift portion and a left shift portion of the shifter stage.

31. A system comprising:

a shifter stage having N-bit data input, N-bit data output, control signal input, a right shift portion, and a left shift portion, wherein the shifter stage is configured to implement different data shifts for multiple data segments of the N-bit data input in parallel in response to a plurality of individual shifting commands of a control signal,

an N-bit data input stage coupled to the N-bit data input of the shifter stage, wherein the N-bit data input stage is configured to provide N-bit input data comprising the multiple data segments to both the right shift portion and the left shift portion of the shifter stage;

an N-bit data output stage coupled to the N-bit data output of the shifter stage, wherein the N-bit data output stage is configured to select data for output based upon data shifting types of the different data shifts; and

a controller coupled to the control signal input of the shifter stage, wherein the controller is configured to provide the plurality of individual shifting commands to the shifter stage, wherein each shifting command of the plurality of individual shifting commands implements a different data shift of the different data shifts for the multiple data segments of the N-bit data input, and wherein the different data shifts implemented by the shifter stage in accordance with the plurality of individual shifting commands provide shifted N-bit data at the N-bit data output having the different data shifts for the multiple data segments.

32. The system of claim 31, wherein the plurality of individual shifting commands include a control signal for individually controlling each data path of the shifter stage.

33. The system of claim 31, wherein data paths of the shifter stage are subdivided into a plurality of sections each including a plurality of data paths, wherein the plurality of individual shifting commands include a control signal for individually controlling each section of the plurality of sections, wherein each data path of the plurality of data paths of a section is controlled by a same control signal of the plurality of individual shifting commands, and wherein each data segment of the multiple data segments starts from a least significant bit (LSB) of a section.

34. The system of claim 31, wherein the multiple different data shifts implemented in parallel include different data shifts selected from the group consisting of different data shift direction for a first segment and a second segment of the multiple data segments, different shift type for the first segment and the second segment, and different shift value for the first segment and the second segment, and wherein the first segment and second segment have different data widths.

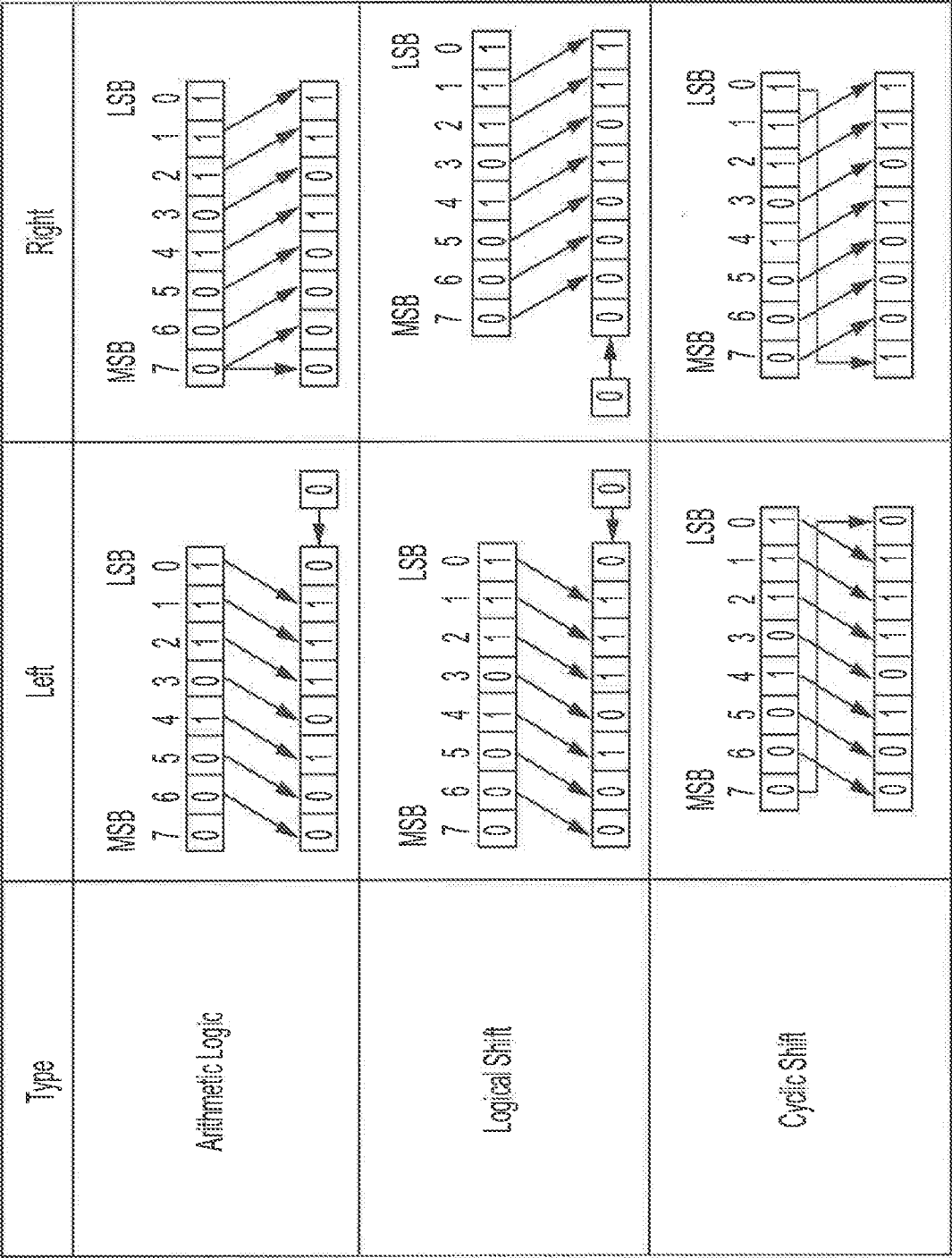


FIG. 1  
PRIOR ART



FIG. 2A  
PRIOR ART

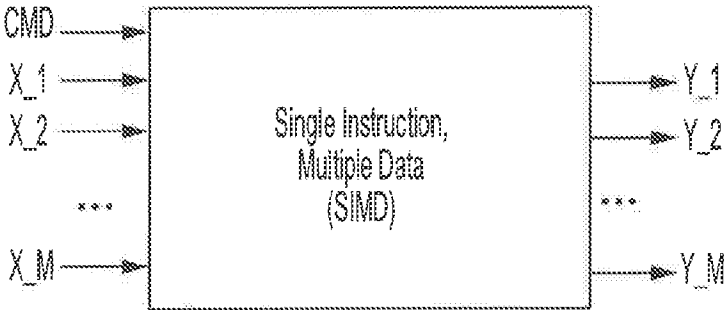


FIG. 2B  
PRIOR ART

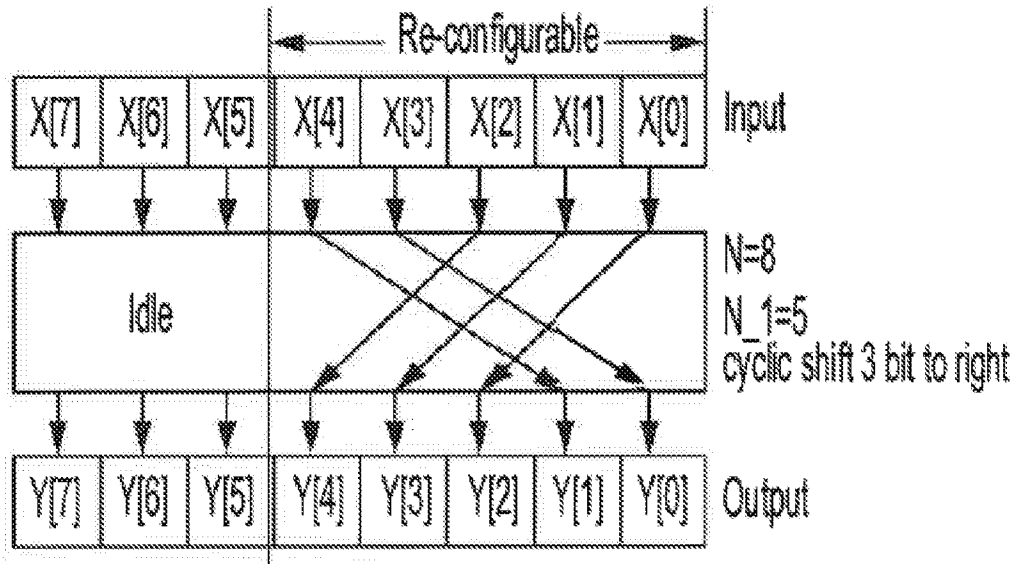


FIG. 3  
PRIOR ART

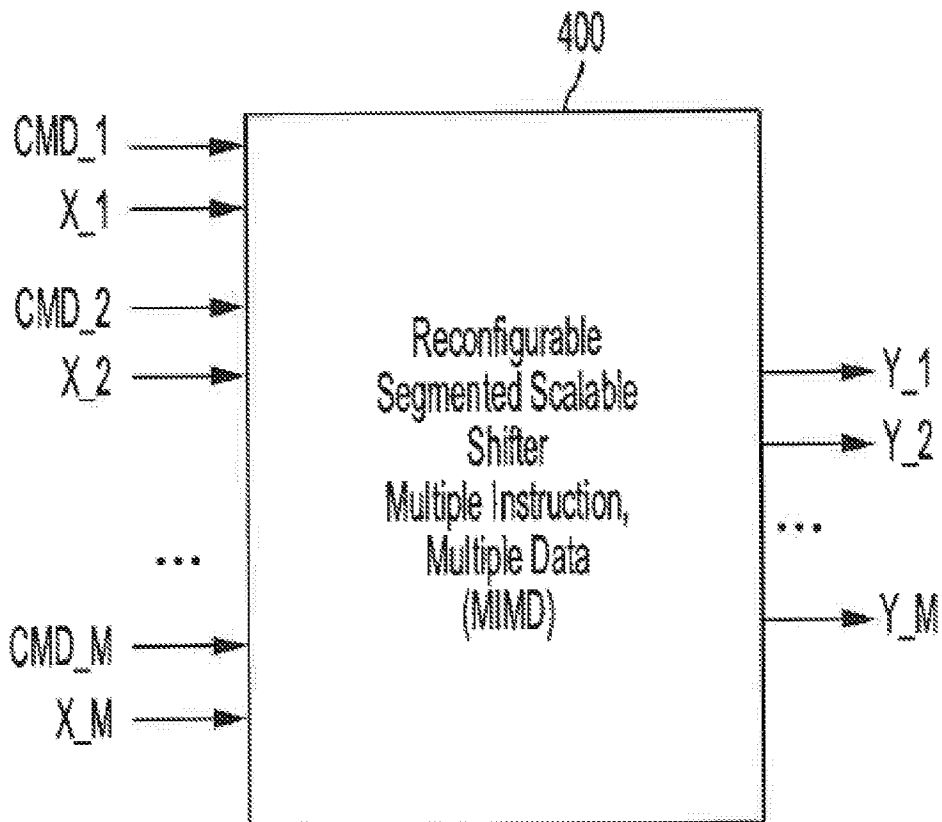


FIG. 4A

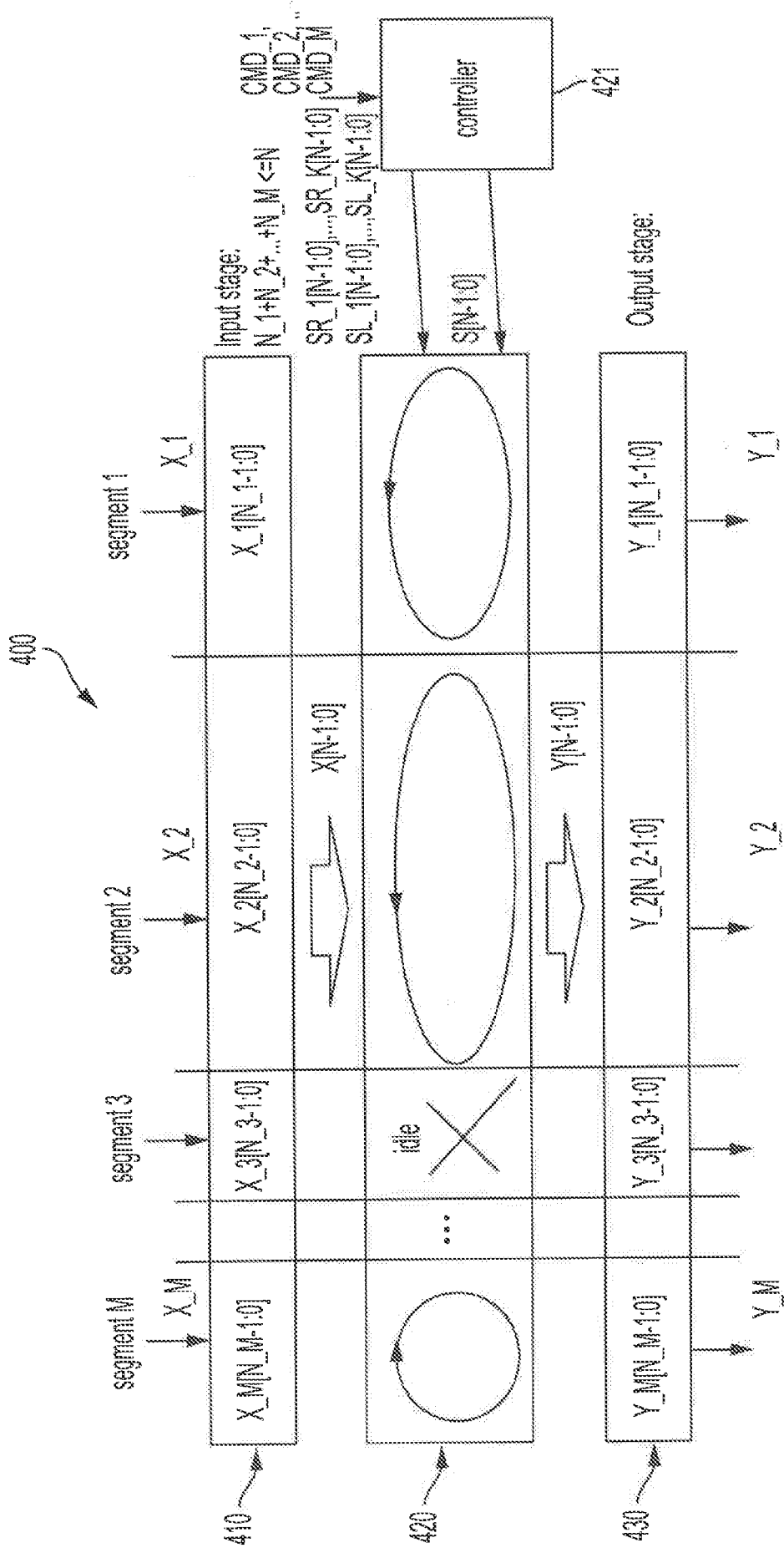


FIG. 4B

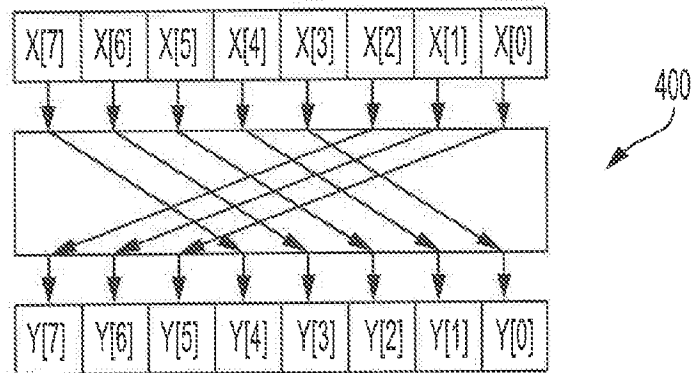


FIG. 5A

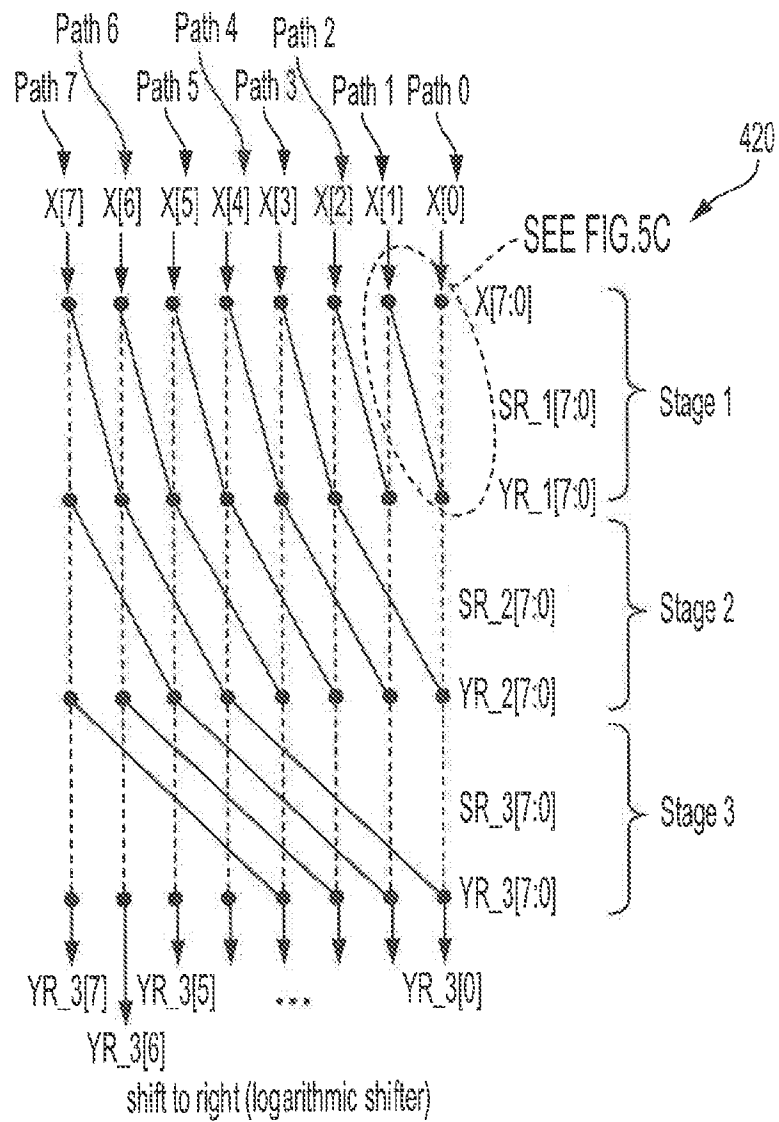


FIG. 5B

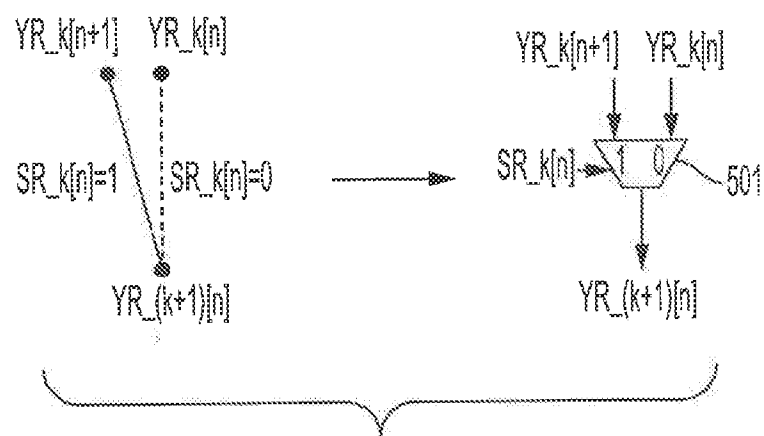


FIG. 5C

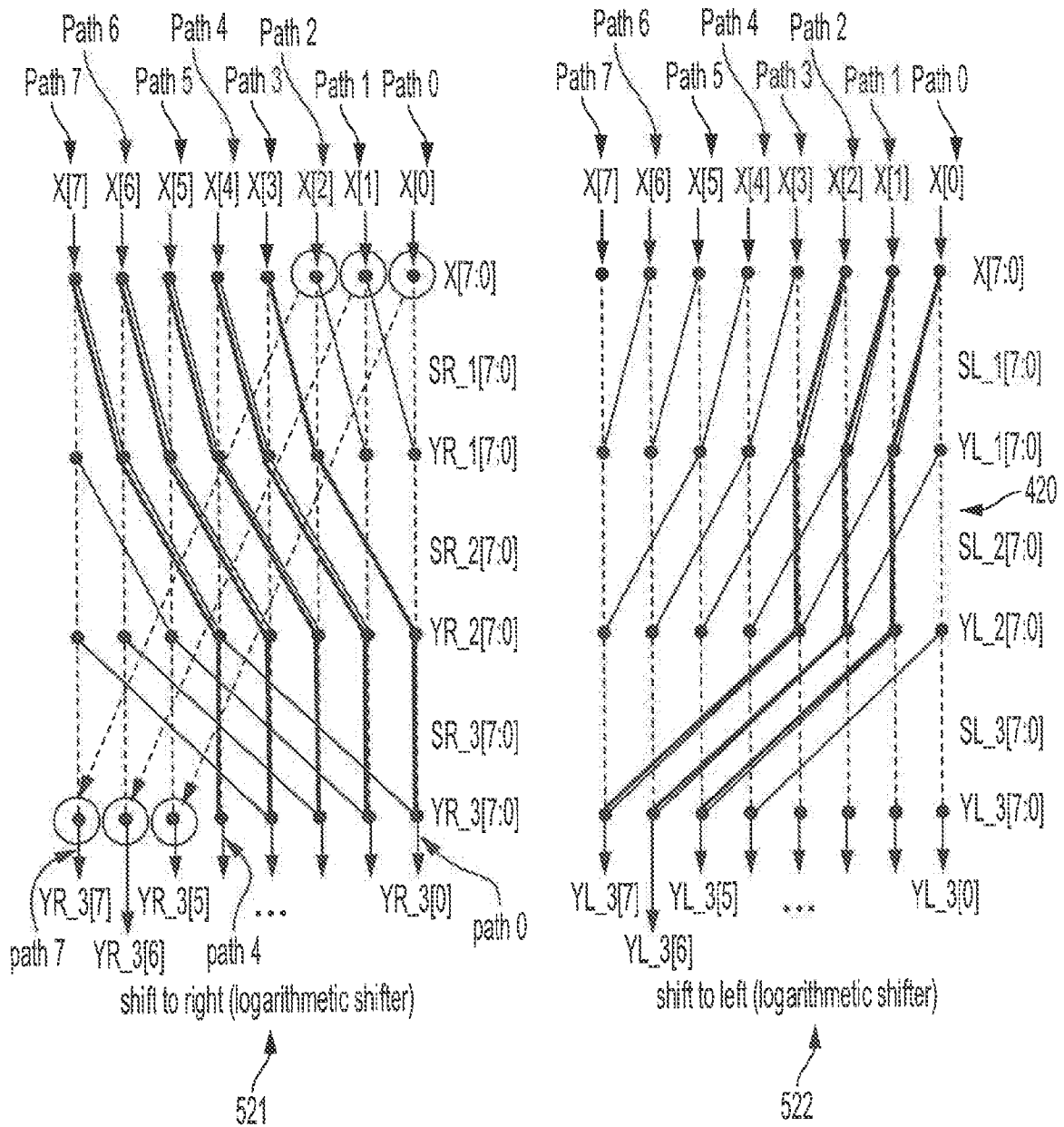


FIG. 5D

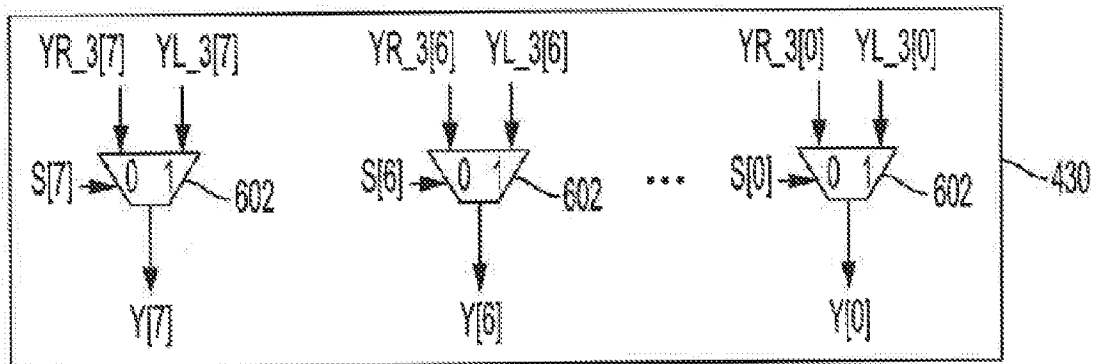


FIG. 6

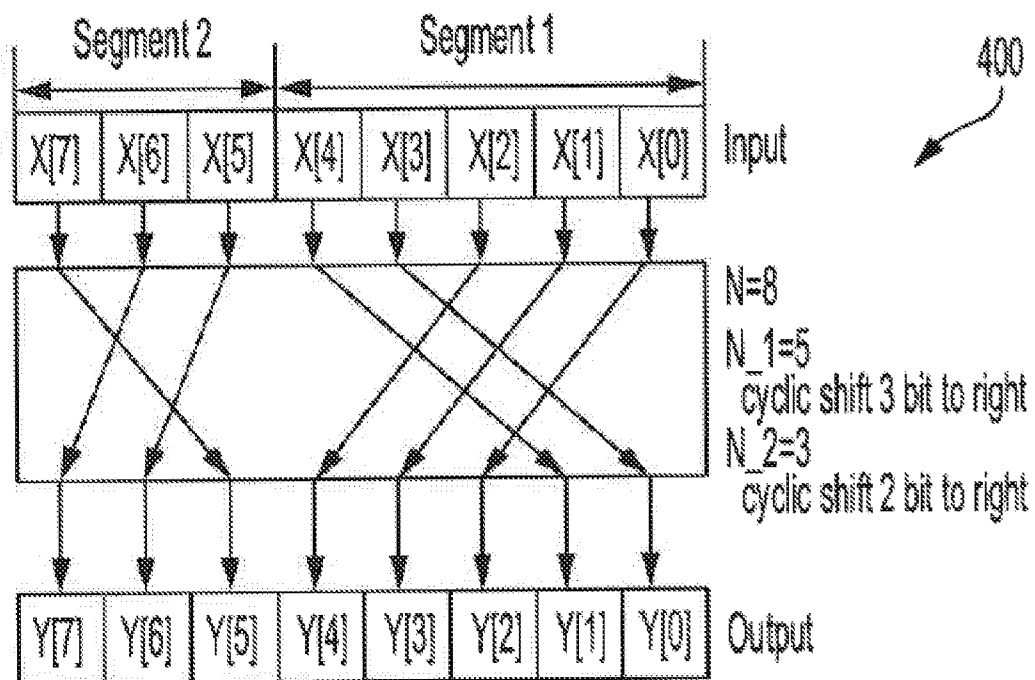


FIG. 7

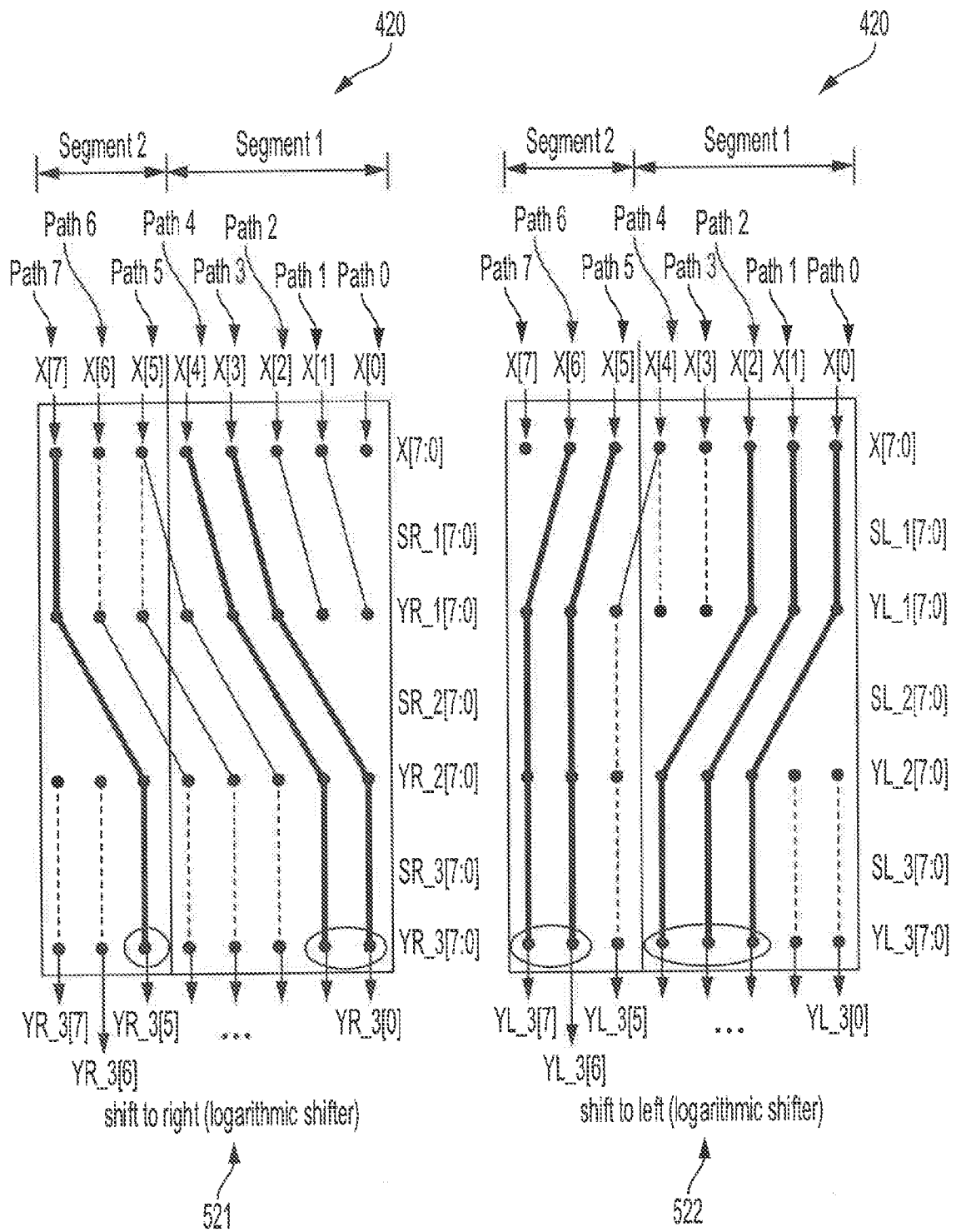


FIG. 8

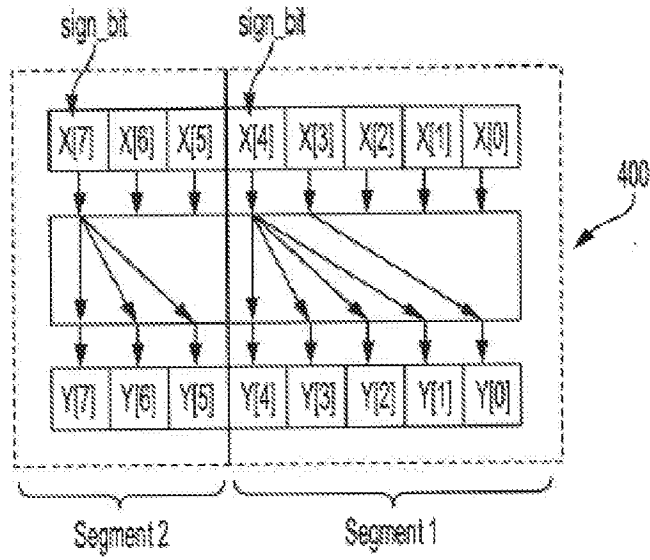


FIG. 9

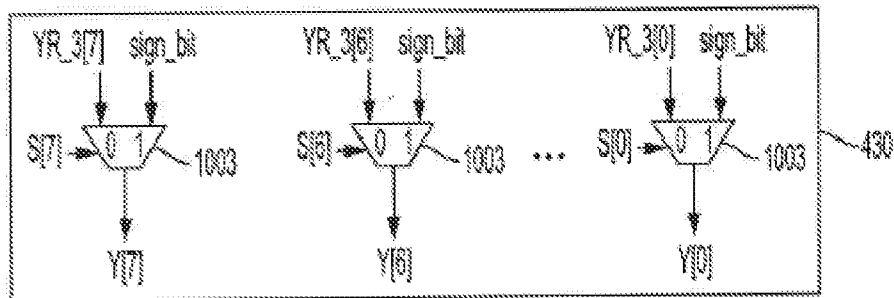


FIG. 10

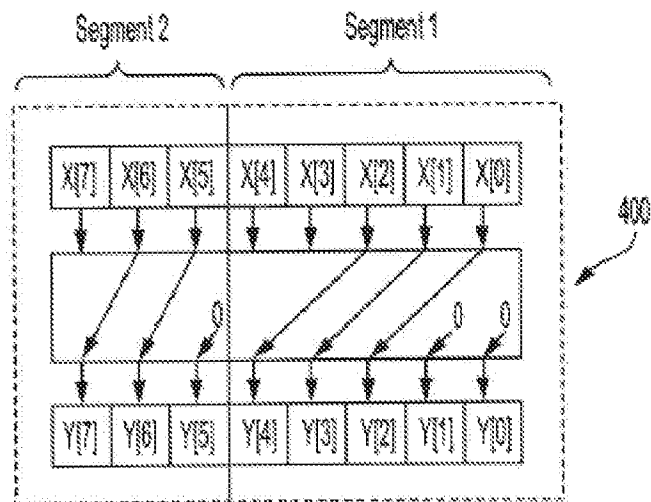


FIG. 11

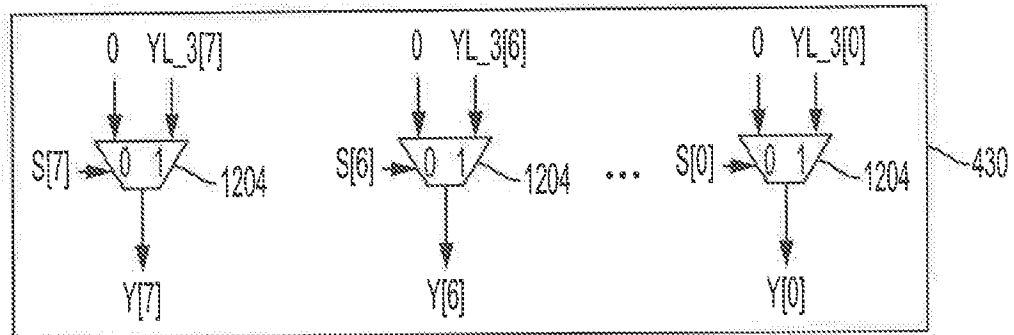


FIG. 12

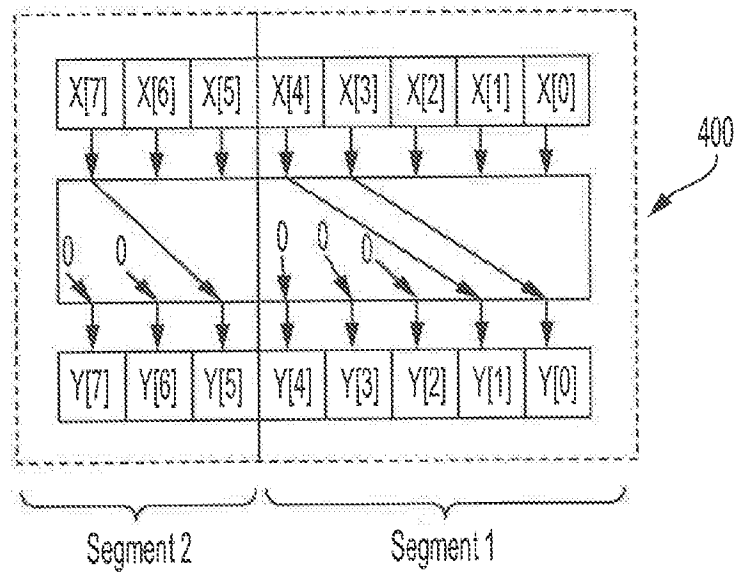


FIG. 13

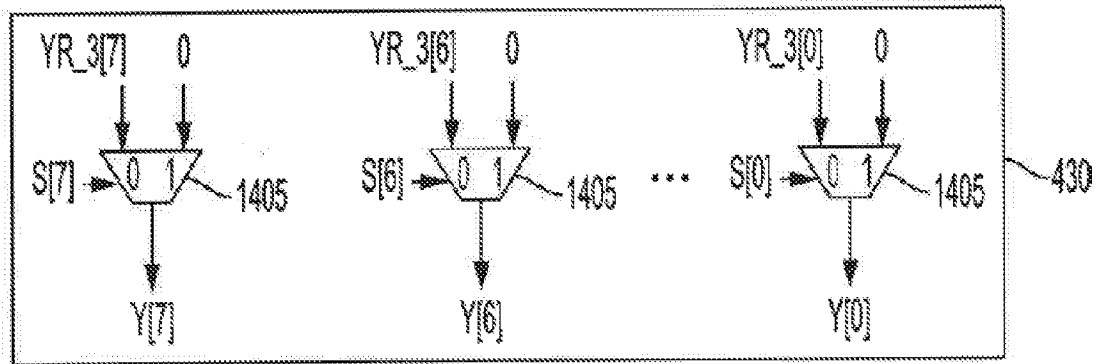


FIG. 14

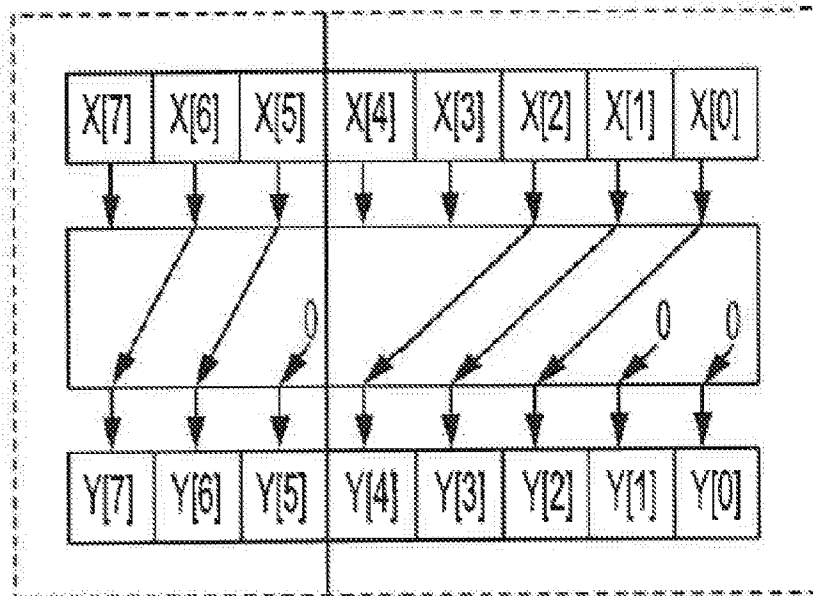
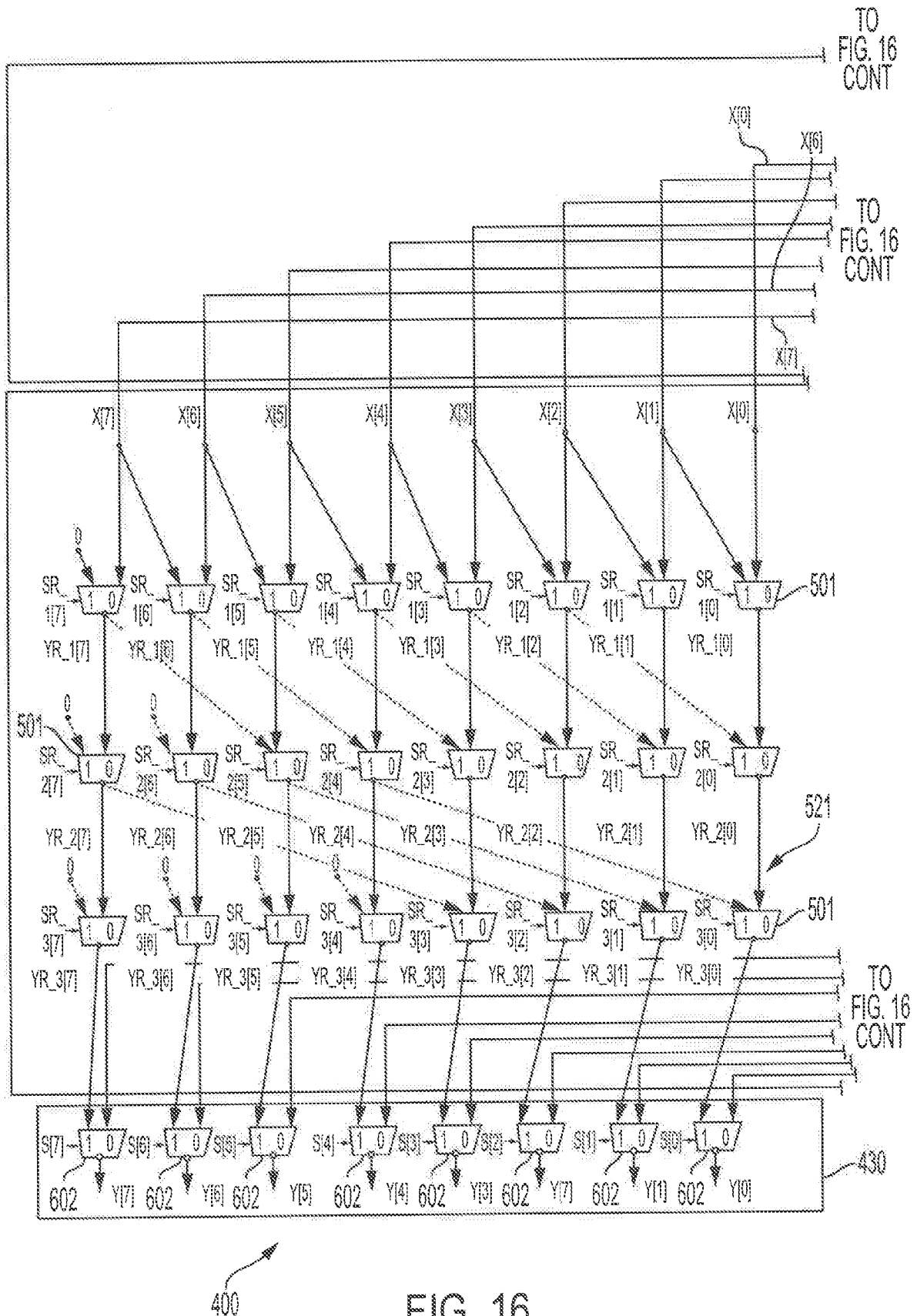
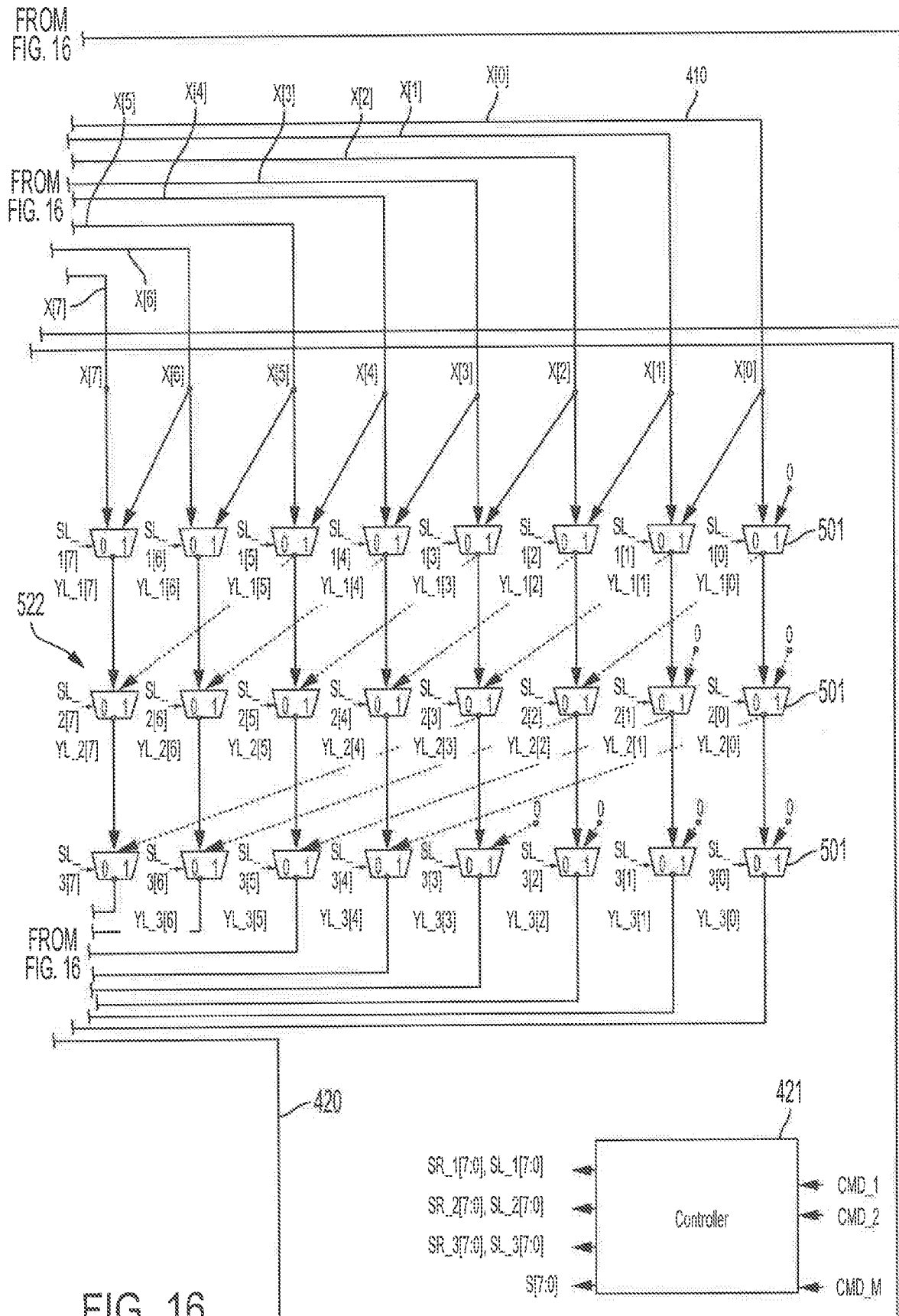


FIG. 15



FIG. 16  
CONTINUED

sign\_bit of each segment =  $\{X_{2[2]}, X_{2[2]}, X_{2[2]}, X_{1[4]}, X_{1[4]}, X_{1[4]}, X_{1[4]}, X_{1[4]}\}$

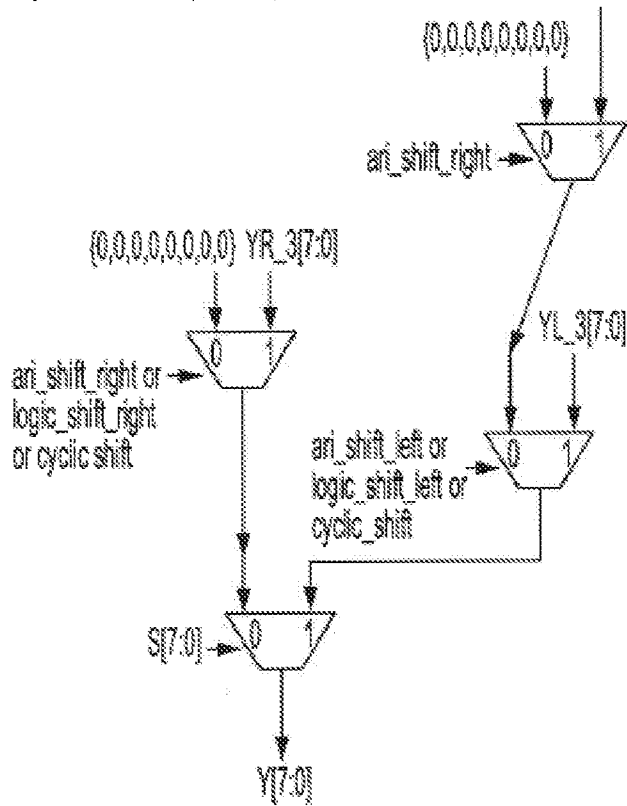
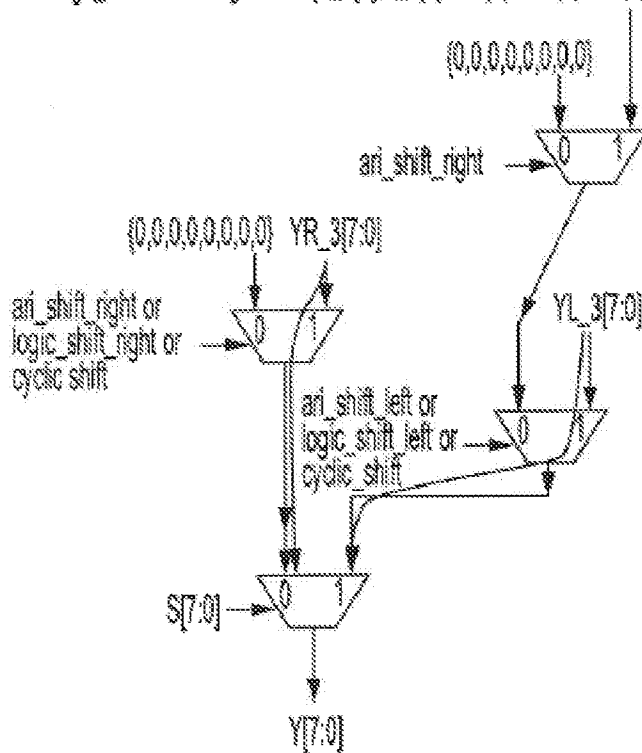


FIG. 17A

sign\_bit of each segment =  $\{X_{2[2]}, X_{2[2]}, X_{2[2]}, X_{1[4]}, X_{1[4]}, X_{1[4]}, X_{1[4]}, X_{1[4]}\}$



Example of cyclic shift left/right

FIG. 17B

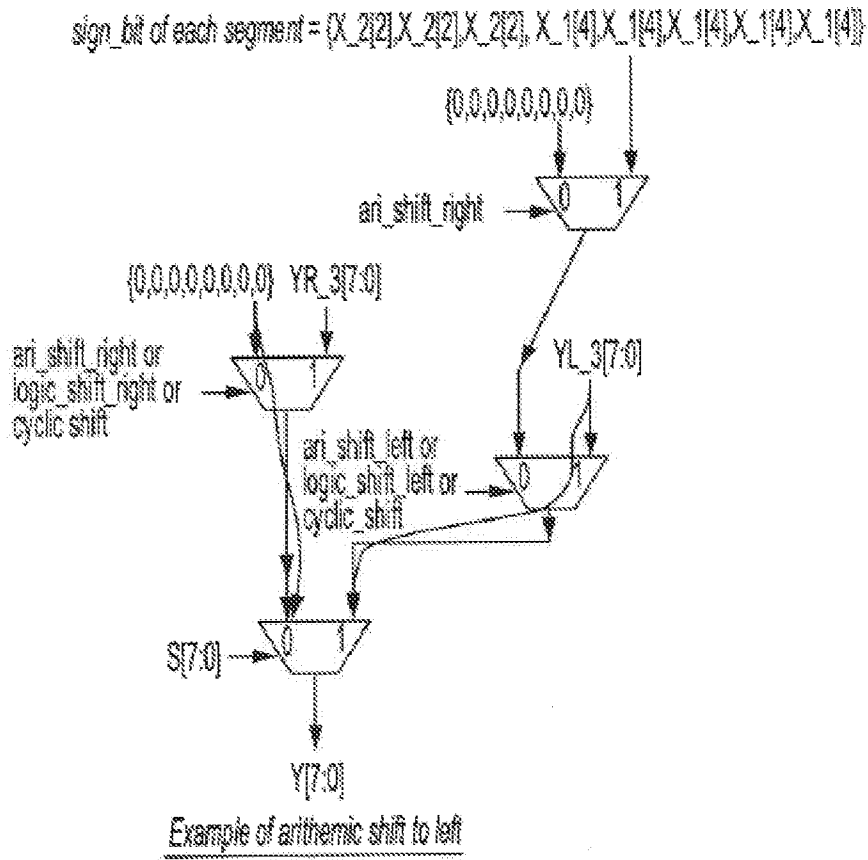


FIG. 17C

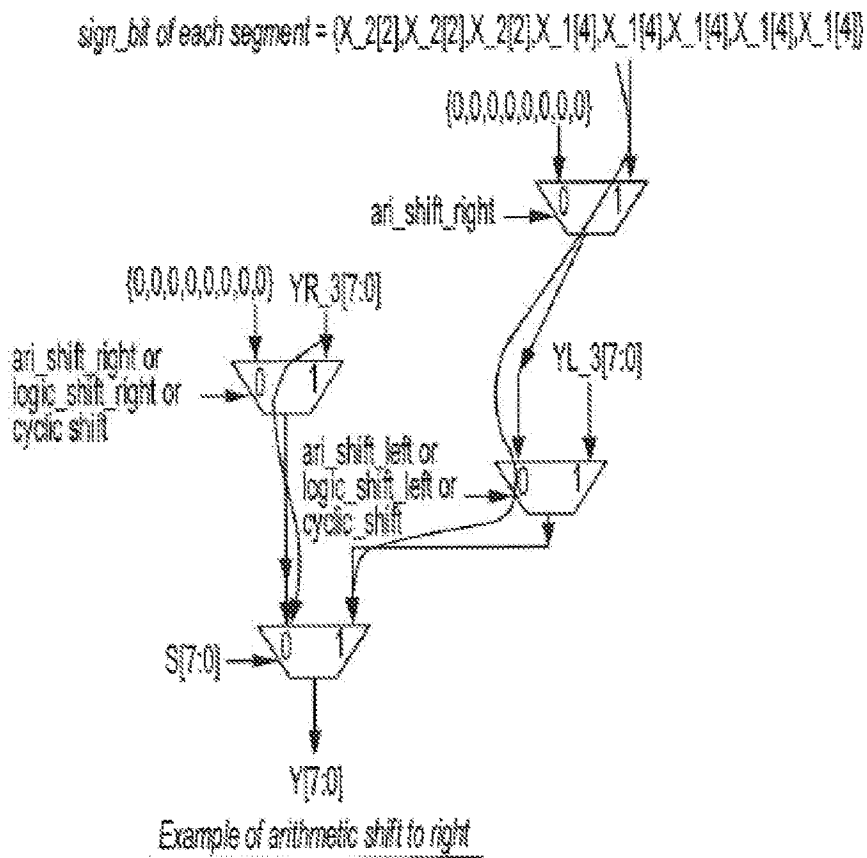


FIG. 17D

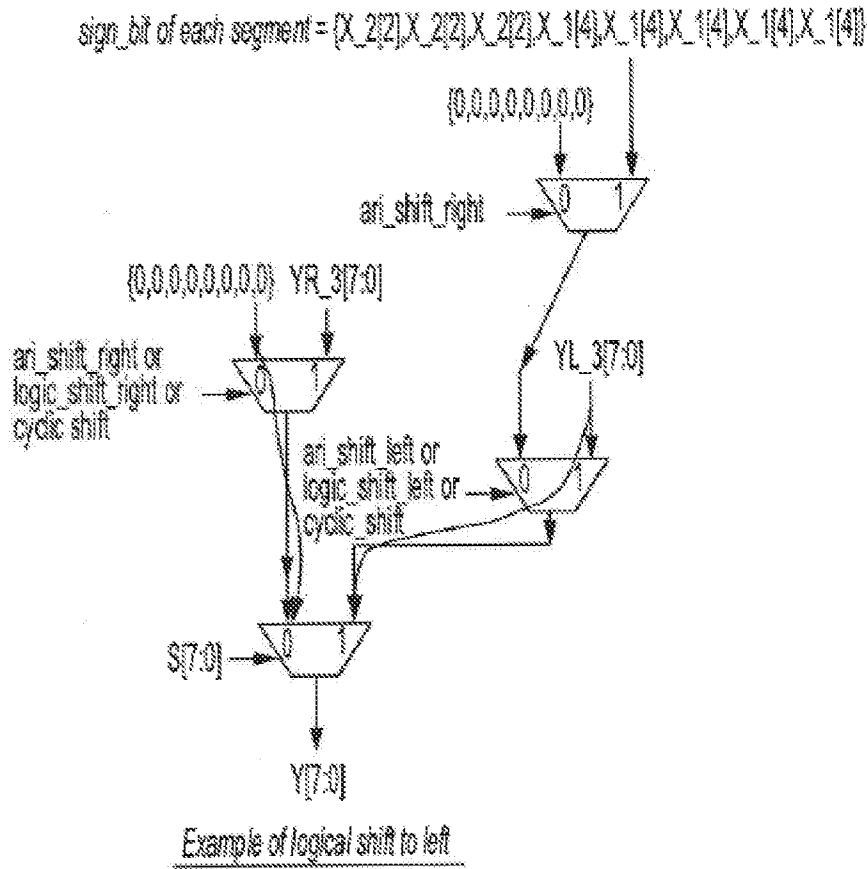


FIG. 17E

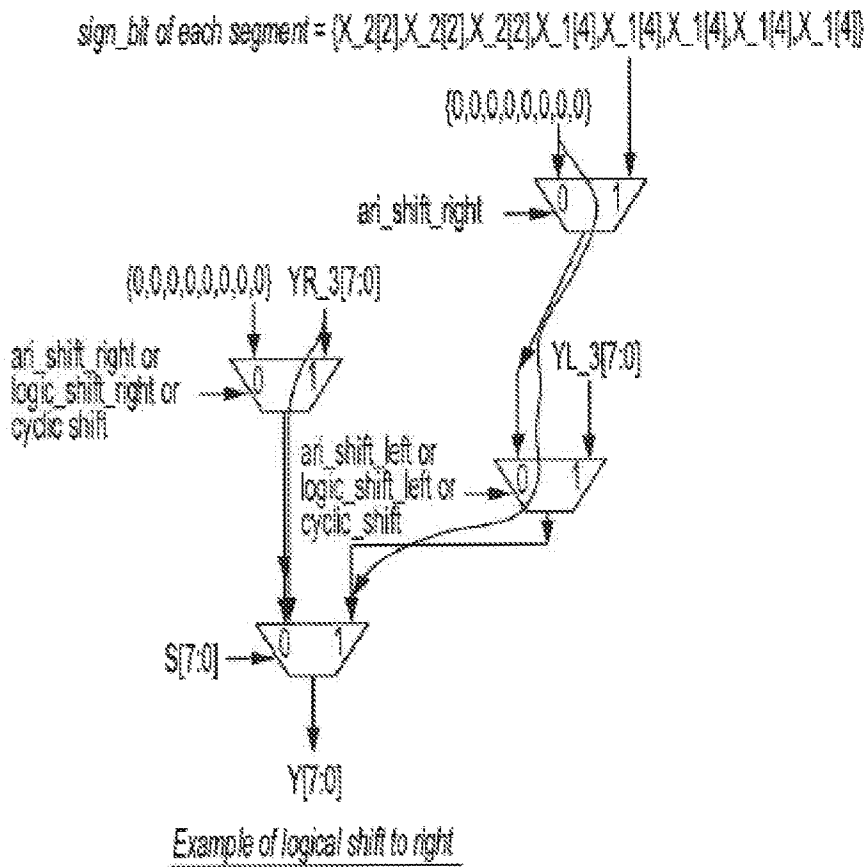


FIG. 17F

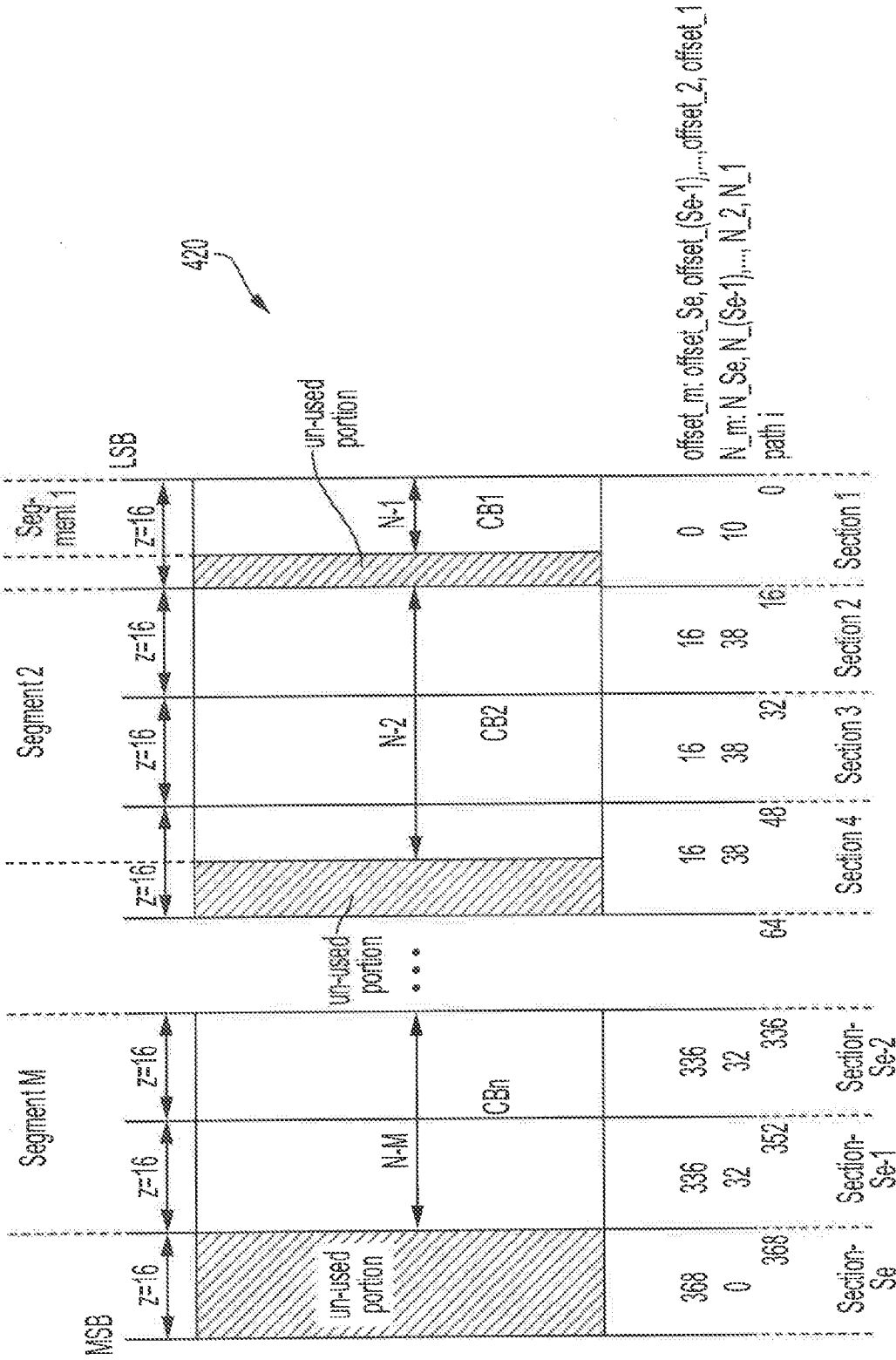
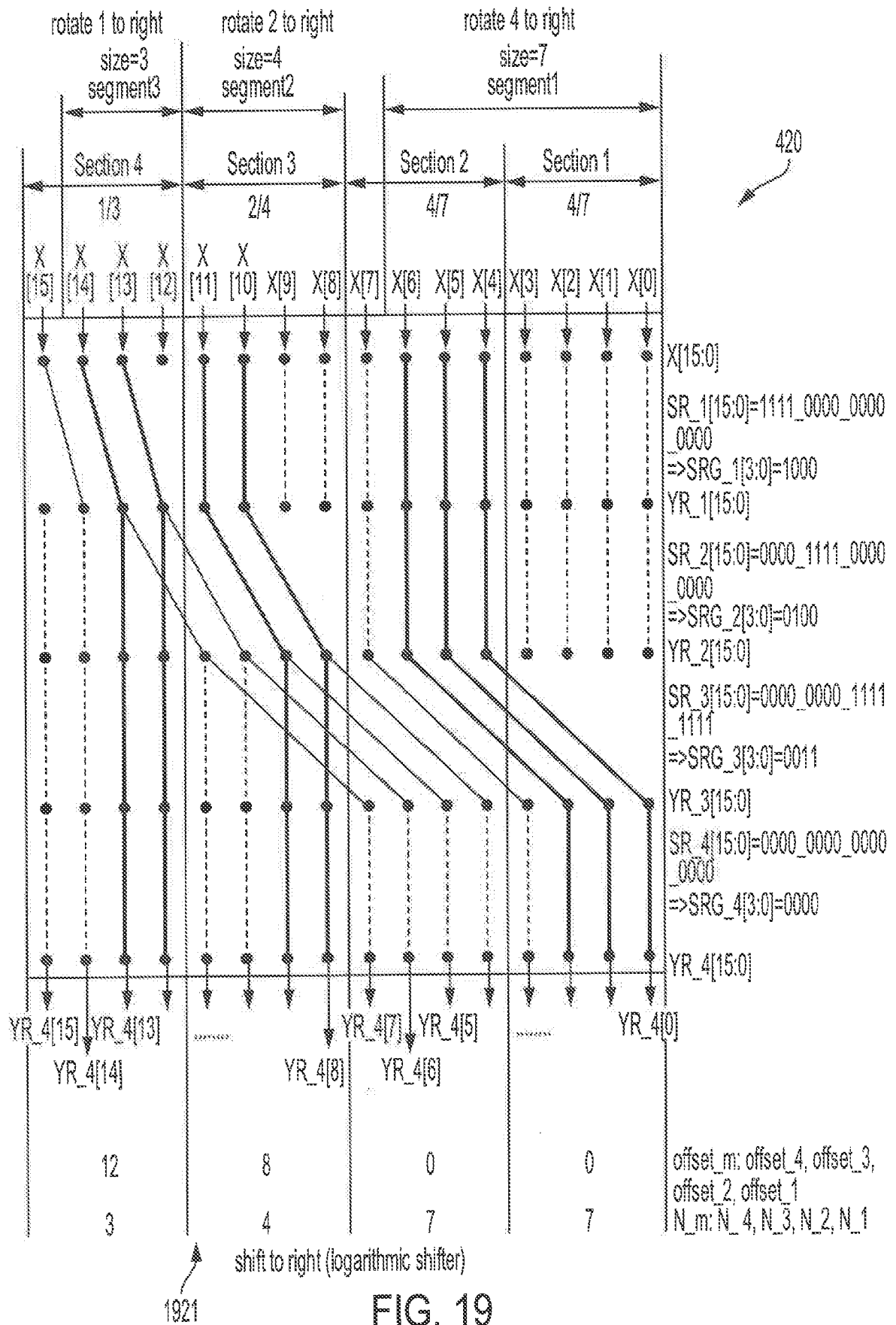
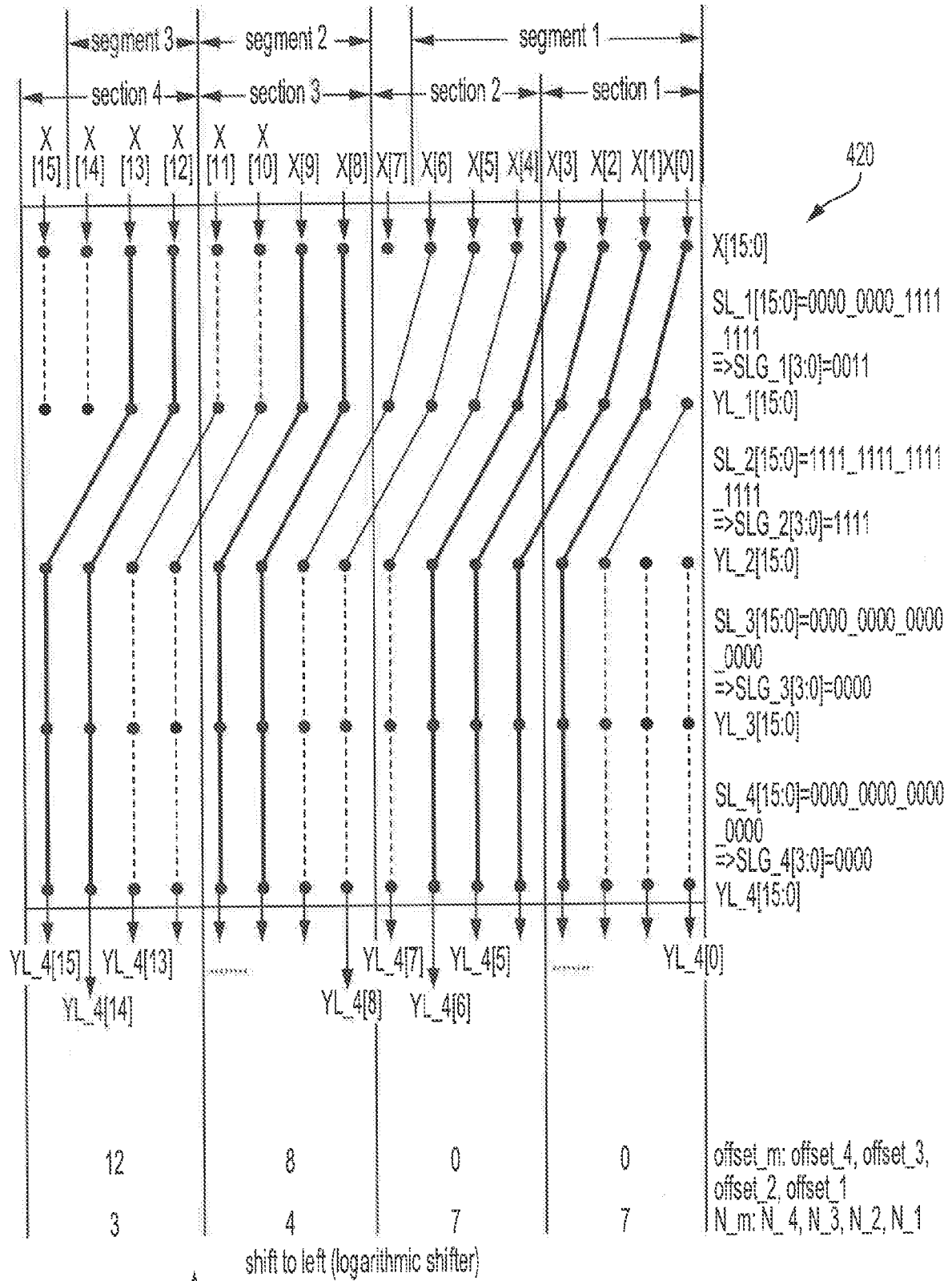


FIG. 18



FIG. 19  
CONTINUED

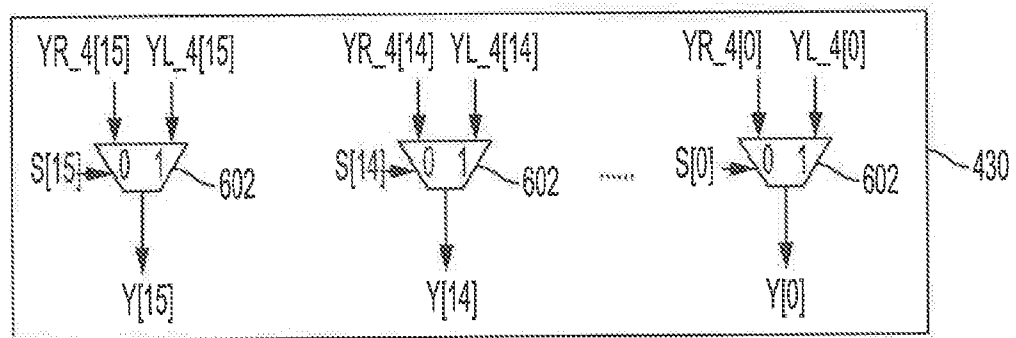


FIG. 20

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2019/074532

**A. CLASSIFICATION OF SUBJECT MATTER**

H03M 13/11(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H03M G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, WPI, EPODOC, CNKI, IEEE: shifter, MIMD, multiple, command, segment, parallel, group, reconfigure, variable, length, width, individual

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                                                            | Relevant to claim No. |
|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| A         | US 2015229330 A1 (PANASONIC INTELLECTUAL PROPERTY MANAGEMENT CO., LTD.) 13 August 2015 (2015-08-13)<br>description, paragraphs [0059]-[0066], and figures 1-2 | 1-34                  |
| A         | US 2009274138 A1 (FREESCALE SEMICONDUCTOR, INC.) 05 November 2009 (2009-11-05)<br>the whole document                                                          | 1-34                  |
| A         | US 8713399 B1 (ANTCOR S.A.) 29 April 2014 (2014-04-29)<br>the whole document                                                                                  | 1-34                  |
| A         | US 5650781 A (DAEWOO ELECTRONICS CO., LTD.) 22 July 1997 (1997-07-22)<br>the whole document                                                                   | 1-34                  |
| A         | CN 1454347 A (NOKIA CORPORATION) 05 November 2003 (2003-11-05)<br>the whole document                                                                          | 1-34                  |

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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“P” document published prior to the international filing date but later than the priority date claimed

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“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

12 October 2019

Date of mailing of the international search report

30 October 2019

Name and mailing address of the ISA/CN

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Facsimile No. (86-10)62019451

Telephone No. 86-(10)-53961357

**INTERNATIONAL SEARCH REPORT**  
**Information on patent family members**

International application No.

**PCT/CN2019/074532**

| Patent document<br>cited in search report |            |    | Publication date<br>(day/month/year) | Patent family member(s) |            |    | Publication date<br>(day/month/year) |
|-------------------------------------------|------------|----|--------------------------------------|-------------------------|------------|----|--------------------------------------|
| US                                        | 2015229330 | A1 | 13 August 2015                       | JP                      | 2015154119 | A  | 24 August 2015                       |
| US                                        | 2009274138 | A1 | 05 November 2009                     | WO                      | 2007138386 | A1 | 06 December 2007                     |
| US                                        | 8713399    | B1 | 29 April 2014                        | None                    |            |    |                                      |
| US                                        | 5650781    | A  | 22 July 1997                         | EP                      | 0663730    | A1 | 19 July 1995                         |
|                                           |            |    |                                      | JP                      | H08116267  | A  | 07 May 1996                          |
|                                           |            |    |                                      | KR                      | 950024069  | A  | 21 August 1995                       |
|                                           |            |    |                                      | DE                      | 69413512   | D1 | 29 October 1998                      |
|                                           |            |    |                                      | CN                      | 1113055    | A  | 06 December 1995                     |
| CN                                        | 1454347    | A  | 05 November 2003                     | DE                      | 60021623   | D1 | 01 September 2005                    |
|                                           |            |    |                                      | WO                      | 0233537    | A1 | 25 April 2002                        |
|                                           |            |    |                                      | EP                      | 1330700    | A1 | 30 July 2003                         |
|                                           |            |    |                                      | AU                      | 1272401    | A  | 29 April 2002                        |
|                                           |            |    |                                      | AT                      | 300761     | T  | 15 August 2005                       |
|                                           |            |    |                                      | US                      | 7257609    | B1 | 14 August 2007                       |