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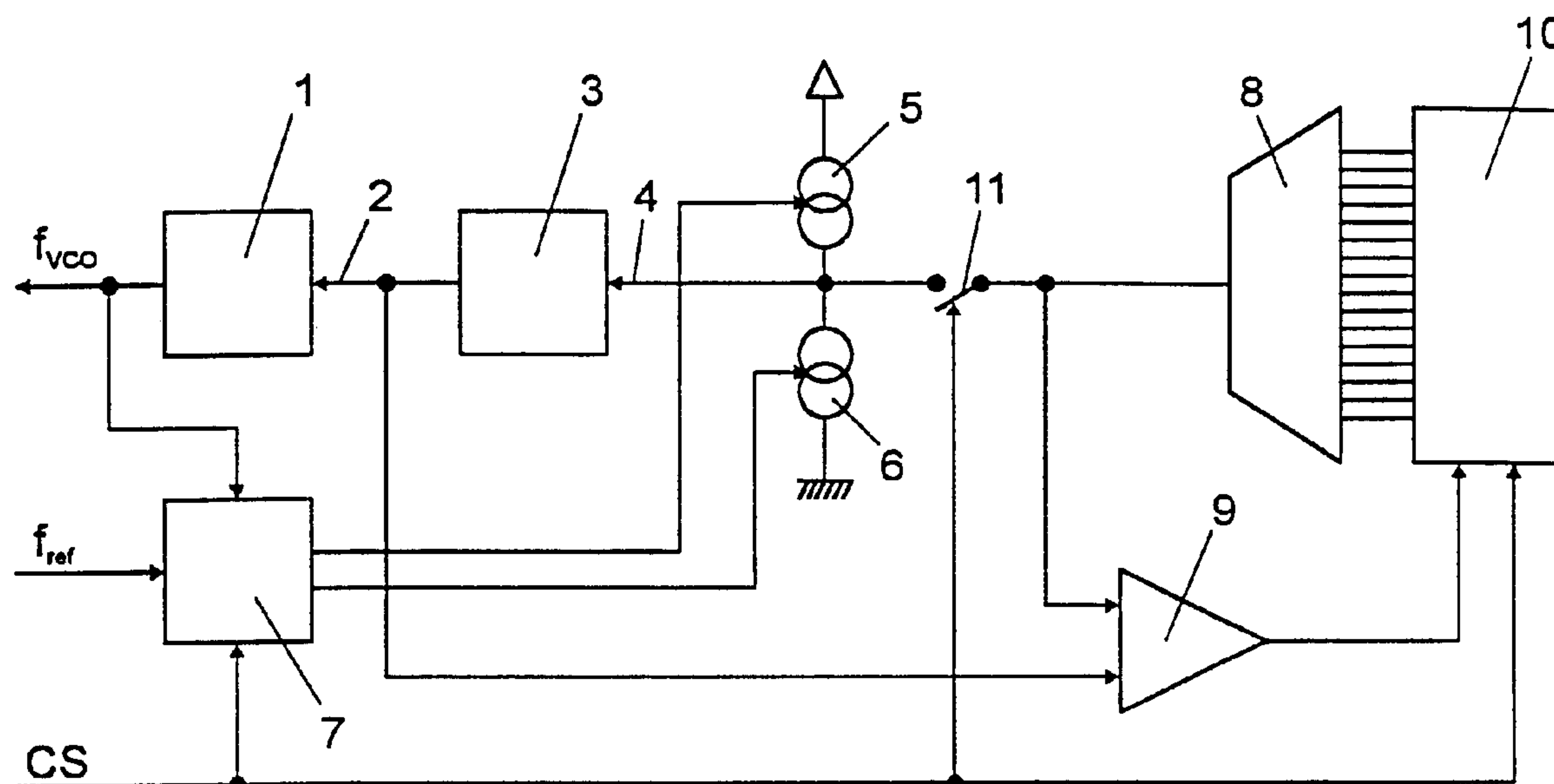
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(54) Title: METHOD AND ARRANGEMENT FOR LOCKING A CONTROL VOLTAGE TO A VOLTAGE-CONTROLLED OSCILLATOR



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To lock a control voltage to a voltage-controlled oscillator (1) in correspondence with a desired frequency (f_{ref}), a comparator (7) compares the output frequency (f_{vco}) of the voltage-controlled oscillator (1) with the desired frequency (f_{ref}). A signal is generated in response to any frequency difference to adjust the control voltage until the frequency difference is zero. A copy of the control voltage is generated at least when said frequency difference is zero, and this generated copy is applied as control signal to the voltage-controlled oscillator (1) to lock its output frequency at the desired frequency (f_{ref}).

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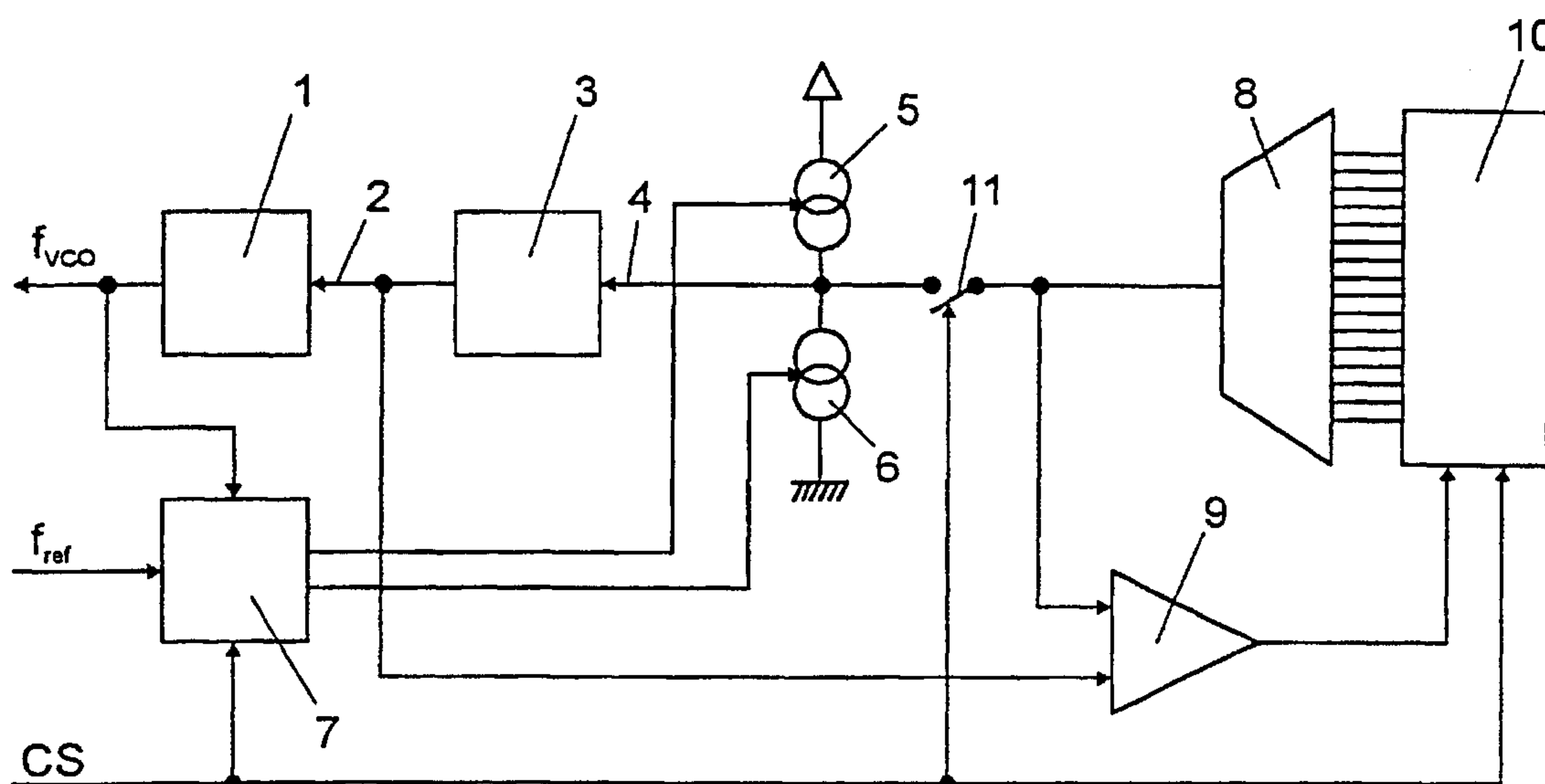
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(54) Title: METHOD AND ARRANGEMENT FOR LOCKING A CONTROL VOLTAGE TO A VOLTAGE-CONTROLLED OSCILLATOR



(57) Abstract: To lock a control voltage to a voltage-controlled oscillator (1) in correspondence with a desired frequency (f_{ref}), a comparator (7) compares the output frequency (f_{vco}) of the voltage-controlled oscillator (1) with the desired frequency (f_{ref}). A signal is generated in response to any frequency difference to adjust the control voltage until the frequency difference is zero. A copy of the control voltage is generated at least when said frequency difference is zero, and this generated copy is applied as control signal to the voltage-controlled oscillator (1) to lock its output frequency at the desired frequency (f_{ref}).

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**METHOD AND ARRANGEMENT FOR LOCKING A CONTROL
VOLTAGE TO A VOLTAGE-CONTROLLED OSCILLATOR**

TECHNICAL FIELD

5 The invention relates generally to voltage-controlled oscillators and more specifically a method and an arrangement for locking a control voltage to a voltage-controlled oscillator.

BACKGROUND OF THE INVENTION

10 In a frequency-hopping radio where a voltage-controlled oscillator (VCO), connected in a phase-locked loop with a phase detector and a loop filter, is directly modulated, the loop filter has a relatively large bandwidth to ensure that a frequency hop can be made quickly enough at repetitive channel changes. In order for the phase-locked loop not to compensate away the greater part of the modulation, the
15 loop has to be opened during transmission. This is controlled by a signal to the phase detector, which opens the loop and turns off current generators that control the control voltage to the VCO.

Thus, when the loop is opened, there is no feedback to the VCO, but its frequency is
20 determined by the output voltage of the loop filter. This output voltage is determined by charges stored in capacitors in the loop filter.

In theory, this works well, but in practice, there are high requirements on the quality of the capacitors, leak currents in the current generators when turned off, leak currents in varactor diodes in the VCO, etc.
25

One major problem is the memory effect of the capacitors that causes them more or less to return to the voltage they had before. If a frequency hop has been made e.g. from low frequency (low voltage) to high frequency (high voltage) in order to start
30 transmitting at the latter, the voltage across the capacitors will initially change in the same direction as the old value. This is due to the memory effect of the capacitors

when the loop is opened and the current generators are turned off. To compensate for this change, more expensive capacitors with less memory effect have to be used.

Another major problem is leakage in the varactor diodes of the VCO and/or in the current generators. Very small leak currents (100 pA) are enough for the capacitors to be charged or discharged enough for the frequency to drift away. The problem is particularly big at increased temperatures.

SUMMARY OF THE INVENTION

The object of the invention is to bring about an improved method and an improved arrangement for locking the control voltage to a VCO.

This is attained in accordance with the invention mainly by generating a copy of the control voltage when the frequency difference between the output frequency of the VCO and a desired frequency is zero, and applying that generated copy of the control voltage as control signal to the VCO to lock its output frequency.

Hereby, the output frequency of the VCO will not drift.

BRIEF DESCRIPTION OF THE DRAWING

The invention will be described more in detail below with reference to the appended drawing, on which the single Figure is a block diagram of an embodiment of an arrangement in accordance with the invention.

DESCRIPTION OF THE INVENTION

On the drawing, an arrangement for locking a control voltage of a VCO 1 in a frequency-hopping radio is illustrated. The rest of the radio is not shown.

The VCO 1 is connected in a phase-locked loop and has a control input 2 connected to an output of a loop filter 3, which in a manner known per se comprises capacitors and resistors (not shown). The input 4 of the loop filter is connected to current gen-

erators 5 and 6, controlled by respective output signals from a phase detector or frequency comparator 7.

The comparator 7 is connected with one input to the output of the VCO 1 and is adapted to compare the output frequency f_{vco} of the VCO 1 with a desired frequency f_{ref} . The desired frequency f_{ref} is obtained in a manner known per se from a control unit (not shown) upon a desired frequency hop.

Upon such a desired frequency hop, an output signal is generated by the comparator 7 in response to any frequency difference between the frequencies f_{vco} and f_{ref} . Depending on whether the frequency difference is positive or negative, the comparator 7 will control one of the current generators 5 and 6 to supply current to the loop filter 3 to control the output frequency of the VCO 1, i.e. f_{vco} , to f_{ref} . The other one of the current generators 5 and 6 will be kept turned off by the comparator 7.

After a certain time, $f_{vco} = f_{ref}$. Then, there will be no output signal from the comparator 7.

At that time, the phase-locked loop will be opened by a control signal CS from the control unit (not shown) to turn off the comparator 7. Hereby, both current generators 5 and 6 will be turned off by the comparator 7.

As indicated in the introductory portion above, this will cause the output frequency of the VCO 1 to drift.

In accordance with the invention, to eliminate this problem, i.e. to stop the output frequency of the VCO 1 from drifting, an arrangement is provided to generate a copy of the VCO control voltage, at least at the time when $f_{vco} = f_{ref}$, i.e. when the frequency difference is zero, and to apply that generated copy as control signal to the VCO 1 when the current generators 5 and 6 have been turned off.

In this connection, it should be understood that the copy of the control voltage can be continuously generated.

5 In the embodiment shown on the drawing, a digital-to-analog converter (DAC) 8 is used to generate the copy of the VCO control voltage.

10 The inputs of the DAC 8 are connected to outputs of a logic unit 10. The logic unit 10 is connected with one input to the output of a comparator 9. The comparator 9 has one of its inputs connected to the control input 2 of the VCO 1, and its other input connected to the output of the DAC 8. Thus, the logic unit 10 will generate a bit-pattern on the inputs of the DAC 8 until the output signal from the comparator 9 is close to zero, i.e. when the output voltage of the DAC 8 is more or less equal to the VCO control voltage.

15 Hereby, a copy of the VCO control voltage appears on the output of the DAC 8.

20 In this connection, it should be mentioned that the copy of the VCO control voltage does not necessarily have to be generated by means of a DAC. Instead, e.g. a sample-and-hold circuit (not shown) can equally well be used. The sample-and-hold circuit would in that case be connected with its input to the output of a comparator, and the comparator would be connected with its inputs to compare the control voltage to the voltage-controlled oscillator with the output voltage of the sample-and-hold circuit.

25 In the embodiment shown on the drawing, the output of the DAC 8 is connectable to the input 4 of the loop filter 3 via a switch 11 which is closed by the same control signal CS from the control unit (not shown) that turns off the comparator 7 when $f_{vco} = f_{ref}$, i.e. when the current generators 5 and 6 are turned off as described above.

30 The radio can now start transmitting at the desired frequency.

At the same time, the control signal CS is supplied to an input of the logic circuit 10 to turn off the logic circuit 10 so that the output signal of the DAC 8 is maintained.

5 Hereby, the copy of the VCO control voltage, generated by the DAC 8 in the embodiment shown, is applied as control signal to the VCO 1 via the loop filter 3 to lock the output frequency f_{vco} of the VCO 1 in correspondence with the desired frequency f_{ref} .

10 Since the generated copy of the control voltage to the VCO 1 remains unchanged on the control input 2 to the VCO 1, its output frequency will not drift.

As should be apparent from the above, the problems with frequency drift are eliminated.

CLAIMS

1. A method of locking a control voltage to a voltage-controlled oscillator in correspondence with a desired frequency, comprising

- comparing the output frequency of the voltage-controlled oscillator with the desired frequency,

- generating a signal in response to any frequency difference, and

- adjusting the control voltage in response to said generated signal until the frequency difference is zero,

characterized by

- generating a copy of the control voltage, at least when said frequency difference is zero, and

- applying said generated copy of the control voltage as control signal to the voltage-controlled oscillator to lock its output frequency, when said frequency difference is zero.

2. The method as claimed in claim 1, characterized in that said copy of the control voltage is continuously generated.

3. An arrangement for locking a control voltage to a voltage-controlled oscillator (1) in correspondence with a desired frequency (f_{ref}), comprising

- a comparator (7) for comparing the output frequency (f_{VCO}) of the voltage-controlled oscillator (1) with the desired frequency (f_{ref}), and for generating a signal in response to any frequency difference, and

- means (5, 6) for adjusting the control voltage in response to said generated signal until the frequency difference is zero, characterized by

- means (8, 9, 10) for generating a copy of the control voltage at least when said frequency difference is zero, and

- means (11) for applying said copy of the control voltage, generated when said frequency difference is zero, as control signal to the voltage-controlled oscillator (1) to lock its output frequency at the desired frequency (f_{ref}).

5 4. The arrangement as claimed in claim 3, characterized by said generating means (8, 9, 10) being adapted to continuously generate said copy of the control voltage.

10 5. The arrangement as claimed in claim 3 or 4, characterized in that said generating means comprises a digital-to-analog converter (8) connected with its input to the output of a comparator (9) via a logic circuit (10), the comparator (9) being connected with its inputs to compare the control voltage to the voltage-controlled oscillator (1) with the output voltage of the digital-to-analog converter (8).

15 6. The arrangement as claimed in claim 3 or 4, characterized in that said generating means comprises a sample-and-hold circuit connected with its input to the output of a comparator, the comparator being connected with its inputs to compare the control voltage to the voltage-controlled oscillator with the output voltage of the sample-and-hold circuit.

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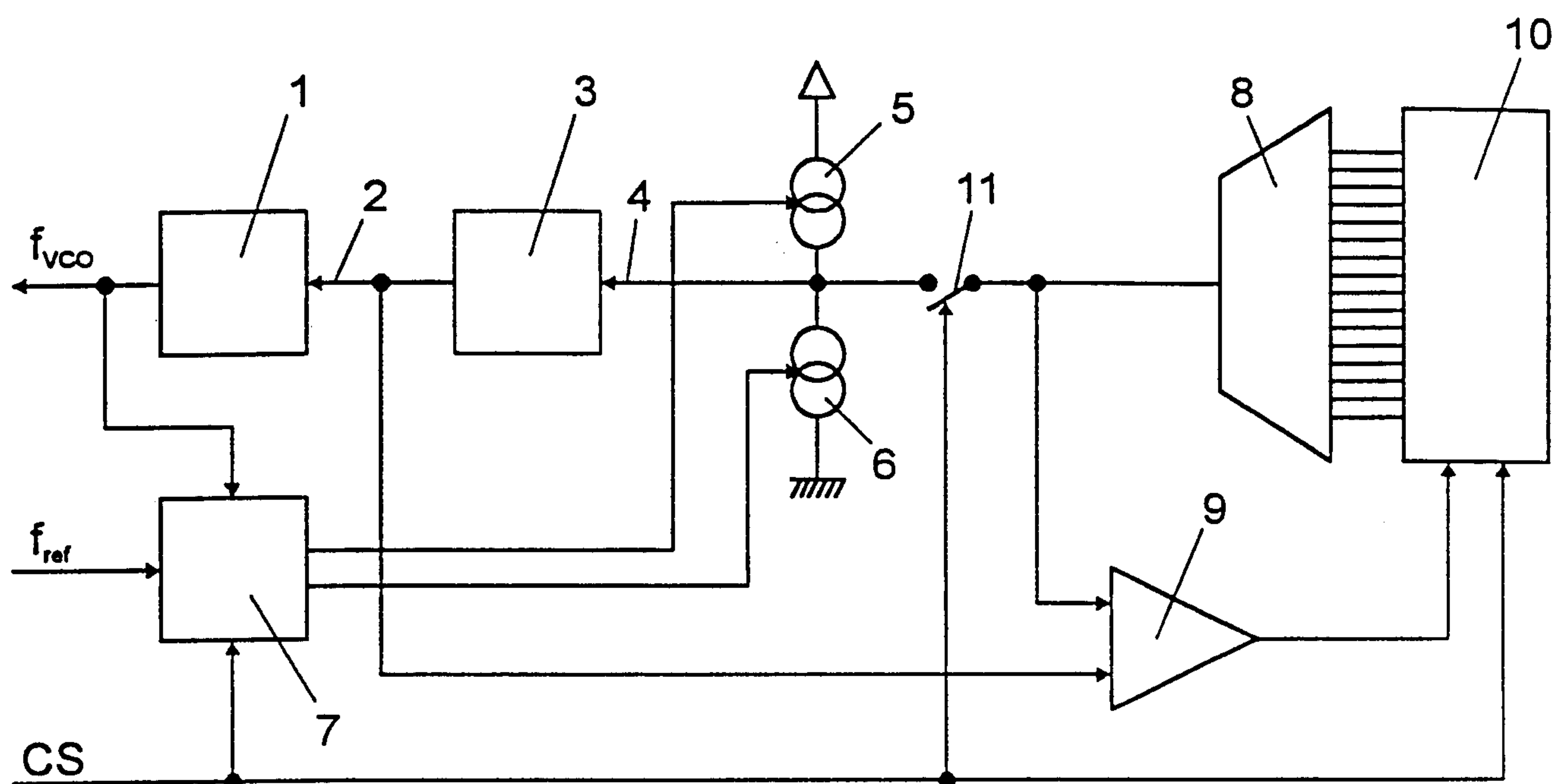


Fig. 1

