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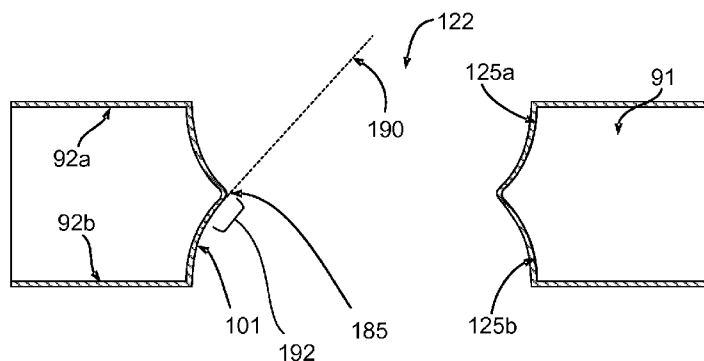
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(54) Title: THIN FILM THROUGH-GLASS VIA AND METHODS FOR FORMING SAME

**Figure 15**

(57) **Abstract:** This disclosure provides systems, methods and apparatus providing electrical connections through glass substrates. In one aspect, a thin film through-glass via including a through-glass via hole and a thin conductive film that conformally coats the sidewalls of the through-glass via hole is provided. A contour of a through-glass via hole may include concave portions that overlap at a midsection of the glass, with the through-glass via hole sidewalls curved inward to form the concave portions. In another aspect, one or more methods of forming through-glass vias are provided. In some implementations, the methods include double-sided processes to form aligned via holes in a glass substrate that together form a contoured through-glass via hole, followed by deposition of a thin continuous film of a conductive material.



THIN-FILM THROUGH-GLASS VIA AND METHODS FOR FORMING SAME

PRIORITY APPLICATION

[0001] This application claims priority to United States Patent Application No. 13/048,768 (Attorney Docket No. QUALP029/101708U1) entitled “THIN-FILM THROUGH-GLASS VIA AND METHODS FOR FORMING SAME” and filed on March 15, 2011, which is hereby incorporated by reference and for all purposes.

TECHNICAL FIELD

[0002] This disclosure relates to structures and processes for glass substrates and more specifically to electrically conductive vias through the glass substrates.

DESCRIPTION OF THE RELATED TECHNOLOGY

[0003] Electromechanical systems include devices having electrical and mechanical elements, actuators, transducers, sensors, optical components (e.g., mirrors) and electronics. Electromechanical systems can be manufactured at a variety of scales including, but not limited to, microscale and nanoscale. For example, microelectromechanical systems (MEMS) devices can include structures having sizes ranging from about a micron to hundreds of microns or more. Nanoelectromechanical systems (NEMS) devices can include structures having sizes smaller than a micron including, for example, sizes smaller than several hundred nanometers. Electromechanical elements may be created using deposition, etching, lithography, and/or other micromachining processes that etch away parts of substrates and/or deposited material layers, or that add layers to form electrical and electromechanical devices.

[0004] One type of electromechanical systems device is called an interferometric modulator (IMOD). As used herein, the term interferometric modulator or interferometric light modulator refers to a device that selectively absorbs and/or reflects light using the principles of optical interference. In some implementations, an interferometric modulator may include a pair of conductive plates, one or both of which may be transparent and/or reflective, wholly or in part, and capable of relative motion upon application of an appropriate electrical signal. In an implementation,

one plate may include a stationary layer deposited on a substrate and the other plate may include a reflective membrane separated from the stationary layer by an air gap. The position of one plate in relation to another can change the optical interference of light incident on the interferometric modulator. Interferometric modulator devices have a wide range of applications, and are anticipated to be used in improving existing products and creating new products, especially those with display capabilities.

[0005] MEMS packaging protects the functional units of the system from the environment, provides mechanical support for the system components, and provides an interface for electrical interconnections.

SUMMARY

[0006] The systems, methods and devices of the disclosure each have several innovative aspects, no single one of which is solely responsible for the desirable attributes disclosed herein.

[0007] One innovative aspect of the subject matter described in this disclosure includes through-glass vias. In some implementations, a through-glass via includes a hole through a glass substrate (referred to as a through-glass via hole) and a thin conductive film that conformally coats the sidewalls of the through-glass via hole. In some implementations, a through-glass via hole in a glass substrate having first and second sides includes a first via hole having sidewalls and a via opening in the first side of the glass substrate and a second via hole having sidewalls and a via opening in the second side of the glass substrate. The first and second via holes intersect, with the sidewalls of each of the first and second via hole curved from their respective via openings to the intersection of the first and second via holes. In some implementations, a dimension of the through-glass via hole at the intersection is less than the corresponding dimension at each via opening. In some implementations, a dimension of each via opening is greater than the thickness of the glass substrate.

[0008] In some implementations, the through-glass via hole is coated with a plated metal film that is continuous from the first side of the glass substrate to the second side. According to various implementations, an interior of a through-glass via hole may be unfilled, partially filled or wholly filled. For example, a through-glass via hole may be partially or substantially filled with one or more of an electrically conductive material, a thermally conductive material, or a non-conductive material.

[0009] According to various implementations, the first and second via holes may each have a constant or variable radius of curvature. For example, the via openings may be circular, slot-shape, or otherwise shaped. A via opening dimension may be, for example, a diameter of a circular opening or a width of a slot-shaped opening. In some implementations, the thickness of the conductive thin film can be between about 0.1 and 5 microns, and more particularly between, e.g., 0.1 and 0.2 microns. In some implementations, the substrate glass thickness can be at least about 100 microns, and more particularly, e.g., at least about 300 microns or at least about 500 microns.

[0010] In some implementations, a device such as an integrated circuit (IC) or MEMS device is mounted on the first side of the glass substrate and electrically connected to the conductive thin film in the through-glass via hole. An electrical component on the second side of the glass substrate may be connected to the IC or MEMS device through the conductive thin film in the through-glass via hole.

[0011] In some implementations, an apparatus includes a display, a processor configured to communicate with the display and configured to process image data and a memory device configured to communicate with the processor.

[0012] Another innovative aspect of the subject matter described in this disclosure includes an apparatus with a glass substrate having first and second sides, a MEMS or IC device mounted to the first side of the glass substrate, and means for electrically connecting the MEMS or IC device to the second side of the glass substrate. For example, the apparatus may include means for connecting the MEMS or IC device to an electrical component on the second side of the glass substrate.

[0013] Another innovative aspect of the subject matter described in this disclosure includes methods of forming a through-glass via. In some implementations, the methods include double-sided processes to form aligned via holes in a glass substrate that together form a contoured through-glass via hole, followed by deposition of a continuous thin film of an electrically conductive material. Double-sided methods of forming the through-glass via hole include wet etching, dry etching, sandblasting or a combination of these techniques. Forming a through-glass via hole may include contouring the hole to form a direct line-of-sight region that facilitates deposition of a continuous conductive thin film through the through-glass via hole. Single-sided or double-sided sputtering or other deposition techniques may be used to deposit a thin film in the through-glass via hole. Via metal thickness may be augmented with electro- or electroless plating. The thin-film through-glass vias may optionally be

filled, for example, with an electrically conductive material, a non-electrically conducting material, or a thermally conductive material.

[0014] In some implementations, the methods involve providing a glass substrate having first and second substantially planar parallel surfaces, forming a first via hole having curved sidewalls in the first surface and a second via hole in the second surface so that the first and second via holes intersect to form a through-glass via hole having via openings at the first and second surfaces and an intersection dimension that is less than the corresponding dimension at each via opening. In some implementations, the methods include coating at least a portion of the through-glass via hole with a conductive thin film that is continuous through the via hole from the first surface to the second surface.

[0015] According to various implementations, the first and second via holes may each have a constant or variable radius of curvature. In some implementations, forming the first and second via holes includes exposing the first and second surfaces to a wet etchant. The method may further involve masking the first and second surfaces, the masks having at least one opening, the smallest of which is d_M . In some implementations, an etch radius of the first and second via holes satisfies $R \geq R_{Min}$ where R is the etch radius, and $R_{Min} = (\sqrt{2})(t_s/2)/(1 + ((d_M + R_{Min})/R_{Min})(1 - (t_s/2R_{Min})^2)^{1/2})^{1/2}$ with t_s being a thickness of the glass substrate.

[0016] In some implementations, the methods involve aligning stencil patterns on the first and second surfaces of the glass substrate and sandblasting the substrate in accordance with the aligned stencil patterns. In some implementations, the methods involve, after sandblasting, wet etching the first and second via holes to form a direct line-of-sight region extending from the intersection of the first and second via holes.

[0017] Coating the through-glass via hole with a conductive thin film may involve deposition from two sides of the glass substrate, or only one side, according to the particular implementation. In some implementations, a metal layer is plated on the conductive thin film. Also in some implementations, the methods involve wholly or partially filling the through-glass via hole.

[0018] Details of one or more implementations of the subject matter described in this specification are set forth in the accompanying drawings and the description below. Other features, aspects, and advantages will become apparent from the description, the drawings, and the claims. Note that the relative dimensions of the following figures may not be drawn to scale.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] Figure 1 shows an example of an isometric view depicting two adjacent pixels in a series of pixels of an interferometric modulator (IMOD) display device.

5 [0020] Figure 2 shows an example of a system block diagram illustrating an electronic device incorporating a 3x3 interferometric modulator display.

[0021] Figure 3 shows an example of a diagram illustrating movable reflective layer position versus applied voltage for the interferometric modulator of Figure 1.

10 [0022] Figure 4 shows an example of a table illustrating various states of an interferometric modulator when various common and segment voltages are applied.

[0023] Figure 5A shows an example of a diagram illustrating a frame of display data in the 3x3 interferometric modulator display of Figure 2.

[0024] Figure 5B shows an example of a timing diagram for common and segment signals that may be used to write the frame of display data illustrated in Figure 5A.

15 [0025] Figure 6A shows an example of a partial cross-section of the interferometric modulator display of Figure 1.

[0026] Figures 6B–6E show examples of cross-sections of varying implementations of interferometric modulators.

20 [0027] Figure 7 shows an example of a flow diagram illustrating a manufacturing process for an interferometric modulator.

[0028] Figures 8A–8E show examples of cross-sectional schematic illustrations of various stages in a method of making an interferometric modulator.

[0029] Figures 9A and 9B show examples of isometric views depicting devices including through-glass vias.

25 [0030] Figures 10A–10E show examples of simplified cross-sectional illustrations of glass substrates having through-glass vias.

[0031] Figure 11A shows an example of a flow diagram illustrating a process for forming a through-glass via.

30 [0032] Figure 11B show examples of cross-sectional schematic illustrations of various stages in a method of forming a through-glass via.

[0033] Figure 12 shows an example of a flow diagram illustrating processes for forming through-glass via holes.

[0034] Figure 13 shows an example of a cross-sectional schematic illustration of a

through-glass via hole formed by double-sided wet etching.

[0035] Figures 14A–14D show examples of cross-sectional schematic illustrations of various stages of sandblasting methods of forming through-glass via holes.

[0036] Figures 14E and 14F show examples of cross-sectional schematic

5 illustrations of various stages of dry etch methods of forming through-glass via holes.

[0037] Figure 15 shows an example of a cross-sectional schematic illustration of a contoured through-glass via.

[0038] Figure 16 shows an example of a cross-sectional schematic illustration of certain etch parameters of a through-glass via hole.

10 [0039] Figure 17 shows an example of cross-sectional schematic illustrations of a glass substrate at various stages of simultaneous etching of aligned via holes to form a through-glass via hole.

[0040] Figures 18A–20B present examples of isometric and cross-sectional views of implementations of circular, slot-shaped, and square-shaped through-glass via

15 holes.

[0041] Figures 21A and 21B show examples of system block diagrams illustrating a display device that includes a plurality of interferometric modulators.

[0042] Like reference numbers and designations in the various drawings indicate like elements.

20 DETAILED DESCRIPTION

[0043] The following detailed description is directed to certain implementations for the purposes of describing the innovative aspects. However, the teachings herein can be applied in a multitude of different ways. The described implementations may be

25 implemented in any device that is configured to display an image, whether in motion (e.g., video) or stationary (e.g., still image), and whether textual, graphical or pictorial. More particularly, it is contemplated that the implementations may be implemented in or associated with a variety of electronic devices such as, but not limited to, mobile telephones, multimedia Internet enabled cellular telephones, mobile

30 television receivers, wireless devices, smartphones, bluetooth devices, personal data assistants (PDAs), wireless electronic mail receivers, hand-held or portable computers, netbooks, notebooks, smartbooks, printers, copiers, scanners, facsimile devices, GPS receivers/navigators, cameras, MP3 players, camcorders, game

consoles, wrist watches, clocks, calculators, television monitors, flat panel displays, electronic reading devices (e.g., e-readers), computer monitors, auto displays (e.g., odometer display, etc.), cockpit controls and/or displays, camera view displays (e.g., display of a rear view camera in a vehicle), electronic photographs, electronic

5 billboards or signs, projectors, architectural structures, microwaves, refrigerators, stereo systems, cassette recorders or players, DVD players, CD players, VCRs, radios, portable memory chips, washers, dryers, washer/dryers, parking meters, packaging (e.g., MEMS and non-MEMS), aesthetic structures (e.g., display of images on a piece of jewelry) and a variety of electromechanical systems devices. The teachings herein

10 also can be used in non-display applications such as, but not limited to, electronic switching devices, radio frequency filters, sensors, accelerometers, gyroscopes, motion-sensing devices, magnetometers, inertial components for consumer electronics, parts of consumer electronics products, varactors, liquid crystal devices, electrophoretic devices, drive schemes, manufacturing processes, electronic test

15 equipment. Thus, the teachings are not intended to be limited to the implementations depicted solely in the Figures, but instead have wide applicability as will be readily apparent to one having ordinary skill in the art.

[0044] Some implementations described herein relate to glass packaging of MEMS devices and other devices. Through-glass vias, which are electrical connections

20 extending through a glass panel or other glass substrate, and related fabrication methods are described herein. While implementations of the methods of fabrication and the resulting through-glass vias are described chiefly in the context of glass packaging of MEMS and IC devices, the methods and vias are not so limited and may be implemented in other contexts that employ, e.g., a conductive path through a glass

25 substrate.

[0045] In some implementations, through-glass vias can be provided in glass substrates having thicknesses of at about 100–700 microns. The through-glass vias include a conductive pathway extending through the glass substrate. In some implementations, the through-glass vias can include a thin film coating all or a portion

30 of the sidewalls of a through-glass via hole. In some implementations, the through-glass vias can include a plated metal coating all or a portion of the sidewalls of a through-glass via hole. The through-glass vias can be unfilled or include conductive or non-conductive fill materials according to the desired implementation.

[0046] In some implementations, a through-glass via can be provided in a planar

glass substrate. The through-glass via can include a sidewall having a concave curvature extending from a planar surface of the glass substrate to a point in the interior of the glass substrate. In some implementations, a through-glass via sidewall has two concave curvatures extending from opposing planar surfaces of the glass substrate and intersecting at a point in the interior of the glass substrate. In some implementations, a through-glass via hole has via openings in opposing surfaces of a glass substrate and an interior dimension that is less than the corresponding dimension at each via opening.

[0047] In some implementations, a glass substrate includes a through-glass via that, alone or in combination with contact pads, metal traces, and the like, electrically connects one or more of a MEMS device, IC device, sensor, circuitry, via, contact pad, SMD pad, or other electrically active device or conductive material on one side of the glass substrate to one or more of a MEMS device, IC device, sensor, circuitry, via, contact pad, SMD pad, or other electrically active device or conductive material on the other side of the glass substrate.

[0048] Methods of fabricating through-glass vias are described herein. In some implementations, the methods involve double-sided processes to form aligned holes in a glass substrate with the holes together forming a through-glass via hole. In some implementations, the methods involve single- or double-sided deposition of a continuous conductive thin film on the sidewalls of a through-glass via hole. Forming a through-glass via hole can involve contouring it to facilitate deposition of a continuous thin film. The methods described herein can involve plating sidewalls of the through-glass via hole and/or filling the through-glass via hole with a conductive or non-conductive fill material according to the desired implementation.

[0049] Particular implementations of the subject matter described in this disclosure can be implemented to realize one or more of the following potential advantages. In some implementations, batch panel-level processing methods can be used to eliminate or reduce die-level processing. Advantages of encapsulation and packaging in a batch process at a panel, or a sub-panel, level include a large number of units fabricated in parallel in the batch process, thus reducing costs per unit as compared to individual die level processing. The use of batch processes such as lithography, etching and plating over a large substrate in some implementations allows tighter tolerances and reduces die-to-die variation. The formation of through-glass interconnections in a single two-sided plating process stage can reduce costs per package. In some

implementations, smaller and/or more reliable packaged MEMS or other devices can be fabricated. Smaller devices can result in a larger number of units fabricated in parallel in the batch process. In some implementations, packaging related stresses on a MEMS or other device can be reduced or eliminated. For example, in some
5 implementations, concerns related to mold process stresses on, e.g., a MEMS device can be eliminated by providing a cover glass with surface mount pads without molding.

[0050] An example of a suitable MEMS device, to which the described implementations may apply, is a reflective display device. Reflective display devices
10 can incorporate interferometric modulators (IMODs) to selectively absorb and/or reflect light incident thereon using principles of optical interference. IMODs can include an absorber, a reflector that is movable with respect to the absorber, and an optical resonant cavity defined between the absorber and the reflector. The reflector can be moved to two or more different positions, which can change the size of the
15 optical resonant cavity and thereby affect the reflectance of the interferometric modulator. The reflectance spectrums of IMODs can create fairly broad spectral bands which can be shifted across the visible wavelengths to generate different colors. The position of the spectral band can be adjusted by changing the thickness of the optical resonant cavity, i.e., by changing the position of the reflector.

[0051] Figure 1 shows an example of an isometric view depicting two adjacent
20 pixels in a series of pixels of an interferometric modulator (IMOD) display device. The IMOD display device includes one or more interferometric MEMS display elements. In these devices, the pixels of the MEMS display elements can be in either a bright or dark state. In the bright (“relaxed,” “open” or “on”) state, the display
25 element reflects a large portion of incident visible light, e.g., to a user. Conversely, in the dark (“actuated,” “closed” or “off”) state, the display element reflects little incident visible light. In some implementations, the light reflectance properties of the on and off states may be reversed. MEMS pixels can be configured to reflect predominantly at particular wavelengths allowing for a color display in addition to
30 black and white.

[0052] The IMOD display device can include a row/column array of IMODs. Each IMOD can include a pair of reflective layers, i.e., a movable reflective layer and a fixed partially reflective layer, positioned at a variable and controllable distance from each other to form an air gap (also referred to as an optical gap or cavity). The

movable reflective layer may be moved between at least two positions. In a first position, i.e., a relaxed position, the movable reflective layer can be positioned at a relatively large distance from the fixed partially reflective layer. In a second position, i.e., an actuated position, the movable reflective layer can be positioned more closely to the partially reflective layer. Incident light that reflects from the two layers can interfere constructively or destructively depending on the position of the movable reflective layer, producing either an overall reflective or non-reflective state for each pixel. In some implementations, the IMOD may be in a reflective state when unactuated, reflecting light within the visible spectrum, and may be in a dark state when unactuated, reflecting light outside of the visible range (e.g., infrared light). In some other implementations, however, an IMOD may be in a dark state when unactuated, and in a reflective state when actuated. In some implementations, the introduction of an applied voltage can drive the pixels to change states. In some other implementations, an applied charge can drive the pixels to change states.

[0053] The depicted portion of the pixel array in Figure 1 includes two adjacent interferometric modulators 12. In the IMOD 12 on the left (as illustrated), a movable reflective layer 14 is illustrated in a relaxed position at a predetermined distance from an optical stack 16, which includes a partially reflective layer. The voltage V_0 applied across the IMOD 12 on the left is insufficient to cause actuation of the movable reflective layer 14. In the IMOD 12 on the right, the movable reflective layer 14 is illustrated in an actuated position near or adjacent the optical stack 16. The voltage V_{bias} applied across the IMOD 12 on the right is sufficient to maintain the movable reflective layer 14 in the actuated position.

[0054] In Figure 1, the reflective properties of pixels 12 are generally illustrated with arrows 13 indicating light incident upon the pixels 12, and light 15 reflecting from the pixel 12 on the left. Although not illustrated in detail, it will be understood by one having ordinary skill in the art that most of the light 13 incident upon the pixels 12 will be transmitted through the transparent substrate 20, toward the optical stack 16. A portion of the light incident upon the optical stack 16 will be transmitted through the partially reflective layer of the optical stack 16, and a portion will be reflected back through the transparent substrate 20. The portion of light 13 that is transmitted through the optical stack 16 will be reflected at the movable reflective layer 14, back toward (and through) the transparent substrate 20. Interference (constructive or destructive) between the light reflected from the partially reflective

layer of the optical stack 16 and the light reflected from the movable reflective layer 14 will determine the wavelength(s) of light 15 reflected from the pixel 12.

[0055] The optical stack 16 can include a single layer or several layers. The layer(s) can include one or more of an electrode layer, a partially reflective and partially transmissive layer and a transparent dielectric layer. In some implementations, the optical stack 16 is electrically conductive, partially transparent and partially reflective, and may be fabricated, for example, by depositing one or more of the above layers onto a transparent substrate 20. The electrode layer can be formed from a variety of materials, such as various metals, for example indium tin oxide (ITO). The partially reflective layer can be formed from a variety of materials that are partially reflective, such as various metals, e.g., chromium (Cr), semiconductors, and dielectrics. The partially reflective layer can be formed of one or more layers of materials, and each of the layers can be formed of a single material or a combination of materials. In some implementations, the optical stack 16 can include a single semi-transparent thickness of metal or semiconductor which serves as both an optical absorber and conductor, while different, more conductive layers or portions (e.g., of the optical stack 16 or of other structures of the IMOD) can serve to bus signals between IMOD pixels. The optical stack 16 also can include one or more insulating or dielectric layers covering one or more conductive layers or a conductive/absorptive layer.

[0056] In some implementations, the layer(s) of the optical stack 16 can be patterned into parallel strips, and may form row electrodes in a display device as described further below. As will be understood by one having skill in the art, the term “patterned” is used herein to refer to masking as well as etching processes. In some implementations, a highly conductive and reflective material, such as aluminum (Al), may be used for the movable reflective layer 14, and these strips may form column electrodes in a display device. The movable reflective layer 14 may be formed as a series of parallel strips of a deposited metal layer or layers (orthogonal to the row electrodes of the optical stack 16) to form columns deposited on top of posts 18 and an intervening sacrificial material deposited between the posts 18. When the sacrificial material is etched away, a defined gap 19, or optical cavity, can be formed between the movable reflective layer 14 and the optical stack 16. In some implementations, the spacing between posts 18 may be approximately 1–1000 μm , while the gap 19 may be approximately less than 10,000 Angstroms ($\text{\AA}$).

[0057] In some implementations, each pixel of the IMOD, whether in the actuated or relaxed state, is essentially a capacitor formed by the fixed and moving reflective layers. When no voltage is applied, the movable reflective layer 14 remains in a mechanically relaxed state, as illustrated by the pixel 12 on the left in Figure 1, with the gap 19 between the movable reflective layer 14 and optical stack 16. However, when a potential difference, e.g., voltage, is applied to at least one of a selected row and column, the capacitor formed at the intersection of the row and column electrodes at the corresponding pixel becomes charged, and electrostatic forces pull the electrodes together. If the applied voltage exceeds a threshold, the movable reflective layer 14 can deform and move near or against the optical stack 16. A dielectric layer (not shown) within the optical stack 16 may prevent shorting and control the separation distance between the layers 14 and 16, as illustrated by the actuated pixel 12 on the right in Figure 1. The behavior is the same regardless of the polarity of the applied potential difference. Though a series of pixels in an array may be referred to in some instances as “rows” or “columns,” a person having ordinary skill in the art will readily understand that referring to one direction as a “row” and another as a “column” is arbitrary. Restated, in some orientations, the rows can be considered columns, and the columns considered to be rows. Furthermore, the display elements may be evenly arranged in orthogonal rows and columns (an “array”), or arranged in non-linear configurations, for example, having certain positional offsets with respect to one another (a “mosaic”). The terms “array” and “mosaic” may refer to either configuration. Thus, although the display is referred to as including an “array” or “mosaic,” the elements themselves need not be arranged orthogonally to one another, or disposed in an even distribution, in any instance, but may include arrangements having asymmetric shapes and unevenly distributed elements.

[0058] Figure 2 shows an example of a system block diagram illustrating an electronic device incorporating a 3x3 interferometric modulator display. The electronic device includes a processor 21 that may be configured to execute one or more software modules. In addition to executing an operating system, the processor 21 may be configured to execute one or more software applications, including a web browser, a telephone application, an email program, or any other software application.

[0059] The processor 21 can be configured to communicate with an array driver 22. The array driver 22 can include a row driver circuit 24 and a column driver circuit 26 that provide signals to, e.g., a display array or panel 30. The cross section of the

IMOD display device illustrated in Figure 1 is shown by the lines 1–1 in Figure 2.

Although Figure 2 illustrates a 3x3 array of IMODs for the sake of clarity, the display array 30 may contain a very large number of IMODs, and may have a different number of IMODs in rows than in columns, and vice versa.

5 **[0060]** Figure 3 shows an example of a diagram illustrating movable reflective layer position versus applied voltage for the interferometric modulator of Figure 1. For MEMS interferometric modulators, the row/column (i.e., common/segment) write procedure may take advantage of a hysteresis property of these devices as illustrated in Figure 3. An interferometric modulator may require, for example, about a 10-volt
10 potential difference to cause the movable reflective layer, or mirror, to change from the relaxed state to the actuated state. When the voltage is reduced from that value, the movable reflective layer maintains its state as the voltage drops back below, e.g., 10-volts, however, the movable reflective layer does not relax completely until the voltage drops below 2-volts. Thus, a range of voltage, approximately 3 to 7-volts, as
15 shown in Figure 3, exists where there is a window of applied voltage within which the device is stable in either the relaxed or actuated state. This is referred to herein as the “hysteresis window” or “stability window.” For a display array 30 having the hysteresis characteristics of Figure 3, the row/column write procedure can be designed to address one or more rows at a time, such that during the addressing of a given row,
20 pixels in the addressed row that are to be actuated are exposed to a voltage difference of about 10-volts, and pixels that are to be relaxed are exposed to a voltage difference of near zero volts. After addressing, the pixels are exposed to a steady state or bias voltage difference of approximately 5-volts such that they remain in the previous strobing state. In this example, after being addressed, each pixel sees a potential
25 difference within the “stability window” of about 3–7-volts. This hysteresis property feature enables the pixel design, e.g., illustrated in Figure 1, to remain stable in either an actuated or relaxed pre-existing state under the same applied voltage conditions. Since each IMOD pixel, whether in the actuated or relaxed state, is essentially a capacitor formed by the fixed and moving reflective layers, this stable state can be
30 held at a steady voltage within the hysteresis window without substantially consuming or losing power. Moreover, essentially little or no current flows into the IMOD pixel if the applied voltage potential remains substantially fixed.

[0061] In some implementations, a frame of an image may be created by applying data signals in the form of “segment” voltages along the set of column electrodes, in

accordance with the desired change (if any) to the state of the pixels in a given row. Each row of the array can be addressed in turn, such that the frame is written one row at a time. To write the desired data to the pixels in a first row, segment voltages corresponding to the desired state of the pixels in the first row can be applied on the column electrodes, and a first row pulse in the form of a specific “common” voltage or signal can be applied to the first row electrode. The set of segment voltages can then be changed to correspond to the desired change (if any) to the state of the pixels in the second row, and a second common voltage can be applied to the second row electrode. In some implementations, the pixels in the first row are unaffected by the change in the segment voltages applied along the column electrodes, and remain in the state they were set to during the first common voltage row pulse. This process may be repeated for the entire series of rows, or alternatively, columns, in a sequential fashion to produce the image frame. The frames can be refreshed and/or updated with new image data by continually repeating this process at some desired number of frames per second.

[0062] The combination of segment and common signals applied across each pixel (that is, the potential difference across each pixel) determines the resulting state of each pixel. Figure 4 shows an example of a table illustrating various states of an interferometric modulator when various common and segment voltages are applied. As will be readily understood by one having ordinary skill in the art, the “segment” voltages can be applied to either the column electrodes or the row electrodes, and the “common” voltages can be applied to the other of the column electrodes or the row electrodes.

[0063] As illustrated in Figure 4 (as well as in the timing diagram shown in Figure 5B), when a release voltage $V_{C_{REL}}$ is applied along a common line, all interferometric modulator elements along the common line will be placed in a relaxed state, alternatively referred to as a released or unactuated state, regardless of the voltage applied along the segment lines, i.e., high segment voltage V_{S_H} and low segment voltage V_{S_L} . In particular, when the release voltage $V_{C_{REL}}$ is applied along a common line, the potential voltage across the modulator (alternatively referred to as a pixel voltage) is within the relaxation window (see Figure 3, also referred to as a release window) both when the high segment voltage V_{S_H} and the low segment voltage V_{S_L} are applied along the corresponding segment line for that pixel.

[0064] When a hold voltage is applied on a common line, such as a high hold

voltage $V_{\text{HOLD_H}}$ or a low hold voltage $V_{\text{HOLD_L}}$, the state of the interferometric modulator will remain constant. For example, a relaxed IMOD will remain in a relaxed position, and an actuated IMOD will remain in an actuated position. The hold voltages can be selected such that the pixel voltage will remain within a stability window both when the high segment voltage $V_{\text{S_H}}$ and the low segment voltage $V_{\text{S_L}}$ are applied along the corresponding segment line. Thus, the segment voltage swing, i.e., the difference between the high $V_{\text{S_H}}$ and low segment voltage $V_{\text{S_L}}$, is less than the width of either the positive or the negative stability window.

[0065] When an addressing, or actuation, voltage is applied on a common line, such as a high addressing voltage $V_{\text{C_ADD_H}}$ or a low addressing voltage $V_{\text{C_ADD_L}}$, data can be selectively written to the modulators along that line by application of segment voltages along the respective segment lines. The segment voltages may be selected such that actuation is dependent upon the segment voltage applied. When an addressing voltage is applied along a common line, application of one segment voltage will result in a pixel voltage within a stability window, causing the pixel to remain unactuated. In contrast, application of the other segment voltage will result in a pixel voltage beyond the stability window, resulting in actuation of the pixel. The particular segment voltage which causes actuation can vary depending upon which addressing voltage is used. In some implementations, when the high addressing voltage $V_{\text{C_ADD_H}}$ is applied along the common line, application of the high segment voltage $V_{\text{S_H}}$ can cause a modulator to remain in its current position, while application of the low segment voltage $V_{\text{S_L}}$ can cause actuation of the modulator. As a corollary, the effect of the segment voltages can be the opposite when a low addressing voltage $V_{\text{C_ADD_L}}$ is applied, with high segment voltage $V_{\text{S_H}}$ causing actuation of the modulator, and low segment voltage $V_{\text{S_L}}$ having no effect (i.e., remaining stable) on the state of the modulator.

[0066] In some implementations, hold voltages, address voltages, and segment voltages may be used which always produce the same polarity potential difference across the modulators. In some other implementations, signals can be used which alternate the polarity of the potential difference of the modulators. Alternation of the polarity across the modulators (that is, alternation of the polarity of write procedures) may reduce or inhibit charge accumulation which could occur after repeated write operations of a single polarity.

[0067] Figure 5A shows an example of a diagram illustrating a frame of display

data in the 3x3 interferometric modulator display of Figure 2. Figure 5B shows an example of a timing diagram for common and segment signals that may be used to write the frame of display data illustrated in Figure 5A. The signals can be applied to the, e.g., 3x3 array of Figure 2, which will ultimately result in the line time 60e

5 display arrangement illustrated in Figure 5A. The actuated modulators in Figure 5A are in a dark-state, i.e., where a substantial portion of the reflected light is outside of the visible spectrum so as to result in a dark appearance to, e.g., a viewer. Prior to writing the frame illustrated in Figure 5A, the pixels can be in any state, but the write procedure illustrated in the timing diagram of Figure 5B presumes that each
10 modulator has been released and resides in an unactuated state before the first line time 60a.

[0068] During the first line time 60a: a release voltage 70 is applied on common line 1; the voltage applied on common line 2 begins at a high hold voltage 72 and moves to a release voltage 70; and a low hold voltage 76 is applied along common
15 line 3. Thus, the modulators (common 1, segment 1), (1,2) and (1,3) along common line 1 remain in a relaxed, or unactuated, state for the duration of the first line time 60a, the modulators (2,1), (2,2) and (2,3) along common line 2 will move to a relaxed state, and the modulators (3,1), (3,2) and (3,3) along common line 3 will remain in their previous state. With reference to Figure 4, the segment voltages applied along
20 segment lines 1, 2 and 3 will have no effect on the state of the interferometric modulators, as none of common lines 1, 2 or 3 are being exposed to voltage levels causing actuation during line time 60a (i.e., $V_{C_{REL}}$ – relax and $V_{C_{HOLD_L}}$ – stable).

[0069] During the second line time 60b, the voltage on common line 1 moves to a high hold voltage 72, and all modulators along common line 1 remain in a relaxed
25 state regardless of the segment voltage applied because no addressing, or actuation, voltage was applied on the common line 1. The modulators along common line 2 remain in a relaxed state due to the application of the release voltage 70, and the modulators (3,1), (3,2) and (3,3) along common line 3 will relax when the voltage along common line 3 moves to a release voltage 70.

30 **[0070]** During the third line time 60c, common line 1 is addressed by applying a high address voltage 74 on common line 1. Because a low segment voltage 64 is applied along segment lines 1 and 2 during the application of this address voltage, the pixel voltage across modulators (1,1) and (1,2) is greater than the high end of the positive stability window (i.e., the voltage differential exceeded a predefined

threshold) of the modulators, and the modulators (1,1) and (1,2) are actuated.

Conversely, because a high segment voltage 62 is applied along segment line 3, the pixel voltage across modulator (1,3) is less than that of modulators (1,1) and (1,2), and remains within the positive stability window of the modulator; modulator (1,3)

5 thus remains relaxed. Also during line time 60c, the voltage along common line 2 decreases to a low hold voltage 76, and the voltage along common line 3 remains at a release voltage 70, leaving the modulators along common lines 2 and 3 in a relaxed position.

[0071] During the fourth line time 60d, the voltage on common line 1 returns to a
10 high hold voltage 72, leaving the modulators along common line 1 in their respective addressed states. The voltage on common line 2 is decreased to a low address voltage 78. Because a high segment voltage 62 is applied along segment line 2, the pixel voltage across modulator (2,2) is below the lower end of the negative stability window of the modulator, causing the modulator (2,2) to actuate. Conversely,
15 because a low segment voltage 64 is applied along segment lines 1 and 3, the modulators (2,1) and (2,3) remain in a relaxed position. The voltage on common line 3 increases to a high hold voltage 72, leaving the modulators along common line 3 in a relaxed state.

[0072] Finally, during the fifth line time 60e, the voltage on common line 1 remains
20 at high hold voltage 72, and the voltage on common line 2 remains at a low hold voltage 76, leaving the modulators along common lines 1 and 2 in their respective addressed states. The voltage on common line 3 increases to a high address voltage 74 to address the modulators along common line 3. As a low segment voltage 64 is applied on segment lines 2 and 3, the modulators (3,2) and (3,3) actuate, while the
25 high segment voltage 62 applied along segment line 1 causes modulator (3,1) to remain in a relaxed position. Thus, at the end of the fifth line time 60e, the 3x3 pixel array is in the state shown in Figure 5A, and will remain in that state as long as the hold voltages are applied along the common lines, regardless of variations in the segment voltage which may occur when modulators along other common lines (not
30 shown) are being addressed.

[0073] In the timing diagram of Figure 5B, a given write procedure (i.e., line times 60a–60e) can include the use of either high hold and address voltages, or low hold and address voltages. Once the write procedure has been completed for a given common line (and the common voltage is set to the hold voltage having the same polarity as the

actuation voltage), the pixel voltage remains within a given stability window, and does not pass through the relaxation window until a release voltage is applied on that common line. Furthermore, as each modulator is released as part of the write procedure prior to addressing the modulator, the actuation time of a modulator, rather than the release time, may determine the necessary line time. Specifically, in implementations in which the release time of a modulator is greater than the actuation time, the release voltage may be applied for longer than a single line time, as depicted in Figure 5B. In some other implementations, voltages applied along common lines or segment lines may vary to account for variations in the actuation and release voltages of different modulators, such as modulators of different colors.

[0074] The details of the structure of interferometric modulators that operate in accordance with the principles set forth above may vary widely. For example, Figures 6A–6E show examples of cross-sections of varying implementations of interferometric modulators, including the movable reflective layer 14 and its supporting structures. Figure 6A shows an example of a partial cross-section of the interferometric modulator display of Figure 1, where a strip of metal material, i.e., the movable reflective layer 14 is deposited on supports 18 extending orthogonally from the substrate 20. In Figure 6B, the movable reflective layer 14 of each IMOD is generally square or rectangular in shape and attached to supports at or near the corners, on tethers 32. In Figure 6C, the movable reflective layer 14 is generally square or rectangular in shape and suspended from a deformable layer 34, which may include a flexible metal. The deformable layer 34 can connect, directly or indirectly, to the substrate 20 around the perimeter of the movable reflective layer 14. These connections are herein referred to as support posts. The implementation shown in Figure 6C has additional benefits deriving from the decoupling of the optical functions of the movable reflective layer 14 from its mechanical functions, which are carried out by the deformable layer 34. This decoupling allows the structural design and materials used for the reflective layer 14 and those used for the deformable layer 34 to be optimized independently of one another.

[0075] Figure 6D shows another example of an IMOD, where the movable reflective layer 14 includes a reflective sub-layer 14a. The movable reflective layer 14 rests on a support structure, such as support posts 18. The support posts 18 provide separation of the movable reflective layer 14 from the lower stationary electrode (i.e., part of the optical stack 16 in the illustrated IMOD) so that a gap 19 is

formed between the movable reflective layer 14 and the optical stack 16, for example when the movable reflective layer 14 is in a relaxed position. The movable reflective layer 14 also can include a conductive layer 14c, which may be configured to serve as an electrode, and a support layer 14b. In this example, the conductive layer 14c is disposed on one side of the support layer 14b, distal from the substrate 20, and the reflective sub-layer 14a is disposed on the other side of the support layer 14b, proximal to the substrate 20. In some implementations, the reflective sub-layer 14a can be conductive and can be disposed between the support layer 14b and the optical stack 16. The support layer 14b can include one or more layers of a dielectric material, for example, silicon oxynitride (SiON) or silicon dioxide (SiO₂). In some implementations, the support layer 14b can be a stack of layers, such as, for example, a SiO₂/SiON/SiO₂ tri-layer stack. Either or both of the reflective sub-layer 14a and the conductive layer 14c can include, e.g., an aluminum (Al) alloy with about 0.5% copper (Cu), or another reflective metallic material. Employing conductive layers 14a, 14c above and below the dielectric support layer 14b can balance stresses and provide enhanced conduction. In some implementations, the reflective sub-layer 14a and the conductive layer 14c can be formed of different materials for a variety of design purposes, such as achieving specific stress profiles within the movable reflective layer 14.

[0076] As illustrated in Figure 6D, some implementations also can include a black mask structure 23. The black mask structure 23 can be formed in optically inactive regions (e.g., between pixels or under posts 18) to absorb ambient or stray light. The black mask structure 23 also can improve the optical properties of a display device by inhibiting light from being reflected from or transmitted through inactive portions of the display, thereby increasing the contrast ratio. Additionally, the black mask structure 23 can be conductive and be configured to function as an electrical bussing layer. In some implementations, the row electrodes can be connected to the black mask structure 23 to reduce the resistance of the connected row electrode. The black mask structure 23 can be formed using a variety of methods, including deposition and patterning techniques. The black mask structure 23 can include one or more layers. For example, in some implementations, the black mask structure 23 includes a molybdenum-chromium (MoCr) layer that serves as an optical absorber, a SiO₂ layer, and an aluminum alloy that serves as a reflector and a bussing layer, with a thickness in the range of about 30–80 Å, 500–1000 Å, and 500–6000 Å, respectively. The one

or more layers can be patterned using a variety of techniques, including photolithography and dry etching, including, for example, carbon tetrafluoride (CF_4) and/or oxygen (O_2) for the MoCr and SiO_2 layers and chlorine (Cl_2) and/or boron trichloride (BCl_3) for the aluminum alloy layer. In some implementations, the black mask 23 can be an etalon or interferometric stack structure. In such interferometric stack black mask structures 23, the conductive absorbers can be used to transmit or bus signals between lower, stationary electrodes in the optical stack 16 of each row or column. In some implementations, a spacer layer 35 can serve to generally electrically isolate the absorber layer 16a from the conductive layers in the black mask 23.

[0077] Figure 6E shows another example of an IMOD, where the movable reflective layer 14 is self supporting. In contrast with Figure 6D, the implementation of Figure 6E does not include support posts 18. Instead, the movable reflective layer 14 contacts the underlying optical stack 16 at multiple locations, and the curvature of the movable reflective layer 14 provides sufficient support that the movable reflective layer 14 returns to the unactuated position of Figure 6E when the voltage across the interferometric modulator is insufficient to cause actuation. The optical stack 16, which may contain a plurality of several different layers, is shown here for clarity including an optical absorber 16a, and a dielectric 16b. In some implementations, the optical absorber 16a may serve both as a fixed electrode and as a partially reflective layer.

[0078] In implementations such as those shown in Figures 6A–6E, the IMODs function as direct-view devices, in which images are viewed from the front side of the transparent substrate 20, i.e., the side opposite to that upon which the modulator is arranged. In these implementations, the back portions of the device (that is, any portion of the display device behind the movable reflective layer 14, including, for example, the deformable layer 34 illustrated in Figure 6C) can be configured and operated upon without impacting or negatively affecting the image quality of the display device, because the reflective layer 14 optically shields those portions of the device. For example, in some implementations a bus structure (not illustrated) can be included behind the movable reflective layer 14 which provides the ability to separate the optical properties of the modulator from the electromechanical properties of the modulator, such as voltage addressing and the movements that result from such addressing. Additionally, the implementations of Figures 6A–6E can simplify

processing, such as, e.g., patterning.

[0079] Figure 7 shows an example of a flow diagram illustrating a manufacturing process 80 for an interferometric modulator, and Figures 8A–8E show examples of cross-sectional schematic illustrations of corresponding stages of such a

5 manufacturing process 80. In some implementations, the manufacturing process 80 can be implemented to manufacture, e.g., interferometric modulators of the general type illustrated in Figures 1 and 6, in addition to other blocks not shown in Figure 7. With reference to Figures 1, 6 and 7, the process 80 begins at block 82 with the formation of the optical stack 16 over the substrate 20. Figure 8A illustrates such an
10 optical stack 16 formed over the substrate 20. The substrate 20 may be a transparent substrate such as glass or plastic, it may be flexible or relatively stiff and unbending, and may have been subjected to prior preparation processes, e.g., cleaning, to facilitate efficient formation of the optical stack 16. As discussed above, the optical stack 16 can be electrically conductive, partially transparent and partially reflective
15 and may be fabricated, for example, by depositing one or more layers having the desired properties onto the transparent substrate 20. In Figure 8A, the optical stack 16 includes a multilayer structure having sub-layers 16a and 16b, although more or fewer sub-layers may be included in some other implementations. In some implementations, one of the sub-layers 16a, 16b can be configured with both optically
20 absorptive and conductive properties, such as the combined conductor/absorber sub-layer 16a. Additionally, one or more of the sub-layers 16a, 16b can be patterned into parallel strips, and may form row electrodes in a display device. Such patterning can be performed by a masking and etching process or another suitable process known in the art. In some implementations, one of the sub-layers 16a, 16b can be an insulating
25 or dielectric layer, such as sub-layer 16b that is deposited over one or more metal layers (e.g., one or more reflective and/or conductive layers). In addition, the optical stack 16 can be patterned into individual and parallel strips that form the rows of the display.

[0080] The process 80 continues at block 84 with the formation of a sacrificial
30 layer 25 over the optical stack 16. The sacrificial layer 25 is later removed (e.g., at block 90) to form the cavity 19 and thus the sacrificial layer 25 is not shown in the resulting interferometric modulators 12 illustrated in Figure 1. Figure 8B illustrates a partially fabricated device including a sacrificial layer 25 formed over the optical stack 16. The formation of the sacrificial layer 25 over the optical stack 16 may

include deposition of a xenon difluoride (XeF_2)-etchable material such as molybdenum (Mo) or amorphous silicon (Si), in a thickness selected to provide, after subsequent removal, a gap or cavity 19 (see also Figures 1 and 8E) having a desired design size. Deposition of the sacrificial material may be carried out using deposition techniques such as physical vapor deposition (PVD, e.g., sputtering), plasma-enhanced chemical vapor deposition (PECVD), thermal chemical vapor deposition (thermal CVD), or spin-coating.

[0081] The process 80 continues at block 86 with the formation of a support structure e.g., a post 18 as illustrated in Figures 1, 6 and 8C. The formation of the post 18 may include patterning the sacrificial layer 25 to form a support structure aperture, then depositing a material (e.g., a polymer or an inorganic material, e.g., silicon oxide) into the aperture to form the post 18, using a deposition method such as PVD, PECVD, thermal CVD, or spin-coating. In some implementations, the support structure aperture formed in the sacrificial layer can extend through both the sacrificial layer 25 and the optical stack 16 to the underlying substrate 20, so that the lower end of the post 18 contacts the substrate 20 as illustrated in Figure 6A. Alternatively, as depicted in Figure 8C, the aperture formed in the sacrificial layer 25 can extend through the sacrificial layer 25, but not through the optical stack 16. For example, Figure 8E illustrates the lower ends of the support posts 18 in contact with an upper surface of the optical stack 16. The post 18, or other support structures, may be formed by depositing a layer of support structure material over the sacrificial layer 25 and patterning portions of the support structure material located away from apertures in the sacrificial layer 25. The support structures may be located within the apertures, as illustrated in Figure 8C, but also can, at least partially, extend over a portion of the sacrificial layer 25. As noted above, the patterning of the sacrificial layer 25 and/or the support posts 18 can be performed by a patterning and etching process, but also may be performed by alternative etching methods.

[0082] The process 80 continues at block 88 with the formation of a movable reflective layer or membrane such as the movable reflective layer 14 illustrated in Figures 1, 6 and 8D. The movable reflective layer 14 may be formed by employing one or more deposition steps, e.g., reflective layer (e.g., aluminum, aluminum alloy) deposition, along with one or more patterning, masking, and/or etching steps. The movable reflective layer 14 can be electrically conductive, and referred to as an electrically conductive layer. In some implementations, the movable reflective layer

14 may include a plurality of sub-layers 14a, 14b, 14c as shown in Figure 8D. In some implementations, one or more of the sub-layers, such as sub-layers 14a, 14c, may include highly reflective sub-layers selected for their optical properties, and another sub-layer 14b may include a mechanical sub-layer selected for its mechanical properties. Since the sacrificial layer 25 is still present in the partially fabricated interferometric modulator formed at block 88, the movable reflective layer 14 is typically not movable at this stage. A partially fabricated IMOD that contains a sacrificial layer 25 may also be referred to herein as an “unreleased” IMOD. As described above in connection with Figure 1, the movable reflective layer 14 can be patterned into individual and parallel strips that form the columns of the display.

[0083] The process 80 continues at block 90 with the formation of a cavity, e.g., cavity 19 as illustrated in Figures 1, 6 and 8E. The cavity 19 may be formed by exposing the sacrificial material 25 (deposited at block 84) to an etchant. For example, an etchable sacrificial material such as Mo or amorphous Si may be removed by dry chemical etching, e.g., by exposing the sacrificial layer 25 to a gaseous or vaporous etchant, such as vapors derived from solid XeF_2 for a period of time that is effective to remove the desired amount of material, typically selectively removed relative to the structures surrounding the cavity 19. Other etching methods, e.g. wet etching and/or plasma etching, also may be used. Since the sacrificial layer 25 is removed during block 90, the movable reflective layer 14 is typically movable after this stage. After removal of the sacrificial material 25, the resulting fully or partially fabricated IMOD may be referred to herein as a “released” IMOD.

[0084] Implementations described herein relate to glass packaging of MEMS, including IMODs, and other devices. The through-glass vias described herein may be implemented for MEMS and non-MEMS devices including on-wafer (or on-panel) devices that are formed prior to die singulation, such as dies embellished with leads or pads for connecting the device to another package or directly to a printed wiring board or flex tape, or for stacked or multi-substrate configurations. While implementations of the methods of fabrication and the resulting through-glass vias are described chiefly in the context of glass packaging of MEMS and IC devices, the methods and vias are not so limited and may be applied in other contexts that employ a conductive path through a glass substrate.

[0085] Figures 9A and 9B shows examples of isometric views depicting devices including through-glass vias. Figure 9A shows an example of device 99 including

glass substrate 91 with through-glass vias 93 formed therein. Glass substrate 91 is a generally planar substrate having two major substantially parallel surfaces, top surface 92a and bottom surface 92b. Although it is depicted as transparent in the associated Figures, glass substrate 91 may be transparent or non-transparent. A through-glass via 93 has curved sidewalls and provides a conductive pathway between portions of top surface 92a and bottom surface 92b through glass substrate 91. In the example depicted in Figure 9A, conductive topside trace 94a on top surface 92a connects through-glass via 93 to a topside bond pad 95a, which can be used for connections to an IC device (not shown) that is flip-chip or wire bonded to glass substrate 91. A MEMS device 96, shown as an outlined region, can be formed on or attached to glass substrate 91. The MEMS and IC devices can be electrically connected to one or more through-glass vias 93 directly or indirectly by topside traces 94a on glass substrate 91. Conductive bottomside traces 94b on bottom surface 92b of glass substrate 91 provide bottomside electrical connections from through-glass vias 93. In the example shown, bottomside bond pads 95b allow for connections to a printed circuit board or other substrate (not shown). Through-glass vias 93 thus provide direct electrical connection from one or more traces, pads, ICs, MEMS devices, or other components on one side of glass substrate 91 to one or more traces, pads, ICs, MEMS devices or other components on the opposing side.

[0086] Figure 9B shows another example of a device having through-glass vias with like-numbered elements corresponding to like-numbered elements in Figure 9A. Device 99 includes glass substrate 91 with top surface 92a and bottom surface 92b having a pair of through-glass vias 93 extending through glass substrate 91. In this example, MEMS device 96 connects electrically to bottomside bond pad 95b through topside trace 94a, through-glass via 93, and bottomside trace 94b.

[0087] Figures 10A–10E show examples of simplified cross-sectional illustrations of glass substrates having through-glass vias. In Figure 10A, a through-glass via 93, including a conductive thin film 101, is provided in a glass substrate 91a, which in this implementation is a MEMS device glass substrate, i.e., a glass substrate on which a MEMS device 96 is formed or otherwise attached. Conductive thin film 101 of through-glass via 93 provides a conductive pathway through MEMS device glass substrate 91a. Accordingly, through-glass via 93 provides an electrical connection between MEMS device 96 on one side of MEMS device glass substrate 91a and a flip-chip bonded integrated circuit 97 on the other side of MEMS device glass

substrate 91a. In Figure 10B, a through-glass via 93 also is provided in a glass substrate 91a, which is a MEMS device substrate. In this implementation, through-glass via 93 having a conductive thin film 101 in the via connects a MEMS device 96 on one side of the MEMS device glass substrate 91a to an electrically active

5 component 98 on the other side. Electrically active component 98 may be, for example, an electronic component or a MEMS sensor. In Figure 10C, a through-glass via 93 is formed in a glass substrate 91b, which in this implementation is a surface mount device (SMD) glass substrate, and provides a conductive path between an SMD pad 95 on one side of SMD glass substrate 91b and an electrical trace 94 on the
10 other side. In Figure 10D, a through-glass via 93 is formed in a MEMS device glass substrate 91a to provide an electrical connection between a MEMS device 96 and an SMD pad 95 on opposite sides of MEMS device glass substrate 91a. MEMS device glass substrate 91a may be directly mounted, for example, on a printed circuit board (PCB) with SMD pad 95 providing an electrical interface to the PCB (not shown).

15 **[0088]** In some implementations, two or more substrates with at least one substrate having a thin-film through-glass via are joined together. For example, in Figure 10E, a through-glass via 93a, including thin film conductive layer 101a, is formed in a MEMS device glass substrate 91a, with another through-glass via 93b, including thin film conductive layer 101b, formed in an SMD glass substrate 91b. MEMS device
20 glass substrate 91a and SMD glass substrate 91b are bonded together, e.g., with a metal or a polymer, such as a UV-curable polymer. Through-glass vias 93a and 93b electrically connect MEMS device 96 fabricated on MEMS device glass substrate 91a to SMD pad 95 formed on SMD glass substrate 91b. In some implementations, one or more contact pads may be formed on the bottom surface of MEMS device glass
25 substrate 91a and/or top of surface of SMD pad 95 to connect through-glass vias 93a and 93b. While through-glass vias 93a and 93b are directly aligned in Figure 10E, in alternate implementations (not shown) the through-glass vias may not be directly aligned, and may be electrically interconnected with conductive traces and contact pads on one or both substrates.

30 **[0089]** While Figures 9A, 9B and 10A–10E provide examples of implementations of the through-glass vias, they are not limited to these implementations, and may be used to provide a conductive path through any glass substrate. According to various implementations, the through-glass vias may be used alone or in connection with contact pads, metal traces, and the like to connect a device, sensor, circuitry, via,

contact pad, SMD pad, or other electrically active device or conductive material on one side of a glass substrate to a device, sensor, circuitry, via, contact pad, SMD pad, or other electrically active device or conductive material on the other side of the glass substrate.

5 **[0090]** According to various implementations, the glass substrate in which the via is formed is substantially planar having substantially parallel major surfaces (also referred to as top and bottom surfaces). One having ordinary skill in the art will understand that each surface may include various recessed or raised features, e.g., to accommodate a MEMS component, an integrated circuit, or other device. According to various implementations, the thickness of the glass substrate is typically between about 50 and 700 microns. The substrate thickness may vary according to the desired implementation. For example, in some implementations in which the glass substrate is a MEMS device substrate that is to be further packaged, the thickness may be between about 50 and 300 microns, such as 100 microns or 300 microns. Substrates that include SMD pads and are configured to mount onto a PCB may have thicknesses of at least about 300 microns, e.g., between about 300 and 500 microns. Configurations that include one or more glass substrates or panels may have thicknesses of 700 microns or more.

20 **[0091]** The through-glass vias described herein may be unfilled or filled. Filled vias may be partially or substantially filled. Partially filled vias are vias in which fill material is present in the via hole, but an unfilled path is present through the via hole. Substantially filled vias include fill material such that there is no unfilled path through the via hole.

25 **[0092]** The through-glass vias have a via opening on each side of the substrate, and a continuous conductive path from one via opening to the other. In some implementations, a dimension of the via openings (e.g., diameter or width) is on the order of the substrate thickness or larger. In the examples provided in Figures 9A and 9B, through-glass vias 93 have a via opening dimension (diameter) of about the same magnitude as the thickness of glass substrate 91. Sizes of through-glass vias according to various implementations are described further below.

30 **[0093]** In Figures 9A and 9B, the via openings are circular. In alternative implementations, via openings may be otherwise shaped, including slot-shaped. An example of a slot-shaped via is depicted in Figure 19, discussed further below. A slot-shaped via opening may be characterized as an elongated rectangle having

rounded corners, with a longer dimension, length L, and a shorter dimension, width W. The via openings also may be oval-shaped, half-circle shaped, rectangular-shaped, square-shaped, square-shaped with rounded corners, etc. In some implementations, multiple vias are arranged in arrays. In some implementations, via
5 openings have rounded edges with no sharp corners.

[0094] An overview of methods of fabricating the through-glass vias are described below with reference to Figures 11A, 11B and 12, with further description of the resulting structures described with reference to Figure 13. Specific implementations are discussed with reference to Figures 14A–20B.

10 **[0095]** Figure 11A shows an example of a flow diagram illustrating a process for forming a through-glass via; Figure 11B shows examples of cross-sectional schematic illustrations of various stages in a method of forming a through-glass via. First turning to Figure 11A, method 110 starts with an operation 111 in which a glass substrate is provided. Thicknesses of the glass substrate according to various
15 implementations are described above. The substrates may be any appropriate area. In some implementations, a glass substrate (sometimes referred to as a glass plate or panel) having an area on the order of four square meters or greater is provided with a thickness, for example, of 0.3, 0.5, or 0.7 millimeters. Alternatively, round substrates with diameters of 100 millimeters, 150 millimeters, or other diameters may be
20 provided. In some other implementations, square or rectangular sub-panels cut from a larger panel of glass may be provided. The glass substrate may be or include, for example, a borosilicate glass, a soda lime glass, quartz, Pyrex, or other suitable glass material. The glass substrate may be provided with or without MEMS devices and/or other components (metal traces, contact pads, circuitry, etc.) already fabricated on one
25 or both sides of the substrate. In some implementations, the MEMS devices and/or other package components are formed after formation of the through-glass vias, or at any appropriate point during formation of the through-glass vias.

[0096] In an operation 113, a double-sided process is performed to form through-glass via holes in the glass substrate. A double-sided process of forming a through-glass via hole involves forming two partially through holes, one on each side of the
30 glass substrate. At some point during or after formation of these two holes, they are joined by etching or otherwise removing glass material between them. The two partially through holes are aligned such that when joined, the aligned through holes overlap near a mid-section of the glass substrate, forming the through-glass via hole.

According to various implementations, double-sided processes involve simultaneous wet or dry etching of aligned partially through holes, sequential wet or dry etching of aligned partially through holes, and simultaneous or sequential sandblasting (also known as powder blasting) of aligned partially through holes. In some

5 implementations, a double-sided process involves a double-sided sandblasting process followed by a wet etching process to further shape and contour the via holes. Further details and examples of double-sided processes are described below with respect to Figure 12. In some implementations, the via holes are shaped to facilitate subsequent deposition of a continuous thin film through the via holes from one or both sides of
10 the glass substrate. This is discussed further below with respect to Figures 15–17.

[0097] Turning to Figure 11B, at 120, a cross-section of a through-glass via hole 122 formed by a double sided process in a glass substrate 91 is depicted. Through-glass via hole 122 includes aligned hemispherically shaped via holes 125a and 125b, formed in the top and bottom surfaces of glass substrate 91, respectively.

15 Hemispherically shaped via holes have nominally circular sidewall profiles and may be formed by etching the glass substrate with an isotropic wet chemical etchant such as a hydrofluoric acid based etchant.

[0098] Returning to Figure 11A, after forming the through-glass via holes, process 110 continues by coating the sidewalls of the via holes with a continuously
20 conductive thin film in operation 115. In some implementations, one or more thin films are deposited by a sputter deposition process (also known as a physical vapor deposition (PVD) process). In some other implementations, the sidewalls are coated by a chemical vapor deposition (CVD) process, an atomic layer deposition (ALD) process, or an evaporation process. In some implementations, operation 115 is a one-
25 sided deposition process. For example, in some implementations, operation 115 is a one-sided sputtering process in which a target positioned above one surface, or the other, of a substrate including a through-glass via hole is sputtered to deposit the target material on the surface of the substrate and on the sidewalls of both the upper and lower via holes. Conductive thin film material enters the through-glass via hole
30 only through the via opening in that surface. In some other implementations, operation 115 is a two-sided process in which material is deposited in a through-glass via hole through each via opening, either simultaneously or sequentially.

[0099] Figure 11B shows thin film 101 coating the sidewalls of through-glass via hole 122 at 130. Thin film 101 coats the sidewalls of through-glass via hole 122

continuously from the top surface to the bottom surface of glass substrate 91.

According to various implementations, all or only a portion of the through-glass via hole is coated through one or both via openings with a conductive thin film that is electrically continuous through the via hole. In the depicted example, the thin film

5 101 is also deposited on the top and bottom surfaces of glass substrate 91. Although not shown, thin film 101 may be selectively patterned and etched on one or both sides of glass substrate 91 to form, for example, electrical traces, bond pads, and other connective features.

[0100] Thicknesses of the thin films formed in operation 115 may range from less
10 than 0.05 to over 5 microns according to various implementations. In some cases, the thickness of a thin film layer on the sidewalls of a through-glass via hole depends on whether plating is to be performed. In implementations in which a thin film provides the electrical connection through the via (i.e., the via hole is unfilled or filled with a non-conductive material), the film may be deposited to a thickness between about 0.1
15 and 5 microns, e.g., 1 micron or 2 microns. In implementations in which a thin film is a seed layer for a plating process, it may be deposited to a thickness of about 0.1 to 0.2 microns. One having ordinary skill in the art will understand that these thicknesses may be varied depending on the desired implementation.

[0101] The thin film is generally a metal, although conductive polymers or other
20 materials may be used in some implementations. Examples of metals include copper (Cu), aluminum (Al), gold (Au), niobium (Nb), chromium (Cr), tantalum (Ta), nickel (Ni), tungsten (W), titanium (Ti) and silver (Ag). In some implementations, depositing the thin film involves depositing a bilayer including an adhesion layer and second layer such as aluminum, gold, copper or another metal. The second layer acts
25 as the main conductor and/or seed layer. Adhesion layers promote adhesion to the glass substrate. Examples of adhesion layers include chromium and titanium. Examples of bilayers include Cr/Cu, Cr/Au and Ti/W. Adhesion layers may have thicknesses of a few nanometers to several hundred nanometers or more.

[0102] According to various implementations, in addition to coating the inside
30 surface of a via hole, a thin film may be deposited on one or both of the top and bottom surfaces of the glass substrate, in at least a portion of the area surrounding the via opening in that surface. The films formed on the top and/or bottom surface may be patterned and etched to form electrical traces and/or contact pads that are electrically connected to the via hole. The patterning and etching may be performed

after operation 115 or 117, as described with respect to Figure 11A. In some implementations, a deposition mask is formed on a top and/or bottom surface prior to deposition of the thin film so that the films are deposited in the desired pattern. The thin metal films also may be deposited to connect to existing metal traces and other features on the top and/or bottom surfaces.

[0103] In some implementations, the thin films formed in operation 115, and, if present, the plated layers formed in operation 117, provide conductive paths through the via, with the interior of the via hole left unfilled or subsequently filled or partially filled with a non-conductive material. In some other implementations, the vias are filled or partially filled by a metal or other conductive material. Accordingly, after deposition of one or more thin films in operation 115 and, if performed, plating in operation 117 in some implementations, the via holes are completely or partially filled with a conductive or non-conductive material in an optional operation 119.

[0104] According to various implementations, the filler material may be a metal, a metal paste, a solder, a solder paste, one or more solder balls, a glass-metal material, a polymer-metal material, a conductive polymer, a non-conductive polymer, an electrically conductive material, a non-conductive material, a thermally conductive material, a heat sink material, or a combination thereof. In some implementations, the filler material reduces the stress on the deposited thin film and/or plated layer. In some other implementations, the filler material seals the via holes to prevent transfer of liquids or gases through the via holes. The filler material may serve as a thermally conductive path to transfer heat from devices mounted on one side of the glass substrate to the other. According to various implementations, the via holes may be filled or partially filled using a process such as plating, a squeegee-based process, dispensing or direct writing a filler material, screen printing, spray coating, or other appropriate via fill process. In implementations in which the thin films are deposited on the top and/or bottom surfaces of the glass substrate, the thin films may be patterned and etched prior to or after the via holes are filled. Figure 11B shows filler material 126 in through-glass via hole 122 to form a filled through-glass via 93 at 150. In the depicted example, filler material 126 is structurally affixed to glass substrate 91 in part by the hemispherically shaped sidewalls of upper and lower via holes 125a and 125b.

[0105] Once the process described above with reference to Figures 11A and 11B is complete and the through-glass vias are formed, the glass substrate may be further

processed by additional deposition, patterning and etching sequences to form electrical connections, devices, or other features. Moreover, the glass substrate may be further processed by attaching other devices or substrates, or by dicing and further packaging as desired.

- 5 [0106] Figure 12 shows an example of a flow diagram illustrating processes for forming through-glass via holes. The flow diagram depicts examples of alternative double-sided methods 160 and 170 of forming through-glass via holes according to various implementations. Both methods begin with forming masks on the top and bottom surfaces of the glass substrate in an operation 171. The glass substrate may be
10 provided with or without MEMS devices and/or other components already fabricated on one or both sides of the substrate. Alternatively, MEMS and other devices may be formed during or after formation of the through-glass vias. Forming a mask generally involves applying a photo-sensitive layer on the glass substrate, exposing a pattern lithographically into the photo-sensitive layer, and then developing the photo-
15 sensitive layer. Alternatively, an etch-resistant layer deposited on the glass substrate can be patterned and etched, and then serve as an etch mask. Stencils or other masking techniques may also be used as masks for wet, dry, or sandblasting operations. The masks are formed to correspond to the placement and size of the via holes. In some implementations, the masks on the top and bottom surfaces are mirror
20 images, with mask openings on either side of the substrate aligned to allow formation of aligned partially through via holes and the subsequent through-glass via hole. To form a through-glass via hole having differently sized via openings on the top and bottom side of the substrate, differently sized aligned mask openings in the masks may be formed.
- 25 [0107] For isotropic removal processes such as isotropic wet chemical etches, the mask openings can be substantially smaller than the eventual desired via opening size. For example, for a circular via opening having a 100 micron diameter, the mask opening may be as small as about 1–20 microns, e.g., 10 microns; for a circular via opening having a 500 micron diameter, the mask opening may be about 10–100
30 microns, etc. For anisotropic removal processes such as sandblasting or dry etching, the mask opening is generally on the size of the eventual desired via opening size. As described above, in many implementations, the eventual via opening size is on the order of the substrate thickness.

[0108] The processes also allow some tolerance in the alignment. In some implementations, because the via openings are fairly large with diameters or lengths on the order of hundreds of microns, corresponding mask openings may be aligned within tens of microns or less. In some other implementations, one or both of the top and bottom masks also may have non-corresponding mask openings to allow formation of recessed features other than the double-sided via holes in addition to the double-sided holes.

[0109] The mask material may be selected depending on the subsequent glass removal operation, i.e., wet-etching or sandblasting. For wet etching, mask materials may include photoresist, deposited layers of polysilicon or silicon nitride, silicon carbide, or thin metal layers of chrome, chrome and gold, or other etch-resistant material. For sandblasting, mask materials include photoresist, a laminated dry-resist film, a compliant polymer, a silicone rubber, a metal mask, or a metal or polymeric screen.

[0110] After the top and bottom surfaces are appropriately masked, the through-glass via holes are formed. In method 160, this involves placing the substrate in a wet etch solution as shown in operation 173. Wet etch solutions include hydrogen fluoride based solutions, e.g., concentrated hydrofluoric acid (HF), diluted HF (HF:H₂O), buffered HF (HF:NH₄F:H₂O), or other suitable etchant with reasonably high etch rate of the glass substrate and high selectivity to the masking material. The etchant also may be applied by spraying, puddling, or other known techniques. The wet etch sequence may be performed consecutively on one side and then the other, or on both sides simultaneously. In method 160, the through-glass via holes are formed in the glass entirely by wet etching, without a previous sandblast or other post-masking glass removal operation. This forms a partially through-via hole with curved sidewalls having a generally constant radius of curvature. The process continues at least until aligned via holes formed in the top and bottom surfaces break through to create a through-glass via hole. In some implementations in which the via opening is circular and the mask opening is small, the resulting through-glass via hole may be characterized as having two intersecting hemispherically shaped via holes. Regardless of the via opening shape, each of the aligned holes of a contoured through-glass via hole has sidewalls with a concave curvature extending from the planar glass substrate surface to a point in the interior of the glass at which the aligned holes meet. For example, a suitably contoured sidewall allows line-of-sight sputter deposition of a

thin metal layer through the via to provide continuous electrical connectivity, even with a single-sided deposition.

[0111] Figure 13 shows an example of a cross-sectional schematic illustration of a through-glass via hole formed by double-sided wet etching. Through-glass via hole 122 includes aligned partially through via holes 125a and 125b that intersect at a point in the interior of a glass substrate 91. The intersection 185 of via holes 125a and 125b is indicated, and is shown with a small yet finite radius of curvature. A mask opening 187 in the top surface of glass substrate 91 is defined by mask 189, with a similar mask opening in the bottom surface. Via hole 125a includes a sidewall 191 concavely curved from the top surface of glass substrate 91 to intersection 185. The radius of this curvature is substantially constant along sidewall 191. Via hole 125b similarly has sidewalls concavely curved from the bottom surface of glass substrate 91 to intersection 185. The dimension (e.g., diameter) at the intersection 185 of the upper and lower via holes 125a and 125b near the midplane of glass substrate 91 is less than a dimension (e.g., diameter) of the via openings at the top and bottom surfaces.

[0112] Returning to Figure 12, according to various implementations, wet etching operation 173 is performed to contour a through-glass via hole so as to facilitate subsequent deposition of a continuously conductive thin film. For example, in some implementations, the wet etching operation is performed such that the intersection of the aligned via holes is smooth and rounded with no sharp edges, having a small yet tailored radius of curvature. In some implementations, the via hole is contoured to permit deposition of a continuous thin film from only a single side. A smooth, continuously curved profile allows uniform, non-shadowed coverage of the exposed sidewalls with a deposited thin film. The wet etching operation is discussed further below with respect to Figures 16 and 17.

[0113] As described above, wet etching operation 173 involves simultaneous double-sided etching. In alternate implementations, the top and bottom sides of the glass substrate may be etched sequentially. Once the through-glass via is etched, the masks are removed from both sides of the glass substrate as shown in operation 179. The substrate is then cleaned in an operation 181 to prepare the substrate for deposition of continuous thin films in the through-glass via holes and other subsequent processing.

[0114] Method 170 describes operations in alternative implementations of forming through-glass via holes. After the top and bottom surfaces of a glass substrate are

masked in operation 171, the substrate is sandblasted to form through-glass via holes in an operation 175. The through-glass via holes may be formed by sandblasting each side of the substrate through, for example, aligned stencil patterns on one or both sides of the substrate. Masking and sandblasting each side may be performed
5 simultaneously or consecutively. Figures 14A–D show examples of cross-sectional schematic illustrations of various stages of sandblasting methods of forming through-glass via holes.

[0115] In some implementations, the sandblasting operation proceeds at least until aligned via holes formed in the top and bottom surfaces break through to create
10 through-glass via holes. In some implementations in which the sandblasting operation is succeeded by a wet etch, the double-sided sandblasting of the aligned via holes may stop before breakthrough, with breakthrough occurring during the wet etch. For example, sandblasting may be performed through small-diameter mask openings that self-limit the depth of sandblasting from each side prior to wet etching, as described
15 below with respect to Figure 14A. Alternatively, sandblasting can be performed for a pre-specified or pre-determined time and stopped prior to breakthrough, with breakthrough occurring during the wet etch as described below with respect to Figure 14B. In another implementation, double-sided sandblasting can be performed past breakthrough to form a through-glass via hole, followed by a wet etch to further
20 contour the through-glass via hole, as described below with respect to Figure 14C. In some implementations, the sandblasting operation forms via holes with tapered, substantially linear sidewalls. In some implementations, forming curved rather than straight tapered sidewalls involves using a higher pressure sandblast to form the top of each via hole with a steeper taper, followed by a lower pressure sandblast to form the
25 bottom of each hole with a less steep taper as the hole nears the mid-plane of the glass substrate. In these implementations, sandblast pressure may be varied in a step-wise or continuous manner. An example of a step-wise sandblasting technique is described below with respect to Figure 14D.

[0116] After double-sided sandblasting, the resulting through-glass via hole is
30 exposed to a wet etchant in operation 177. In some implementations, the wet etchant serves only to re-texture the sidewalls, smoothing them for subsequent depositions. In some other implementations, the wet etch is allowed to continue to contour the through-glass via. One example is depicted in Figure 14A, which shows an example of a cross-section of a glass substrate 91 with a through-glass via hole 122 formed by

sequential double-sided sandblasting with self-limiting partially through via holes. In the depicted implementation, three stages of forming a through-glass via hole 122 are shown. Two aligned via holes 125a and 125b are sequentially formed by sandblasting glass substrate 91 through mask openings 187a and 187b. After sandblasting, the via holes 125a and 125b are tapered with substantially straight sidewalls. Also after sandblasting the aligned via holes 125a and 125b are not connected, though in alternate implementations they may be. A wet etch can then be performed and allowed to proceed for a length of time sufficient to break through and form a through-glass via hole 122 with contoured sidewalls. The contoured sidewalls facilitate improved thin film deposition over constantly tapered sidewalls in some implementations, such as when a direct line-of-sight region is formed near the intersection of via holes 125a and 125b. The wet etchant may be used to remove unwanted damage to the substrate sidewalls from the sandblasting, although it also can be applied in a manner sufficient to avoid shadowing effects with subsequently deposited thin films.

[0117] In another implementation, Figure 14B shows a glass substrate 91 that is masked and sandblasted to form upper via hole 125a, then masked and sandblasted from the opposite side to form lower via hole 125b without breaking through. Upper and lower via holes 125a and 125b can have substantially flat bottom surfaces. After a wet-etch operation, via holes 125a and 125b are connected to form a through-glass via hole 122. In another implementation, a glass substrate 91 is masked and sandblasted on a first side to form upper via hole 125a, then masked and sandblasted on the other side to form a lower via hole 125b of sufficient depth to break through glass substrate 91, as shown in Figure 14C. A wet etch operation further contours the sidewalls of via holes 125a and 125b to form through-glass via hole 122.

[0118] In an example of a step-wise sandblasting method, Figure 14D shows a glass substrate 91 with upper and lower masks such as a stencil or a screen having mask openings 187a and 187b through which sandblasting is performed in a step-wise manner. Upper via hole 125a is first formed, with its sidewall having two sections 191a and 191b having substantially straight sidewalls of different slopes formed by two sandblasting steps having different pressures. In alternate implementations, more than two steps may be performed. After an upper via hole 125a is formed, a lower via hole 125b is similarly formed, resulting in a through-glass via hole 122. A wet-etch operation may optionally follow to further contour the through-glass via hole 122.

[0119] Returning to Figure 12, after wet etch operation 177 is performed, method 170 ends similarly to method 160, e.g., by removing the masks from both sides of the glass substrate in operation 179 and cleaning the substrate in operation 181. In alternate implementations, the wet etch or sandblast operations may be replaced by a dry etch or a combination of dry etching and wet etching. Dry etching involves exposing the masked substrate to a plasma, such as, a fluorine-containing plasma. The plasma may be direct (in situ) or remote. Examples of plasmas that may be used include inductively-coupled or capacitively-coupled RF plasmas and microwave plasmas. Figures 14E and 14F show examples of cross-sectional schematic illustrations of various stages of dry etch methods of forming through-glass via holes. In one example, Figure 14E shows dry-etched glass substrate 91 with partially through via holes 125a and 125b, which have generally rectangular cross-sectional profiles. The partially through via holes 125a and 125b are subsequently wet etched to form through-glass via hole 122. In the example depicted in Figure 14F, a dry-etched glass substrate 91 with an upper via hole 125a on one side can be immersed in a wet etchant to enlarge via hole 125a and simultaneously form lower via hole 125b, which after sufficient etching time merge to form a through-glass via hole 122. In this example, upper via hole 125a and lower via hole 125b intersect at a point other than the midpoint. In some implementations, aligned via holes intersect at a point between 50% and 90% the height of the substrate as measured from either a top or bottom surface of the substrate. Note also that with this process, less time may be used for the wet etch operation, and the exposed area used for the dry-etch operation is reduced or minimal. In another variant (not shown), dry etching can form a small-diameter via hole from one side of a glass substrate and wet etching can form a hemispherically shaped via hole from the other side to connect the two via holes, so that the area consumed by the via hole opening on the dry-etched side is minimized.

[0120] In some implementations, the through-glass via hole is contoured, i.e., shaped and sized, to allow deposition of a thin film on the sidewalls that is continuous through the hole. The through-glass via hole may be contoured to allow single-sided deposition of a thin film that is continuous through the hole. As described above, a through-glass via hole includes two aligned via holes formed in opposite sides of the glass substrate. In some implementations, the through-glass via hole is contoured such that a tangent line extending from any curved surface of one or both partially through via holes extends through the via opening of the opposite hole. Figure 15

shows an example of a cross-sectional schematic illustration of a contoured through-glass via. As depicted in Figure 15, through-glass via hole 122 includes aligned hemispherically shaped via holes 125a and 125b that meet at intersection 185, where aligned via hole 125a is formed in top surface 92a and aligned via hole 125b is formed in bottom surface 92b of glass substrate 91. A tangent line 190 that is tangent to a sidewall of aligned via hole 125b near intersection 185 is depicted. Region 192, which extends from intersection 185 to a point along the sidewall surface of via hole 125b, is in some implementations the most challenging region to access from a topside deposition source. However, because tangent line 190 extends through the via opening of via hole 125a in top surface 92a, region 192 is a direct line-of-sight region for an overhead sputtering target or other deposition source (not shown); accordingly region 192 and all other sidewall surfaces of via holes 125a and 125b are accessible for topside thin-film deposition with clear line-of-sight exposure. As a result, topside thin-film deposition by sputtering, plasma deposition, or other suitable deposition technique results in deposition of a continuous thin film 101 through through-glass via hole 122. Increasing the tangent line 190 angle can improve continuity of subsequently deposited thin films, although excessively large via holes can be more difficult to fill and can make the glass substrate 91 fragile.

[0121] Through-glass via holes contoured as described in Figure 15 also may be coated with a continuous thin film using double-sided thin film deposition techniques, such as chemical vapor deposition or low-pressure chemical vapor deposition. Each half of the through-glass via hole can be accessible to deposition from both sides of the glass substrate, resulting in improved deposition as compared to single-sided deposition.

[0122] In some implementations, a through-glass via hole contoured as described above with reference to Figure 15 is formed via a double-sided isotropic wet etch. The etch is allowed to proceed until the etch radius, R , i.e., the distance that the etch proceeds in any direction, is at least the minimum etch radius, R_{Min} , that is needed to contour the via hole:

$$R \geq R_{\text{Min}} \text{ where}$$

$$R_{\text{Min}} = (\sqrt{2})(t_s/2)/(1+((d_M+R_{\text{Min}})/R_{\text{Min}})(1-(t_s/2R_{\text{Min}})^2)^{1/2})^{1/2} \quad (\text{Equation 1})$$

with d_M being the mask opening dimension and t_s the substrate thickness. For example, d_M represents the mask opening diameter for circular vias, and the smallest mask opening dimension (e.g., the width) for slot-shaped mask openings. Figure 16 shows an example of a cross-sectional schematic illustration of certain etch parameters of a through-glass via hole. Through-glass via hole 122 in glass substrate 91 and mask 189 are depicted. Mask 189 allows an etchant to selectively contact the top surface of glass substrate 91 in the area exposed by mask opening 187. Mask opening 187 may be a circle, a slot, a rectangle or other shape. For a circular mask opening, d_M is the diameter of the mask feature. For a non-circular mask opening, d_M is the smaller dimension, e.g., the width of a slot-shaped mask opening. Equation 1 assumes (i) uniform double-sided isotropic etching with no etch acceleration under the mask, (ii) that a similar mask and mask opening feature are aligned on the opposite side of glass substrate 91, and (iii) that the masks are removed prior to thin-film deposition. Examples of minimum etch radii for various mask opening dimensions and substrate thicknesses are given in Tables 1 and 2 for circular and slot vias, respectively. The resulting through-glass via sizes at the top and bottom surfaces and at an intersection of the aligned via holes for a uniform double-sided isotropic wet etch under the above-stated assumptions governing Equation 1 are also given.

Table 1: Minimum Etch Radii for Wet-Etched Circular Vias

Substrate Thickness (μm)	100		300		500	
Mask Opening (diameter, μm)	10	20	10	50	10	100
Minimum Etch Radius (μm)	56.7	55.8	172.1	168.2	287.6	278.8
Minimum Etch Radius (Normalized to $\frac{1}{2} t_s$)	1.134	1.116	1.147	1.122	1.150	1.115
Diameter – Upper Surface (μm)	123.4	131.6	354.2	386.5	585.2	657.7
Diameter – Mid Surface (μm)	63.5	69.6	178.8	202.4	294.3	347.0
Diameter – Lower Surface (μm)	123.4	131.6	354.2	386.5	585.2	657.7

Table 2: Minimum Etch Radii for Wet-Etched Slot Vias

Substrate Thickness (μm) Mask Opening (w x l, μm)	50 10 x 300	100 10 x 300	300 10 x 300	500 10 x 300
Minimum Etch Radius (μm)	27.9	56.7	172.1	287.6
Minimum Etch Radius (Normalized to $\frac{1}{2} t_s$)	1.115	1.134	1.147	1.150
Via Size – Upper Surface (μm)	66 x 356	123 x 413	354 x 644	585 x 875
Via Size – Mid Surface (μm)	35 x 325	64 x 354	179 x 469	294 x 584
Via Size – Lower Surface (μm)	66 x 356	123 x 413	354 x 644	585 x 875

[0123] While Tables 1 and 2 provide minimum etch radii for examples of differently sized circular and slot-shaped vias, Equation 1 also may be solved by an iterative or other technique to determine the minimum etch radius for a given substrate thickness and mask opening size. In some implementations, the etch radius, R , is some factor above the minimum, e.g., 1.1–1.4 R_{Min} , to further improve thin film deposition, resulting in a via opening with a dimension on the order of 1.1–1.5 times the thickness of the glass substrate. An overetch ratio of 10–15% is generally desirable to enable electrical continuity of subsequently deposited thin metal films while keeping the resulting diameter of the via hole small. Robust etch sequences can handle overetch ratios of 40% or higher.

[0124] Figure 17 shows an example of cross-sectional schematic illustrations of a glass substrate at various stages of simultaneous etching of aligned via holes to form a through-glass via hole. As depicted in Figure 17, simultaneous etching of aligned via holes 125a and 125b in glass substrate 91 using masks 189a and 189b with aligned mask openings 187a and 187b forms a through-glass via hole 122. First, at 210, glass substrate 91 is depicted prior to the etch operation. At 220, aligned via holes 125a and 125b are formed, but they have not yet broken through to create a completed through-glass via hole. At 230, there is breakthrough and aligned via holes 125a and 125b are connected to form a through-glass via hole 122. However, the contour of the through-glass via hole 122 is not sufficient to allow single-sided line-of-sight deposition from an overhead target. This is shown by tangent line 190 that is tangent to a sidewall of via opening 187a near the intersection of via holes 125a and 125b, and which does not extend through the opening of via hole 125a in the top surface of glass substrate 91. At 240, the etch has proceeded long enough such that the minimum etch radius, R_{Min} , is reached as shown by tangent line 190 just clearing the

via opening of via hole 125a (but not yet clearing mask 189a). The etch is permitted to proceed and contour the via holes, and at 250, tangent line 190 extends through the interior of the via opening to form a direct line-of-sight region 192 near the intersection of via holes 125a and 125b. Note that a line (not shown) that is tangent to a sidewall of via hole 125a near the intersection of via holes 125a and 125b may extend through the opening of via 125b.

[0125] Figures 18A–20B present examples of isometric and cross-sectional views of implementations of circular, slot-shaped, and square-shaped through-glass via holes. Figures 18A and 18B provide an isometric view and a cross-sectional view, respectively, of a device 99 with an array of circular through-glass via holes 122 having hemispherically shaped sidewalls that may be fabricated using a double-sided isotropic wet etch process of a glass substrate 91 having, for example, a thickness of 500 microns, a mask opening dimension of 10 microns, and an etch radius of 288 microns (R_{Min} as calculated using Equation 1). With these parameters, upper and lower surface via opening diameters as given in Table 1 are each 586 microns and the mid-surface intersection diameter is 294 microns. Other parameters can be used according to the desired implementation. Via opening size and other dimensions of the through-glass via size can also vary depending on the desired implementation and particular etch process used. For example, in some implementations in which there is accelerated etching under the mask, the opening diameter can be larger. Through-glass via holes 122 may be coated with a thin film (not shown) and optionally plated and/or filled with a suitable filler material.

[0126] Figures 19A and 19B provide an isometric view and a cross-sectional view, respectively, of a device 99 with a slot-shaped through-glass via hole 122 that may be fabricated using an isotropic wet etch process of a glass substrate 122 having, for example, a thickness of 500 microns, a mask opening dimension of 10 x 1000 microns, and an etch radius of 288 microns (R_{Min} as calculated using Equation 1). With these parameters, upper and lower surface via opening dimensions as given in Table 2 are each 586 x 1576 microns, and intersection dimensions are 294 x 1284 microns. Other parameters can be used according to the desired implementation. Via opening size and other dimensions of the through-glass via size can also vary depending on the desired implementation and particular etch process used. Through-glass via holes 122 may be coated with a thin film (not shown) and optionally plated and/or filled with a suitable filler material.

[0127] Figures 20A and 20B provide an isometric view and a cross-sectional view, respectively, of a device 99 with a square-shaped through-glass via hole 122 that may be fabricated using an isotropic wet etch process of a glass substrate 91 having, for example, a thickness of 500 microns, a mask opening dimension of 1500 x 1500 microns with corner radii of 250 microns, and an etch radius of 288 microns (R_{Min} as calculated using Equation 1). Via opening dimensions at the upper and lower surfaces are 2076 x 2076 microns, and via intersection dimensions are 1786 x 1786 microns, for a uniform double-sided isotropic wet etch under the above-stated assumptions governing Equation 1. Other parameters can be used according to the desired implementation. Via opening size and other dimensions of the through-glass via size can also vary depending on the desired implementation and particular etch process used. Through-glass via hole 122 is filled with a filler material 126. For example, filler material 126 can be a thermally conductive material that serves as a heat sink or a heat spreader for devices that may be mounted on glass substrate 91.

[0128] Figures 21A and 21B show examples of system block diagrams illustrating a display device 40 that includes a plurality of interferometric modulators. The display device 40 can be, for example, a cellular or mobile telephone. However, the same components of the display device 40 or slight variations thereof are also illustrative of various types of display devices such as televisions, e-readers and portable media players.

[0129] The display device 40 includes a housing 41, a display 30, an antenna 43, a speaker 45, an input device 48, and a microphone 46. The housing 41 can be formed from any of a variety of manufacturing processes, including injection molding, and vacuum forming. In addition, the housing 41 may be made from any of a variety of materials, including, but not limited to: plastic, metal, glass, rubber, and ceramic, or a combination thereof. The housing 41 can include removable portions (not shown) that may be interchanged with other removable portions of different color, or containing different logos, pictures, or symbols.

[0130] The display 30 may be any of a variety of displays, including a bi-stable or analog display, as described herein. The display 30 also can be configured to include a flat-panel display, such as plasma, EL, OLED, STN LCD, or TFT LCD, or a non-flat-panel display, such as a CRT or other tube device. In addition, the display 30 can include an interferometric modulator display, as described herein.

[0131] The components of the display device 40 are schematically illustrated in Figure 21B. The display device 40 includes a housing 41 and can include additional components at least partially enclosed therein. For example, the display device 40 includes a network interface 27 that includes an antenna 43 which is coupled to a transceiver 47. The transceiver 47 is connected to a processor 21, which is connected to conditioning hardware 52. The conditioning hardware 52 may be configured to condition a signal (e.g., filter a signal). The conditioning hardware 52 is connected to a speaker 45 and a microphone 46. The processor 21 is also connected to an input device 48 and a driver controller 29. The driver controller 29 is coupled to a frame buffer 28, and to an array driver 22, which in turn is coupled to a display array 30. A power supply 50 can provide power to all components as required by the particular display device 40 design.

[0132] The network interface 27 includes the antenna 43 and the transceiver 47 so that the display device 40 can communicate with one or more devices over a network.

The network interface 27 also may have some processing capabilities to relieve, e.g., data processing requirements of the processor 21. The antenna 43 can transmit and receive signals. In some implementations, the antenna 43 transmits and receives RF signals according to the IEEE 16.11 standard, including IEEE 16.11(a), (b), or (g), or the IEEE 802.11 standard, including IEEE 802.11a, b, g or n. In some other implementations, the antenna 43 transmits and receives RF signals according to the BLUETOOTH standard. In the case of a cellular telephone, the antenna 43 is designed to receive code division multiple access (CDMA), frequency division multiple access (FDMA), time division multiple access (TDMA), Global System for Mobile communications (GSM), GSM/General Packet Radio Service (GPRS), Enhanced Data GSM Environment (EDGE), Terrestrial Trunked Radio (TETRA), Wideband-CDMA (W-CDMA), Evolution Data Optimized (EV-DO), 1xEV-DO, EV-DO Rev A, EV-DO Rev B, High Speed Packet Access (HSPA), High Speed Downlink Packet Access (HSDPA), High Speed Uplink Packet Access (HSUPA), Evolved High Speed Packet Access (HSPA+), Long Term Evolution (LTE), AMPS, or other known signals that are used to communicate within a wireless network, such as a system utilizing 3G or 4G technology. The transceiver 47 can pre-process the signals received from the antenna 43 so that they may be received by and further manipulated by the processor 21. The transceiver 47 also can process signals received

from the processor 21 so that they may be transmitted from the display device 40 via the antenna 43.

[0133] In some implementations, the transceiver 47 can be replaced by a receiver. In addition, the network interface 27 can be replaced by an image source, which can store or generate image data to be sent to the processor 21. The processor 21 can control the overall operation of the display device 40. The processor 21 receives data, such as compressed image data from the network interface 27 or an image source, and processes the data into raw image data or into a format that is readily processed into raw image data. The processor 21 can send the processed data to the driver controller 29 or to the frame buffer 28 for storage. Raw data typically refers to the information that identifies the image characteristics at each location within an image. For example, such image characteristics can include color, saturation, and gray-scale level.

[0134] The processor 21 can include a microcontroller, CPU, or logic unit to control operation of the display device 40. The conditioning hardware 52 may include amplifiers and filters for transmitting signals to the speaker 45, and for receiving signals from the microphone 46. The conditioning hardware 52 may be discrete components within the display device 40, or may be incorporated within the processor 21 or other components.

[0135] The driver controller 29 can take the raw image data generated by the processor 21 either directly from the processor 21 or from the frame buffer 28 and can re-format the raw image data appropriately for high speed transmission to the array driver 22. In some implementations, the driver controller 29 can re-format the raw image data into a data flow having a raster-like format, such that it has a time order suitable for scanning across the display array 30. Then the driver controller 29 sends the formatted information to the array driver 22. Although a driver controller 29, such as an LCD controller, is often associated with the system processor 21 as a stand-alone Integrated Circuit (IC), such controllers may be implemented in many ways. For example, controllers may be embedded in the processor 21 as hardware, embedded in the processor 21 as software, or fully integrated in hardware with the array driver 22.

[0136] The array driver 22 can receive the formatted information from the driver controller 29 and can re-format the video data into a parallel set of waveforms that are

applied many times per second to the hundreds, and sometimes thousands (or more), of leads coming from the display's x-y matrix of pixels.

[0137] In some implementations, the driver controller 29, the array driver 22, and the display array 30 are appropriate for any of the types of displays described herein.

5 For example, the driver controller 29 can be a conventional display controller or a bi-stable display controller (e.g., an IMOD controller). Additionally, the array driver 22 can be a conventional driver or a bi-stable display driver (e.g., an IMOD display driver). Moreover, the display array 30 can be a conventional display array or a bi-stable display array (e.g., a display including an array of IMODs). In some
10 implementations, the driver controller 29 can be integrated with the array driver 22. Such an implementation is common in highly integrated systems such as cellular phones, watches and other small-area displays.

[0138] In some implementations, the input device 48 can be configured to allow, e.g., a user to control the operation of the display device 40. The input device 48 can
15 include a keypad, such as a QWERTY keyboard or a telephone keypad, a button, a switch, a rocker, a touch-sensitive screen, or a pressure- or heat-sensitive membrane. The microphone 46 can be configured as an input device for the display device 40. In some implementations, voice commands through the microphone 46 can be used for controlling operations of the display device 40.

20 [0139] The power supply 50 can include a variety of energy storage devices as are well known in the art. For example, the power supply 50 can be a rechargeable battery, such as a nickel-cadmium battery or a lithium-ion battery. The power supply 50 also can be a renewable energy source, a capacitor, or a solar cell, including a plastic solar cell or solar-cell paint. The power supply 50 also can be configured to
25 receive power from a wall outlet.

[0140] In some implementations, control programmability resides in the driver controller 29 which can be located in several places in the electronic display system. In some other implementations, control programmability resides in the array driver 22. The above-described optimization may be implemented in any number of
30 hardware and/or software components and in various configurations.

[0141] The various illustrative logics, logical blocks, modules, circuits and algorithm steps described in connection with the implementations disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. The interchangeability of hardware and software has been described generally,

in terms of functionality, and illustrated in the various illustrative components, blocks, modules, circuits and steps described above. Whether such functionality is implemented in hardware or software depends upon the particular application and design constraints imposed on the overall system.

5 [0142] The hardware and data processing apparatus used to implement the various illustrative logics, logical blocks, modules and circuits described in connection with the aspects disclosed herein may be implemented or performed with a general purpose single- or multi-chip processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other
10 programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor may be a microprocessor, or, any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, e.g., a combination of a DSP
15 and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration. In some implementations, particular steps and methods may be performed by circuitry that is specific to a given function.

[0143] In one or more aspects, the functions described may be implemented in
20 hardware, digital electronic circuitry, computer software, firmware, including the structures disclosed in this specification and their structural equivalents thereof, or in any combination thereof. Implementations of the subject matter described in this specification also can be implemented as one or more computer programs, i.e., one or more modules of computer program instructions, encoded on a computer storage
25 media for execution by, or to control the operation of, data processing apparatus.

[0144] Various modifications to the implementations described in this disclosure may be readily apparent to those having ordinary skill in the art, and the generic principles defined herein may be applied to other implementations without departing from the spirit or scope of this disclosure. Thus, the disclosure is not intended to be
30 limited to the implementations shown herein, but is to be accorded the widest scope consistent with the claims, the principles and the novel features disclosed herein. The word “exemplary” is used exclusively herein to mean “serving as an example, instance, or illustration.” Any implementation described herein as “exemplary” is not necessarily to be construed as preferred or advantageous over other implementations.

Additionally, a person having ordinary skill in the art will readily appreciate, the terms “upper” and “lower” are sometimes used for ease of describing the figures, and indicate relative positions corresponding to the orientation of the figure on a properly oriented page, and may not reflect the proper orientation of the IMOD as implemented.

[0145] Certain features that are described in this specification in the context of separate implementations also can be implemented in combination in a single implementation. Conversely, various features that are described in the context of a single implementation also can be implemented in multiple implementations separately or in any suitable subcombination. Moreover, although features may be described above as acting in certain combinations and even initially claimed as such, one or more features from a claimed combination can in some cases be excised from the combination, and the claimed combination may be directed to a subcombination or variation of a subcombination.

[0146] Similarly, while operations are depicted in the drawings in a particular order, this should not be understood as requiring that such operations be performed in the particular order shown or in sequential order, or that all illustrated operations be performed, to achieve desirable results. Further, the drawings may schematically depict one more example processes in the form of a flow diagram. However, other operations that are not depicted can be incorporated in the example processes that are schematically illustrated. For example, one or more additional operations can be performed before, after, simultaneously, or between any of the illustrated operations. In certain circumstances, multitasking and parallel processing may be advantageous. Moreover, the separation of various system components in the implementations described above should not be understood as requiring such separation in all implementations, and it should be understood that the described program components and systems can generally be integrated together in a single software product or packaged into multiple software products. Additionally, other implementations are within the scope of the following claims. In some cases, the actions recited in the claims can be performed in a different order and still achieve desirable results.

[0147] The through-glass vias and processing methods described herein may be implemented in various packages for MEMS devices. Moreover, the methods and devices described herein are not limited to packaging of MEMS or other devices, but may be used to provide a path through any glass substrate.

CLAIMS

What is claimed is:

- 5 1. An apparatus comprising:
a glass substrate having first and second sides;
a concave first via hole having sidewalls and a via opening in the first side;
a concave second via hole having sidewalls and a via opening in the second
side,
10 wherein the first and second via holes intersect to form a through-glass
via hole and wherein the sidewalls of each of the first and second via hole are curved
from their respective via openings to the intersection of the first and second via holes,
wherein a dimension of the through-glass via hole at the intersection is
less than the corresponding dimension at each via opening, and
15 wherein a dimension at each via opening is greater than a thickness of
the glass substrate; and
a conductive thin film conformally coating the through-glass via hole, the thin
film continuous from the first side to the second side.
- 20 2. The apparatus of claim 1, further comprising a plated metal film coating the
through-glass via hole, the plated metal film continuous from the first side to the
second side.
3. The apparatus of claim 2, wherein the through-glass via hole is substantially
25 filled with one of an electrically conductive material, a non-electrically conductive
material, or a thermally conductive material.
4. The apparatus of claim 2, wherein the through-glass via hole is partially filled
with at least one of an electrically conductive material, a non-electrically conductive
30 material, or a thermally conductive material.
5. The apparatus of claim 1 or 2, wherein the through-glass via hole is unfilled.

6. The apparatus of any of claims 1 through 5, wherein the via openings in the first and second sides are circular and have a diameter that is no more than 1.5 times greater than the thickness of the glass substrate.
- 5 7. The apparatus of any of claims 1 through 6, wherein a tangent to a sidewall of the first via hole at the intersection with the second via hole extends through the via opening of the second via hole.
8. The apparatus of any of claims 1 through 7, wherein the via openings are
10 circular.
9. The apparatus of any of claims 1 through 8, wherein the via openings are slot-shaped.
- 15 10. The apparatus of any of claims 1 through 9, wherein the thickness of the conductive thin film is between about 0.1 and 5 microns.
11. The apparatus of any of claims 1 through 10, wherein the glass substrate has a thickness of at least about 100 microns.
20
12. The apparatus of any of claims 1 through 11, further comprising at least one of a MEMS or IC device mounted on the first side of the glass substrate and electrically connected to the conductive thin film in the through-glass via hole.
- 25 13. The apparatus of claim 12, further comprising an electrical component on the second side of the glass substrate, wherein at least one of the MEMS or IC device is electrically connected to the electrical component through the conductive thin film in the through-glass via hole.
- 30 14. The apparatus of any of claims 1 through 13, further comprising:
a display;
a processor that is configured to communicate with the display, the processor being configured to process image data; and
a memory device that is configured to communicate with the processor.

15. The apparatus of claim 14 further comprising:
a driver circuit configured to send at least one signal to the display; and
a controller configured to send at least a portion of the image data to the driver circuit.

5

16. The apparatus of claim 14, further comprising:
an image source module configured to send the image data to the processor.

17. The apparatus of claim 16, wherein the image source module includes at least
10 one of a receiver, transceiver, and transmitter.

18. The apparatus of claim 14, further comprising:
an input device configured to receive input data and to communicate the input
data to the processor.

15

19. An apparatus comprising:
a glass substrate having first and second sides;
a MEMS or IC device mounted to the first side of the glass substrate; and
means for electrically connecting the MEMS or IC device to the second side
20 of the glass substrate.

20. The apparatus of claim 19, further comprising an electrical component on the
second side of the glass substrate, and wherein the means for electrically connecting
the MEMS or IC device to the second side of the glass substrate include means for
25 electrically connecting the MEMS or IC device to the electrical component.

21. A method, comprising:
providing a glass substrate having first and second substantially planar parallel
surfaces;

30 forming a first via hole having curved sidewalls in the first surface and a
second via hole having curved sidewalls in the second surface, wherein the first and
second via holes intersect to form a through-glass via hole having via openings at the
first and second surfaces and an intersection dimension that is less than the
corresponding dimension at each via opening; and

coating at least a portion of the through-glass via hole with a conductive thin film that is continuous through the via hole from the first surface to the second surface.

5 22. The method of claim 21, wherein forming the first and second via holes includes exposing the first and second planar parallel surfaces to a wet etchant to form the first via hole in the first surface and the second via hole in the second surface.

10 23. The method of claim 21 or 22, further comprising forming a mask on each of the first and second surfaces, the masks having at least one opening with a smallest mask opening dimension d_M .

15 24. The method of claim 23, wherein forming at least one of the first and second via holes includes exposing the glass substrate to the wet etchant at least until a direct line-of-sight region extending from the intersection of the first and second via holes is formed, and wherein an etch radius R of the first and second via holes satisfies $R \geq R_{Min}$ where R is the etch radius; and

$$R_{Min} = (\sqrt{2})(t_S/2)/(1+((d_M+R_{Min})/R_{Min})(1-(t_S/2R_{Min})^2)^{1/2})^{1/2}$$

20 and where t_S is a thickness of the glass substrate.

25 25. The method of claim 21, wherein forming the first and second via holes includes aligning stencil patterns on the first surface and second surface of the glass substrate and sandblasting the glass substrate in accordance with the aligned stencil patterns.

26. The method of claim 25, further comprising, after sandblasting the glass substrate, wet etching the first and second via holes to form a direct line-of-sight region extending from the intersection between the first and second via holes.

30 27. The method of claims 25 or 26, wherein sandblasting the glass substrate includes a variable pressure sandblasting operation.

28. The method of claim 27, wherein the variable pressure sandblasting operation includes a higher pressure sandblasting operation followed by a lower pressure sandblasting operation.

5 29. The method of any of claims 21 through 24, wherein each via hole has a constant radius of curvature.

30. The method of any of claims 21 through 29, further comprising plating a metal layer on the conductive thin film.

10

31. The method of any of claims 21 through 30, further comprising filling the through-glass via hole with a filler material.

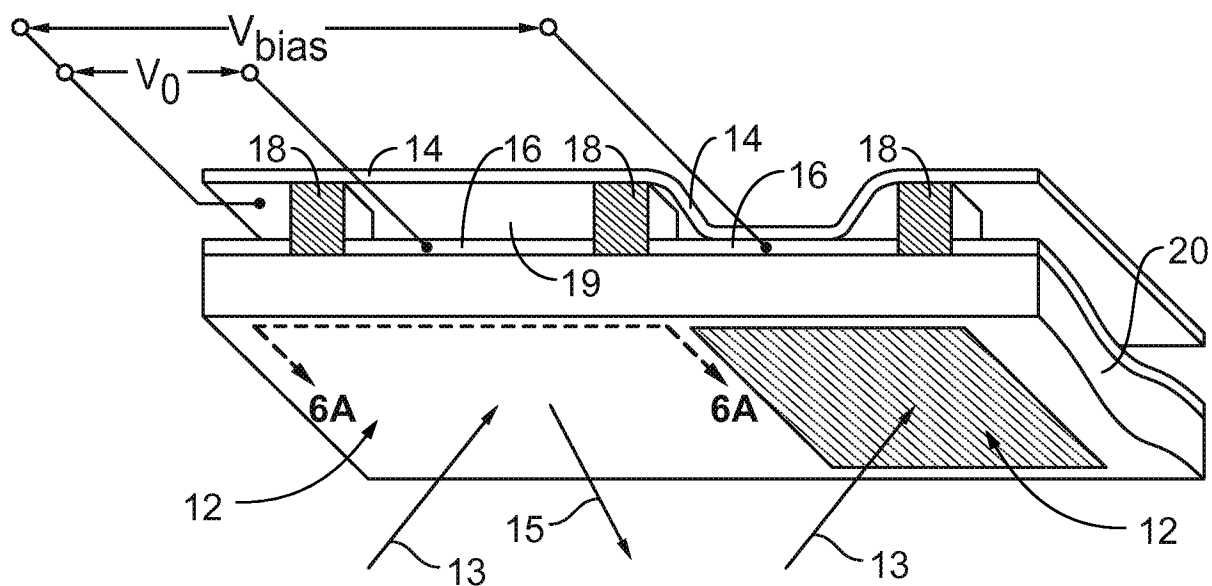
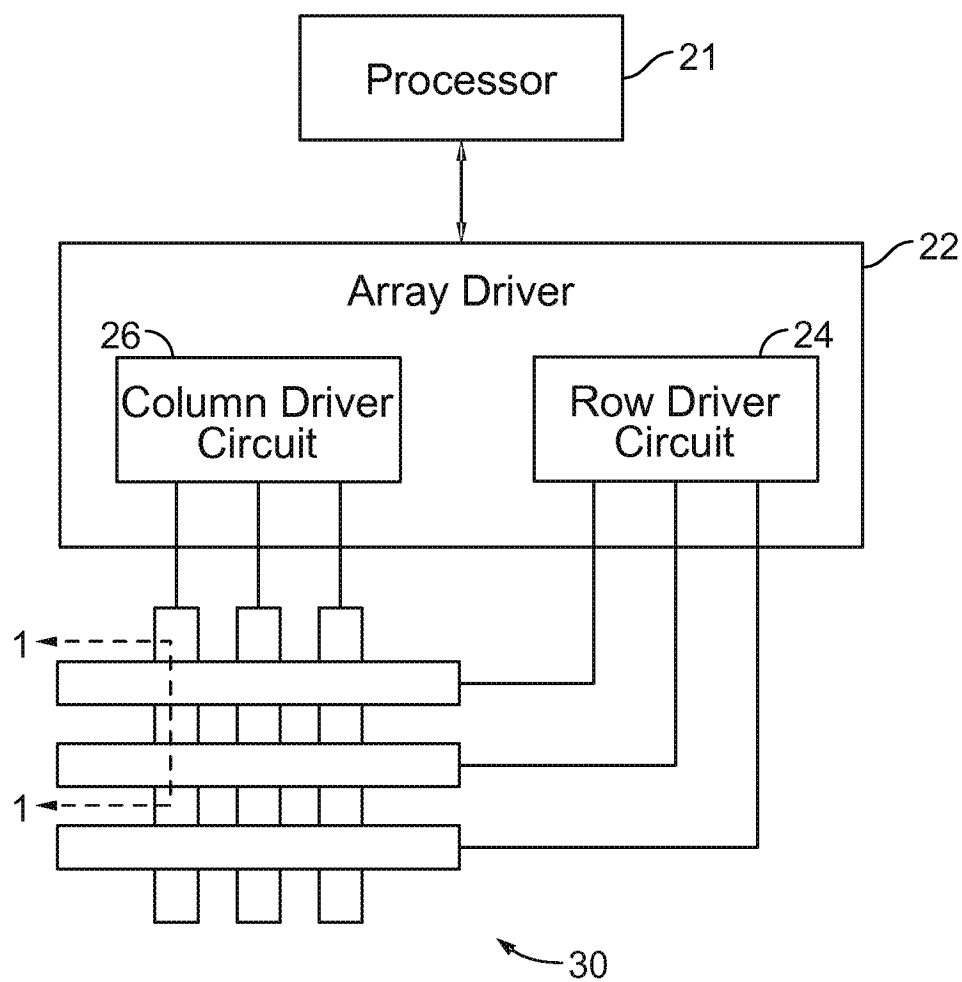
15 32. The method of any of claims 21 through 31, wherein the via openings of the through-glass via hole are circular.

33. The method of any of claims 21 through 31, wherein the via openings of the through-glass via hole are at least one of slot-shaped, rectangular-shaped, or square-shaped.

20

34. The method of any of claims 21 through 33, wherein coating at least a portion of the through-glass via hole includes depositing the conductive thin film through only one of the via openings of the through-glass via hole.

25 35. The method of any of claims 21 through 34, wherein the thickness of the conductive thin film is between about 0.1 and 5 microns.

**Figure 1****Figure 2**

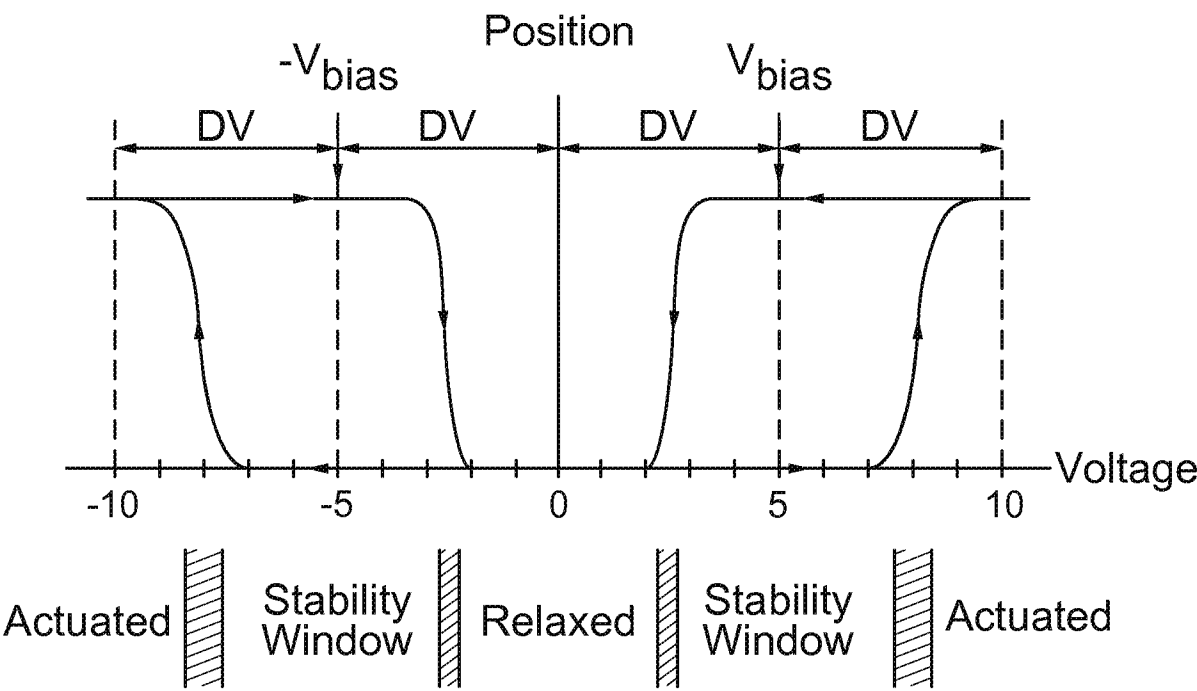
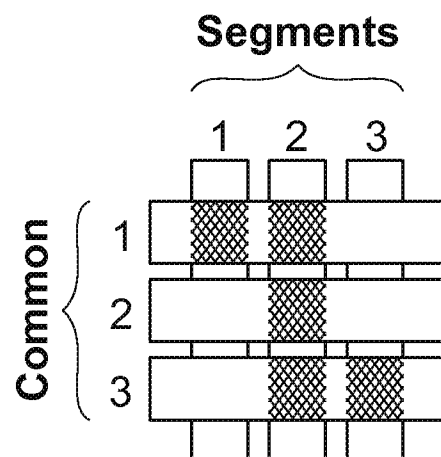
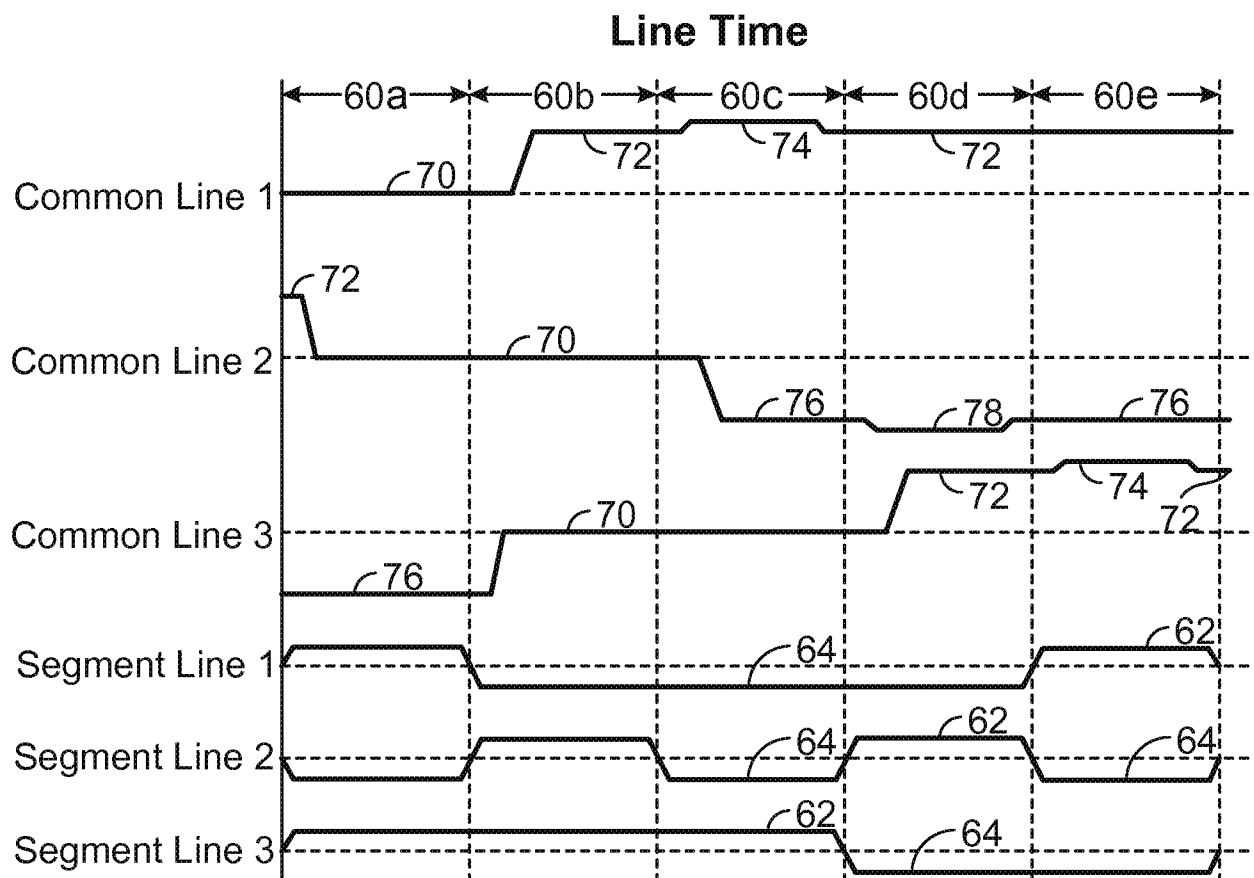


Figure 3

Common Voltages						
Segment Voltages		$V_{C_ADD_H}$	$V_{C_HOLD_H}$	V_{C_REL}	$V_{C_HOLD_L}$	$V_{C_ADD_L}$
	V_{S_H}	Stable	Stable	Relax	Stable	Actuate
	V_{S_L}	Actuate	Stable	Relax	Stable	Stable

Figure 4

**Figure 5A****Figure 5B**

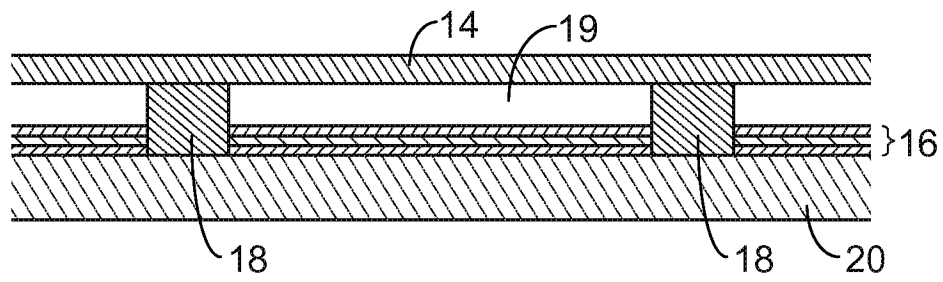


Figure 6A

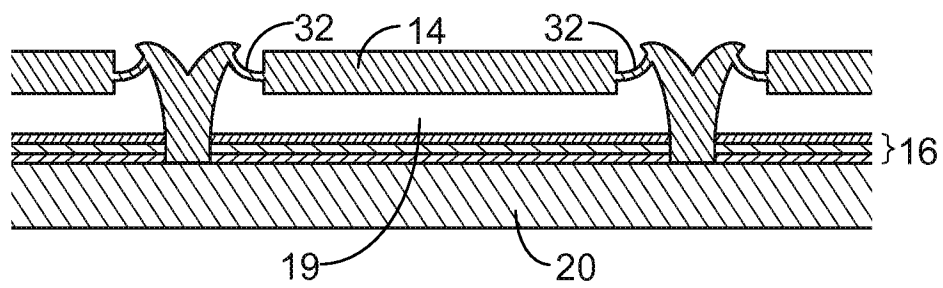


Figure 6B

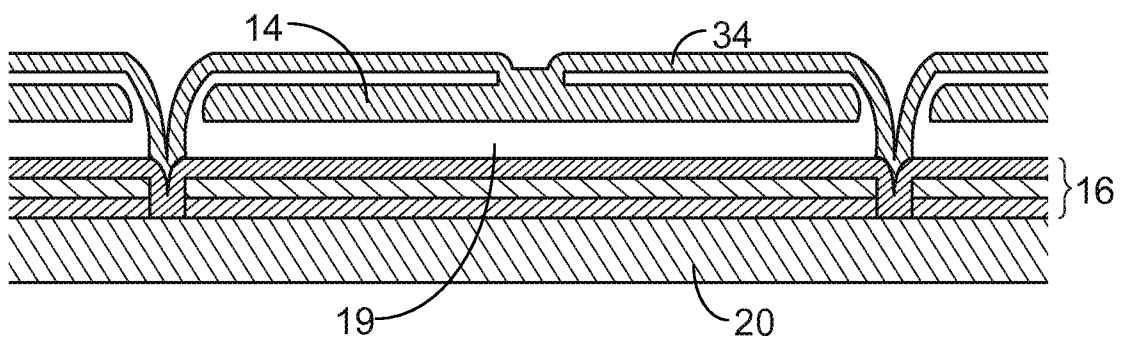


Figure 6C

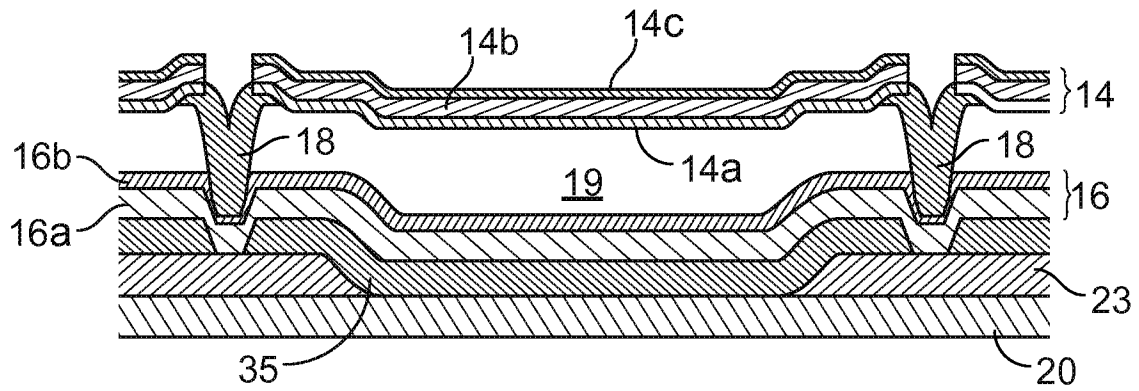


Figure 6D

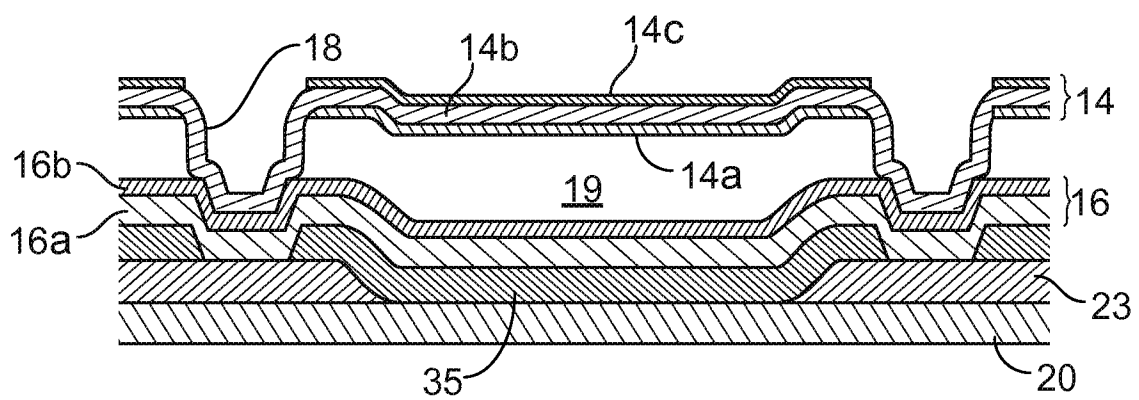
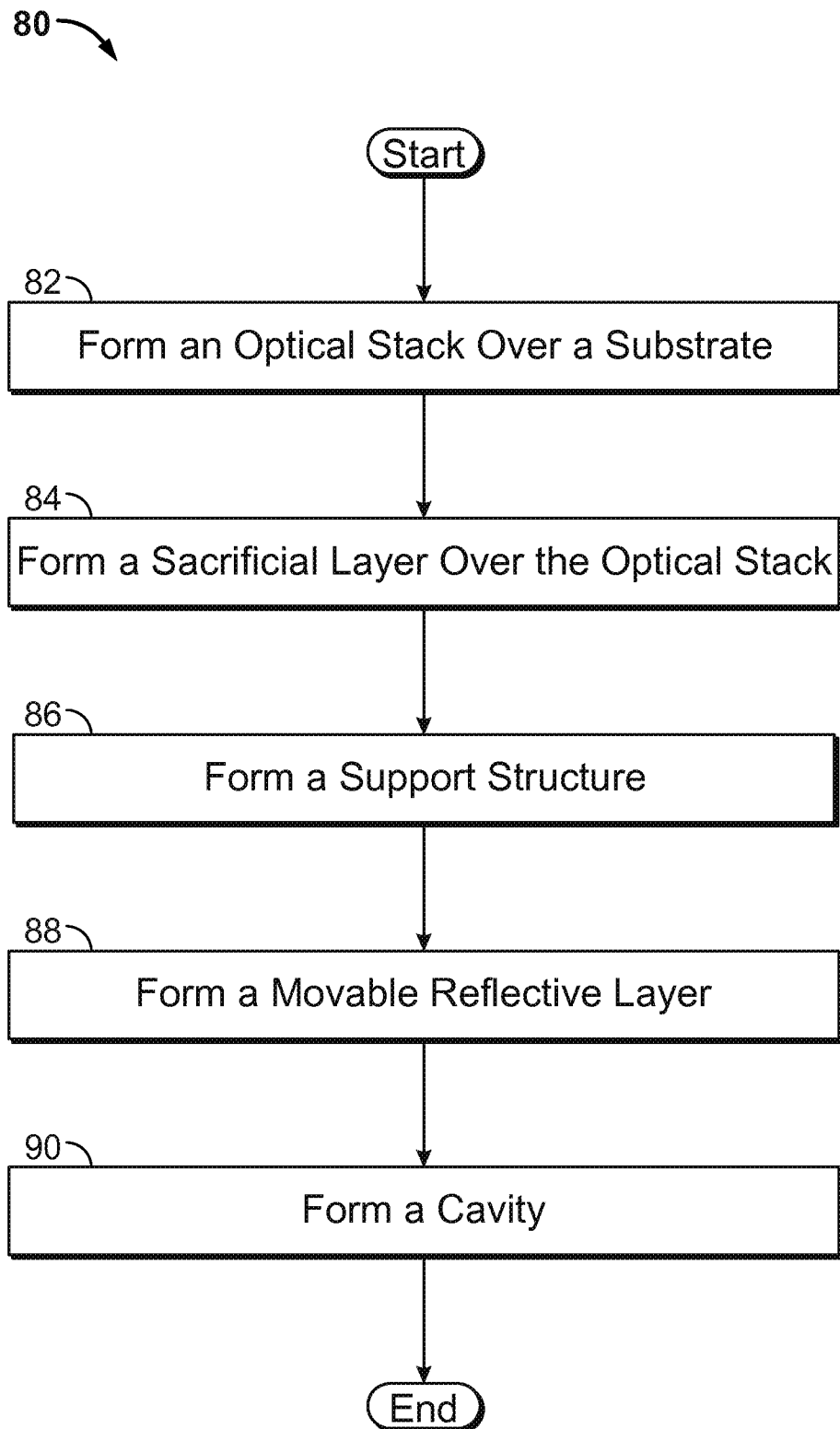


Figure 6E

**Figure 7**

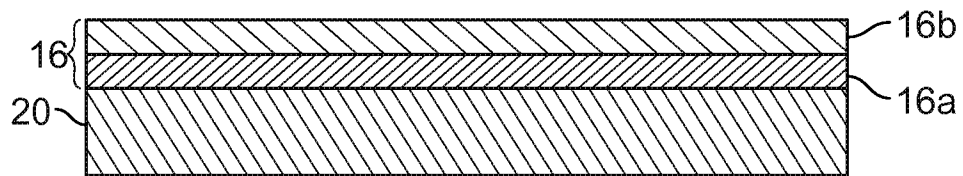


Figure 8A

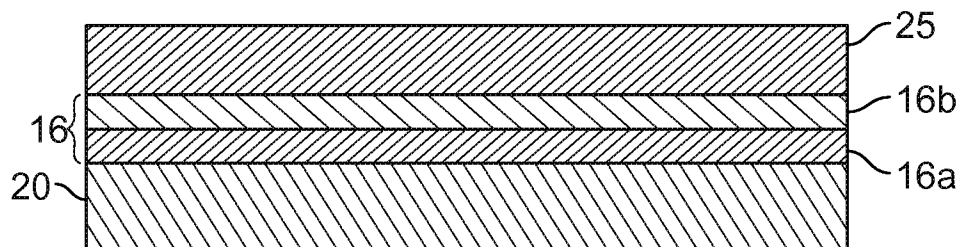


Figure 8B

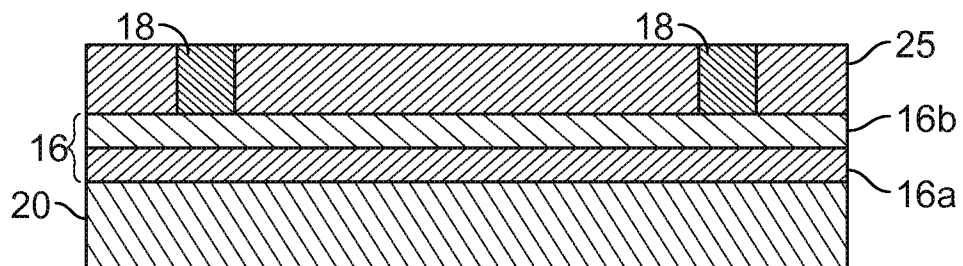


Figure 8C

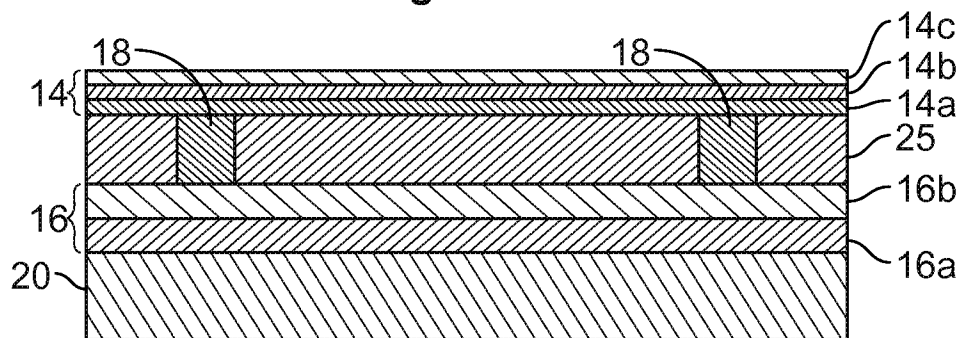


Figure 8D

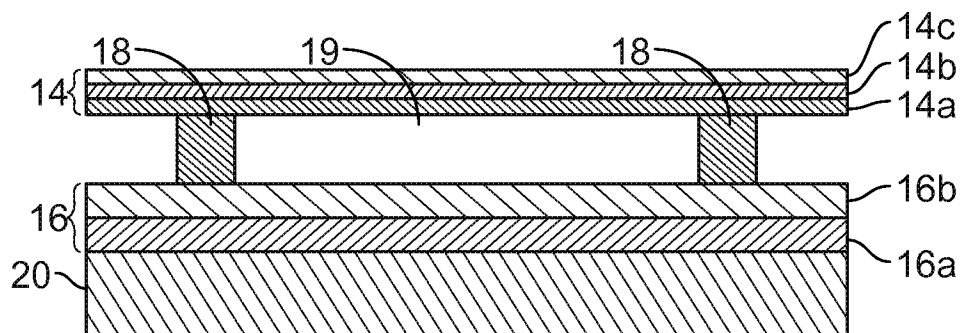
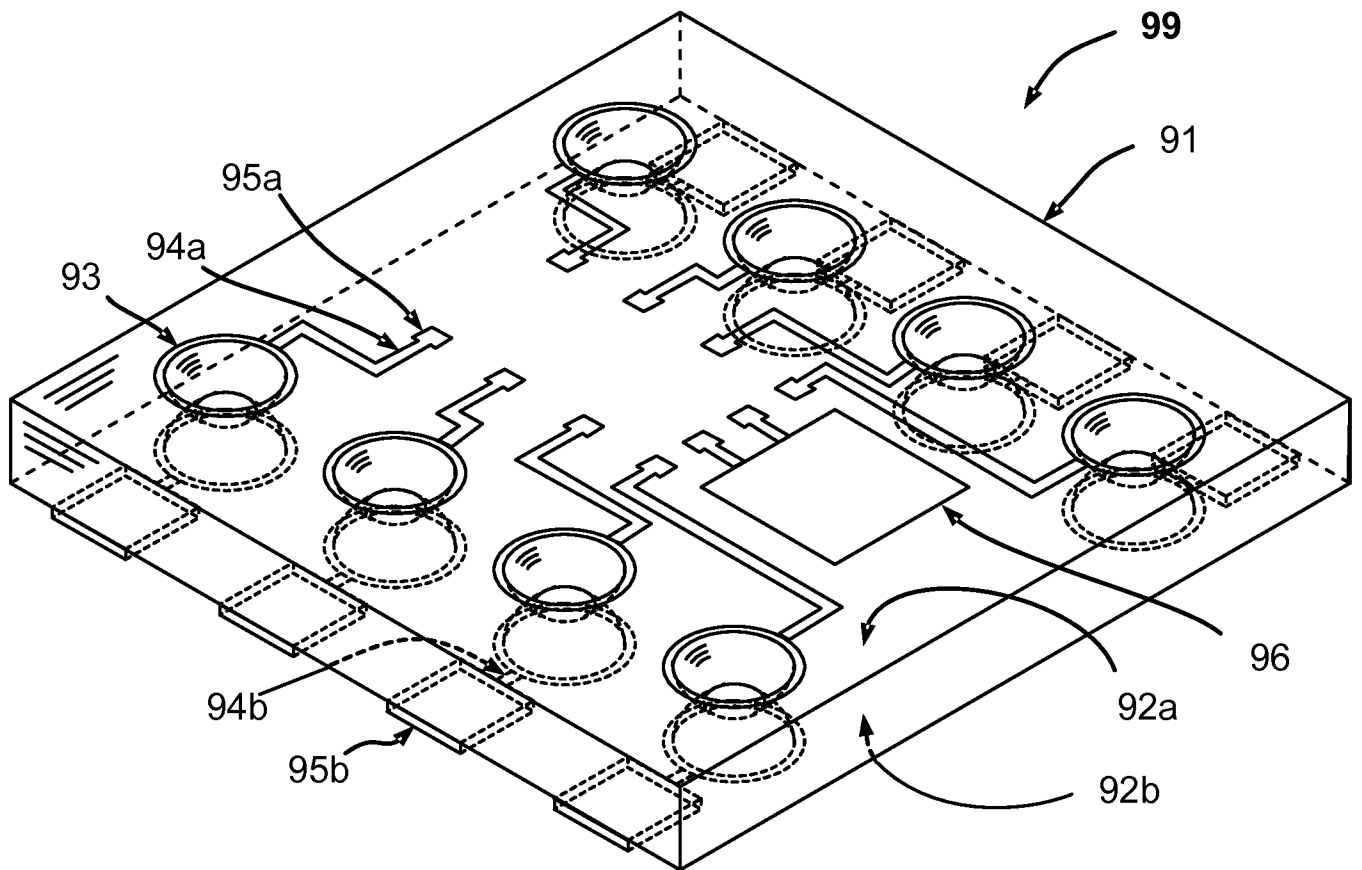
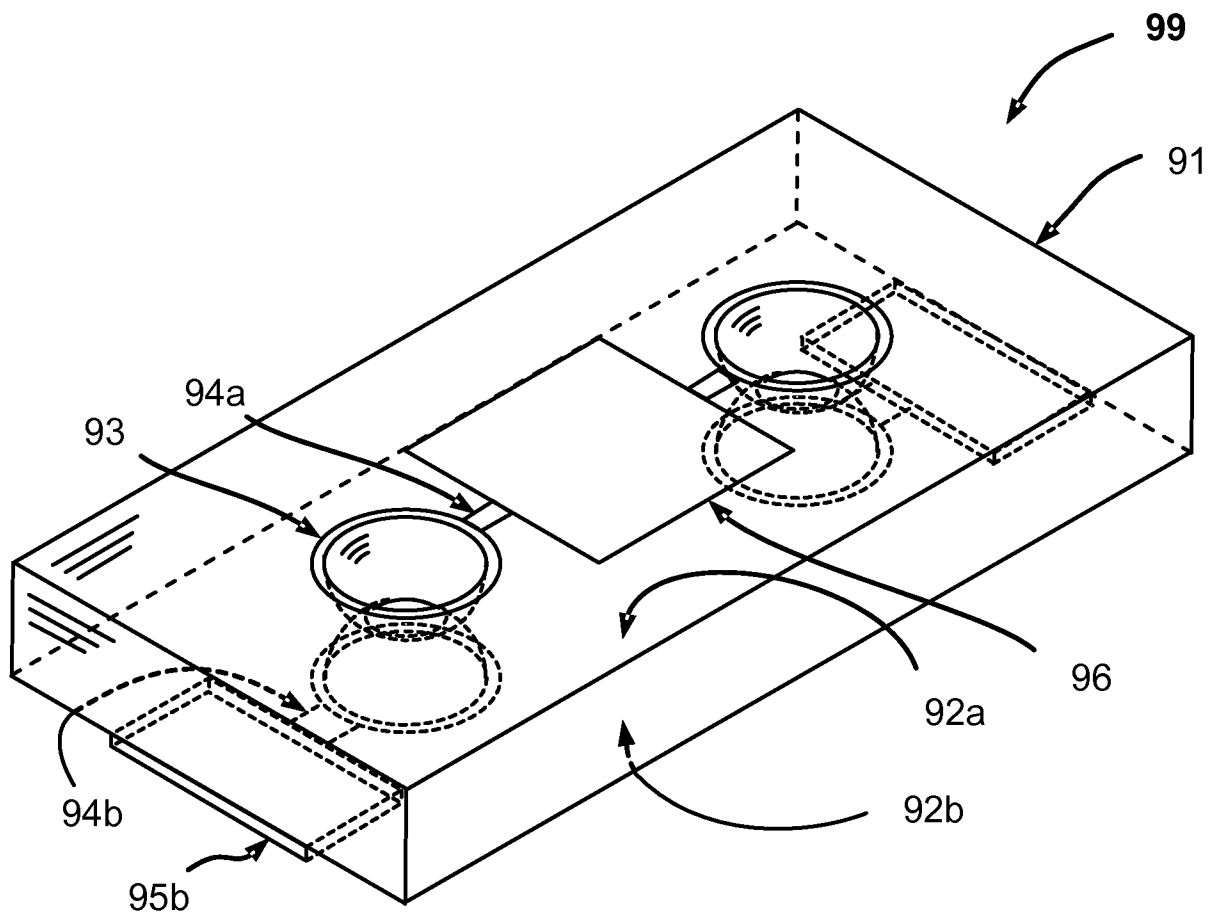


Figure 8E

**Figure 9A**

**Figure 9B**

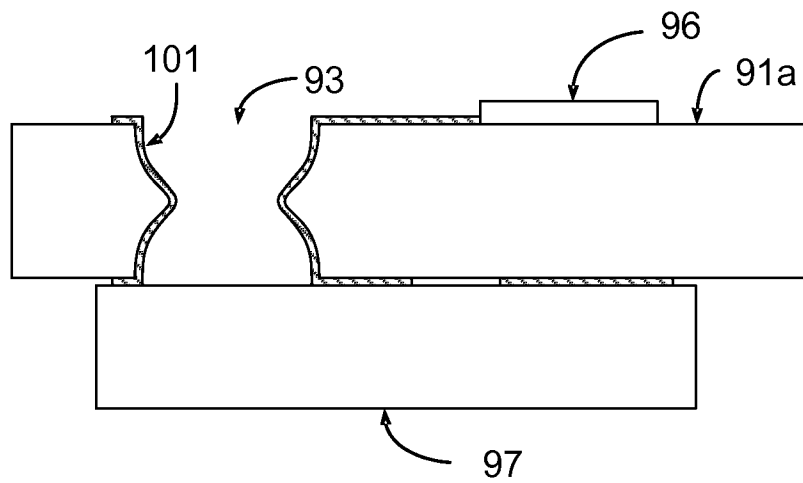


Figure 10A

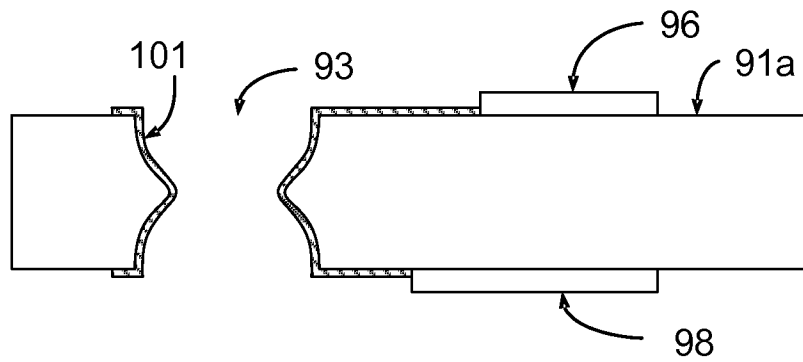


Figure 10B

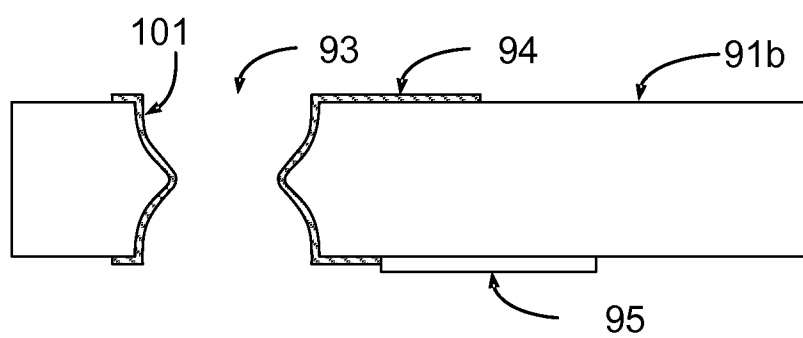
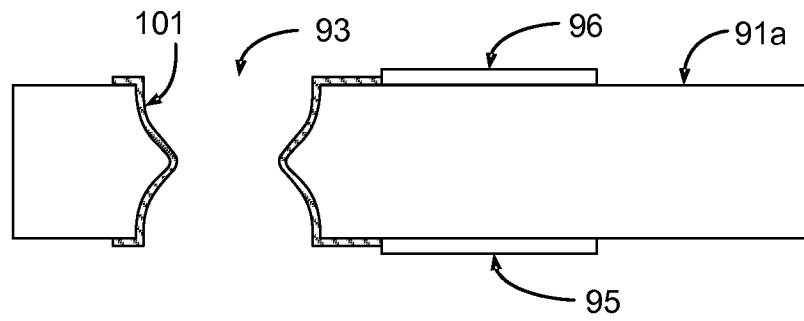
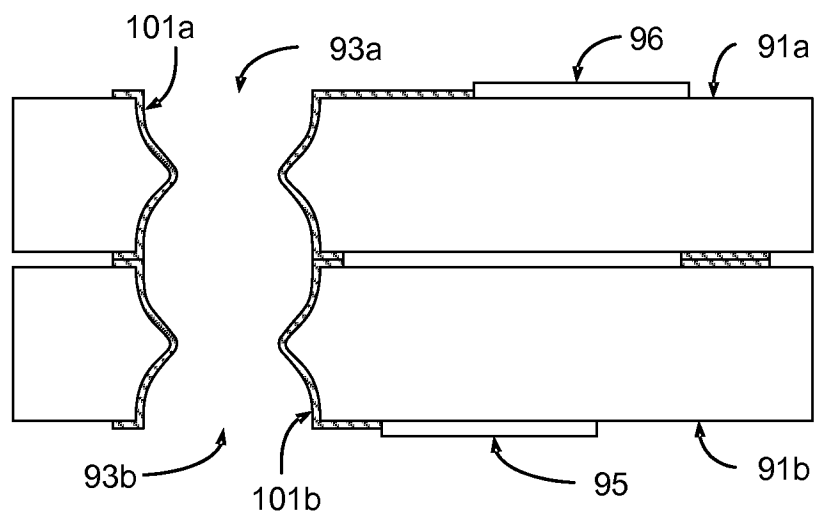
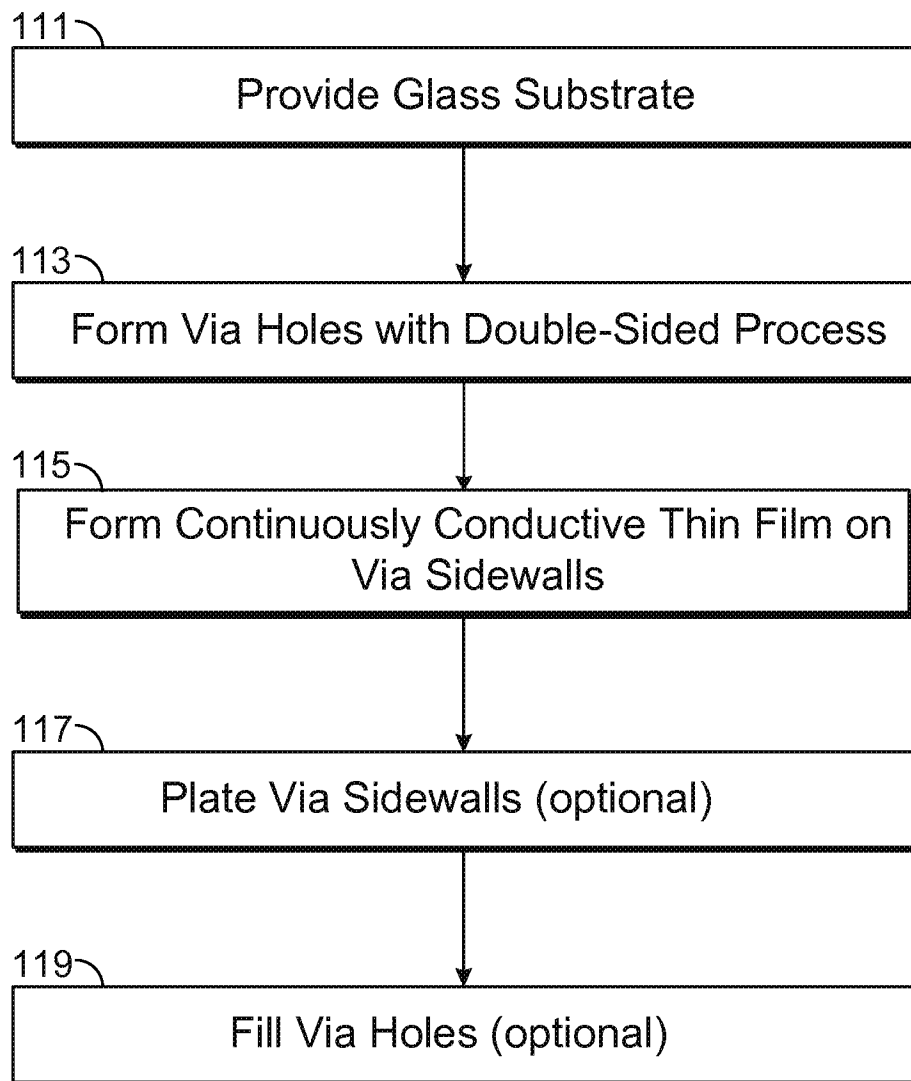


Figure 10C

**Figure 10D****Figure 10E**

110 **Figure 11A**

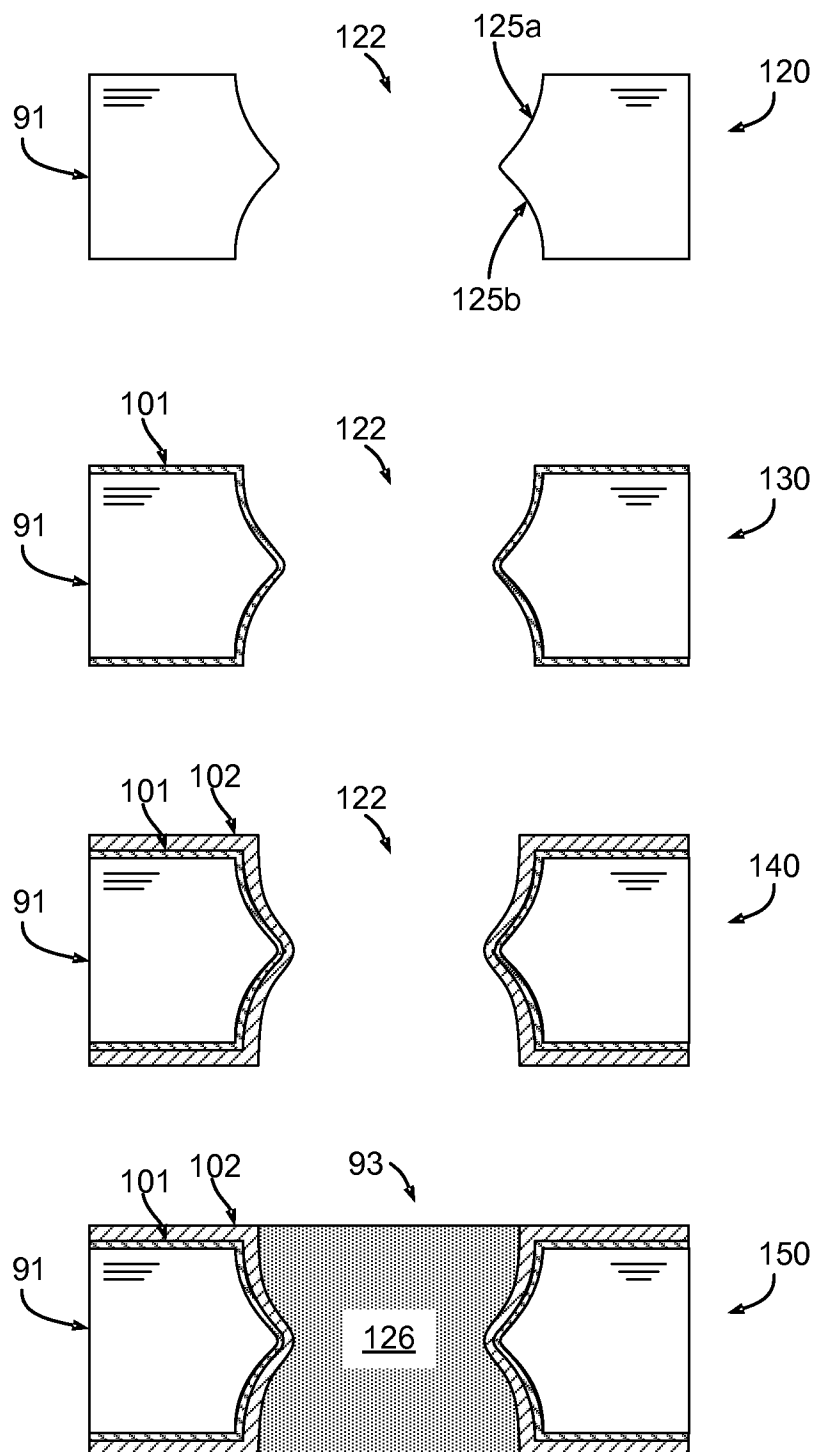


Figure 11B

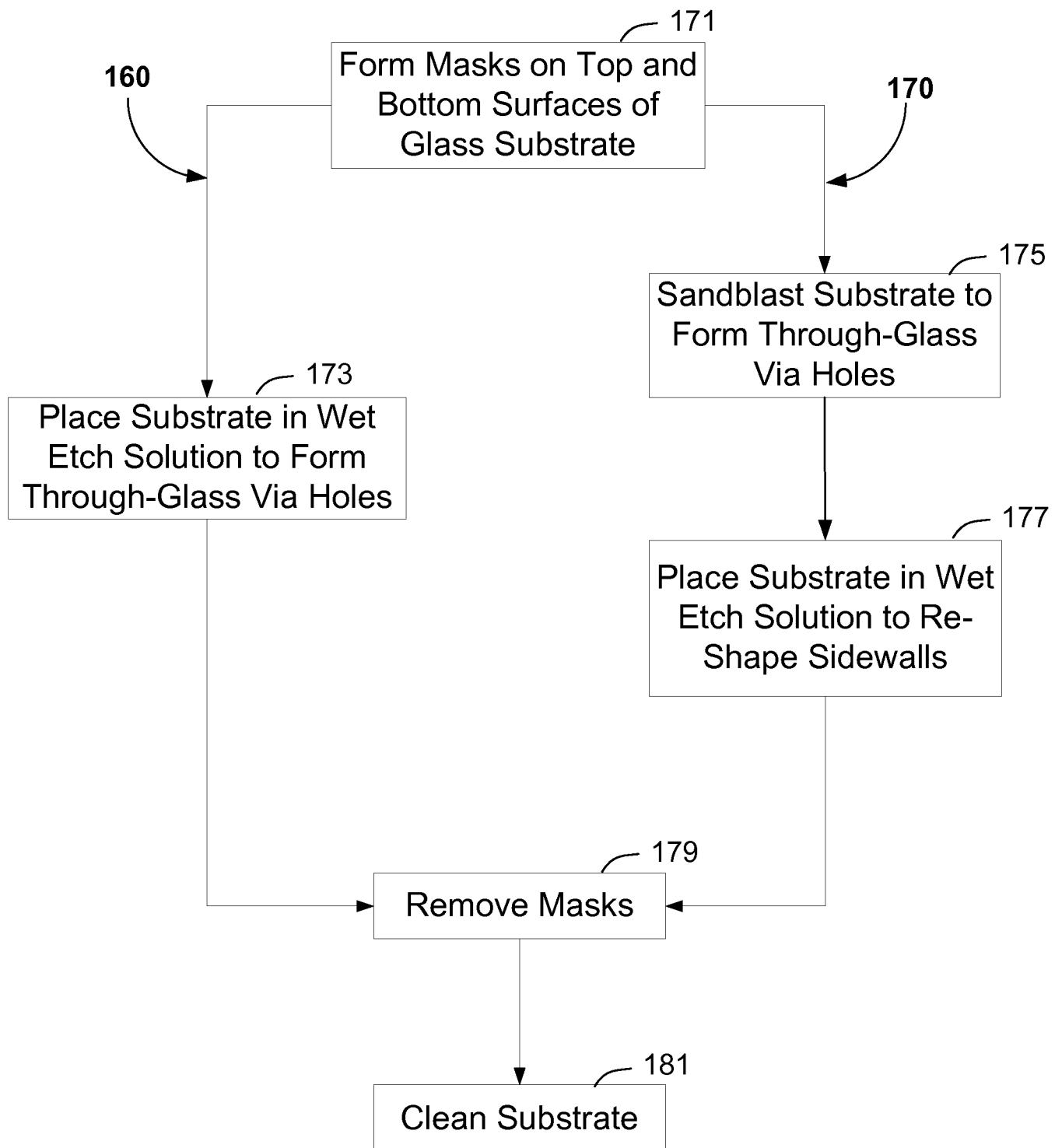


Figure 12

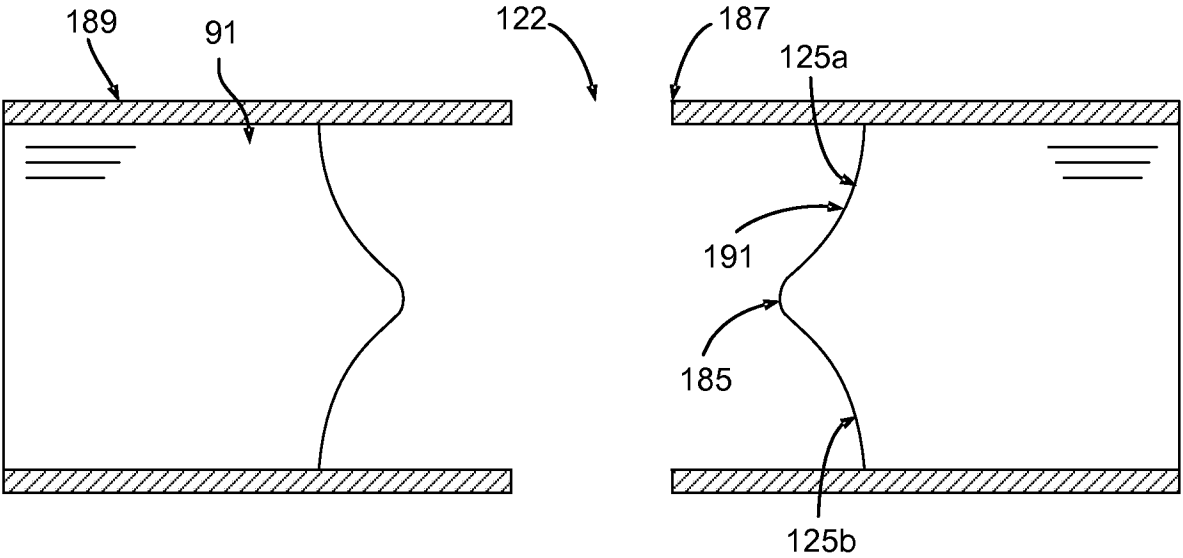


Figure 13

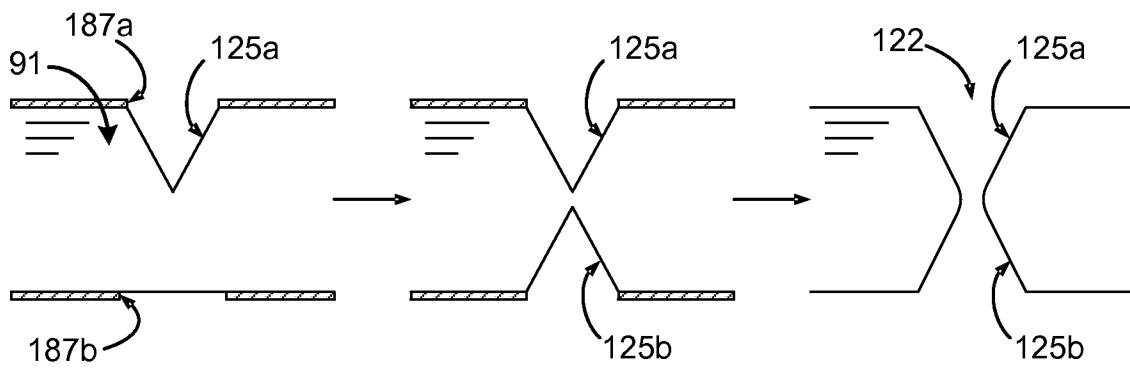


Figure 14A

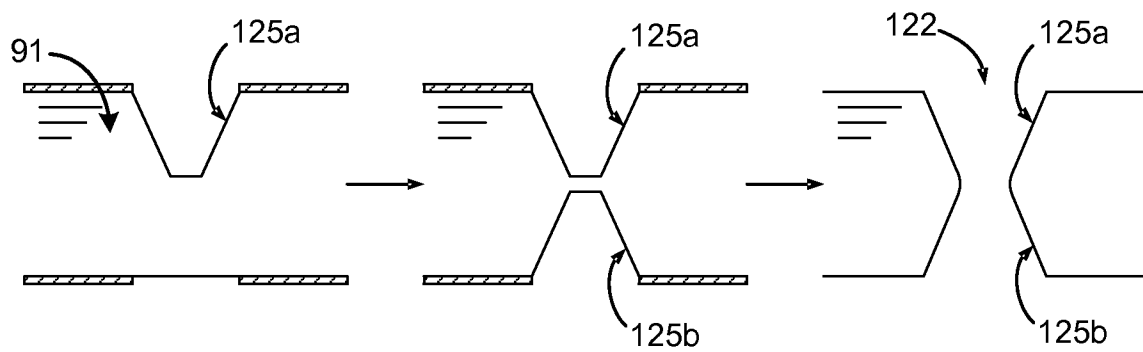


Figure 14B

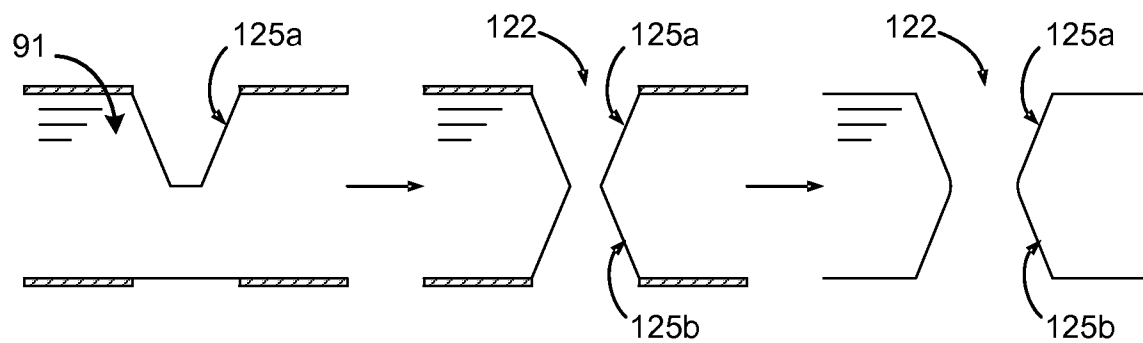


Figure 14C

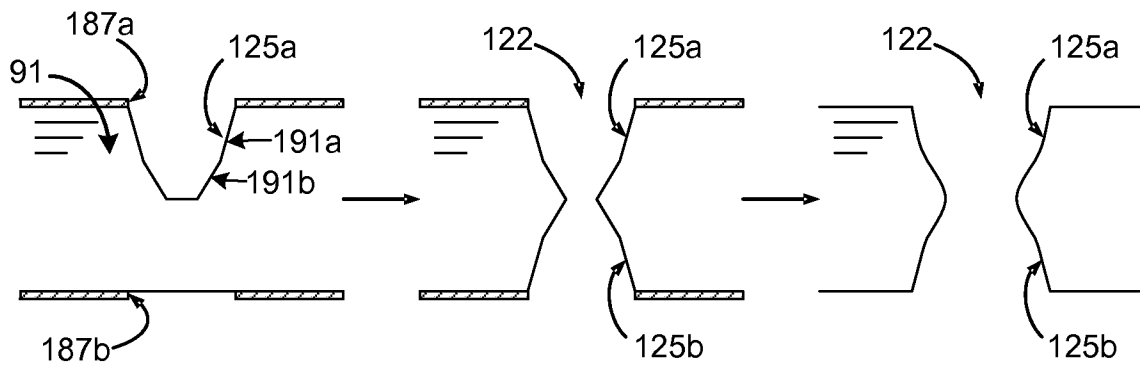


Figure 14D

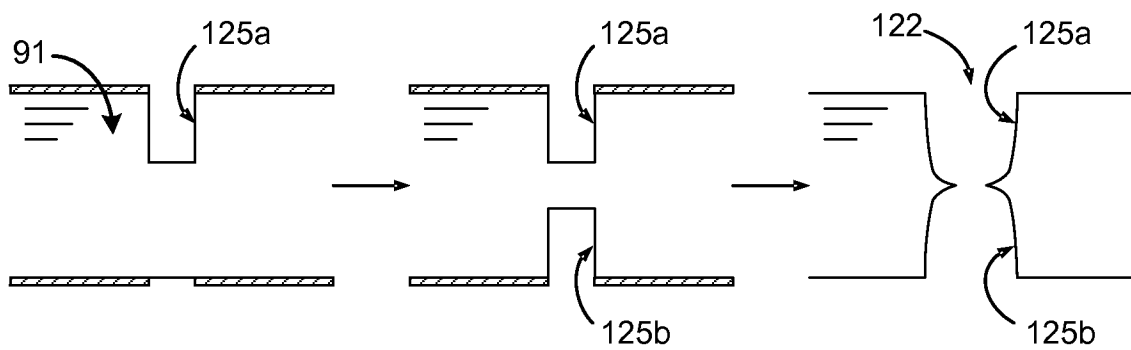


Figure 14E

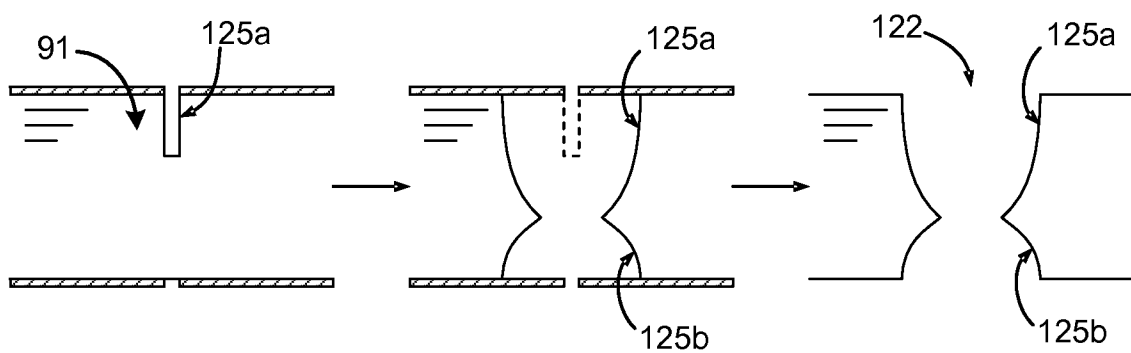
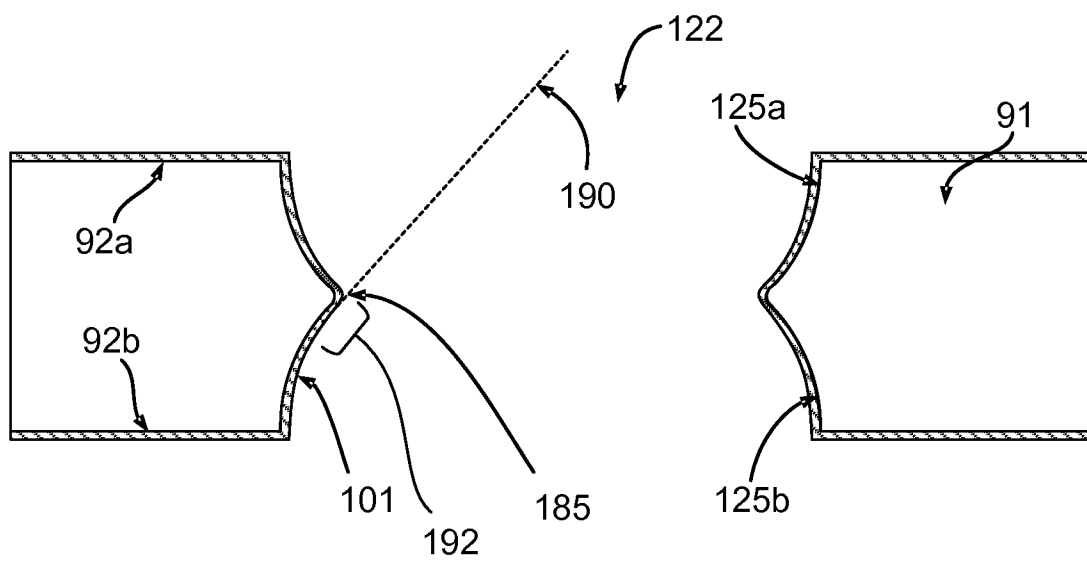
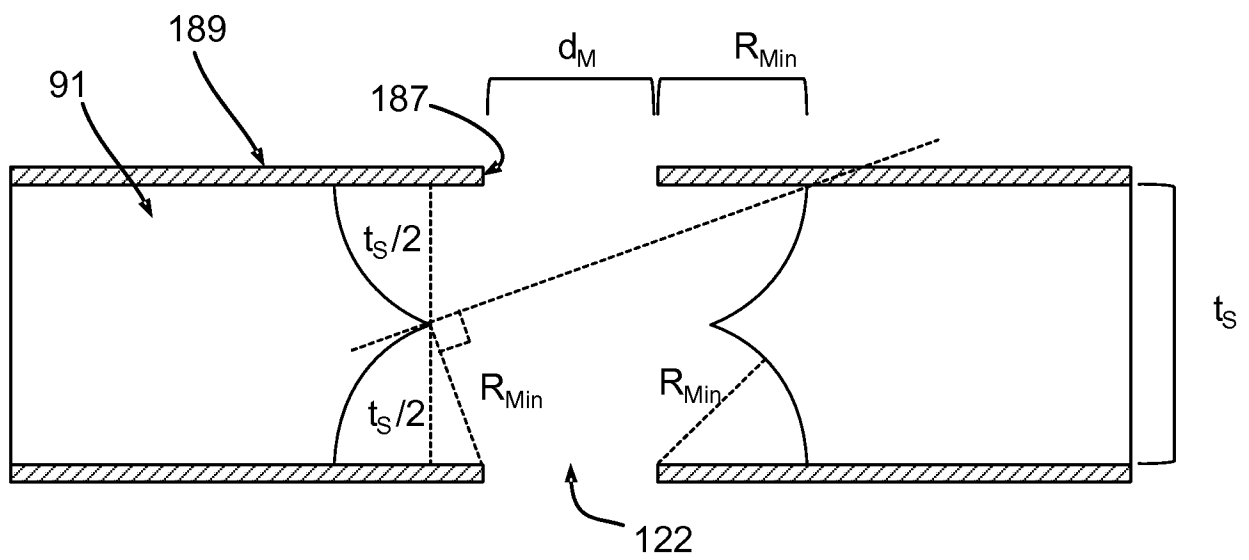
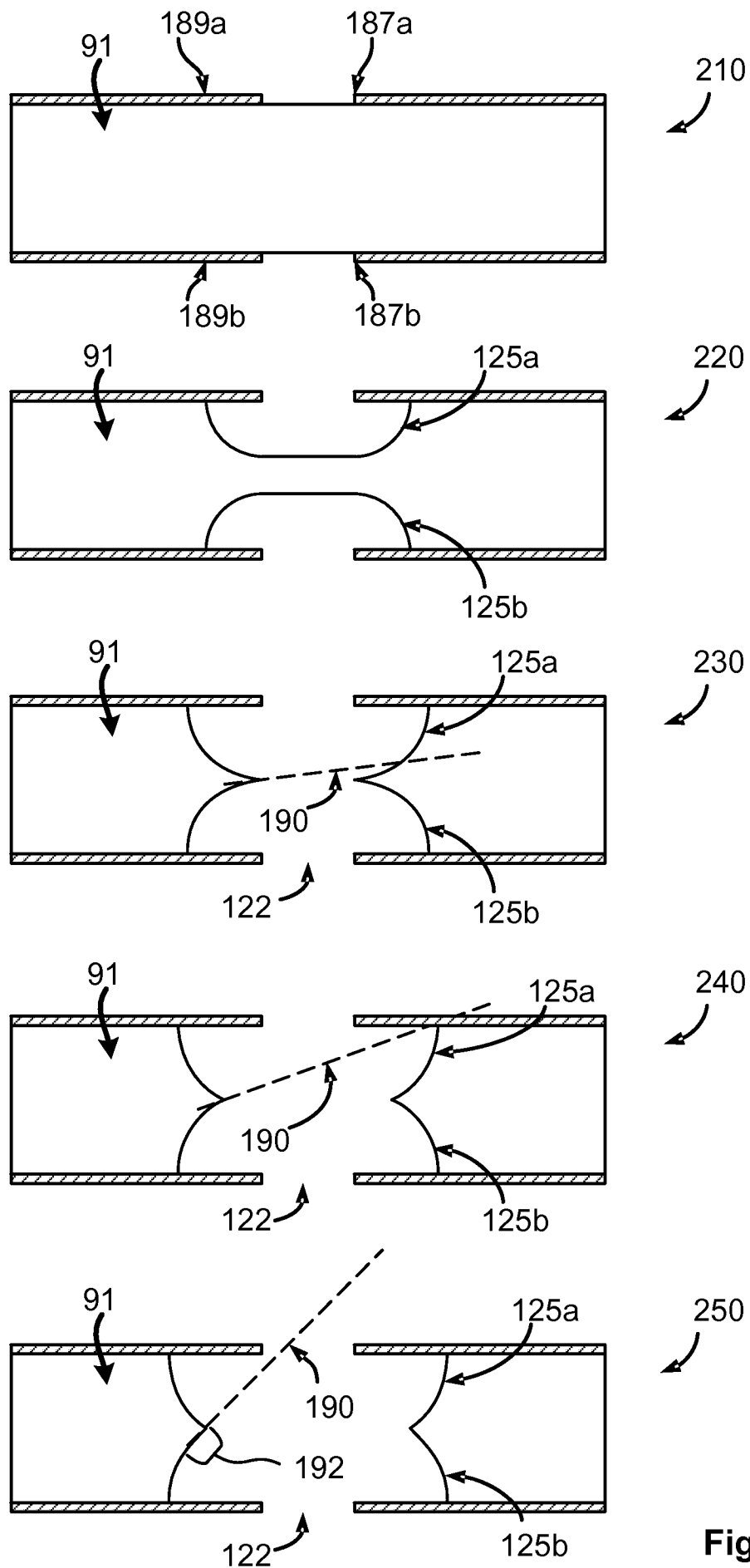
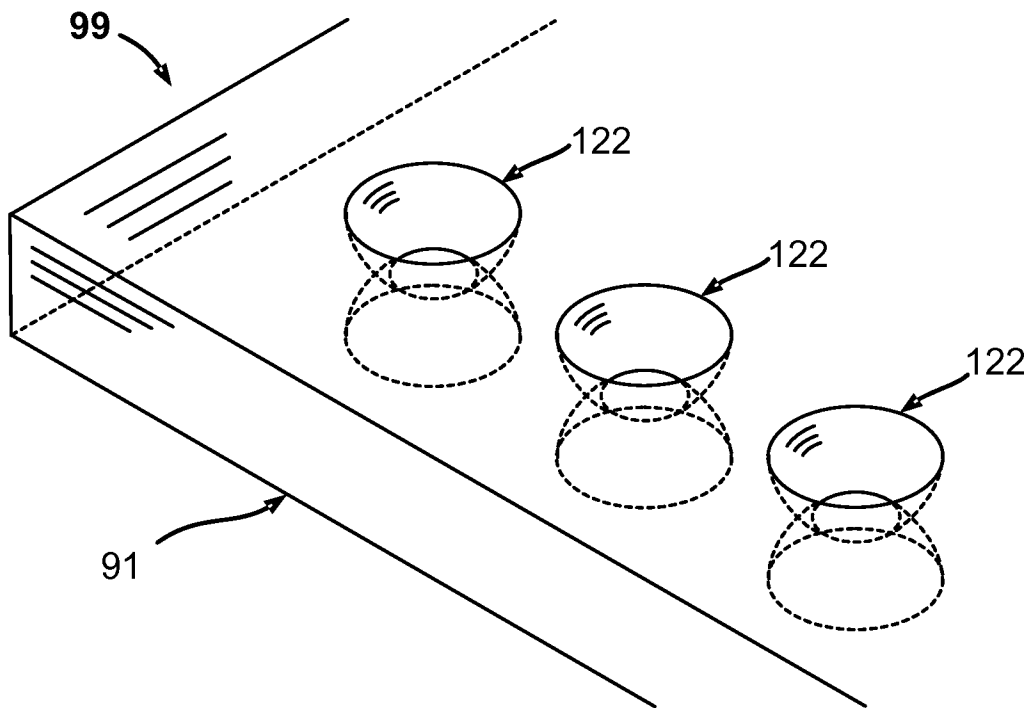
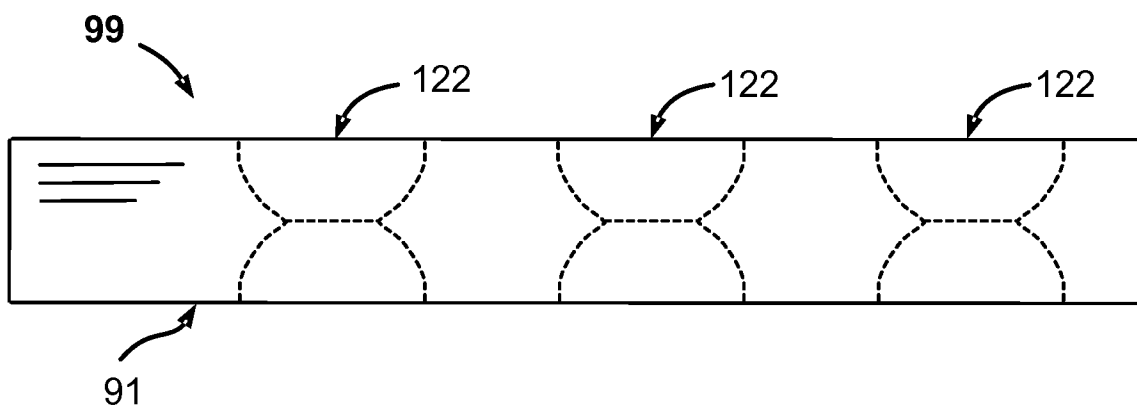


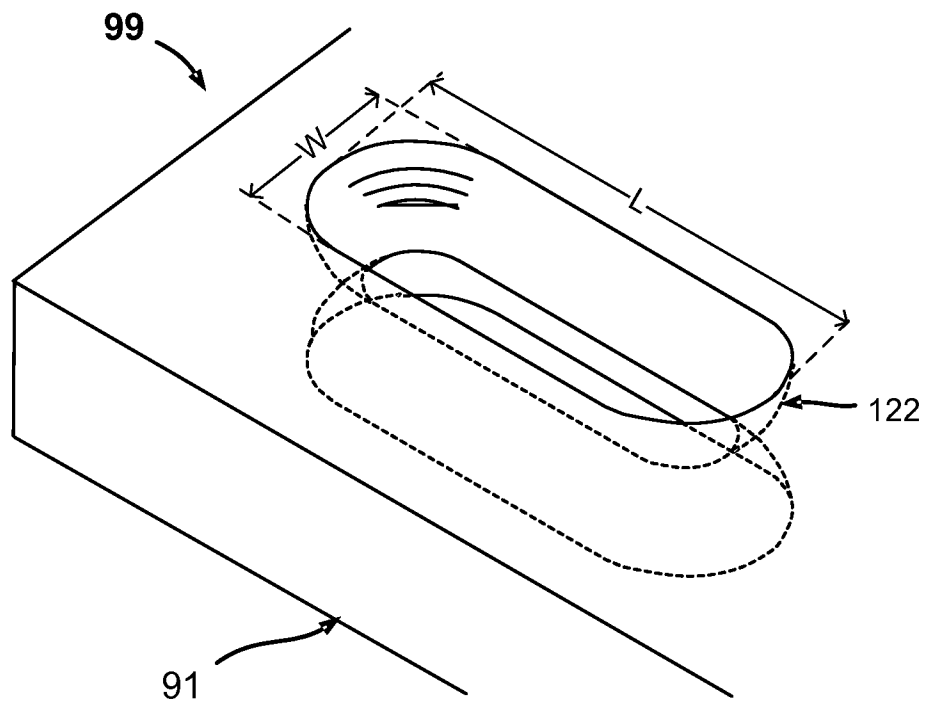
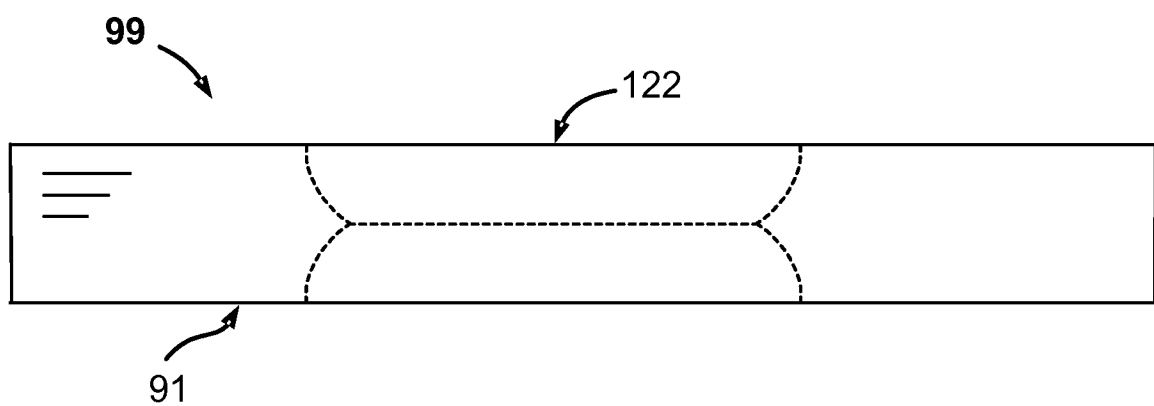
Figure 14F

**Figure 15**

**Figure 16**

**Figure 17**

**Figure 18A****Figure 18B**

**Figure 19A****Figure 19B**

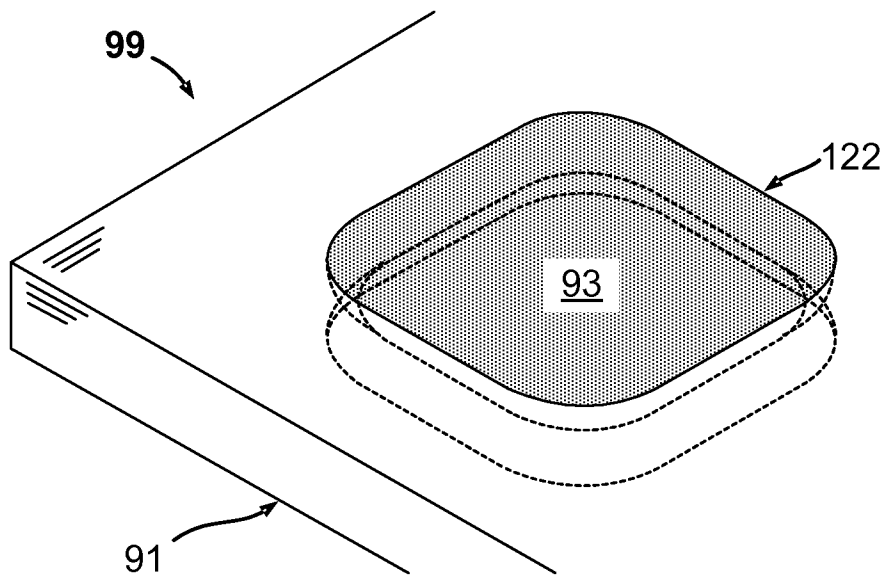


Figure 20A

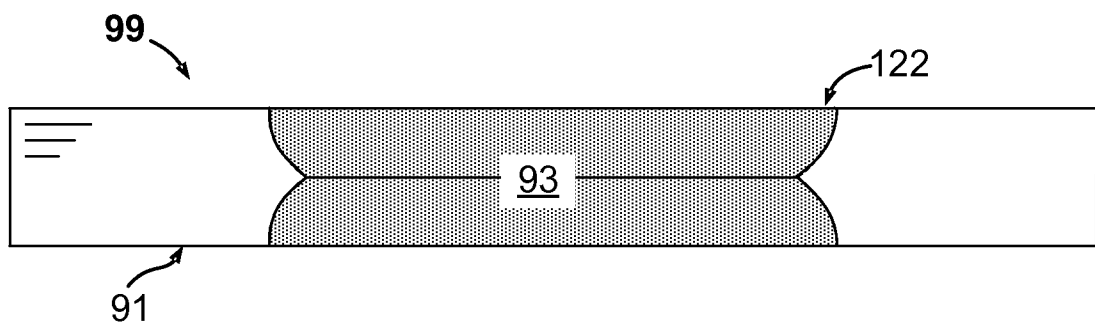


Figure 20B

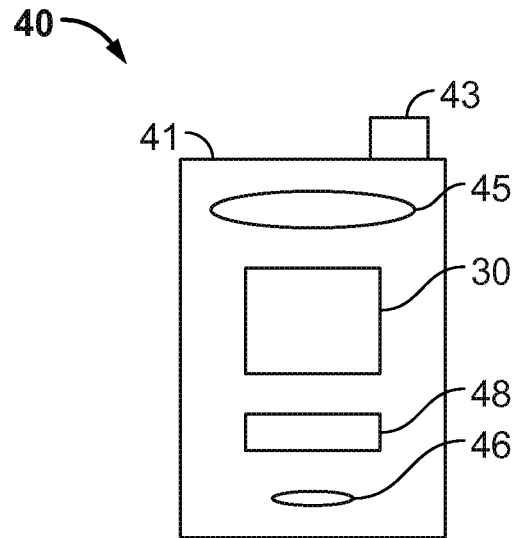


FIGURE 21A

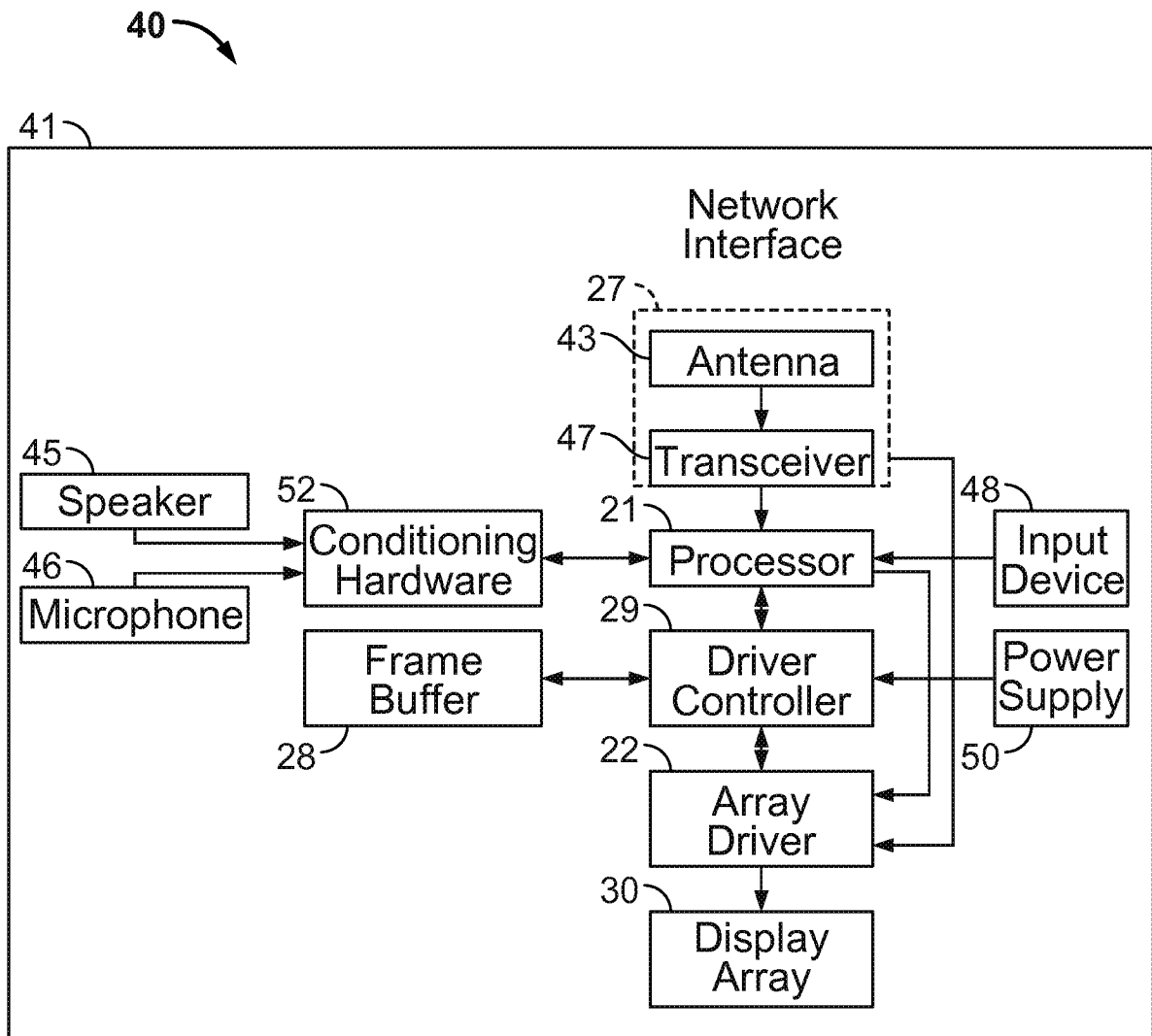


FIGURE 21B