(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

PCT

(43) International Publication Date
18 August 2011 (18.08.2011)

(10) International Publication Number
WO 2011/100647 A2

(51) International Patent Classification:
H01L 31/042 (2006.01) *H01L 21/306* (2006.01)
H01L 31/18 (2006.01) *H01L 21/20* (2006.01)

(21) International Application Number:
PCT/US2011/024670

(22) International Filing Date:
12 February 2011 (12.02.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/304,340 12 February 2010 (12.02.2010) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG,

[Continued on next page]

(54) **Title**: DOUBLE-SIDED REUSABLE TEMPLATE FOR FABRICATION OF SEMICONDUCTOR SUBSTRATES FOR PHOTOVOLTAIC CELL AND MICROELECTRONICS DEVICE MANUFACTURING

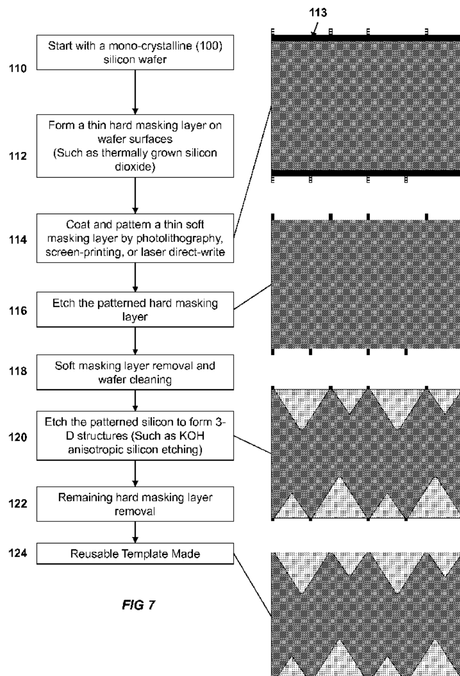

FIG 7

(57) **Abstract**: This disclosure presents manufacturing methods and apparatus designs for making TFSSs from both sides of a re -usable semiconductor template, thus effectively increasing the substrate manufacturing throughput and reducing the substrate manufacturing cost. This approach also reduces the amortized starting template cost per manufactured substrate (TFSS) by about a factor of 2 for a given number of template reuse cycles.

WO 2011/100647 A2

ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

DOUBLE-SIDED REUSABLE TEMPLATE FOR FABRICATION OF SEMICONDUCTOR SUBSTRATES FOR PHOTOVOLTAIC CELL AND MICROELECTRONICS DEVICE MANUFACTURING

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Provisional Patent Application Serial No. 61/304,340, filed February 12, 2010, which is hereby incorporated by reference in its entirety. Other related applications having common inventorship and/or ownership are mentioned throughout this disclosure, and they are also incorporated by reference in their entirety.

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FIELD

[0002] This disclosure relates in general to the field of photovoltaics and microelectronics, and more particularly to fabrication processes and manufacturing equipment for thin-film (or thin foil) crystalline (monocrystalline, multicrystalline, and polycrystalline) semiconductor substrates,
15 in some embodiments with the film or foil thickness ranging between about 1 micron up to about 100 microns. This disclosure provides for such manufacturing at low costs and high throughputs.

BACKGROUND

[0003] Currently, crystalline silicon has the largest market share in the photovoltaics (PV)
20 industry, accounting for over 80% of the overall PV market share. Although going to thinner crystalline silicon solar cells is long understood to be one of the most potent ways to reduce PV cost (because of the relatively high material cost of crystalline silicon wafers used in solar cells as a fraction of the total PV module cost), it is fraught with the problem of mechanical breakage due to the thin and large substrate sizes, and also to some extent that of light trapping in a thin
25 structure (since silicon is an indirect bandgap semiconductor material). The requirement of high mechanical yield and reduced wafer breakage rate is further problematic with the realization that for cost-effectiveness, the yields in PV manufacturing factories must be very high. On a standalone crystalline silicon solar cell (without support), going even somewhat below the current thickness range of 140 - 250 microns starts to severely compromise mechanical yield
30 during manufacturing. Thus, any solution to process very thin solar cell structures must either be fully supported by a host carrier throughout the cell process or use a novel self-supporting, standalone, substrate with an accompanying structural innovation.

[0004] Innovative manufacturing processes to produce solar cells at low costs using thin-film semiconductor substrates (TFSSs) as the active material have been disclosed in related applications. In some embodiments, the TFSSs comprise crystalline semiconductor (more specifically silicon in some embodiments). This technology platform produces solar cells from re-usable semiconductor templates. In certain embodiment, the surfaces of the templates have a periodic array of pre-structured 3-dimensional (3-D) structures. Examples of the 3-D TFSS based solar cells include but are not limited to prism honey-comb and inverted pyramidal cavities, which are described in earlier applications having common inventorship and/or ownership. The following are examples of related applications.

[0005] U.S. Patent Publications US2008/0157283 A1, US2008/0289684 A1, US2010/0148318 A1, US2010/0300518; U.S. Patent Application Serial No. 13/057,104; PCT Application Serial Nos. PCT/US10/60591, PCT/US10/62614.

[0006] As disclosed by the above documents, the epitaxial substrate is grown on top of a reusable template and is subsequently dislodged. In one embodiment, the template and substrate each comprise monocrystalline silicon. Afterwards, the reusable template may be reused several times, with or without reconditioning, to grow more epitaxial substrates. The reusable template has a planar top surface or a top surface with pre-formed 3-D microstructures, such as hexagonal honey-comb cavities or inverted pyramidal cavities. The releasing of the 3-D TFSS is achieved with an interim sacrificial layer. The sacrificial layer should satisfy two important criteria. First, it needs to transfer the information on crystallinity from the reusable template to the epitaxial layer. Second, it should be able to be removed selectively compared to the substrate and the reusable template. One specific embodiment of the sacrificial layer is porous silicon, whose porosity can be modulated to achieve both the aforementioned critical functions.

[0007] As disclosed by the above documents, the planar or 3-D TFSSs are made and released from one-side, i.e., the top surface of a reusable template. In other words, one solar substrate is made from a reusable template in each of its reuse cycles. In those disclosures, the template and substrate making equipment, and the porous silicon forming and epitaxial silicon growing equipment is capable of processing on only one side of the silicon template. The equipment is capable of processing multiple wafers at a time in a batching processing mode, but only one side of each template is used.

[0008] Solar cell manufacturing requires much higher productivity with much lower costs compared with semiconductor processes. Therefore, there it may be advantageous to develop manufacturing processes and equipment capable of making thin semiconductor substrates from both sides of a reusable template simultaneously.

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SUMMARY

[0009] In order to reduce the thin-film crystalline semiconductor (such as silicon) substrate manufacturing costs and increase the production throughputs, this disclosure provides manufacturing methods and apparatus designs for making TFSSs (or thin semiconductor such as 10 silicon foils) from both sides of a re-usable semiconductor template, thus effectively increasing the substrate manufacturing throughput and reducing the substrate manufacturing cost. This approach also reduces the amortized starting template cost per manufactured substrate (TFSS) by about a factor of 2 for a given number of template reuse cycles.

[0010] In accordance with the present disclosure, a double-sided semiconductor (such as 15 silicon) wafer with either planar surfaces or pre-structured 3-D structures is prepared for use as a re-usable template (or a reusable micromold). The planar templates may be surface polished or surface textured with random or regular arrayed surface roughness. The 3-D templates have 3-D structures, such as honey-comb prisms or inverted pyramidal cavities made on both sides of the templates. The surface structures on the front and back sides of a template may or may not be 20 same in terms of surface structures. For example, the back side structures may be misaligned compared to the front side structures to ensure increased template mechanical strength. In another example, the front side of a template may consist of 3-D structures, while the back side may be planar; however both sides may actively be used for making TFSSs. In yet another example, both sides of the template may be planar to manufacture TFSS (or thin silicon foil) 25 without any pre-structured 3D patterns.

[0011] In accordance with the present disclosure, suitable thin sacrificial layers, such as porous silicon layers, are formed on both sides of the templates for substrate release. These may be formed using a single batch processing tool (although the sacrificial layers may be formed on both sides sequentially using two separate sequential steps in one or two porous silicon formation 30 processing tools). The porous silicon layers are used as seed layers for epitaxial silicon growth and also used as a mechanically weak layer to facilitate the spatially selective release of the

epitaxial silicon layers (i.e., the TFSS) from the template (both frontside and backside, thus effectively doubling the throughput).

[0012] In accordance with the present disclosure, thin epitaxial silicon layers are grown concurrently on both sides of the templates in a single load of epitaxial process using chemical-vapor deposition (CVD).

[0013] In accordance with the present disclosure, TFSSs made from epitaxial silicon layers are released from both sides of the template after exposing the buried porous silicon layer from the template edges. The released TFSS films or foils (or wafers) from both sides may or may not be the same in terms of their physical structures. However, regardless of their shapes and sizes, TFSS parts released from front and back sides of a template may both be used to make solar cells (or microelectronic devices).

[0014] In accordance with the present disclosure, after releasing the TFSS from each side of a template, the template may be reconditioned and cleaned as needed followed by its next reuse cycle. Each template in this disclosure may be used multiple cycles until it becomes too thin to handle or until it loses its structural properties. In those cases, the used templates may be recycled.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The features, nature, and advantages of the disclosed subject matter will become more apparent from the detailed description set forth below when taken in conjunction with the drawings, in which like reference numerals indicate like features and wherein:

[0016] **FIGURES 1A** and **1B** illustrate cross-sectional schematic drawings of a double-sided planar template before and after its TFSS releasing, respectively;

[0017] **FIGURE 2A** illustrates a front view of a double-sided reusable template with hexagonal honeycomb interconnected trenches;

[0018] **FIGURE 2B** illustrates a cross-sectional schematic drawing of a double-sided template with prism honey-comb 3-D structures and TFSSs released from both sides of the template;

[0019] **FIGURE 3A** illustrates a front-view schematic drawing of a double-sided reusable template with inverted pyramidal cavities;

[0020] **FIGURE 3B** illustrates a schematic drawings of a double-sided template with inverted pyramid 3-D structures and TFSSs released from both sides of the template;

[0021] **FIGURE 4** illustrates a block diagram of making planar TFSSs using the double-sided re-usable template;

5 **[0022]** **FIGURES 5A–5E** illustrate cross-sectional schematic drawings of the planar TFSS making process, after major process steps, using the double-sided re-usable template;

[0023] **FIGURE 6** illustrates major fabrication process steps for making double-sided re-usable template that have hexagonal honeycomb trenches;

[0024] **FIGURE 7** illustrates major fabrication process steps for making double-sided re-

10 usable templates that have inverted pyramidal cavities;

[0025] **FIGURE 8** illustrates a conceptual cross-sectional drawing of an apparatus for forming porous silicon layers on both sides of a silicon template in a batch process; and

[0026] **FIGURE 9** illustrates a conceptual cross-sectional drawing of an apparatus for growing epitaxial silicon layers on both sides of a silicon template in a batch process.

15

DETAILED DESCRIPTION

[0027] Although the present disclosure is described with reference to specific embodiments, one skilled in the art could apply the principles discussed herein to other areas and/or embodiments without undue experimentation.

5 **[0028]** **FIGURE 1A** and **FIGURE 1B** illustrate cross-sectional schematic drawings of double-sided planar template **10** before and after TFSSs **12** are released from both sides. As illustrated in **FIGURE 1A**, epitaxially grown silicon layers are formed, in some embodiments concurrently, by an epitaxial silicon growth process, on both sides of a planar template and on top of porous silicon layers **14** on the template frontside and backside surfaces. The template
10 may be made of a monocrystalline silicon wafer with polished surfaces surface (although wafers with non-polished surfaces and/or polycrystalline or multicrystalline silicon wafers may also be used as templates). The wafer diameter may be in the range of approximately 150 to 450 mm and the wafer thickness may be in the range of approximately 0.5 to 1 mm. Even thicker wafers may be used, up to several millimeters in thickness. The template may be in a circular shape, a
15 square/rectangular shape, or a pseudo-square/pseudo-rectangular shape with rounded corners. The porous silicon layer may consist of a single layer, a bilayer or multilayer having different porosities, or a graded porosity layer. For example, the porous silicon sub-layer that contacts the template may have a higher porosity than the sub-layer that contacts the epitaxial layer. The overall epitaxial layer thickness may be in the range of approximately 1 to 100 microns and it
20 may consist of layers of different types and levels of doping. For example for solar cell applications, thin layer **16** that makes contact to the buried porous silicon layer may be n^+ (phosphorous) doped to form the front-surface-field (FSF) of the solar cell; middle layer **18** may be n (phosphorous) doped to form the base region of the solar cell; and outer epitaxial layer **20** may be p^+ (boron) doped to form the emitter region of the solar cell (or alternatively with
25 opposite doping polarities for solar cells with p-type base).

[0029] The epitaxial layer on the wafer edge may be removed (as shown in **FIGURE 1B**) to expose the buried porous silicon layer so that the epitaxial layers may be released from the template. Alternatively, the epitaxial layers may be prevented from growing at the template edges by mechanical shadowing and/or a hydrogen gas flow depletion purge. In another
30 alternative method, the TFSS edges are defined by laser trench cutting with the cutting depth no larger than approximately the epitaxial layer thickness. In this method, the remaining epitaxial

silicon layers at template edges may be removed after the TFSS is released by template edge lapping, grinding or polishing. As illustrated in **FIGURE 1B**, the epitaxial layers are released from the template to form TFSSs with optional reinforcement / support plates **22**. The thin silicon reinforcement or support plates may be temporarily or permanently mounted on the TFSSs to enhance their handle-ability during subsequence solar cell processing steps. As disclosed in related applications, the reinforcement plates may be made from solar grade glass, polymers, or other materials. There also may be solar grade adhesive layers used for making permanent bond between the reinforcement plate and TFSS. In the case that the epitaxial layer is thicker than about 50 microns and the TFSS size is smaller than about 150 mm in diameter, the reinforcement plates may not be needed. After the TFSS releasing, the template may be cleaned, reconditioned (in this sequence or in the reverse sequence of reconditioning followed by cleaning) and then reused. The TFSSs then go through the subsequent solar cell making process, including but not limited to surface cleaning, doping, passivation and contact making steps as disclosed in related applications.

[0030] **FIGURES 2A** and **2B** illustrate a double-sided template with hexagonal honeycomb 3-D structures and TFSSs made from both sides of the reusable template. **FIGURE 2A** illustrates a partial front-view schematic drawing of the template. The template may be made of a monocrystalline silicon wafer, although polycrystalline or multicrystalline wafers may also be used as templates. The template has pre-structured front and back side surfaces. More specifically, sidewall tapered hexagonal honeycomb trenches **30** are made in the silicon template on both of its sides. **FIGURE 2B** illustrates a cross-sectional schematic drawing (along the A-A cut direction) of the template after the release of TFSSs **34** (the drawing dimensions are not shown to scale). As shown, trench sidewalls **32** are tapered and the taper angle may be from several degrees to tens of degrees (in some embodiments approximately 3 to 10 degrees). The trench height may be approximately 50 to 300 microns, or more specifically in some embodiments 75 to 150 microns. The top trench width may be approximately 10 to 100 microns, or more specifically in some embodiments 20 to 50 microns. The backside structures may be misaligned to the front side structures to ensure increased template mechanical strength. The template wafer diameter is in the range of approximately 150 to 450 mm, and the wafer thickness is approximately in the range of 0.5 to over 1 mm (even thicker wafers may be used, up to several mm in thickness). Porous silicon layers (not shown) are initially formed on both sides of

the template surfaces, as discussed in the planar TFSS case. Then epitaxially grown silicon layers are formed on both sides of the template on top of the porous silicon layers. The epitaxial layer thickness is in the range of about 1 to 100 microns and it may consist of various doping types and levels across its depth, as explained in the planar TFSS case. For simplicity of schematic
5 drawing purpose, the doping types and levels are not shown in **FIGURE 2B**. In order to release the epitaxial layers from the template, the epitaxial layer on the wafer edge is removed to expose the buried porous silicon layer.

[0031] Alternatively, the epitaxial growth is prevented from growing at template edges by mechanical shadowing. In another alternative method, the TFSS edges are defined by laser
10 trench cutting with the cutting depth is no larger than approximately the epitaxial layer thickness. In this method, the remaining epitaxial silicon layers at template edges may be removed after TFSS release by template edge lapping, grinding or polishing. As illustrated in **FIGURE 2B**, the epitaxial layers are released from the template to form free-standing TFSSs without the needs of reinforcement plates. After TFSS release, the template may be cleaned, reconditioned and then
15 reused. The TFSSs then go through the subsequent solar cell making process, including but not limited to surface cleaning, doping, passivation and contact making steps as disclosed in related applications.

[0032] **FIGURES 3A** and **3B** illustrate a double-sided template with inverted pyramid 3-D structures and TFSSs made from both sides of the reusable template. **FIGURE 3A** illustrates a
20 partial front-view schematic drawing of the template. The template may be made of a monocrystalline silicon wafer, although polycrystalline or multicrystalline wafers may also be used as templates. The template has pre-structured front and back side surfaces. More specifically, inverted pyramidal cavities **40** are made into the silicon template on both of its sides. To facilitate formation of the pyramidal pattern, the template may be a (100)
25 monocrystalline silicon wafer. The inverted pyramidal cavities are aligned to the (100) directions and have their sidewalls etched to (111) crystallographic planes of mono-crystalline silicon. The sidewalls have 54.7^{o} angles against the top lateral plane. The cavity top openings are in the range of approximately 50 to 500 microns and depths are in the range of approximately 50 to 250 microns. **FIGURE 3B** illustrates a cross-sectional schematic drawing (along the A-A cut
30 direction) of the template after the release of TFSSs **42** (the drawing dimensions are not shown to scale). The back side structures may be misaligned to the front side structures to ensure increased

template mechanical strength. The template wafer diameter may be in the range of approximately 150 to 450 mm, and the wafer thickness may be approximately in the range of 0.5 to 1 mm (or even a few mm). As described above, a porous silicon layer or layers may be formed on both sides of the template. Then epitaxially grown silicon layers are formed on both sides of the
5 template on top of the porous silicon layers. The epitaxial layer thickness is in the range of about 1 to 100 microns and it may consist of various doping types and levels across its depth, as explained in the planar TFSS case. For simplicity of schematic drawing purpose, the doping types and levels are not shown in **FIGURE 3B**. In order to release the epitaxial layers from the template, the epitaxial layer on the wafer edge is removed to expose the buried porous silicon
10 layer.

[0033] Alternatively, the epitaxial layer is prevented from growing at template edges by mechanical shadowing. In another alternative method, the TFSS edges are defined by laser trench cutting with the cutting depth no larger than approximately the epitaxial layer thickness. In this method, the remaining epitaxial silicon layers at template edges may be removed after the
15 TFSS releasing by template edge lapping, grinding or polishing.

[0034] As illustrated in **FIGURE 3B**, the epitaxial layers are released from the template to form free-standing TFSSs without the need for reinforcement plates. After the TFSS releasing, the template may be cleaned, reconditioned and then reused. The TFSSs then go through the subsequent solar cell making process, including but not limited to surface cleaning, doping,
20 passivation and contact making steps as disclosed in related applications.

[0035] **FIGURE 4** outlines the major process steps in one embodiment of a process flow for making planar TFSSs using the double-sided re-usable template approach of this disclosure. The fabrication process starts at step **50** from a substantially planar template, which may be a monocrystalline (100) silicon wafer. The starting wafer could be in circular or square or
25 rectangular or polygonal shapes. Both sides of the template surface may be the same in term of their surface finishes, or they may be different. In one embodiment, the front and back surfaces are non-textured and polished. In another embodiment, shallow (e.g. less than about 10 microns) and random textures are formed on both sides of the template surfaces. The (100) silicon wafer surface texturing processes are known in the prior arts and are usually conducted by diluted
30 alkaline chemistry, such as KOH or NaOH silicon etching.

[0036] At step **52**, a porous silicon layer is formed by electrochemical anodic HF etching of silicon on both the front and back sides of the template surfaces. During the porous silicon forming in an HF/IPA (or HF / acetic acid) solution, the electrical current polarity is periodically switched between positive and negative currents so that each template side is successively etched in order to form the bilayer or multi-layer porous silicon structure on both template sides. In addition to the periodical current polarity switching, the current intensity is also changed in a controlled manner to form a porous silicon bilayer or multilayer that consists of the desired different (low and high) porosities. The first thin porous silicon layer is on the top and is first formed from the bulk silicon wafer. The first thin layer has a lower porosity of approximately 15% to 30%. The second thin porous silicon layer is directly grown from the bulk silicon and is underneath the first thin layer of porous silicon. The second thin porous silicon layer may have a higher porosity in the range of approximately 40% - 80%. The top lower porosity layer is used as a crystalline seed layer for high quality epitaxial silicon growth, and the underneath higher porosity porous silicon layer is used for facilitating TFSS releasing due to its low-density physical connections (between the epitaxial and bulk silicon interfaces) and its weak mechanical strength.

[0037] Alternatively, a single porosity release layer with a progressively increased porosity from top to bottom can also be used. In this case, the top portion of the porous silicon layer has a low porosity of approximately 15% to 30%, and the lower portion of the porous silicon layer has a high porosity of approximately 40% to 80%, with a region of graded porosity in between.

[0038] At step **54**, and before the epitaxial silicon growth, the wafer is baked in a high temperature (at approximately 950°C to 1200°C, and more specifically in some embodiments in the range of 1050°C to 1150°C) hydrogen environment within the epitaxial silicon deposition reactor in order to form coalesced structures (with relatively large voids) within the higher-porosity buried porous silicon layer while forming a continuous surface seed layer of crystalline silicon on the top of the lower-porosity porous silicon layer.

[0039] Next, at step **56**, a mono-crystalline epitaxial silicon layer is concurrently deposited on both sides of the template, preferably in a high-throughput large-batch epitaxial furnace. The epitaxial layer may be in-situ doped. For example for solar cell applications, the bulk base of the epitaxial layer may be n (phosphorous) doped, the inner layer may be n^+ (phosphorous) doped to

form the FSF, and the outer layer may be p (boron) doped to form the emitter region of the solar cell. The thickness of the epitaxial layer is in the range of 1 to 100 microns.

[0040] In optional step **58**, a thin oxide layer is thermally grown on the epitaxial surface. The thin oxide layer may be used for solar cell surface passivation or a masking layer for
5 subsequent selective surface openings.

[0041] In optional step **60**, temporary or permanent reinforcement plates are mounted on the front and back silicon surfaces. The reinforcement plates also serve as carriers for enabling handling and processing thin TFSSs using commercially available solar cell manufacturing equipment, as disclosed in PCT application serial nos. PCT/US10/60591 and PCT/US10/62614.

10 **[0042]** Next, at step **62**, the epitaxial layer on the wafer edge is removed by template edge lapping, grinding or polishing, to expose the buried porous silicon layer so that the epitaxial layers may be released from the template. Alternatively, the epitaxial growth is prevented from growing at template edges by mechanical shadowing. In another alternative method, as disclosed in related applications, the TFSS edges are defined by laser trench cutting the cutting depth no
15 larger than approximately the epitaxial layer thickness.

[0043] In step **64**, the optionally reinforced epitaxial layer of silicon is released/separated from the template, and the released epitaxial silicon layer is therefore referred as a thin film silicon substrate. Related applications disclose detailed methods of releasing the epitaxial layer to form a TFSS. In one of the disclosed methods, the TFSS is released in an ultrasonic DI-water
20 bath. In another disclosed method, the TFSS is released by direct pulling with the wafer backside and the top epitaxial layer vacuum chucked.

[0044] In step **66**, the released TFSS backside surface is cleaned by short silicon etching using KOH or TMAH solutions to remove the silicon debris and fully or partially remove the quasi-monocrystalline silicon (QMS) layer. In the meantime and after removal of the edge
25 epitaxial silicon layer from the template, the template is cleaned by using diluted HF and diluted wet silicon etch solution, such as TMAH and/or KOH to remove the remaining porous silicon layers and silicon particles. Then the template is further cleaned by conventional silicon wafer cleaning methods, such as SC1 and SC2 wet cleaning (or the so-called RCA cleaning process) to removal possible organic and metallic contaminations. Finally, after proper rinsing with DI water
30 and N_2 drying, the template is ready for another re-use cycle.

[0045] **FIGURES 5A-5E** illustrate cross-sectional schematic drawings of the planar TFSS making process, after major processing steps, using the double-sided re-usable template. The dimensions in these drawings are not drawn to scale. **FIGURE 5A** illustrates starting template **70** that has substantially planar front and back surfaces.

5 **[0046]** **FIGURE 5B** illustrates the template after formation of porous silicon **72** on both its front and back surfaces. However, the porous silicon layers on the front and back surfaces are not connected, since there is no porous silicon formed on the very edge or bevel area of the template.

[0047] **FIGURE 5C** illustrates the grown epitaxial layers **74** on both the front and back template surfaces. Epitaxial layers **74** in this example comprise n^+ doped FSF layer **76**, n doped

10 base **78**, and p^+ doped emitter **80**. Depending on the template holding configuration in the epitaxial growth chamber, there may or may not be thin epitaxial silicon layers grown on the very edge or bevel area of the template surface.

[0048] **FIGURE 5D** illustrates the step after reinforcement plates **82** are mounted and border definition trenches **84** are made at the edges of the TFSS. Edge epitaxial layers **86** may be

15 removed before or after TFSS separation.

[0049] **FIGURE 5E** illustrates the release of TFSSs **88** with the reinforcement plates. The separation of TFSSs **88** from the template surface happens in the buried porous silicon layers. The remaining porous silicon layers and/or QMS thin layers on the TFSS and template surfaces are etched off by wet chemical etching, such as diluted KOH or NaOH solution (or alternatively

20 using an HF-nitric-acetic (HNA) solution), after the TFSS release. The remaining epitaxial and QMS silicon layers on the template edges are also removed or etched off prior to the next template reuse cycle.

[0050] **FIGURE 6** shows a process flow and illustrates the template after major fabrication process steps for making double-sided re-usable templates that have hexagonal honeycomb

25 trenches. Such 3-D templates are used to make honeycomb TFSSs.

[0051] The template fabrication process starts at step **90** with a mono-crystalline (100) silicon wafer. In step **92**, photoresist layers **93** are coated and patterned on both the front and back side surfaces of the template. Alternatively, resist layers could be screen printed.

[0052] Next, at step **94**, the front and back side silicon trenches are etched in a deep-

30 reactive-ion-etch (DRIE) or a reactive-ion-etch (RIE) process using silicon etching gases, such as SF_6. In the DRIE process, periodic surface passivation using C_4F_8 gas is performed to control the

trench sidewall surfaces. The trench etching is time-controlled. After the trench etching, the remaining resist layer is removed at step **96**, and all the exposed silicon surfaces are fully cleaned at step **98**. Optionally, the trench sidewall rough surfaces are slightly etched to make them smoother. At step **100**, the reusable template is complete.

5 **[0053]** The 3-D TFSS manufacturing process of using the double-sided honeycomb template is substantially the same as the planar TFSS making process, except the reinforcement plates may not be needed prior to the TFSS releasing. For simplicity, the 3-D TFSS making process is not shown in figures.

[0054] **FIGURE 7** illustrates major fabrication process steps for making double-sided re-
10 usable templates that have inverted pyramidal cavities. Such 3-D templates are used to make pyramidal TFSSs. The template fabrication process starts at step **110** with a monocrystalline (100) silicon wafer. The thickness of the wafers is in the range of approximately 0.5 to 1 mm (or even a few mm). In step **112**, a thermally grown oxide layer of about 0.5 to 1.5 microns is used as hard mask layer **113**. The silicon oxide layer covers the entire wafer surfaces including the
15 edges. The oxide on the wafer edge is not shown.

[0055] Next, at step **114**, photolithographic defined or screen-printed photoresist pattern is applied on the front and back wafer surface. The photolithography process includes photoresist coating, baking, exposure, developing and post baking. The photoresist pattern consists of staggered large square openings and small square openings. It is important the square-opening
20 patterns are precisely aligned to the wafer <100> direction on the front surface.

[0056] The patterned resist pattern is then transferred at step **116** to the hard masking layer, i.e. the front oxide layer. The pattern transferring from the photoresist layer to the oxide layer is achieved by controlled oxide etching in a buffered HF solution. During the HF wet etching, the front and back oxide opening are etched in the same time and the edge oxide layer is fully
25 protected and kept at its original thickness. The oxide pattern on the wafer surfaces also consists of staggered large and small square openings that are aligned to the <100> crystallographic directions.

[0057] After the pattern transfer, at step **118**, the remaining photoresist layer is removed by wet or dry photoresist removal methods. Next, at step **120**, silicon anisotropic etching is
30 conducted by a time-controlled KOH, NaOH, or TMAH etching that results in large pyramidal silicon cavities. The etching temperature may be in the range of approximately 50°C to 80°C.

The exposed silicon surfaces on the front and back sides are etched in the same time and the wafer edge surfaces are fully protected by the un-patterned oxide layer. The KOH etch may be time-controlled so that a certain pyramidal cavity depth may be reached. Alternatively, the KOH etching may be self-terminated when the four pyramid (111) sidewalls meet at the cavity bottom.

5 **[0058]** After the KOH etching, the remaining oxide layer is thinner than before the etching since the oxide is also etched to some extent in the KOH or TMAH solution, albeit with a much slower etch rate than silicon etch. The remaining oxide layer is then removed at step **122** in a diluted HF solution followed by standard wafer cleaning in SC2 and SC2, DI water rinsing and N_2 drying. At step **124**, reusable pyramidal double-sided template is finished.

10 **[0059]** The 3-D TFSS manufacturing process of using the double-sided pyramidal template is same as the planar TFSS making process, except the reinforcement plates may not be needed prior to the TFSS releasing. For simplicity, the 3-D TFSS making process is not shown in figures.

[0060] **FIGURE 8** illustrates a conceptual cross-sectional drawing of one possible 15 embodiment of an apparatus for forming porous silicon layers on both sides of the silicon template in a batch electrochemical anodic etch process. Templates **130** are batch loaded in the etching chamber and they are individually held from and sealed at their edges with seals **132**. Therefore there are no porous silicon layers formed at the very edge surface of the template. The loaded templates are spaced uniformly in the etching chamber and the electrolytic liquid (HF, 20 IPA, and DI water mixture) between the templates has a consistent concentration and volume. The temperature of the liquid is actively controlled and gas bubbles generated during the process are timely removed by external liquid circulation and gas bubble extraction. Power supply **134** supplies power with current intensity control, time control, and polarity switching capability to electrodes **136**. The electrical current polarity is periodically switched so that each template side 25 is consecutively and cumulatively etched. In addition to the periodical current polarity switching, the current intensity is also changed in a controlled manner to form a porous silicon layer that may consists of two or thin layers with different porosities, or a graded porosity. One of ordinary skill will understand that different electrolyte volumes and concentrations, etch chamber sizes, distances between adjacent templates, current levels and polarities may be used in the 30 embodiment of **FIGURE 8**. The passage of electrical current creates porous silicon layers **138**.

[0061] **FIGURE 9** illustrates a conceptual cross-sectional drawing of an apparatus for concurrently growing epitaxial silicon layers on both sides of the silicon template in a batch process. As described above, porous silicon layers are formed on both sides of the silicon templates, except the very edges of the templates. The templates are batch loaded in the epitaxial reaction chamber and they are individually held from their edges where there are no porous silicon layers.

[0062] This edge-holding method prevents broken porous silicon debris from accumulating during the template loading and unloading process. The loaded templates are spaced uniformly in the reaction chamber. With the distributed gas injection layout, reactive gases are evenly delivered from gas injector **144** to all the exposed silicon surfaces and exhausted via exhaust **146**, enabling uniform epitaxial growth within a single wafer and among wafers. The reaction chamber is heated to a high temperature in the range of 950°C to 1200°C during the process. The heating and its control function are not shown in **FIGURE 9** for simplicity.

[0063] Those with ordinary skill in the art will recognize that the disclosed embodiments have relevance to a wide variety of areas in addition to those specific examples described above.

[0064] The foregoing description of the exemplary embodiments is provided to enable any person skilled in the art to make or use the claimed subject matter. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without the use of the innovative faculty. Thus, the claimed subject matter is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

[0065] It is intended that all such additional systems, methods, features, and advantages that are included within this description be within the scope of the claims.

WHAT IS CLAIMED IS:

1. A method for making a pair of monocrystalline thin-film silicon substrates, said method comprising:

5 providing a monocrystalline silicon wafer;

patterning a first surface and a second surface of said monocrystalline silicon wafer with a resist layer having a hexagonal pattern;

etching said monocrystalline silicon wafer, thereby producing a set of structural surface topography features on said first surface and said second surface, said structural surface 10 topography features comprising a plurality of isolated hexagonal posts;

removing said resist layer from said monocrystalline silicon wafer; and

cleaning said first surface and said second surface of said monocrystalline silicon wafer, said monocrystalline silicon wafer comprising a double-sided reusable template;

producing a first porous silicon layer on said first surface and a second porous silicon 15 layer on said second surface of said double-sided reusable template via an anodic etching process, said porous silicon layers having a crystallinity consistent with said double-sided reusable template;

epitaxially depositing a first monocrystalline thin-film silicon substrate on said first porous silicon layer and a second monocrystalline thin-film silicon substrate on said second 20 porous silicon layer, said monocrystalline thin-film silicon substrates having a crystallinity consistent with said porous silicon layers;

separating said first and said second monocrystalline thin-film silicon substrates from said first and said second porous silicon layers.

25 2. The method of Claim 1, wherein said first porous silicon layer comprises a first porous silicon bilayer having at least two different porosities, and said second porous silicon layer comprises a second porous silicon bilayer having at least two different porosities.

3. The method of Claim 1, wherein said first porous silicon layer comprises a first graded 30 porosity layer, and said second porous silicon layer comprises a second graded porosity layer.

4. The method of Claim 1, wherein said monocrystalline thin-film silicon substrates comprise in-situ doped monocrystalline thin-film silicon substrates.

5 5. The method of Claim 4, wherein each of said in-situ doped monocrystalline thin-film silicon substrates comprises a front-surface field layer and a base layer for a photovoltaic solar cell.

6. The method of Claim 4, wherein each of said in-situ doped monocrystalline thin-film 10 silicon substrates comprises a front-surface field layer, a base layer, and an emitter layer for a photovoltaic solar cell.

7. The method of Claim 1, further comprising the step of heating said double-sided reusable template in an atmosphere of hydrogen after producing said first and said second 15 porous silicon layers in situ and prior to said epitaxial depositing step.

8. A method for making a pair of monocrystalline thin-film silicon substrates, said method comprising:

providing a monocrystalline silicon wafer;

20 producing a thermally grown silicon oxide layer on a first surface and a second surface of said monocrystalline silicon wafer;

patterning said first surface and said second surface of said monocrystalline silicon wafer with a resist layer comprising large squares and small squares, said large and small squares being aligned to a <110> direction of said monocrystalline silicon wafer;

25 transferring said pattern of large squares and small squares to said silicon oxide layer;

anisotropically etching said monocrystalline silicon wafer, thereby producing a set of structural surface topography features on said first surface and said second surface, said structural surface topography features comprising a plurality of square pyramidal cavities;

removing said resist layer from said monocrystalline silicon wafer; and

30 cleaning said first surface and said second surface of said monocrystalline silicon wafer, said monocrystalline silicon wafer comprising a double-sided reusable template;

producing a first porous silicon layer on said first surface and a second porous silicon layer on said second surface of said double-sided reusable template via an anodic etching process, said porous silicon layers having a crystallinity consistent with said double-sided reusable template;

5 epitaxially depositing a first monocrystalline thin-film silicon substrate on said first porous silicon layer and a second monocrystalline thin-film silicon substrate on said second porous silicon layer, said monocrystalline thin-film silicon substrates having a crystallinity consistent with said porous silicon layers;

separating said first and said second monocrystalline thin-film silicon substrates from
10 said first and said second porous silicon layers.

9. The method of Claim 8, wherein said first porous silicon layer comprises a first porous silicon bilayer having at least two different porosities, and said second porous silicon layer comprises a second porous silicon bilayer having at least two different porosities.

15

10. The method of Claim 8, wherein said first porous silicon layer comprises a first graded porosity layer, and said second porous silicon layer comprises a second graded porosity layer.

20 11. The method of Claim 8, wherein said monocrystalline thin-film silicon substrates comprise in-situ doped monocrystalline thin-film silicon substrates.

12. The method of Claim 11, wherein each of said in-situ doped monocrystalline thin-film silicon substrates comprises a front-surface field layer, a base layer, and an emitter layer.

25

13. The method of Claim 8, further comprising the step of heating said double-sided reusable template in an atmosphere of hydrogen after producing said first and said second porous silicon layers.

30 14. A method for making a pair of monocrystalline thin-film silicon substrates, said method comprising:

providing a monocrystalline silicon wafer;

polishing, lapping, or removing saw damage from a first surface and a second surface of said monocrystalline silicon wafer;

cleaning said first surface and said second surface of said monocrystalline silicon wafer,
5 said monocrystalline silicon wafer comprising a double-sided reusable template;

producing a first porous silicon layer on said first surface and a second porous silicon layer on said second surface of said double-sided reusable template via an anodic etching process, said porous silicon layers having a crystallinity consistent with said double-sided reusable template;

10 epitaxially depositing a first monocrystalline thin-film silicon substrate on said first porous silicon layer and a second monocrystalline thin-film silicon substrate on said second porous silicon layer, said monocrystalline thin-film silicon substrates having a crystallinity consistent with said porous silicon layers;

separating said first and said second monocrystalline thin-film silicon substrates from
15 said first and said second porous silicon layers.

15. The method of Claim 14, wherein said first porous silicon layer comprises a first porous silicon bilayer having at least two different porosities, and said second porous silicon layer comprises a second porous silicon bilayer having at least two different porosities.

20

16. The method of Claim 14, wherein said first porous silicon layer comprises a first graded porosity layer, and said second porous silicon layer comprises a second graded porosity layer.

25 17. The method of Claim 14, wherein said monocrystalline thin-film silicon substrates comprise in-situ doped monocrystalline thin-film silicon substrates.

18. The method of Claim 17, wherein each of said in-situ doped monocrystalline thin-film silicon substrates comprises at least one of a front-surface field layer, a base layer, or an
30 emitter layer.

19. The method of Claim 14, further comprising the step of heating said double-sided reusable template in an atmosphere of hydrogen after producing said first and said second porous silicon layers.

5 20. A method for making a pair of crystalline thin-film semiconductor substrates, said method comprising:

providing a crystalline semiconductor wafer;

pre-structuring a first surface and a second surface of said crystalline semiconductor wafer with a random texture or a regular pattern, thereby producing a set of structural surface
10 topography features on said first surface and said second surface, said structural surface topography features comprising a plurality of topography features; and

cleaning said first surface and said second surface of said crystalline semiconductor wafer, said crystalline semiconductor wafer serving as a double-sided reusable template;

producing a first porous semiconductor layer on said first surface and a second porous
15 semiconductor layer on said second surface of said double-sided reusable template via an anodic etching process, said porous semiconductor layers having a crystallinity consistent with said double-sided reusable template;

depositing a first crystalline thin-film semiconductor substrate on said first porous semiconductor layer and a second crystalline thin-film semiconductor substrate on said
20 second porous semiconductor layer, said crystalline thin-film semiconductor substrates having a crystallinity consistent with said porous semiconductor layers and said reusable template;

separating said first and said second monocrystalline thin-film semiconductor substrates from said first and said second porous semiconductor layers.

25

21. A method for making a pair of crystalline thin-film silicon substrates, said method comprising:

providing a crystalline silicon wafer;

concurrently pre-structuring a first surface and a second surface of said crystalline silicon
30 wafer with a random texture, thereby producing a set of structural surface topography

features on said first surface and said second surface, said structural surface topography features comprising a plurality of topography features; and

cleaning said first surface and said second surface of said crystalline silicon wafer, said crystalline silicon wafer serving as a double-sided reusable template;

5 producing a first porous silicon layer on said first surface and a second porous silicon layer on said second surface of said double-sided reusable template via an anodic etching process, said porous silicon layers having a crystallinity consistent with said double-sided reusable template;

depositing a first crystalline thin-film silicon substrate on said first porous silicon layer 10 and a second crystalline thin-film silicon substrate on said second porous silicon layer, said crystalline thin-film silicon substrates having a crystallinity consistent with said porous silicon layers and said reusable template;

separating said first and said second monocrystalline thin-film semiconductor substrates from said first and said second porous semiconductor layers.

15

22. A method for making a pair of monocrystalline thin-film silicon substrates, said method comprising:

providing a monocrystalline semiconductor wafer;

pre-structuring a first surface and a second surface of said monocrystalline silicon wafer 20 with a three-dimensional texture, thereby producing a set of structural surface topography features on said first surface and said second surface, said structural surface topography features comprising a plurality of topography features creating a non-planar structure; and

cleaning said first surface and said second surface of said monocrystalline silicon wafer, said monocrystalline silicon wafer serving as a double-sided reusable template;

25 producing a first porous silicon layer on said first surface and a second porous silicon layer on said second surface of said double-sided reusable template via an anodic etching process, said porous silicon layers having a crystallinity consistent with said double-sided reusable template;

epitaxially depositing a first monocrystalline thin-film silicon substrate on said first 30 porous silicon layer and a second monocrystalline thin-film silicon substrate on said second

porous silicon layer, said monocrystalline thin-film silicon substrates having a crystallinity consistent with said porous silicon layers and said reusable template;

separating said first and said second monocrystalline thin-film silicon substrates from said first and said second porous silicon layers.

5

23. A method for making a pair of monocrystalline thin-film silicon substrates, said method comprising:

providing a monocrystalline semiconductor wafer;

concurrently cleaning said first surface and said second surface of said monocrystalline

10 silicon wafer, said monocrystalline silicon wafer serving as a double-sided reusable template;

producing a first porous silicon layer on said first surface and a second porous silicon layer on said second surface of said double-sided reusable template via an anodic etching process, said porous silicon layers having a crystallinity consistent with said double-sided reusable template;

15 epitaxially depositing a first monocrystalline thin-film silicon substrate on said first porous silicon layer and a second monocrystalline thin-film silicon substrate on said second porous silicon layer, said monocrystalline thin-film silicon substrates having a crystallinity consistent with said porous silicon layers and said reusable template;

separating said first and said second monocrystalline thin-film silicon substrates from

20 said first and said second porous silicon layers.

24. An apparatus for forming porous silicon layers on at least two surfaces of a plurality of silicon templates in a batch electrochemical anodic etch process, said apparatus comprising:

25 a plurality of edge-sealing template mounts, with a plurality of templates disposed within said mounts, said plurality of mounts operable to prevent formation of porous silicon at said template edges;

an electrolyte disposed among said plurality of templates;

an electrolyte temperature controller;

30 a gas bubble extractor operable to remove gas bubbles from said plurality of templates by circulating said electrolyte; and

a power supply operable to switch polarity, change current intensity, and control etching time to produce said porous silicon layers.

25. An apparatus for concurrently growing epitaxial silicon layers on at least two surfaces
5 of a plurality of silicon templates, said apparatus comprising:

a plurality of evenly space vertical edge-holding template mounts;

a plurality of evenly spaced holes operable to inject and exhaust a gas to deposit said epitaxial silicon layers.

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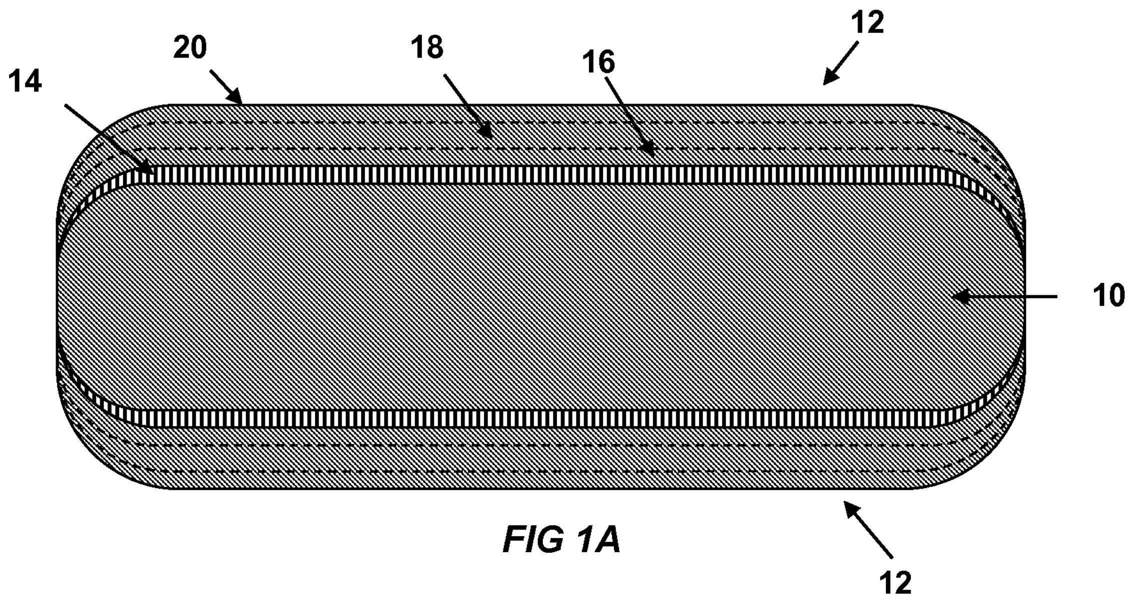

FIG 1A

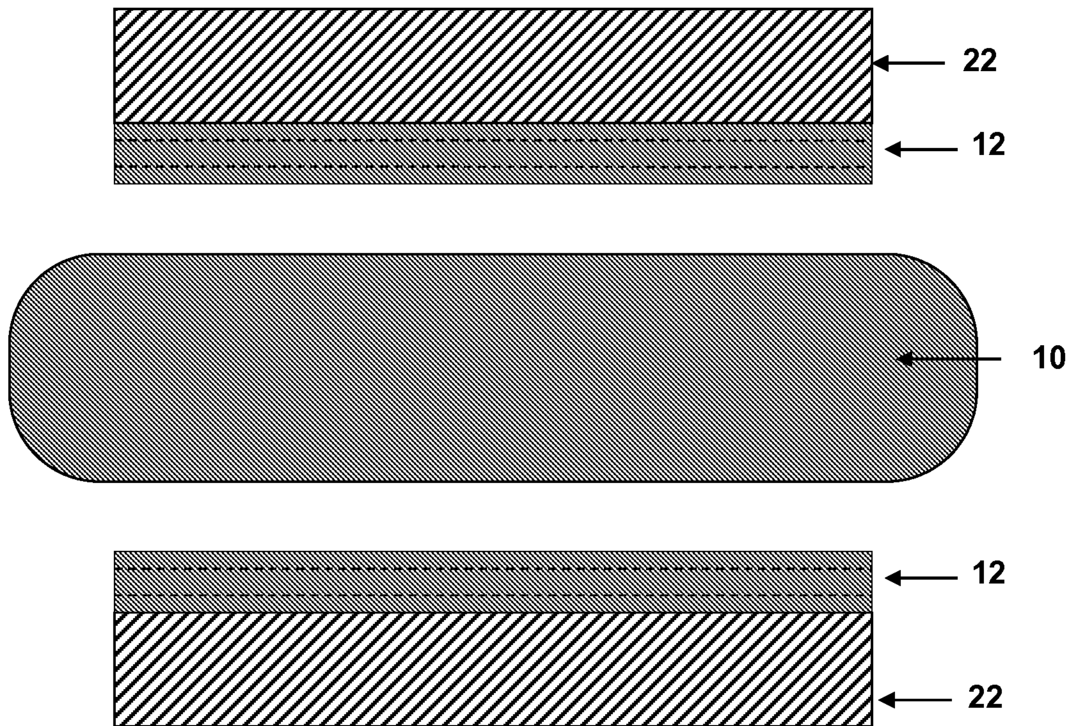

FIG 1B

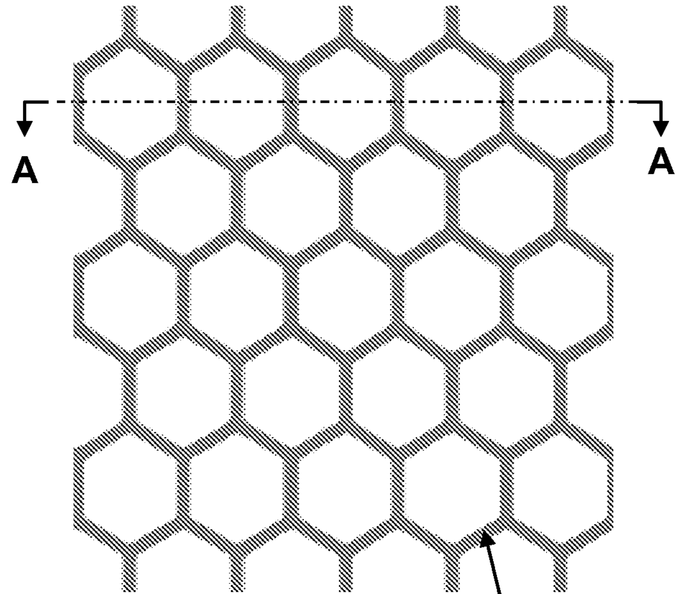

FIG 2A

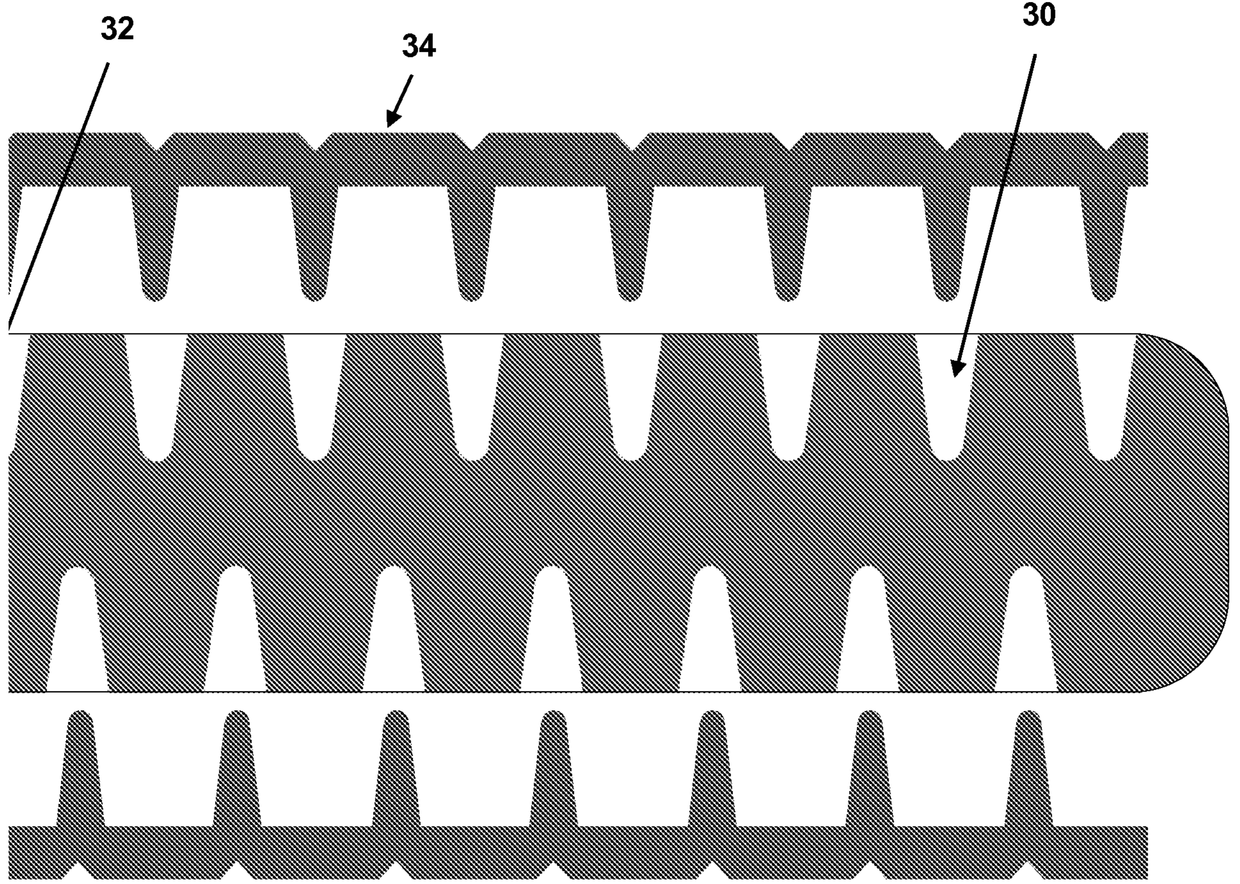

FIG 2B

FIG 3A

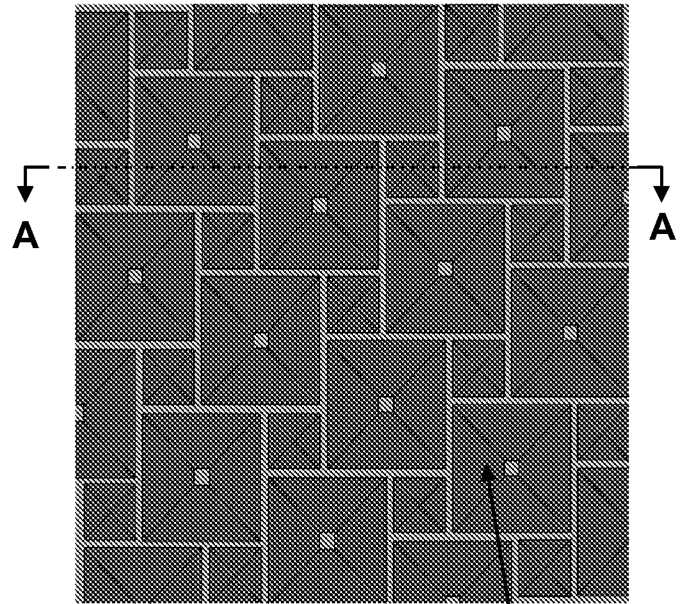

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FIG 3B

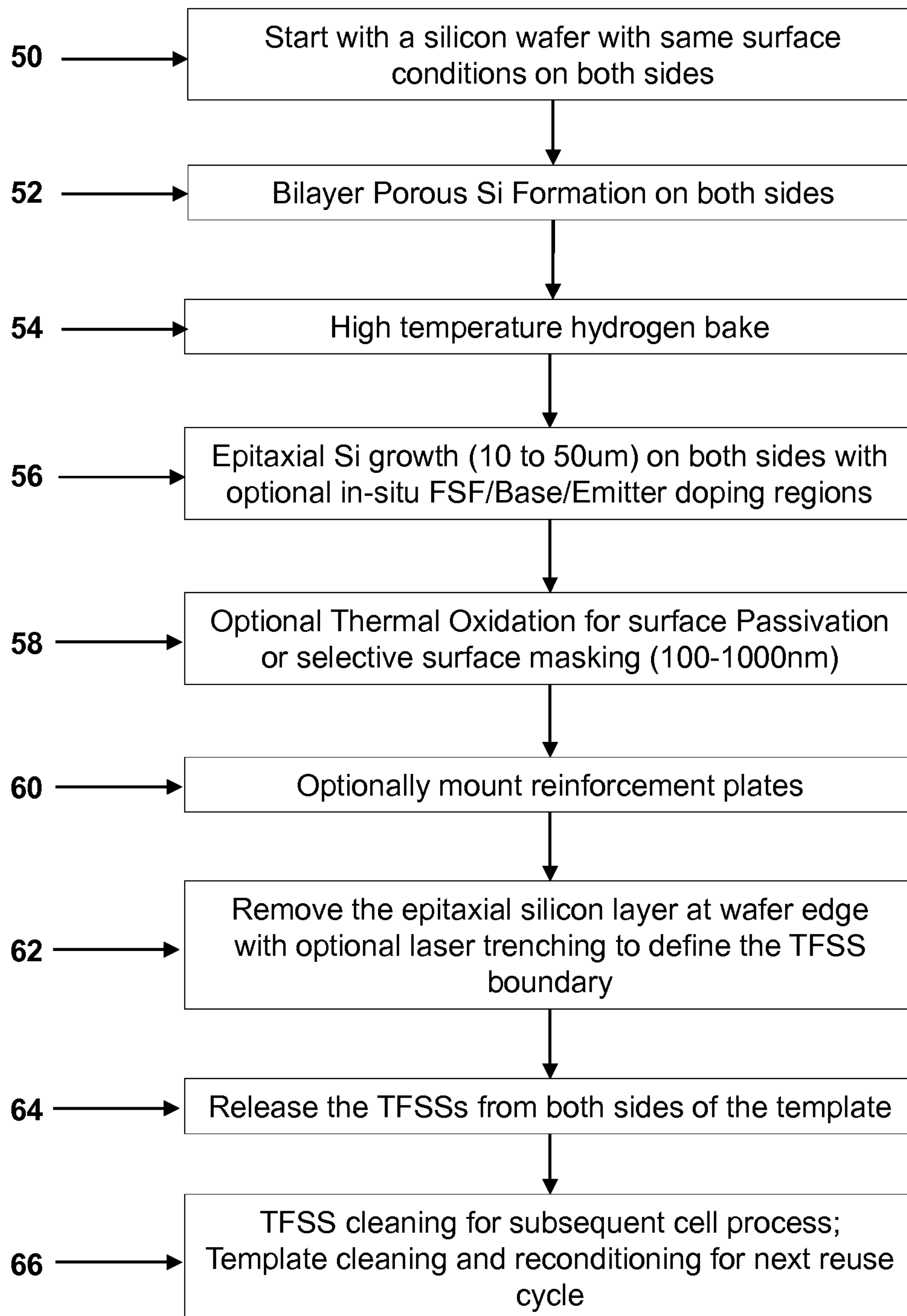


FIG 4

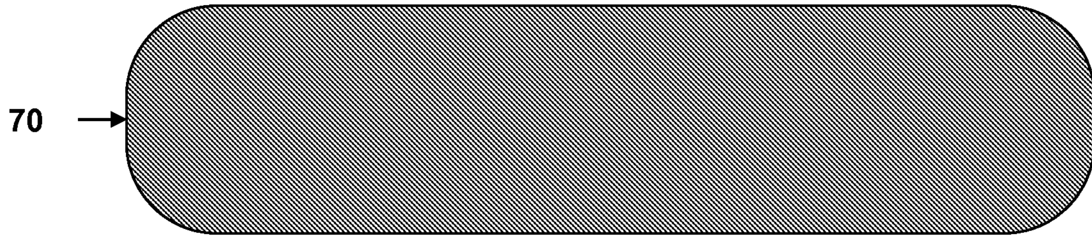


FIG 5A

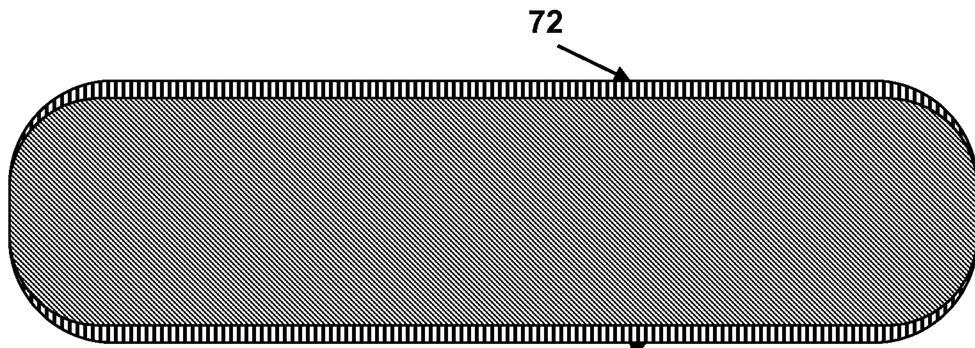


FIG 5B

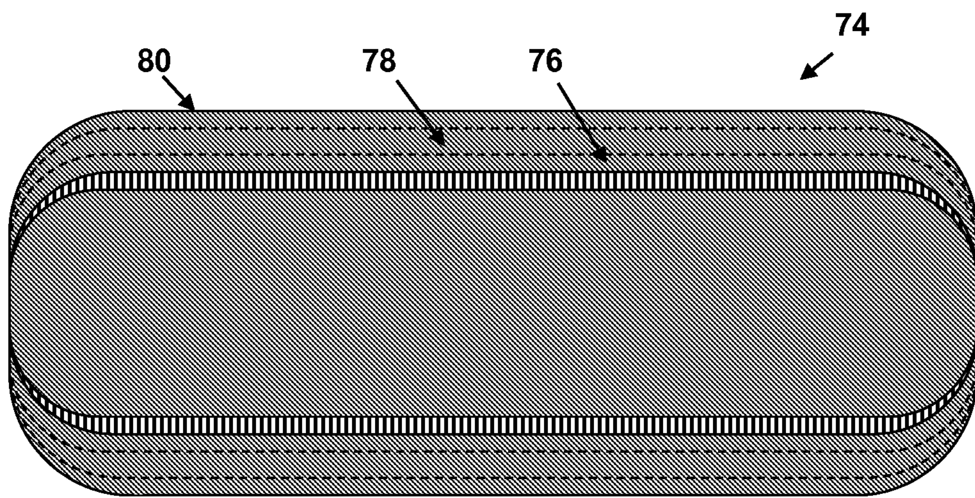


FIG 5C

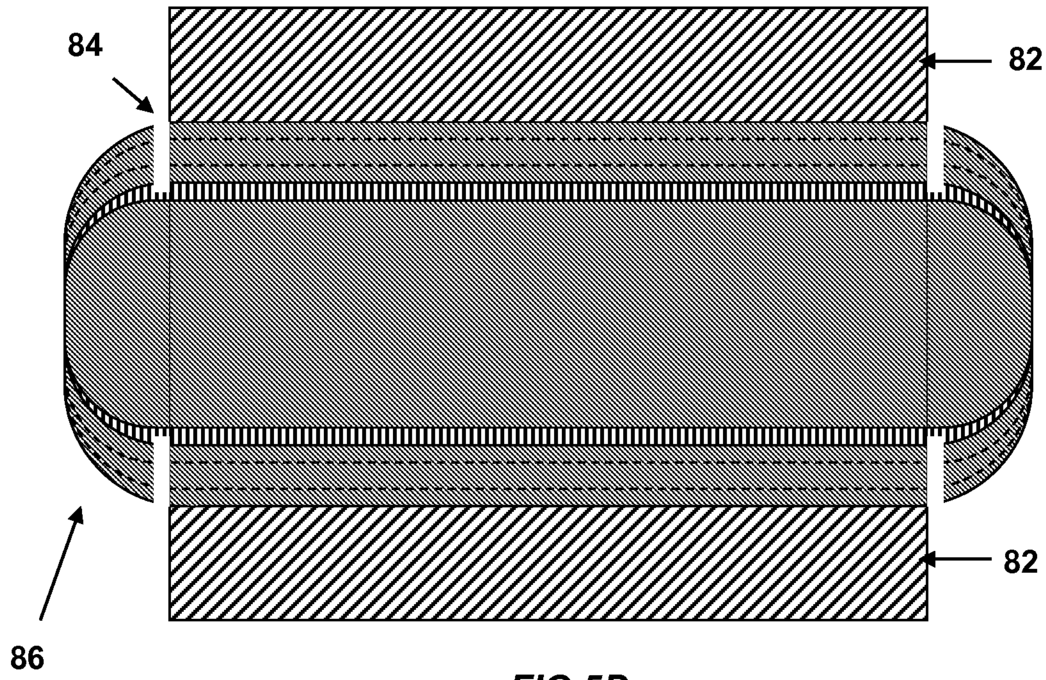


FIG 5D

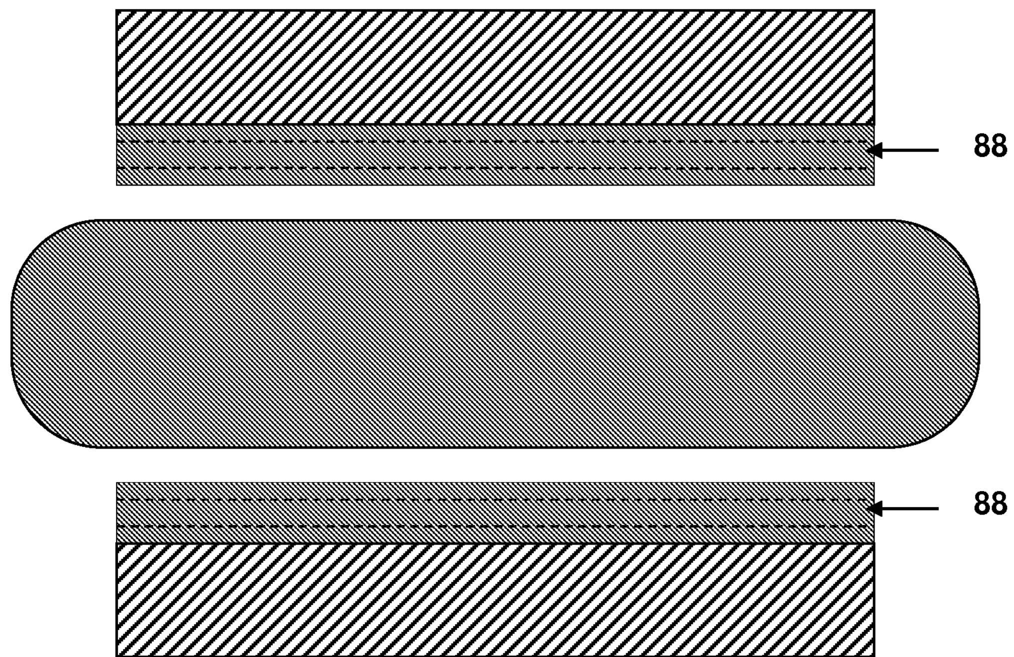


FIG 5E

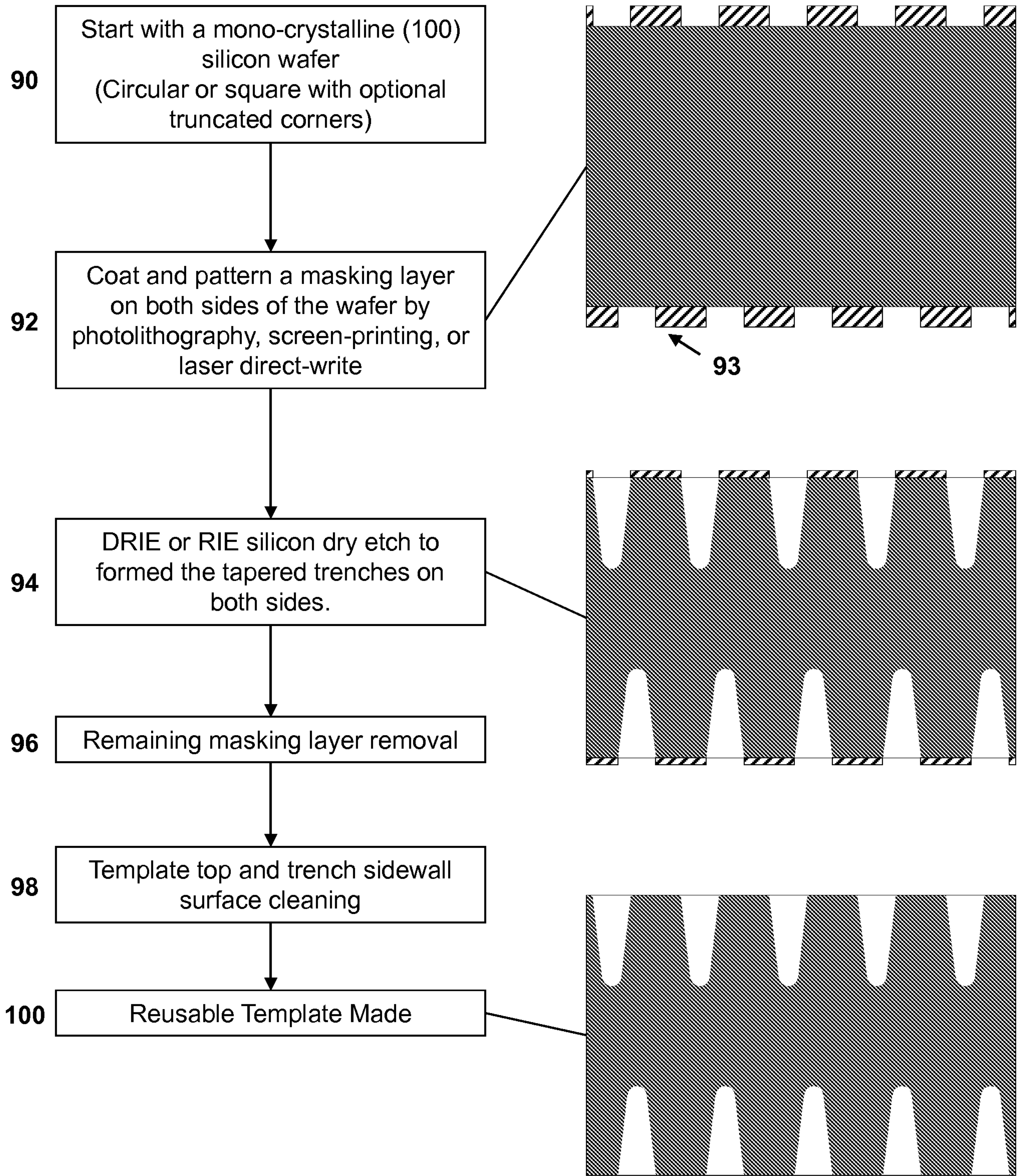
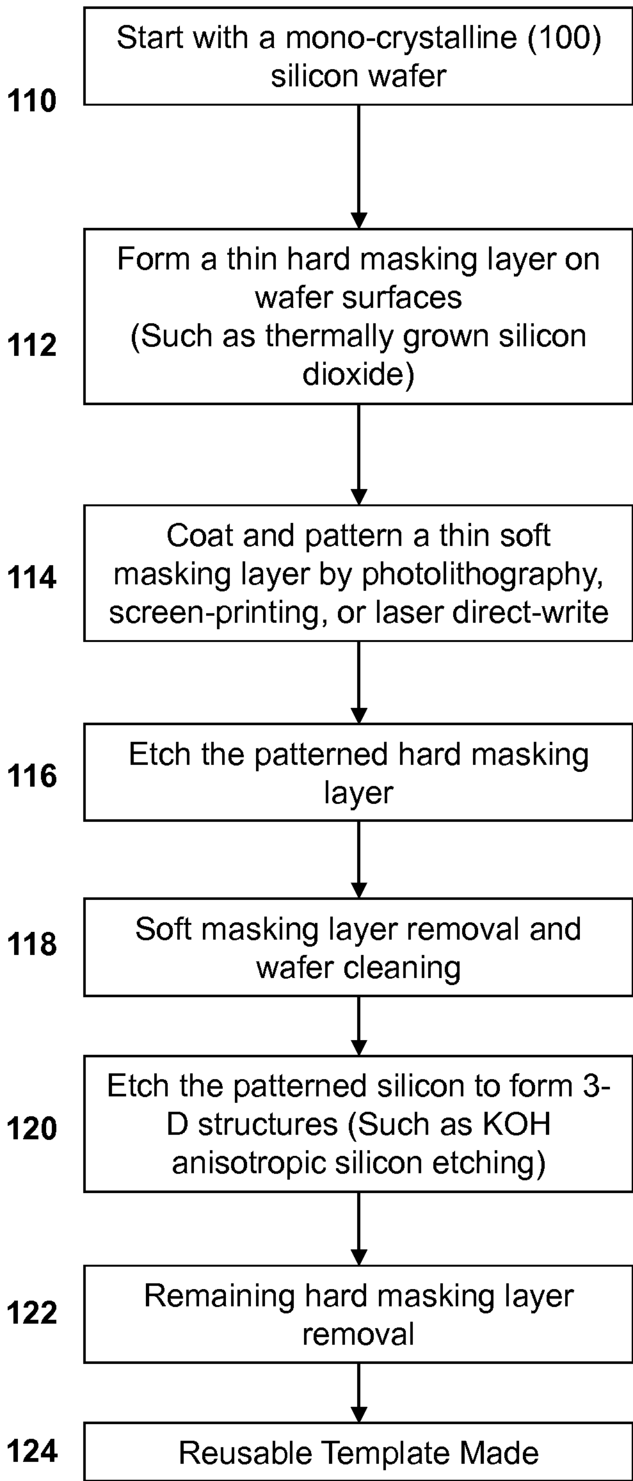


FIG 6



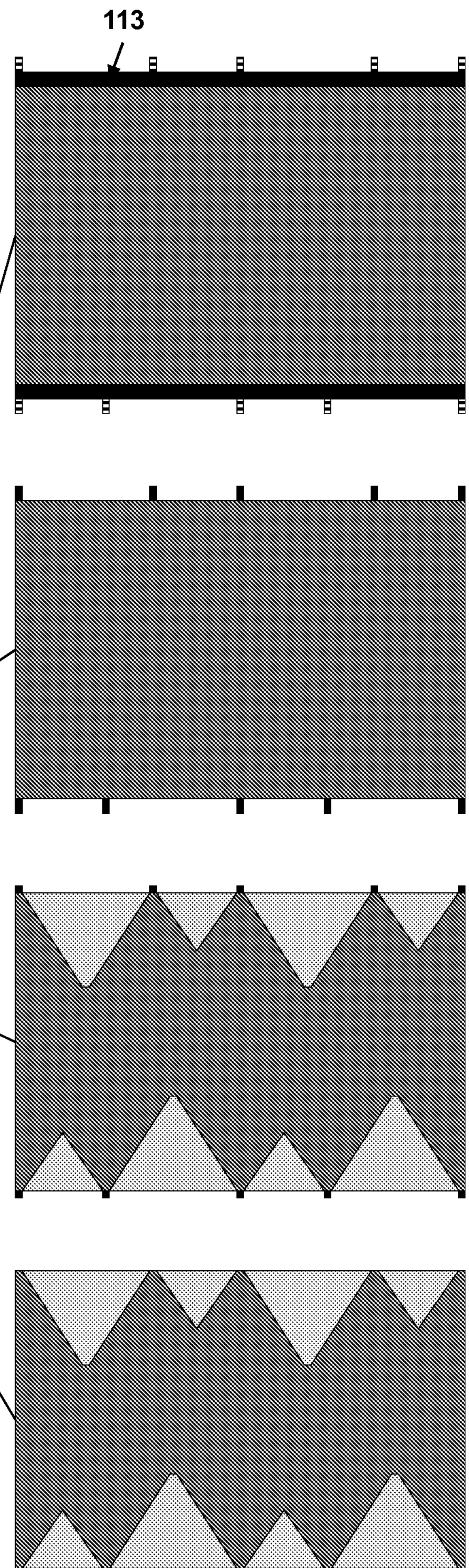


FIG 7

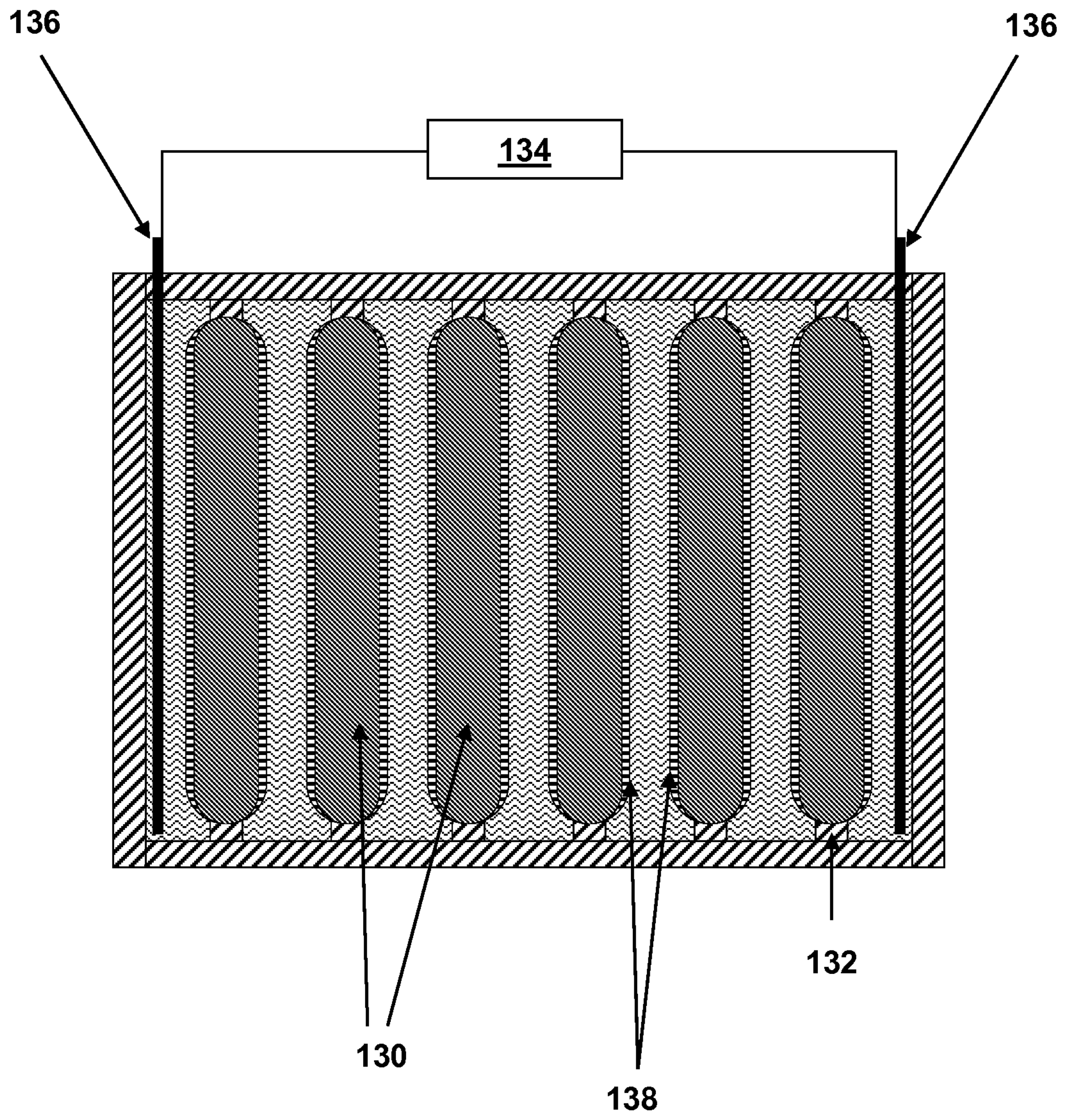


FIG 8

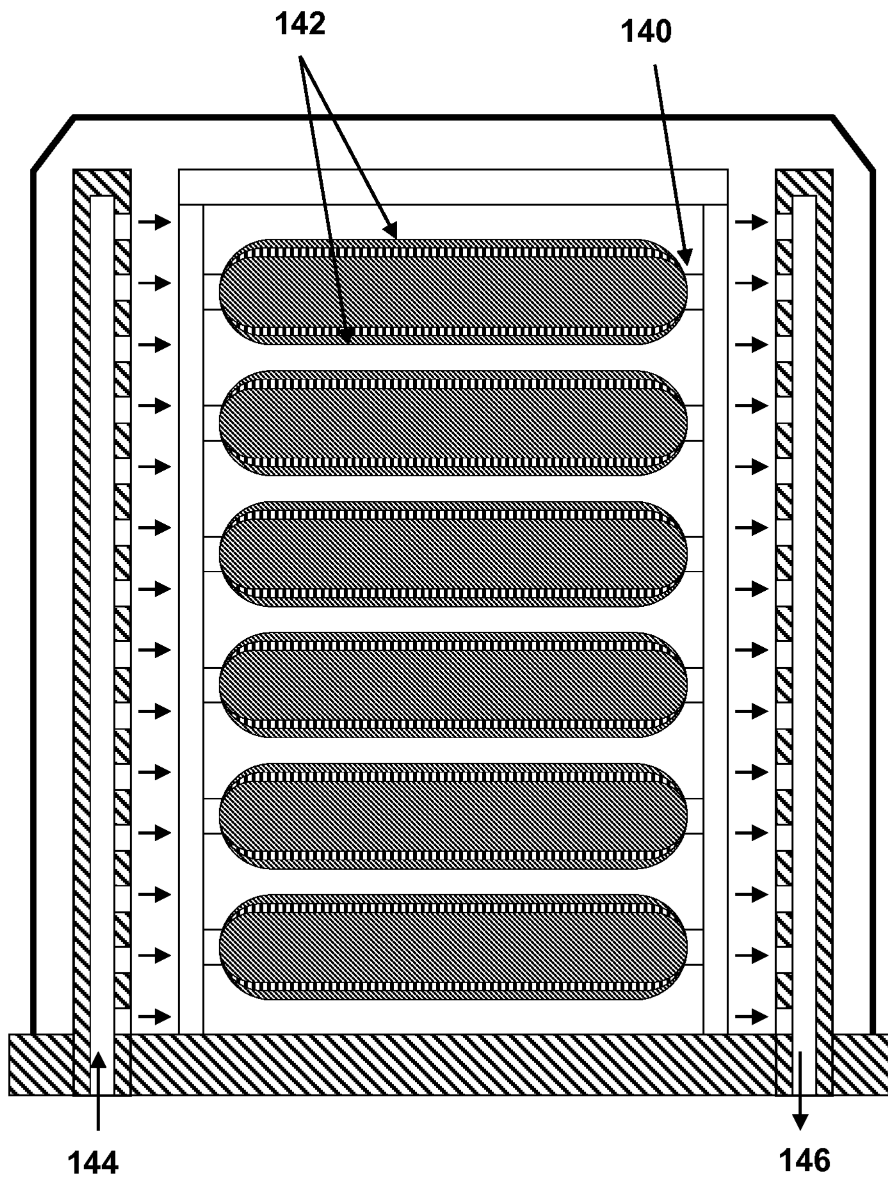


FIG 9