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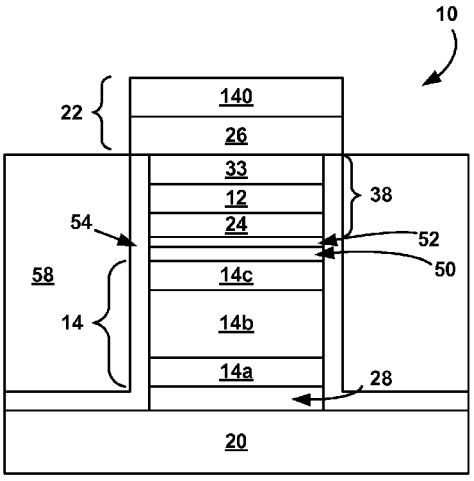

FIG. 3

(57) Abstract: In some aspects, a method of forming a reversible resistance-switch¬ ing metal-insulator-metal ("MIM") stack is provided, the method in¬ cluding: forming a first conducting layer (24) comprising a titani¬ um-rich titanium nitride (TiN) material having between about 50% Ti and about 95% Ti, forming a carbon nano-tube (CNT) material (12) above the first conducting layer, forming a second conducting layer (33) above the CNT material, and etching the first conducting layer, CNT material and second conducting layer to form the MIM stack. Nu merous other aspects are provided, amongst which an anneal step that results in the formation of a titanium carbide layer between the TiN layer (24) and the CNT layer (12).

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METHODS FOR INCREASING BOTTOM ELECTRODE PERFORMANCE IN CARBON- BASED MEMORY DEVICES, USING TITANIUM - RICH TITANIUM NITRIDE

REFERENCE TO RELATED APPLICATIONS

This application claims priority from U.S. Provisional Patent Application Serial No. 61/448,477, filed March 2, 2011, and U.S. Patent Application Serial No. 13/204,772, filed August 8, 2011, each of which is incorporated by reference herein in its entirety for all purposes.

BACKGROUND

This invention relates to non-volatile memories, and more particularly to methods for increasing bottom electrode performance in carbon-based memory devices.

Non-volatile memories formed from reversible resistance switching elements are known. For example, U.S. Patent Application Serial No. 11/968,154, filed December 31, 2007, titled "Memory Cell That Employs A Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element And Methods Of Forming The Same" (the "'154 Application"), which is hereby incorporated by reference herein in its entirety for all purposes, describes a rewriteable non-volatile memory cell

that includes a diode coupled in series with a carbon-based reversible resistivity switching material.

However, fabricating memory devices from carbon-based materials is technically challenging, and improved methods of forming memory devices that employ carbon-based materials are desirable.

SUMMARY

In a some aspects of the invention, a method of forming a reversible resistance-switching metal-insulator-metal ("MIM") stack is provided, the method including: (1) forming a first conducting layer comprising a titanium nitride material having between about 50% Ti and about 95% Ti; (2) forming a carbon nano-tube ("CNT") material above the first conducting layer; (3) forming a second conducting layer above the CNT material; and (4) etching the first conducting layer, CNT material and second conducting layer to form the MIM stack.

In some aspects of the invention, a method of forming a CNT memory cell is provided, the method including: (1) forming a first conductor; (2) forming a steering element above the first conductor; (3) forming a first conducting layer above the first conductor, wherein the first conducting layer comprises a titanium nitride material having between about 50% Ti and about 95% Ti; (4) forming a CNT material above the first conducting layer; (5) forming a second conducting layer above the CNT material; (6) etching the first conducting layer, CNT material and second conducting layer to form a MIM stack; and (7) forming a second conductor above the CNT material and the steering element.

In some aspects of the invention, a CNT memory cell is provided, the CNT memory cell including: (1) a first conductor; (2) a steering element above the first conductor; (3) a MIM stack including: (a) a first conducting layer above the first conductor, wherein the first conducting layer comprises a titanium nitride material having between about 50% Ti and about 95% Ti; (b) a CNT material above the first conducting layer; and (c) a second conducting layer above the CNT material; and (4) a second conductor above the CNT material and the steering element.

Other features and aspects of the present invention will become more fully apparent from the following detailed description, the appended claims and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Features of the present invention can be more clearly understood from the following detailed description considered in conjunction with the following drawings, in which the same reference numerals denote the same elements throughout, and in which:

FIG. 1 is a diagram of an example memory cell in accordance with this invention;

FIG. 2A is a simplified perspective view of an example memory cell in accordance with this invention;

FIG. 2B is a simplified perspective view of a portion of a first example memory level formed from a plurality of the memory cells of FIG. 2A;

FIG. 2C is a simplified perspective view of a portion of a first example three-dimensional memory array in accordance with this invention;

FIG. 2D is a simplified perspective view of a portion of a second example three-dimensional memory array in accordance with this invention;

FIG. 3 is a cross-sectional view of an example embodiment of a memory cell in accordance with this invention; and

FIGS. 4A-4F illustrate cross-sectional views of a portion of a substrate during an example fabrication of a single memory level in accordance with this invention.

DETAILED DESCRIPTION

Some CNT materials may exhibit resistivity switching properties that may be used to form microelectronic non-volatile memories. Such films therefore are candidates for integration within a three-dimensional memory array.

Indeed, CNT materials have demonstrated memory switching properties on lab-scale devices with a 100x separation between ON and OFF states and mid-to-high range resistance changes. Such a separation between ON and OFF states renders CNT materials viable candidates for memory cells in which the CNT material is coupled in series with vertical diodes, thin film transistors or other steering elements. For example, a MIM stack formed from a CNT material sandwiched between two metal or otherwise conducting layers (commonly referred to as top and bottom electrodes) may serve as a resistance-switching element for a memory cell.

In particular, a CNT MIM stack may be integrated in series with a diode or transistor to create a read-writable memory device as described, for example, in U.S. Patent Application Serial No. 11/968,154, filed December 31, 2007,

and titled "Memory Cell That Employs A Selectively Fabricated Carbon Nano-Tube Reversible Resistance-Switching Element And Methods Of Forming The Same," which is hereby incorporated by reference herein in its entirety for all purposes.

Manufacturing high-yield memory devices that include CNT MIM stacks has proven difficult. A CNT MIM stack is typically fabricated by forming a bottom electrode material, depositing CNT material on the bottom electrode material, and then forming a top electrode material above the CNT material. Some researchers have speculated that the bottom electrode material may be altered during the CNT deposition process. As a result of such alteration, the yield of the resulting memory devices may suffer.

In accordance with embodiments of the invention, a CNT MIM stack may be formed that includes a bottom electrode that includes a metal nitride, such as titanium nitride ("TiN"), tantalum nitride ("TaN"), hafnium nitride ("HfN"), zirconium nitride ("ZrN"), or other similar metal nitride.

In particular, in example embodiments, methods and apparatus in accordance with this invention form or include a CNT MIM bottom electrode that includes a metal-rich metal nitride layer, such as a titanium-rich TiN material layer, a tantalum-rich TaN material layer, a hafnium-rich HfN material layer, a zirconium-rich ZrN material layer, or other similar metal-rich metal nitride layer.

For simplicity, the term "α-rich αN" will be used herein to describe an α-nitride material, where "α" may be Ti, Ta, Hf, Zr, or other similar metal, and in which the "α" concentration is between about 50% α and about 95% α, more particularly between about 55% α and 75% α. The α-

rich αN material layer may encompass all or a part of the CNT MIM bottom electrode.

In other example embodiments, methods and apparatus in accordance with this invention form or include a CNT MIM that includes metal carbide contacts between the CNT material and the metal nitride bottom electrode. For example, the metal carbide contacts may include titanium carbide ("TiC"), tantalum carbide ("TaC"), hafnium carbide ("HfC"), zirconium carbide ("ZrC"), or other similar metal carbide contacts. For simplicity, the term "αC" will be used herein to describe an α-carbides, where "α" may be Ti, Ta, Hf, Zr, or other similar metal.

For instance, example methods in accordance with this invention may form a CNT MIM by depositing CNT material on an α-rich α-nitride bottom electrode, and subsequently performing an anneal at a temperature of about 700°C for about 5 to about 30 seconds to form αC contacts between the CNT material and the bottom electrode, where "α" may be Ti, Ta, Hf, Zr, or other similar metal. As used herein, the term "αC contact" means an αC material in which the carbon concentration is between about 1% C to about 60% C, more specifically between about 10% C to about 50% C.

For example, in a first example embodiment, a CNT-based MIM stack is formed by forming a first conducting layer comprising a titanium nitride material having between about 50% Ti and about 95% Ti, forming a CNT material above the first conducting layer, forming a second conducting layer above the CNT material, and etching the first conducting layer, CNT material and second conducting layer to form the MIM stack.

Although not wanting to be bound by any particular theory, it is believed that using a metal-rich metal

nitride (e.g., Ti-rich TiN, Ta-rich TaN, Hf-rich HfN, Zr-rich ZN, or other similar metal-rich metal nitride) bottom electrode may result in improved device yield and electrical performance. In embodiments in which α-rich αN is employed, after CNT deposition and further processing, the CNT-to-bottom electrode contact may be composed of $\alpha_x O_y C_z N_v$, where α may be Ti, Ta, Hf, Zr, or other similar metal, x+y+z+v = 1, and any one or two of the following can be zero: y, z, v. Additionally, it is believed that forming αC contacts may result in improved and reproducible electrical contact between the CNT and the bottom electrode. The αC can be initially formed with or without α-rich αN material.

These and other embodiments of the invention are described further below with reference to FIGS. 1-4G.

EXAMPLE INVENTIVE MEMORY CELL

FIG. 1 is a schematic illustration of an example memory cell 10 in accordance with an embodiment of this invention. Memory cell 10 includes a reversible resistance switching element 12 coupled to a steering element 14. Reversible resistance switching element 12 includes a reversible resistivity switching material (not separately shown) having a resistivity that may be reversibly switched between two or more states.

For example, the reversible resistivity switching material of element 12 may be in an initial, low-resistivity state upon fabrication. Upon application of a first voltage and/or current, the material is switchable to a high-resistivity state. Application of a second voltage and/or current may return the reversible resistivity switching material to a low-resistivity state.

Alternatively, reversible resistance switching element 12 may be in an initial, high-resistance state upon fabrication that is reversibly switchable to a low-resistance state upon application of the appropriate voltage(s) and/or current(s). When used in a memory cell, one resistance state may represent a binary "0," whereas another resistance state may represent a binary "1," although more than two data/resistance states may be used.

Numerous reversible resistivity switching materials and operation of memory cells employing reversible resistance switching elements are described, for example, in U.S. Patent Application Serial No. 11/125,939, filed May 9, 2005 and titled "Rewriteable Memory Cell Comprising A Diode And A Resistance Switching Material" (the "'939 Application"), which is hereby incorporated by reference herein in its entirety for all purposes.

Steering element 14 may include a thin film transistor, a diode, a metal-insulator-metal tunneling current device, or another similar steering element that exhibits non-ohmic conduction by selectively limiting the voltage across and/or the current flow through reversible resistance switching element 12. In this manner, memory cell 10 may be used as part of a two or three dimensional memory array and data may be written to and/or read from memory cell 10 without affecting the state of other memory cells in the array.

Example embodiments of memory cell 10, reversible resistance switching element 12 and steering element 14 are described below with reference to FIGS. 2A-2D and FIG. 3.

EXAMPLE EMBODIMENTS OF MEMORY CELLS AND MEMORY ARRAYS

FIG. 2A is a simplified perspective view of an example embodiment of a memory cell 10 in accordance with

an embodiment of this invention that includes a steering element 14 and a carbon-based reversible resistance switching element 12. Reversible resistance switching element 12 is coupled in series with steering element 14 between a first conductor 20 and a second conductor 22.

In some embodiments, a first conducting layer 24 may be formed between reversible resistance switching element 12 and steering element 14, a barrier layer 28 may be formed between steering element 14 and first conductor 20, and a second conducting layer 33 may be formed between reversible resistance switching element 12 and second conductor 22. Second conducting layer 33, and barrier layer 28 each may include titanium, TiN, tantalum, TaN, tungsten, tungsten nitride ("WN"), molybdenum or another similar material. In accordance with this invention, and as described in more detail below, first conducting layer 24 includes an α-rich αN material in contact with carbon-based reversible resistance switching element 12, where α may be Ti, Ta, Hf, Zr, or other similar metal.

First conducting layer 24, reversible resistance switching element 12 and second conducting layer 33 may form a MIM stack 38 in series with steering element 14, with first conducting layer 24 forming a bottom electrode, and second conducting layer 33 forming a top electrode of MIM stack 38. For simplicity, first conducting layer 24 and second conducting layer 33 will be referred to in the remaining discussion as "bottom electrode 24" and "top electrode 33," respectively. In some embodiments, reversible resistance switching element 12 and/or MIM stack 38 may be positioned below steering element 14.

As discussed above, steering element 14 may include a thin film transistor, a diode, a metal-insulator-metal

tunneling current device, or another similar steering element that exhibits non-ohmic conduction by selectively limiting the voltage across and/or the current flow through reversible resistance switching element 12. In the example of FIG. 2A, steering element 14 is a diode. Accordingly, steering element 14 is sometimes referred to herein as "diode 14."

Diode 14 may include any suitable diode such as a vertical polycrystalline p-n or p-i-n diode, whether upward pointing with an n-region above a p-region of the diode or downward pointing with a p-region above an n-region of the diode. For example, diode 14 may include a heavily doped n+ polysilicon region 14a, a lightly doped or an intrinsic (unintentionally doped) polysilicon region 14b above the n+ polysilicon region 14a, and a heavily doped p+ polysilicon region 14c above intrinsic region 14b. It will be understood that the locations of the n+ and p+ regions may be reversed. Example embodiments of diode 14 are described below with reference to FIG. 3.

Reversible resistance switching element 12 may include a carbon-based material (not separately shown) having a resistivity that may be reversibly switched between two or more states. For example, reversible resistance switching element 12 may include a CNT material or other similar carbon-based material. For simplicity, reversible resistance switching element 12 will be referred to in the remaining discussion as "CNT element 12."

First conductor 20 and/or second conductor 22 may include any suitable conductive material such as tungsten, any appropriate metal, heavily doped semiconductor material, a conductive silicide, a conductive silicide-germanide, a conductive germanide, or the like. In the embodiment of FIG. 2A, first and second conductors 20

and 22, respectively, are rail-shaped and extend in different directions (e.g., substantially perpendicular to one another). Other conductor shapes and/or configurations may be used. In some embodiments, barrier layers, adhesion layers, antireflection coatings and/or the like (not shown) may be used with the first conductor 20 and/or second conductor 22 to improve device performance and/or aid in device fabrication.

FIG. 2B is a simplified perspective view of a portion of a first memory level 30 formed from a plurality of memory cells 10, such as memory cell 10 of FIG. 2A. For simplicity, MIM 38, diode 14, and barrier layer 28 are not separately shown. Memory level 30 is a "cross-point" array including a plurality of bit lines (second conductors 22) and word lines (first conductors 20) to which multiple memory cells are coupled (as shown). Other memory array configurations may be used, as may multiple levels of memory.

For example, FIG. 2C is a simplified perspective view of a portion of a monolithic three dimensional array 40a that includes a first memory level 42 positioned below a second memory level 44. Memory levels 42 and 44 each include a plurality of memory cells 10 in a cross-point array. Persons of ordinary skill in the art will understand that additional layers (e.g., an interlevel dielectric) may be present between the first and second memory levels 42 and 44, but are not shown in FIG. 2C for simplicity. Other memory array configurations may be used, as may additional levels of memory. In the embodiment of FIG. 2C, all diodes may "point" in the same direction, such as upward or downward depending on whether p-i-n diodes having a p-doped region on the bottom or top of the diodes are employed, simplifying diode fabrication.

In some embodiments, the memory levels may be formed as described in U.S. Patent No. 6,952,030, titled "High-Density Three-Dimensional Memory Cell" which is hereby incorporated by reference herein in its entirety for all purposes. For instance, the upper conductors of a first memory level may be used as the lower conductors of a second memory level that is positioned above the first memory level as shown in the alternative example three dimensional memory array 40b illustrated in FIG. 2D.

In such embodiments, the diodes on adjacent memory levels preferably point in opposite directions as described in U.S. Patent Application Serial No. 11/692,151, filed March 27, 2007, and titled "Large Array Of Upward Pointing P-I-N Diodes Having Large And Uniform Current" (hereinafter "the '151 Application"), which is hereby incorporated by reference herein in its entirety for all purposes.

For example, as shown in FIG. 2D, the diodes of the first memory level 42 may be upward pointing diodes as indicated by arrow D1 (e.g., with p regions at the bottom of the diodes), whereas the diodes of the second memory level 44 may be downward pointing diodes as indicated by arrow D2 (e.g., with n regions at the bottom of the diodes), or vice versa.

A monolithic three dimensional memory array is one in which multiple memory levels are formed above a single substrate, such as a wafer, with no intervening substrates. The layers forming one memory level are deposited or grown directly over the layers of an existing level or levels. In contrast, stacked memories have been constructed by forming memory levels on separate substrates and adhering the memory levels atop each other, as in Leedy, U.S. Patent No. 5,915,167, titled "Three Dimensional Structure Memory." The substrates may be thinned or removed from the memory

levels before bonding, but as the memory levels are initially formed over separate substrates, such memories are not true monolithic three dimensional memory arrays.

In some embodiments, a resistivity of the CNT material used to form CNT element 12 is at least $1x10^{1}$ ohm cm when CNT element 12 is in an ON-state, whereas a resistivity of the CNT material used to form CNT element 12 is at least $1x10^{3}$ ohm-cm when CNT element 12 is in an OFF-state. Other resistivities may be used.

FIG. 3 is a cross-sectional view of an example embodiment of memory cell 10 of FIG. 1. In particular, FIG. 3 shows an example memory cell 10 which includes CNT element 12, diode 14, and first and second conductors 20 and 22, respectively. Memory cell 10 may also include bottom electrode 24, barrier layer 28, top electrode 33, a silicide layer 50, a silicide-forming metal layer 52, and dielectric layer 58, as well as adhesion layers, antireflective coating layers and/or the like (not shown) which may be used with first and/or second conductors 20 and 22, respectively, to improve device performance and/or facilitate device fabrication. In some embodiments, a sidewall liner 54 may be used to separate selected layers of memory cell 10 from dielectric layer 58.

In FIG. 3, diode 14 may be a vertical p-n or p-i-n diode, which may either point upward or downward. In the embodiment of FIG. 2D in which adjacent memory levels share conductors, adjacent memory levels preferably have diodes that point in opposite directions such as downward-pointing p-i-n diodes for a first memory level and upward-pointing p-i-n diodes for an adjacent, second memory level (or vice versa).

In some embodiments, diode 14 may be formed from a polycrystalline semiconductor material such as polysilicon,

a polycrystalline silicon-germanium alloy, polygermanium or any other suitable material. For example, diode 14 may include a heavily doped n+ polysilicon region 14a, a lightly doped or an intrinsic (unintentionally doped) polysilicon region 14b above the n+ polysilicon region 14a, and a heavily doped p+ polysilicon region 14c above intrinsic region 14b. It will be understood that the locations of the n+ and p+ regions may be reversed.

In some embodiments, a thin germanium and/or silicon-germanium alloy layer (not shown) may be formed on n+ polysilicon region 14a to prevent and/or reduce dopant migration from n+ polysilicon region 14a into intrinsic region 14b. Use of such a layer is described, for example, in U.S. Patent Application Serial No. 11/298,331, filed December 9, 2005 and titled "Deposited Semiconductor Structure To Minimize N-Type Dopant Diffusion And Method Of Making" (hereinafter "the '331 Application"), which is hereby incorporated by reference herein in its entirety for all purposes. In some embodiments, a few hundred angstroms or less of silicon-germanium alloy with about 10 at% or more of germanium may be employed.

Barrier layer 28, such as titanium, TiN, tantalum, TaN, tungsten, WN, molybdenum, etc., may be formed between the first conductor 20 and the n+ region 14a (e.g., to prevent and/or reduce migration of metal atoms into the polysilicon regions).

If diode 14 is fabricated from deposited silicon (e.g., amorphous or polycrystalline), a silicide layer 50 may be formed on diode 14 to place the deposited silicon in a low resistivity state, as fabricated. Such a low resistivity state allows for easier programming of memory cell 10 as a large voltage is not required to switch the deposited silicon to a low resistivity state.

For example, a silicide-forming metal layer 52 such as titanium or cobalt may be deposited on p+ polysilicon region 14c. During a subsequent anneal step (described below), silicide-forming metal layer 52 and the deposited silicon of diode 14 interact to form silicide layer 50, consuming all or a portion of the silicide-forming metal layer 52. In some embodiments, a nitride layer (not shown) may be formed at a top surface of silicide-forming metal layer 52. For example, if silicide-forming metal layer 52 is titanium, a TiN layer may be formed at a top surface of silicide-forming metal layer 52.

A rapid thermal anneal ("RTA") step may then be performed to form silicide regions by reaction of silicide-forming metal layer 52 with p+ region 14c. The RTA may be performed at about 540°C for about 1 minute, and causes silicide-forming metal layer 52 and the deposited silicon of diode 14 to interact to form silicide layer 50, consuming all or a portion of the silicide-forming metal layer 52. An additional, higher temperature anneal (e.g., such as at about 750°C as described below) may be used to crystallize the diode.

As described in U.S. Patent No. 7,176,064, titled "Memory Cell Comprising A Semiconductor Junction Diode Crystallized Adjacent To A Silicide," which is hereby incorporated by reference herein in its entirety for all purposes, silicide-forming materials such as titanium and/or cobalt react with deposited silicon during annealing to form a silicide layer. The lattice spacings of titanium silicide and cobalt silicide are close to that of silicon, and it appears that such silicide layers may serve as "crystallization templates" or "seeds" for adjacent deposited silicon as the deposited silicon crystallizes (e.g., the silicide layer enhances the crystalline

structure of the diode 14 during annealing). Lower resistivity silicon thereby is provided. Similar results may be achieved for silicon-germanium alloy and/or germanium diodes.

In embodiments in which a nitride layer was formed at a top surface of silicide-forming metal layer 52, following the RTA step, the nitride layer may be stripped using a wet chemistry. For example, if silicide-forming metal layer 52 includes a TiN top layer, a wet chemistry (e.g., ammonium, peroxide, water in a 1:1:1 ratio) may be used to strip any residual TiN. In some embodiments, the nitride layer formed at a top surface of silicide-forming metal layer 52 may remain, or may not be used at all.

Bottom electrode 24 is formed above metal-forming silicide layer 52. In some embodiments, bottom electrode 24 may have a thickness of about 10 to 2000 angstroms, although other thicknesses may be used. In some embodiments, bottom electrode 24 may be an αN layer, where α is Ti, Ta, Hf, Zr, or other similar metal. For example, the inventors have found that using an α-rich αN bottom electrode 24 may significantly increase device yield. As described above, as used herein, α-rich αN means an αN material in which the α concentration is between about 50% α and about 95% α, more particularly between about 55% α and 75% α, where α is Ti, Ta, Hf, Zr, or other similar metal.

For simplicity, the remaining description will describe a Ti-rich TiN bottom electrode 24. Persons of ordinary skill in the art will understand that bottom electrode 24 alternatively may be a Ta-rich TaN, Hf-rich HfN, Zr-rich ZrN, or other similar metal-rich metal nitride layer.

Persons of ordinary skill in the art will understand that bottom electrode 24 may entirely include Ti-rich TiN material, or only a portion of bottom electrode 24 may include Ti-rich TiN material. For example, bottom electrode 24 may include a layer a Ti-rich TiN material layer above a layer of TiN, tungsten, tungsten nitride, or other conductor material. The Ti-rich TiN layer may have a thickness of between about 2 angstroms to about 500 angstroms. In such instances, bottom electrode 24 is oriented so that the Ti-rich TiN layer contacts CNT element 12.

Ti-rich TiN bottom electrode 24 may be formed by any suitable process, such as physical vapor deposition ("PVD"), chemical vapor deposition ("CVD"), plasma-enhanced CVD ("PECVD"), sputter deposition, atomic layer deposition ("ALD"), or other similar process.

Table 1, below, includes example Ti-rich TiN PVD deposition process conditions:

TABLE 1: EXAMPLE TI-RICH TIN PVD DEPOSITION PARAMETERS

PROCESS PARAMETER	EXAMPLE RANGE	PREFERRED RANGE
Argon Flow Rate (sccm)	20-40	20-30
Ar With Dilute H_2 (<10%) Flow Rate (sccm)	0-30	0-10
Nitrogen Flow Rate (sccm)	5-65	10-50
Pressure (milliTorr)	1-5000	1800-2400
Power (Watts)	10-9000	2000-9000
Power Ramp Rate (Watts/sec)	10-5000	2000-5000
Process Temperature (°C)	100-600	200-350
Deposition Time (sec)	5-200	10-150

Other flow rates, pressures, powers, power ramp rates, process temperatures and/or deposition times may be used.

For example, Table 2, below, includes alternative example Ti-rich TiN PVD deposition process conditions:

TABLE 2: EXAMPLE TI-RICH TIN PVD DEPOSITION PARAMETERS

PROCESS PARAMETER	EXAMPLE RANGE	PREFERRED RANGE
Argon Flow Rate (sccm)	10 - 100	10 - 70
Ar With Dilute H_2 (<10%) Flow Rate (sccm)	0 - 30	1 - 10
Nitrogen Flow Rate (sccm)	5-25	5-15
Pressure (milliTorr)	1 - 5000	1 - 100
Power (Watts)	10-9000	2000-6000
Power Ramp Rate (Watts/sec)	10 - 5000	1000 - 4000
Process Temperature (°C)	15-30	20-25
Deposition Time (sec)	1 - 400	1 - 30

Other flow rates, pressures, powers, power ramp rates, process temperatures and/or deposition times may be used.

Example deposition chambers include the Endura 2 tool available from Applied Materials, Inc. of Santa Clara, CA. Other processing tools may be used. In some embodiments, a buffer chamber pressure of about $1\text{-}2\times10^{-7}$ Torr and a transfer chamber pressure of about $2\text{-}5\times10^{-8}$ Torr may be used. The deposition chamber may be stabilized for about 250-350 seconds with about 60-80 sccm Ar, 60-70 sccm N_2, and about 5-10 sccm of Ar with dilute H_2 at about 1800-2400 milliTorr. In some embodiments, it may take about 2-5 seconds to strike the target. Other buffer

chamber pressures, transfer chamber pressures and/or deposition chamber stabilization parameters may be used.

CNT element 12 is formed above Ti-rich TiN bottom electrode 24 by depositing or otherwise forming a layer of CNT material. CNT material may be formed over Ti-rich TiN bottom electrode 24 using any suitable CNT formation process. One technique involves spray- or spin-coating a carbon nanotube suspension over Ti-rich TiN bottom electrode 24, thereby creating a random CNT material. Another technique involves growing carbon nanotubes from a seed anchored to the substrate by CVD, PECVD or the like.

Discussions of various CNT deposition techniques are found in related applications, hereby incorporated by reference herein in their entireties, U.S. Patent Application Serial No. 11/968,154, "Memory Cell That Employs A Selectively Fabricated Carbon Nano-Tube Reversible Resistance-Switching Element And Methods Of Forming The Same;" U.S. Patent Application Serial No. 11/968,156, "Memory Cell That Employs A Selectively Fabricated Carbon Nano-Tube Reversible Resistance-Switching Element Formed Over A Bottom Conductor And Methods Of Forming The Same;" and U.S. Patent Application Serial No. 11/968,159, "Memory Cell With Planarized Carbon Nanotube Layer And Methods Of Forming The Same."

Any suitable thickness may be employed for the CNT material of CNT element 12. In one embodiment, a CNT material thickness of about 100 to about 1000, and more preferably about 400-600 angstroms, may be used.

An anneal step may then be performed to form TiC contacts between CNT element 12 and Ti-rich TiN bottom electrode 24 by reaction of CNT element 12 with Ti-rich TiN bottom electrode 24. The anneal may be performed at about 700°C for about 5 to about 30 seconds, and may cause

CNT element 12 and Ti-rich TiN bottom electrode 24 to interact to form TiC contacts between CNT element 12 and Ti-rich TiN bottom electrode 24. Persons of ordinary sill in the art will understand that higher temperatures close to the TiC phase transformation, such as 800 to 900°C can be used as well.

Because all of the CNT material in CNT element 12 does not make contact with Ti-rich TiN bottom electrode 24, persons of ordinary skill in the art will understand that there may be a localized variance in composition. Thus, as described above, as used herein, "TiC contact" means a TiC material in which the carbon concentration is between about 1% C to about 60% C, more specifically between about 10% C to about 50% C.

Persons of ordinary skill in the art will understand that a subsequent, higher temperature anneal (e.g., such as at about 750°C as described below) alternatively may be used to form TiC contacts between CNT element 12 and Ti-rich TiN bottom electrode 24.

Top electrode 33, such as titanium, TiN, tantalum, TaN, tungsten, WN, molybdenum, etc., is formed above CNT element 12. In some embodiments, top electrode 33 may be TiN with a thickness of about 100 to 2000 angstroms, although other materials and/or thicknesses may be used.

Memory cell 10 also includes a sidewall liner 54 formed along the sides of the memory cell layers. Liner 54 may be formed using a dielectric material, such as boron nitride, silicon nitride, silicon oxynitride, low K dielectrics, etc. Example low K dielectrics include carbon doped oxides, silicon carbon layers, or the like.

In some embodiments, the CNT element 12 may be positioned below diode 14.

EXAMPLE FABRICATION PROCESSES FOR MEMORY CELLS

Referring now to FIGS. 4A-4F, a first example method of forming a memory level in accordance with this invention is described. In particular, FIGS. 4A-4F illustrate an example method of forming a memory level including memory cells 10 of FIG. 3. As will be described below, the first memory level includes a plurality of memory cells that each include a steering element and a carbon-based (e.g., CNT) reversible resistance switching element coupled to the steering element. Additional memory levels may be fabricated above the first memory level (as described previously with reference to FIGS. 2C-2D).

With reference to FIG. 4A, substrate 100 is shown as having already undergone several processing steps. Substrate 100 may be any suitable substrate such as a silicon, germanium, silicon-germanium, undoped, doped, bulk, silicon-on-insulator ("SOI") or other substrate with or without additional circuitry. For example, substrate 100 may include one or more n-well or p-well regions (not shown).

Isolation layer 102 is formed above substrate 100. In some embodiments, isolation layer 102 may be a layer of silicon dioxide, silicon nitride, silicon oxynitride or any other suitable insulating layer.

Following formation of isolation layer 102, an adhesion layer 104 is formed over isolation layer 102 (e.g., by physical vapor deposition or another method). For example, adhesion layer 104 may be about 20 to about 500 angstroms, and preferably about 100 angstroms, of titanium nitride or another suitable adhesion layer such as tantalum nitride, tungsten nitride, tungsten, molybdenum, combinations of one or more adhesion layers, or the like. Other adhesion layer materials and/or thicknesses may be

employed. In some embodiments, adhesion layer 104 may be optional.

After formation of adhesion layer 104, a conductive layer 106 is deposited over adhesion layer 104. Conductive layer 106 may include any suitable conductive material such as tungsten or another appropriate metal, heavily doped semiconductor material, a conductive silicide, a conductive silicide-germanide, a conductive germanide, or the like deposited by any suitable method (e.g., CVD, PVD, etc.). In at least one embodiment, conductive layer 106 may comprise about 200 to about 2500 angstroms of tungsten. Other conductive layer materials and/or thicknesses may be used.

Following formation of conductive layer 106, adhesion layer 104 and conductive layer 106 are patterned and etched. For example, adhesion layer 104 and conductive layer 106 may be patterned and etched using conventional lithography techniques, with a soft or hard mask, and wet or dry etch processing. In at least one embodiment, adhesion layer 104 and conductive layer 106 are patterned and etched to form substantially parallel, substantially co-planar first conductors 20. Example widths for first conductors 20 and/or spacings between first conductors 20 range from about 200 to about 2500 angstroms, although other conductor widths and/or spacings may be used.

After first conductors 20 have been formed, a dielectric layer 58a is formed over substrate 100 to fill the voids between first conductors 20. For example, approximately 3000-7000 angstroms of silicon dioxide may be deposited on the substrate 100 and planarized using chemical mechanical polishing or an etchback process to form a planar surface 110. Planar surface 110 includes exposed top surfaces of first conductors 20 separated by

dielectric material (as shown). Other dielectric materials such as silicon nitride, silicon oxynitride, low K dielectrics, etc., and/or other dielectric layer thicknesses may be used. Example low K dielectrics include carbon doped oxides, silicon carbon layers, or the like.

In other embodiments of the invention, first conductors 20 may be formed using a damascene process in which dielectric layer 58a is formed, patterned and etched to create openings or voids for first conductors 20. The openings or voids then may be filled with adhesion layer 104 and conductive layer 106 (and/or a conductive seed, conductive fill and/or barrier layer if needed). Adhesion layer 104 and conductive layer 106 then may be planarized to form planar surface 110. In such an embodiment, adhesion layer 104 will line the bottom and sidewalls of each opening or void.

Following planarization, the diode structures of each memory cell are formed. With reference to FIG. 4B, a barrier layer 28 is formed over planarized top surface 110 of substrate 100. In some embodiments, barrier layer 28 may be about 20 to about 500 angstroms, and preferably about 100 angstroms, of titanium nitride or another suitable barrier layer such as tantalum nitride, tungsten nitride, tungsten, molybdenum, combinations of one or more barrier layers, barrier layers in combination with other layers such as titanium/titanium nitride, tantalum/tantalum nitride or tungsten/tungsten nitride stacks, or the like. Other barrier layer materials and/or thicknesses may be employed.

After deposition of barrier layer 28, deposition of the semiconductor material used to form the diode of each memory cell begins (e.g., diode 14 in FIGS. 1 and 3). Each diode may be a vertical p-n or p-i-n diode as

previously described. In some embodiments, each diode is formed from a polycrystalline semiconductor material such as polysilicon, a polycrystalline silicon-germanium alloy, polygermanium or any other suitable material. For convenience, formation of a polysilicon, downward-pointing diode is described herein. It will be understood that other materials and/or diode configurations may be used.

With reference to FIG. 4B, following formation of barrier layer 28, a heavily doped n+ silicon layer 14a is deposited on barrier layer 28. In some embodiments, n+ silicon layer 14a is in an amorphous state as deposited. In other embodiments, n+ silicon layer 14a is in a polycrystalline state as deposited. CVD or another suitable process may be employed to deposit n+ silicon layer 14a. In at least one embodiment, n+ silicon layer 14a may be formed, for example, from about 100 to about 1000 angstroms, preferably about 100 angstroms, of phosphorus or arsenic doped silicon having a doping concentration of about 10^{21} cm^{-3}. Other layer thicknesses, doping types and/or doping concentrations may be used. N+ silicon layer 14a may be doped in situ, for example, by flowing a donor gas during deposition. Other doping methods may be used (e.g., implantation).

After deposition of n+ silicon layer 14a, a lightly doped, intrinsic and/or unintentionally doped silicon layer 14b may be formed over n+ silicon layer 14a. In some embodiments, intrinsic silicon layer 14b may be in an amorphous state as deposited. In other embodiments, intrinsic silicon layer 14b may be in a polycrystalline state as deposited. CVD or another suitable deposition method may be employed to deposit intrinsic silicon layer 14b. In at least one embodiment, intrinsic silicon layer 14b may be about 300 to about 4800 angstroms,

preferably about 2500 angstroms, in thickness. Other intrinsic layer thicknesses may be used.

A thin (e.g., a few hundred angstroms or less) germanium and/or silicon-germanium alloy layer (not shown) may be formed on n+ silicon layer 14a prior to depositing intrinsic silicon layer 14b to prevent and/or reduce dopant migration from n+ silicon layer 14a into intrinsic silicon layer 14b (as described in the '331 Application).

P-type silicon may be either deposited and doped by ion implantation or may be doped in situ during deposition to form a p+ silicon layer 14c. For example, a blanket p+ implant may be employed to implant boron a predetermined depth within intrinsic silicon layer 14b. Example implantable molecular ions include BF_2, BF_3, B and the like. In some embodiments, an implant dose of about $1\text{-}5x10^{15}$ ions/cm^2 may be employed. Other implant species and/or doses may be used. Further, in some embodiments, a diffusion process may be employed. In at least one embodiment, the resultant p+ silicon layer 14c has a thickness of about 100-700 angstroms, although other p+ silicon layer sizes may be used.

Following formation of p+ silicon layer 14c, a silicide-forming metal layer 52 is deposited over p+ silicon layer 14c. Example silicide-forming metals include sputter or otherwise deposited titanium or cobalt. In some embodiments, silicide-forming metal layer 52 has a thickness of about 10 to about 200 angstroms, preferably about 20 to about 50 angstroms and more preferably about 20 angstroms. Other silicide-forming metal layer materials and/or thicknesses may be used. A nitride layer (not shown) may be formed at the top of silicide-forming metal layer 52.

Following formation of silicide-forming metal layer 52, an RTA step may be performed at about 540°C for about one minute to form silicide layer 50 (FIG. 3), consuming all or a portion of the silicide-forming metal layer 52. Following the RTA step, any residual nitride layer from silicide-forming metal layer 52 may be stripped using a wet chemistry, as described above. Other annealing conditions may be used.

Following the RTA step and the nitride strip step, bottom electrode 24 is formed above silicide layer 50. In some embodiments, Ti-rich TiN bottom electrode 24 may be about 20 to about 500 angstroms, and preferably about 100 angstroms. Some or all of the bottom electrode may be Ti-rich TiN. For example, in some embodiments, bottom electrode 24 may have a thickness of about 10 angstroms to about 2000 angstroms, with the Ti-rich TiN portion having a thickness of about 2 angstroms to about 500 angstroms.

As described above, Ti-rich TiN bottom electrode 24 may be formed by PVD, CVD, PECVD, sputter deposition, ALD, or other similar process. Example PVD processes for forming Ti-rich TiN bottom electrode 24 are listed above in Table 1 and Table 2. Persons of ordinary skill in the art will understand that other processes may be used.

CNT element 12 is formed above Ti-rich TiN bottom electrode 24. CNT material may be deposited by various techniques. One technique involves spray- or spin-coating a carbon nanotube suspension, thereby creating a random CNT material. Another technique involves growing carbon nanotubes from a seed anchored to the substrate by CVD, PECVD or the like. Discussions of various CNT deposition techniques are found in previously incorporated U.S. Patent Application Serial No. 11/968,154, "Memory Cell That Employs A Selectively Fabricated Carbon Nano-Tube

Reversible Resistance-Switching Element And Methods Of Forming The Same;" U.S. Patent Application Serial No. 11/968,156, "Memory Cell That Employs A Selectively Fabricated Carbon Nano-Tube Reversible Resistance-Switching Element Formed Over A Bottom Conductor And Methods Of Forming The Same;" and U.S. Patent Application Serial No. 11/968,159, "Memory Cell With Planarized Carbon Nanotube Layer And Methods Of Forming The Same."

Any suitable thickness may be employed for the CNT material of CNT element 12. In one embodiment, a CNT material thickness of about 100 to about 1000, and more preferably about 400-600 angstroms, may be used.

Above CNT element 12, top electrode 33 is formed. Top electrode 33 may be about 20 to about 500 angstroms, and preferably about 100 angstroms, of titanium nitride or another suitable barrier layer such as tantalum nitride, tungsten nitride, tungsten, molybdenum, combinations of one or more barrier layers, barrier layers in combination with other layers such as titanium/titanium nitride, tantalum/tantalum nitride or tungsten/tungsten nitride stacks, or the like. Other barrier layer materials and/or thicknesses may be employed. For example, in some embodiments, the top electrode 33 may be TiN with a thickness of about 100 to 2000 angstroms.

In at least one embodiment, top electrode 33 may be deposited without a pre-clean or pre-sputter step prior to deposition. Example deposition process conditions are as set forth in Table 3.

TABLE 3: EXAMPLE ADHESION/BARRIER LAYER DEPOSITION PARAMETERS

PROCESS PARAMETER	EXAMPLE RANGE	PREFERRED RANGE
Argon Flow Rate (sccm)	20-40	20-30
Ar With Dilute H_2 (<10%) Flow Rate (sccm)	0-30	0-10
Nitrogen Flow Rate (sccm)	50-90	60-70
Pressure (milliTorr)	1-5000	1800-2400
Power (Watts)	10-9000	2000-9000
Power Ramp Rate (Watts/sec)	10-5000	2000-4000
Process Temperature (°C)	100-600	200-350
Deposition Time (sec)	5-200	10-150

Other flow rates, pressures, powers, power ramp rates, process temperatures and/or deposition times may be used.

Example deposition chambers include the Endura 2 tool available from Applied Materials, Inc. of Santa Clara, CA. Other processing tools may be used. In some embodiments, a buffer chamber pressure of about $1\text{-}2\text{x}10^{-7}$ Torr and a transfer chamber pressure of about $2\text{-}5\text{x}10^{-8}$ Torr may be used. The deposition chamber may be stabilized for about 250-350 seconds with about 60-80 sccm Ar, 60-70 sccm N_2, and about 5-10 sccm of Ar with dilute H_2 at about 1800-2400 milliTorr. In some embodiments, it may take about 2-5 seconds to strike the target. Other buffer chamber pressures, transfer chamber pressures and/or deposition chamber stabilization parameters may be used.

As shown in FIG. 4C, top electrode 33, CNT element 12, Ti-rich TiN bottom electrode 24, silicide-forming metal layer 52, diode layers 14a-14c, and barrier layer 28 are patterned and etched to form pillars 132.

Pillars 132 may be formed above corresponding conductors 20 and have substantially the same width as conductors 20, for example, although other widths may be used. Some misalignment may be tolerated. The memory cell layers may be patterned and etched in a single pattern/etch procedure or using separate pattern/etch steps. In at least one embodiment, top electrode 33, CNT element 12 and Ti-rich TiN bottom electrode 24 are etched together to form MIM stack 38 (FIG. 3).

For example, photoresist may be deposited, patterned using standard photolithography techniques, layers 28, 14a-14c, 52, 24, 12, and 33 may be etched, and then the photoresist may be removed. Alternatively, a hard mask of some other material, for example silicon dioxide, may be formed on top of top electrode 33, with bottom antireflective coating ("BARC") on top, then patterned and etched. Similarly, dielectric antireflective coating ("DARC") may be used as a hard mask. In some embodiments, one or more additional metal layers may be formed above the CNT element 12 and diode 14 and used as a metal hard mask that remains part of the pillars 132. Use of metal hard masks is described, for example, in U.S. Patent Application Serial No. 11/444,936, filed May 13, 2006 and titled "Conductive Hard Mask To Protect Patterned Features During Trench Etch" (hereinafter "the '936 Application") which is hereby incorporated by reference herein in its entirety for all purposes.

Pillars 132 may be formed using any suitable masking and etching process. For example, layers 28, 14a-14c, 52, 24, 12, and 33 may be patterned with about 1 to about 1.5 micron, more preferably about 1.2 to about 1.4 micron, of photoresist ("PR") using standard photolithographic techniques. Thinner PR layers may be

used with smaller critical dimensions and technology nodes. In some embodiments, an oxide hard mask may be used below the PR layer to improve pattern transfer and protect underlying layers during etching.

In at least some embodiments, a technique for etching CNT material using BCl_3 and Cl_2 chemistries may be employed. For example, U.S. Patent Application Serial No. 12/421,803, filed April 10, 2009, titled "Methods For Etching Carbon Nano-Tube Films For Use In Non-Volatile Memories," which is hereby incorporated by reference herein in its entirety for all purposes, describes techniques for etching CNT material using BCl_3 and Cl_2 chemistries. In other embodiments, a directional, oxygen-based etch may be employed such as is described in U.S. Provisional Patent Application Serial No. 61/225,487, filed July 14, 2009, which is hereby incorporated by reference herein in its entirety for all purposes. Any other suitable etch chemistries and/or techniques may be used.

In some embodiments, after etching, pillars 132 may be cleaned using a dilute hydrofluoric/sulfuric acid clean. Such cleaning, whether or not PR ashing is performed before etching, may be performed in any suitable cleaning tool, such as a Raider tool, available from Semitool of Kalispell, Montana. Example post-etch cleaning may include using ultra-dilute sulfuric acid (e.g., about 1.5-1.8 wt%) for about 60 seconds and/or ultra-dilute hydrofluoric ("HF") acid (e.g., about 0.4-0.6 wt%) for 60 seconds. Megasonics may or may not be used. Other clean chemistries, times and/or techniques may be employed.

A dielectric liner 54 is deposited conformally over pillars 132, as illustrated in FIG. 4D. In at least one embodiment, dielectric liner 54 may be formed with an oxygen-poor deposition chemistry (e.g., without a high

oxygen plasma component) to protect the CNT material of reversible resistance switching element 12 during a subsequent deposition of an oxygen-rich gap-fill dielectric 58b (e.g., SiO_2) (not shown in FIG. 4D). For instance, dielectric sidewall liner 54 may comprise about 200 to about 500 angstroms of silicon nitride. However, the structure optionally may comprise other layer thicknesses and/or other materials, such as $Si_xC_yN_z$ and $Si_xO_yN_z$ (with low O content), etc., where x, y and z are non-zero numbers resulting in stable compounds. Persons of ordinary skill in the art will understand that other dielectric materials may be used to form dielectric liner 54.

In one example embodiment, a SiN dielectric liner 54 may be formed using the process parameters listed in Table 4. Liner film thickness scales linearly with time. Other powers, temperatures, pressures, thicknesses and/or flow rates may be used.

TABLE 4: PECVD SiN LINER PROCESS PARAMETERS

PROCESS PARAMETER	EXAMPLE RANGE	PREFERRED RANGE
SiH_4 Flow Rate (sccm)	0.1-2.0	0.4-0.7
NH_3 Flow Rate (sccm)	2-10	3-5
N_2 Flow Rate (sccm)	0.3-4	1.2-1.8
Temperature (°C)	300-500	350-450
Low Frequency Bias (kW)	0-1	0.4-0.6
High Frequency Bias (kW)	0-1	0.4-0.6
Thickness (Angstroms)	200-500	280-330

A dielectric layer 58b is deposited over pillars 132 to fill the voids between pillars 132. For example, approximately 2000 - 7000 angstroms of silicon dioxide may be deposited and planarized using chemical mechanical polishing or an etchback process to form a planar surface 136, resulting in the structure illustrated in FIG. 4E. Planar surface 136 includes exposed top

surfaces of pillars 132 separated by dielectric material 58b (as shown). Other dielectric materials such as silicon nitride, silicon oxynitride, low K dielectrics, etc., and/or other dielectric layer thicknesses may be used.

With reference to FIG. 4F, second conductors 22 may be formed above pillars 132 in a manner similar to the formation of first conductors 20. For example, in some embodiments, one or more barrier layers and/or adhesion layers 26 may be deposited over pillars 132 prior to deposition of a conductive layer 140 used to form second conductors 22.

Conductive layer 140 may be formed from any suitable conductive material such as tungsten, another suitable metal, heavily doped semiconductor material, a conductive silicide, a conductive silicide-germanide, a conductive germanide, or the like deposited by PVD or any other any suitable method (e.g., CVD, etc.). Other conductive layer materials may be used. Barrier layer and/or adhesion layer 26 may include titanium nitride or another suitable layer such as tantalum nitride, tungsten nitride, tungsten, molybdenum, combinations of one or more layers, or any other suitable material(s). The deposited conductive layer 140 and barrier and/or adhesion layer 26 may be patterned and etched to form second conductors 22. In at least one embodiment, second conductors 22 are substantially parallel, substantially coplanar conductors that extend in a different direction than first conductors 20.

In other embodiments of the invention, second conductors 22 may be formed using a damascene process in which a dielectric layer is formed, patterned and etched to create openings or voids for conductors 22. The openings

or voids may be filled with adhesion layer 26 and conductive layer 140 (and/or a conductive seed, conductive fill and/or barrier layer if needed). Adhesion layer 26 and conductive layer 140 then may be planarized to form a planar surface.

Following formation of second conductors 22, the resultant structure may be annealed to crystallize the deposited semiconductor material of diodes 14 (and/or to form silicide regions by reaction of the silicide-forming metal layer 52 with p+ region 14c). The lattice spacing of titanium silicide and cobalt silicide are close to that of silicon, and it appears that such silicide layers may serve as "crystallization templates" or "seeds" for adjacent deposited silicon as the deposited silicon crystallizes. Lower resistivity diode material thereby is provided. Similar results may be achieved for silicon-germanium alloy and/or germanium diodes.

Thus in at least one embodiment, a crystallization anneal may be performed for about 10 seconds to about 2 minutes in nitrogen at a temperature of about 600 to 800°C, and more preferably between about 650 and 750°C. Other annealing times, temperatures and/or environments may be used.

This crystallization anneal may also cause CNT element 12 and Ti-rich TiN bottom electrode 24 to interact to form TiC contacts between CNT element 12 and Ti-rich TiN bottom electrode 24. As described above, because all of the CNT material in CNT element 12 does not make contact with Ti-rich TiN bottom electrode 24, persons of ordinary skill in the art will understand that there may be a localized variance in composition.

Persons of ordinary skill in the art will understand that a subsequent anneal at temperatures of

about 700°C or higher (e.g., such as at about 750°C as described below) alternatively may be used to form TiC contacts between CNT element 12 and Ti-rich TiN bottom electrode 24.

Additional memory levels may be similarly formed above the memory level of FIGS. 4A-F. Persons of ordinary skill in the art will understand that alternative memory cells in accordance with this invention may be fabricated with other suitable techniques.

The foregoing description discloses only example embodiments of the invention. Modifications of the above disclosed apparatus and methods which fall within the scope of the invention will be readily apparent to those of ordinary skill in the art. For instance, in any of the above embodiments, the carbon-based material may be located below diode(s) 14.

Additionally, the techniques described above with respect to bottom electrodes may be used with top electrodes. That is, a CNT MIM stack may be formed that includes a top electrode that includes a Ti-rich TiN material layer that contacts the CNT material. Alternatively, a CNT MIM stack may be formed that includes TiC contacts between the CNT material and the top electrode.

Moreover, the various techniques may be combined, such that a CNT MIM stack may be formed that includes a top electrode that includes a metal-rich metal nitride material layer (e.g., Ti-rich TiN, Ta-rich TaN, Hf-rich HfN, Zr-rich ZrN, or other similar metal-rich metal nitride) that contacts the CNT material, and a bottom electrode that includes a metal-rich metal nitride material layer that contacts the CNT material. Likewise, a CNT MIM stack may be formed that includes metal carbide (e.g., TiC, TaC, HfC,

ZrC, or other similar metal carbide) contacts between the CNT material and the top and bottom electrode.

Accordingly, although the present invention has been disclosed in connection with example embodiments thereof, it should be understood that other embodiments may fall within the spirit and scope of the invention, as defined by the following claims.

CLAIMS

1. A method of forming a reversible resistance-switching metal-insulator-metal (MIM) stack comprising:

forming a first conducting layer comprising a titanium nitride material having between about 50% Ti and about 95% Ti;

forming a carbon nano-tube (CNT) material above the first conducting layer;

forming a second conducting layer above the CNT material; and

etching the first conducting layer, CNT material and second conducting layer to form the MIM stack.

2. The method of claim 1, wherein the first conducting layer comprises a titanium nitride material having between about 55% Ti and 75% titanium.

3. The method of claim 1, wherein the first conducting layer has a thickness of about 10 to 2000 angstroms.

4. The method of claim 1, further comprising annealing the MIM stack to form titanium carbide contacts between the first conducting layer and the CNT material.

5. The method of claim 4, wherein the titanium carbide contacts comprises between about 1% C to about 60% C.

6. The method of claim 4, wherein the titanium carbide contacts comprises between about 10% C to about 50% C.

7. A method of forming a carbon nano-tube (CNT) memory cell comprising:

forming a first conductor;

forming a steering element above the first conductor;

forming a first conducting layer above the first conductor, wherein the first conducting layer comprises a titanium nitride material having between about 50% Ti and about 95% Ti;

forming a CNT material above the first conducting layer;

forming a second conducting layer above the CNT material;

etching the first conducting layer, CNT material and second conducting layer to form a metal-insulator-metal (MIM) stack; and

forming a second conductor above the CNT material and the steering element.

8. The method of claim 7, wherein the first conducting layer comprises a titanium nitride material having between about 55% Ti and 75% Ti.

9. The method of claim 7, wherein the first conducting layer has a thickness of about 10 to 2000 angstroms.

10. The method of claim 7, further comprising annealing the MIM stack to form titanium carbide contacts between the first conducting layer and the CNT material.

11. The method of claim 10, wherein the titanium carbide contacts comprises between about 1% C to about 60% C.

12. The method of claim 10, wherein the titanium carbide contacts comprises between about 10% C to about 50% C.

13. The method of claim 7, wherein the steering element comprises a vertical polysilicon diode.

14. The method of claim 7, wherein the MIM stack and steering element are coupled in series.

15. A memory cell formed by the method of claim 7.

16. A memory level formed by the method of claim 7.

17. A three-dimensional memory array formed by the method of claim 7.

18. A carbon nano-tube (CNT) memory cell comprising:
a first conductor;
a steering element above the first conductor;
a metal-insulator-metal (MIM) stack comprising:
a first conducting layer above the first conductor, wherein the first conducting layer comprises a titanium nitride material having between about 50% Ti and about 95% Ti;
a CNT material above the first conducting layer; and
a second conducting layer above the CNT material; and
a second conductor above the CNT material and the steering element.

19. The memory cell of claim 19, wherein the first conducting layer comprises a titanium nitride material having between about 55% Ti and 75% Ti.

20. The memory cell of claim 19, further comprising titanium carbide contacts between the first conducting layer and the CNT material.

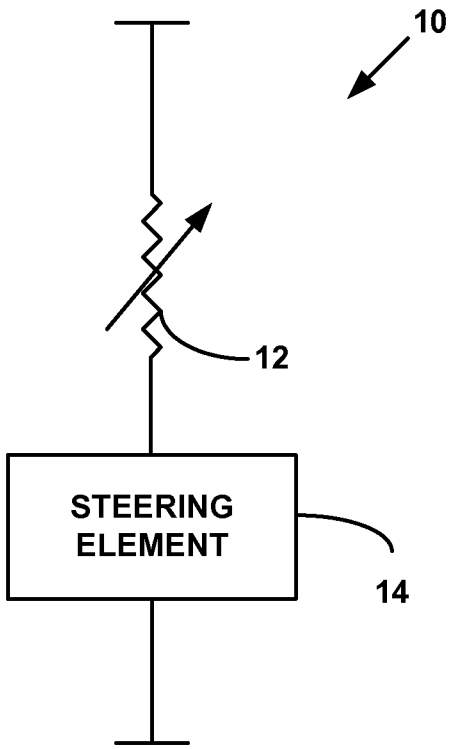


FIG. 1

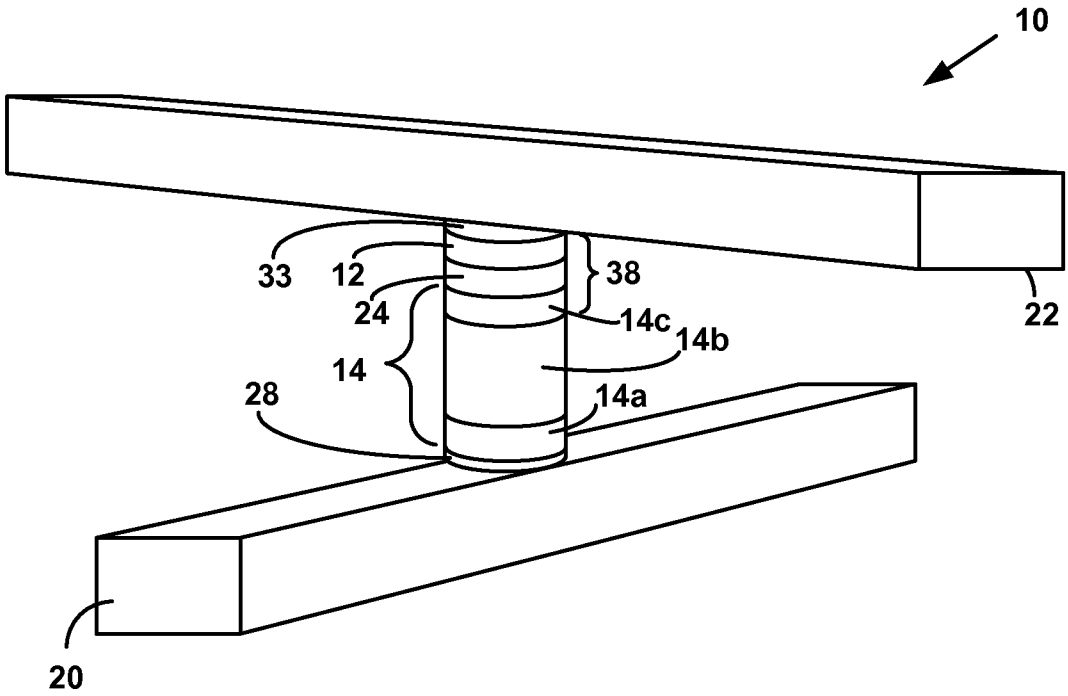


FIG. 2A

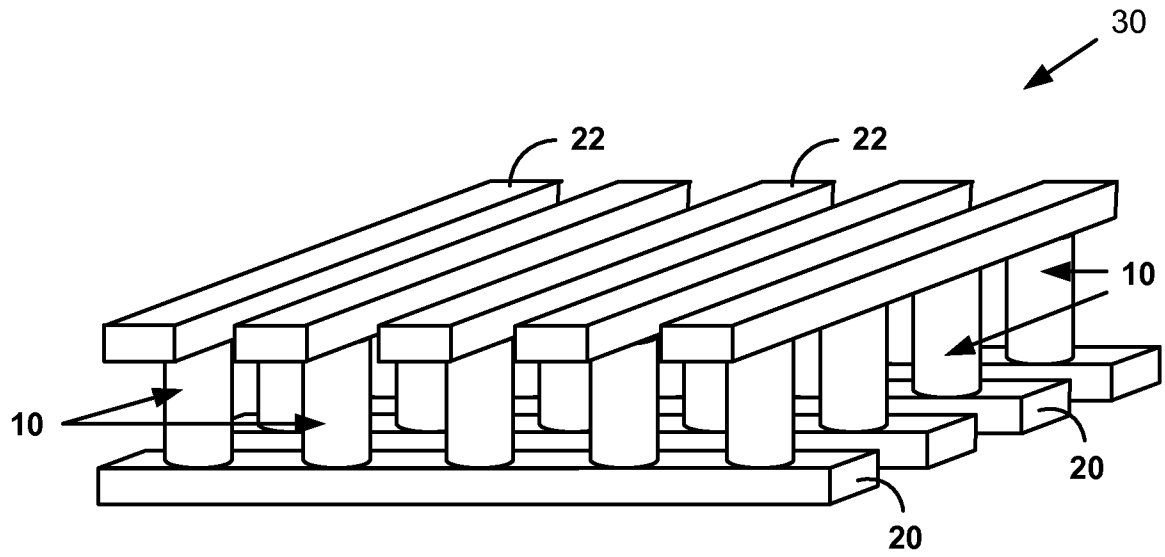


FIG. 2B

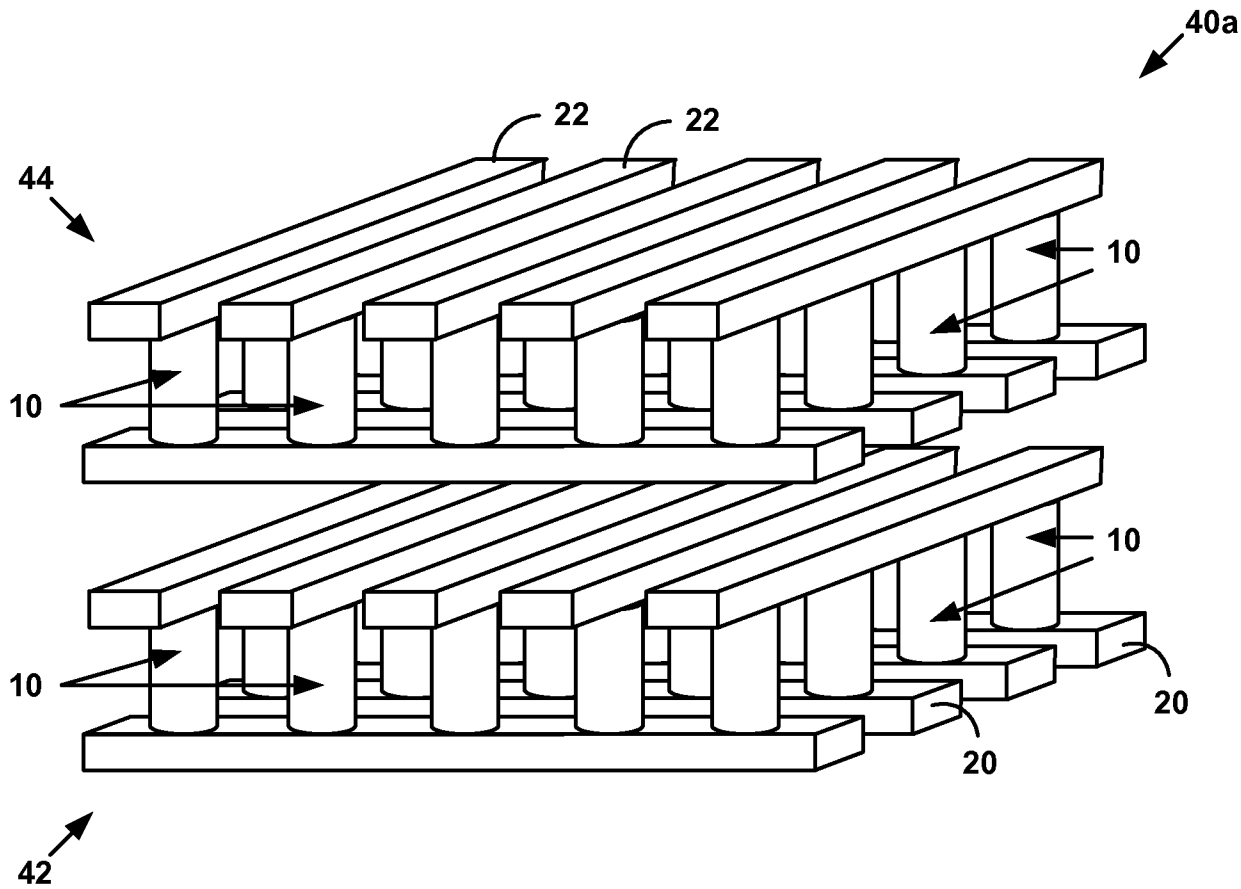


FIG. 2C

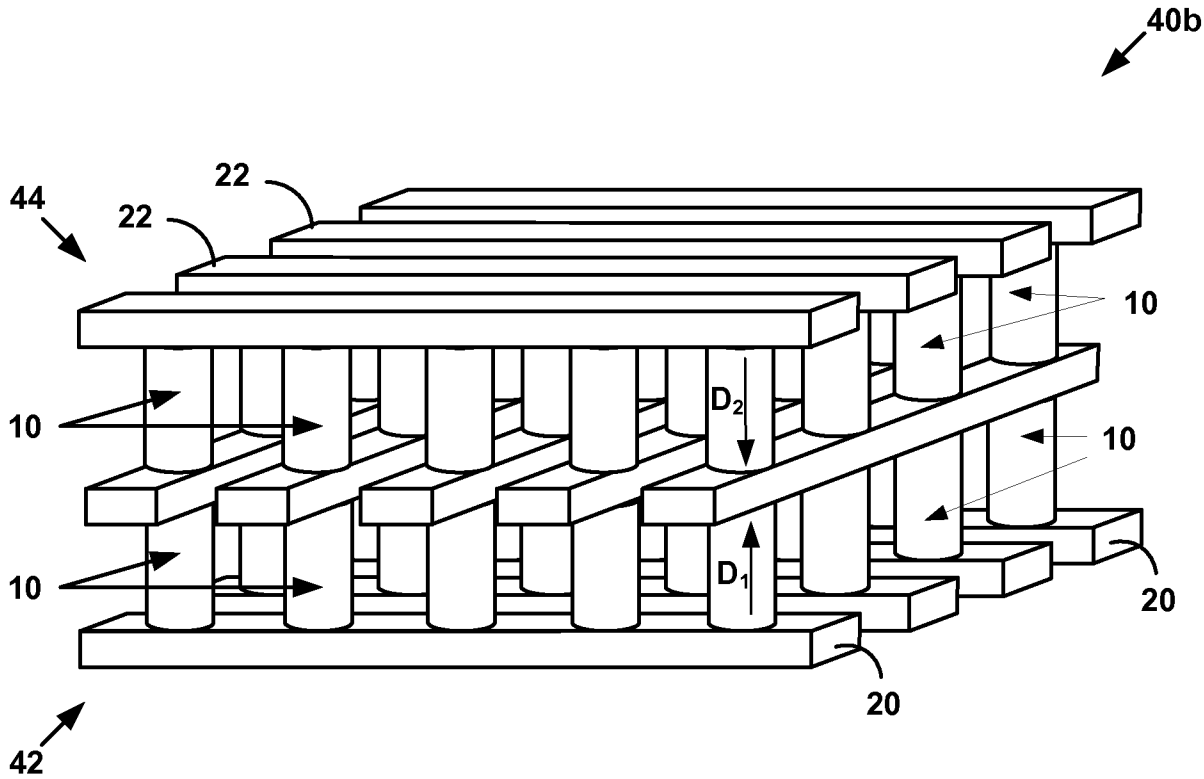


FIG. 2D

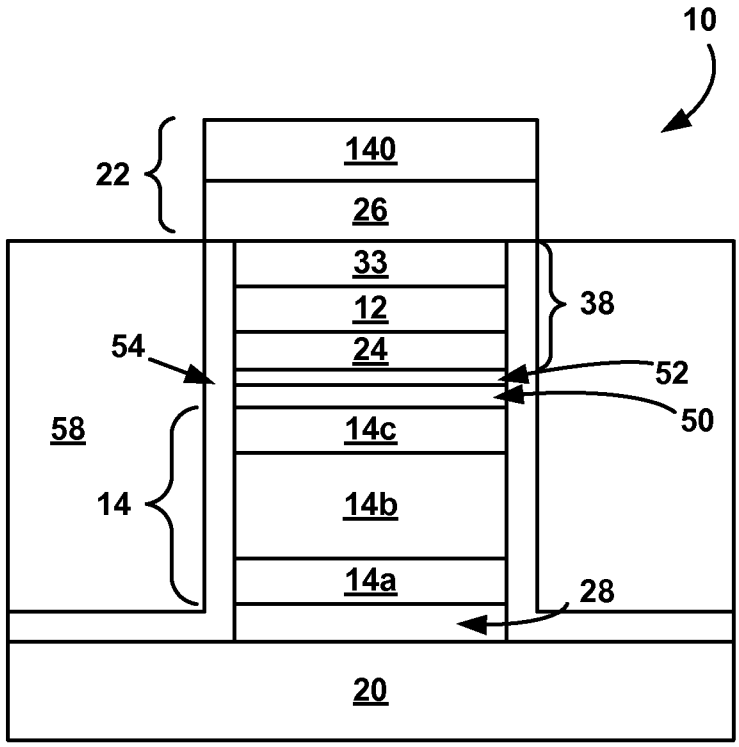
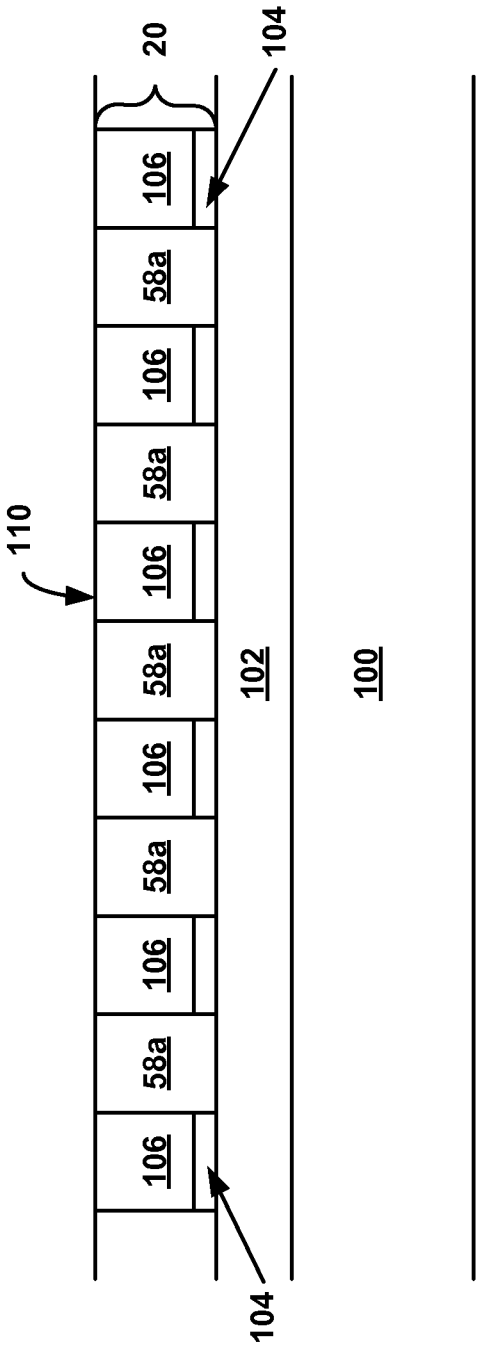


FIG. 3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104
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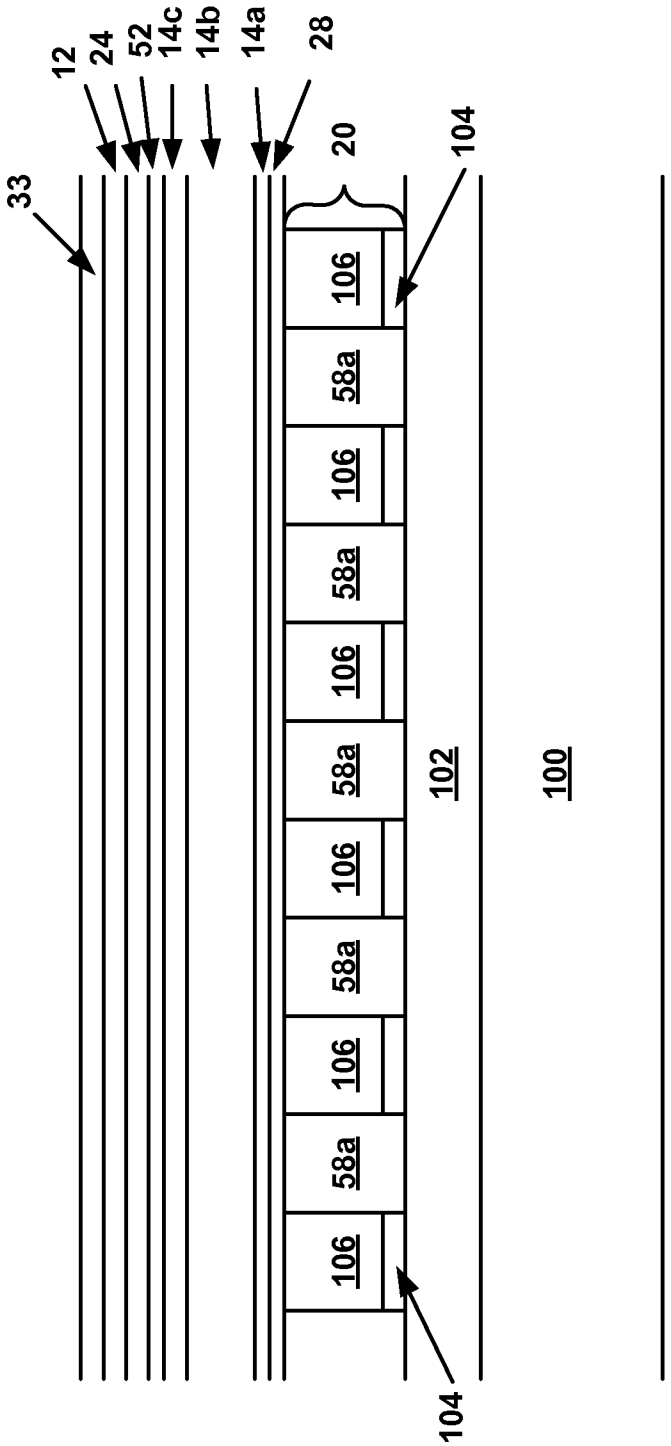
100
104

FIG. 4A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14c
14b
14a
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58a
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58a
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58a
106
58a
106
102
100
104

FIG. 4B

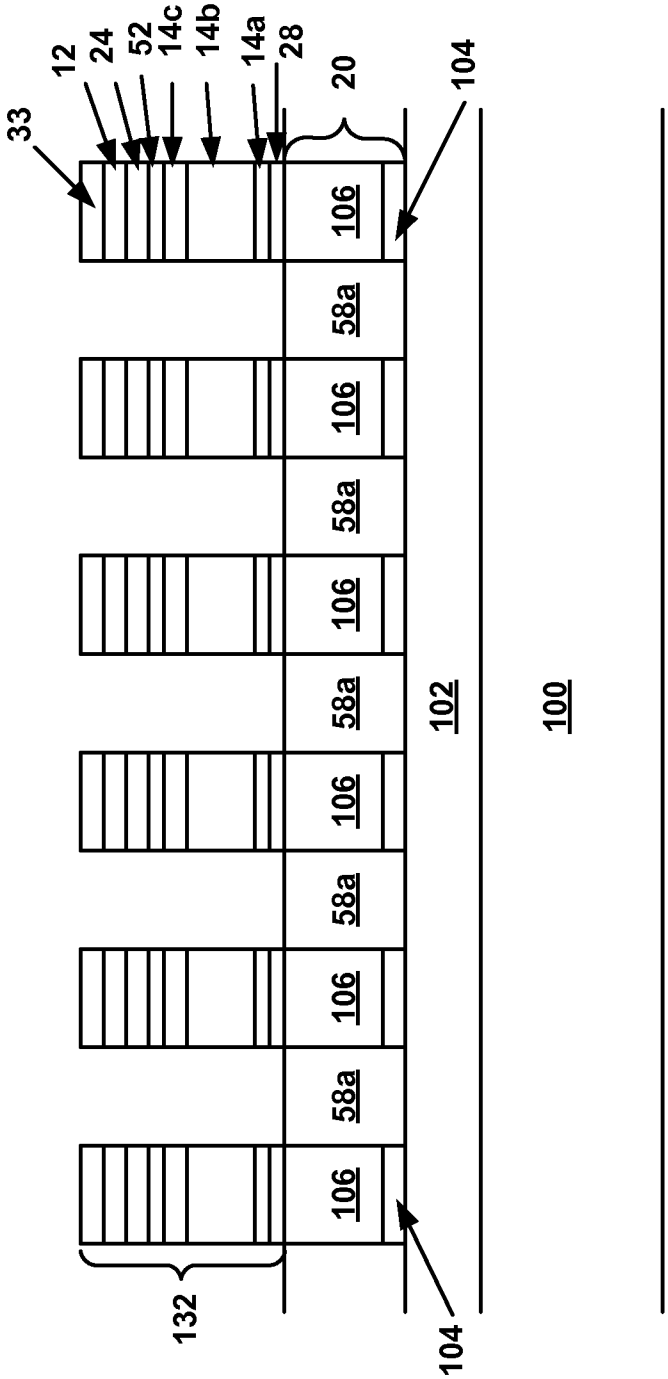
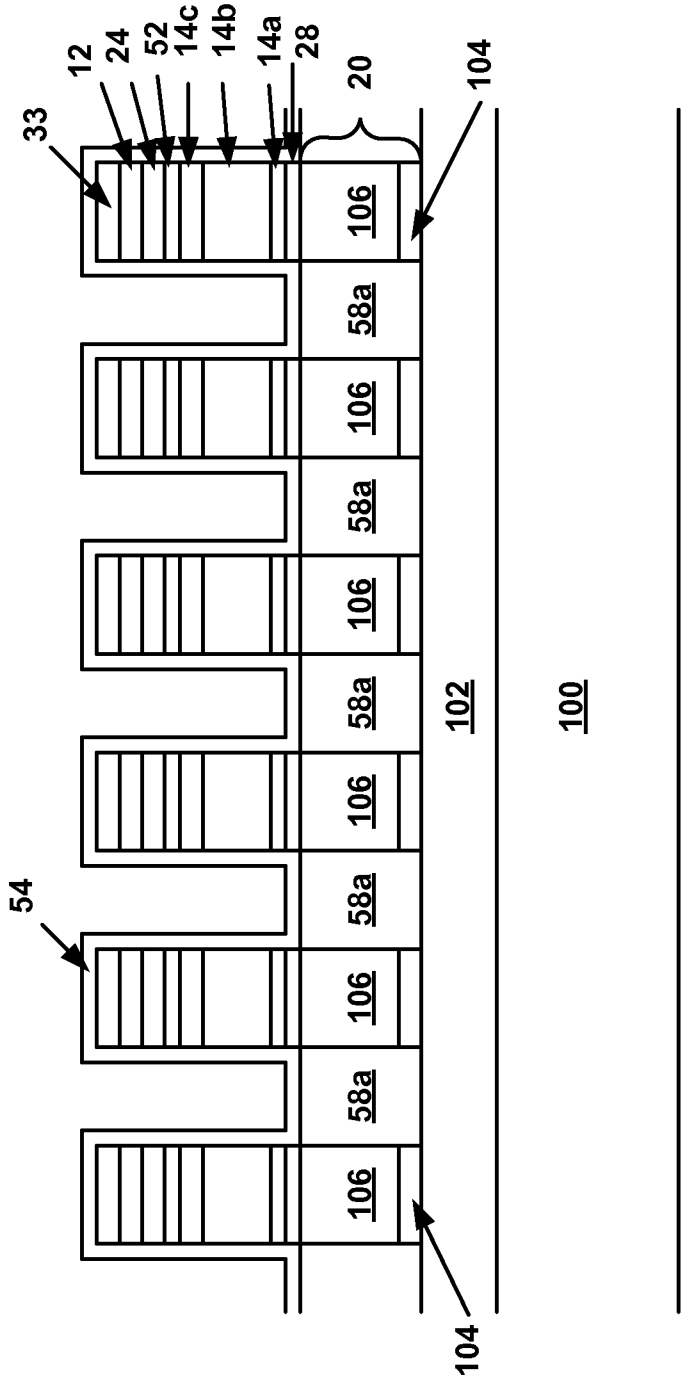


FIG. 4C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14b
14a
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58a
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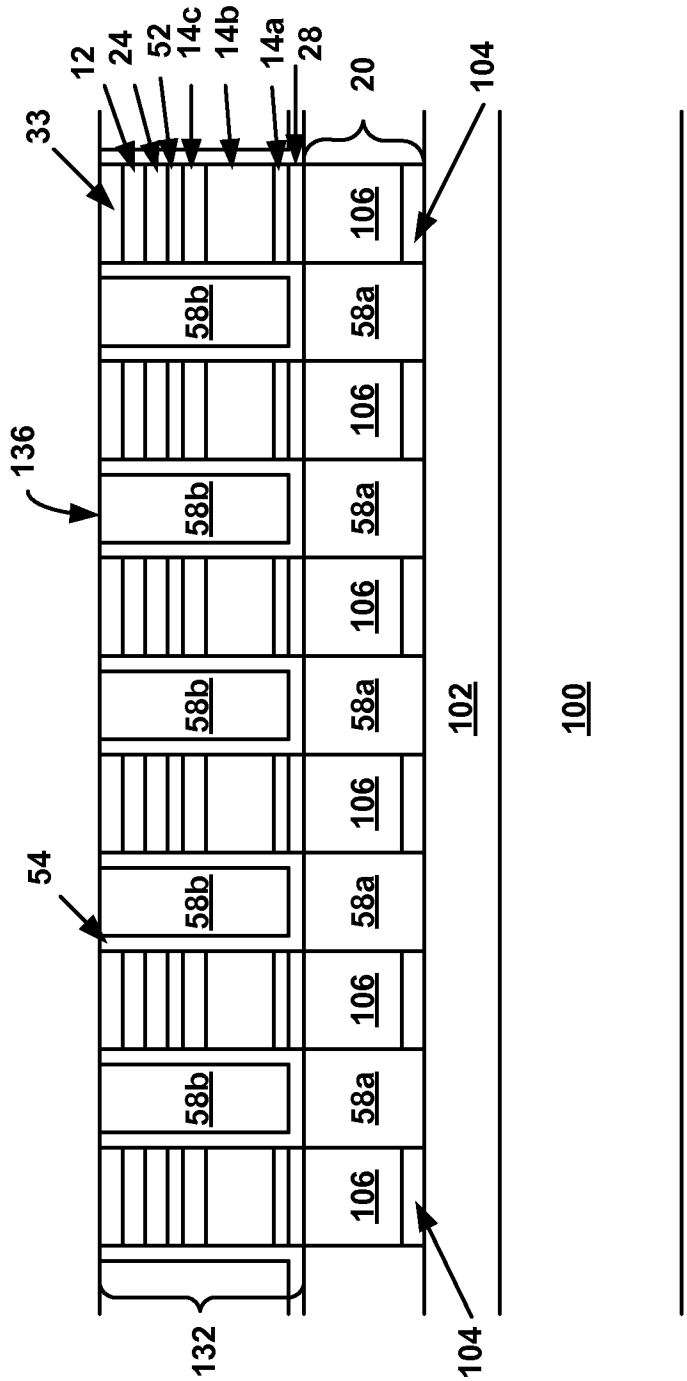
58a
106
54
102
100
104

FIG. 4D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14b
14a
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58b
58a
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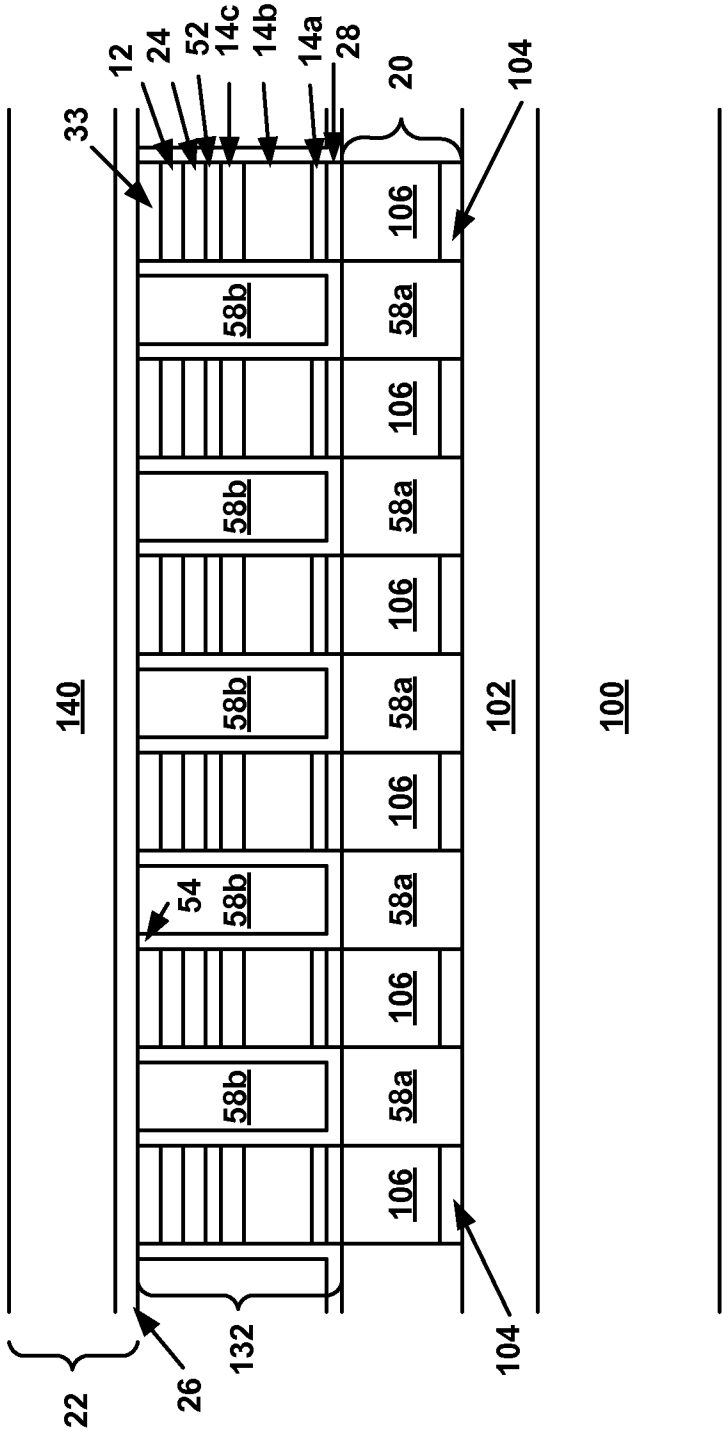
100
132
104

FIG. 4E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24
52
14c
14b
14a
28
20
104
33
106
58b
58a
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102
100
54
132
22
26

FIG. 4F

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2012/026914

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L27/10 G11C13/02 H01L51/05 H01L27/24 H01L45/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2010/327254 A1 (CHEN XIYING [US] ET AL) 30 December 2010 (2010-12-30) Figs. 2a-2c and corresponding text.; paragraphs [0012] - [0031] -----	1,3,7,9, 13-18 2,4-6,8, 10-12, 19,20
Y	US 2010/012914 A1 (XU HUIWEN [US] ET AL) 21 January 2010 (2010-01-21) paragraphs [0071] - [0080]; figures 6-12 -----	2,4-6,8, 10-12, 19,20
A	US 2004/026731 A1 (FOURNIER JEFFREY P [US] ET AL) 12 February 2004 (2004-02-12) paragraphs [0028] - [0030]; figure 6 ----- -/--	1-20

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 July 2012	06/08/2012

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Dauw, Xavier

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2012/026914

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	"Titanium Nitride article from Wikipedia.org (history)", Wikipedia.org, 27 February 2011 (2011-02-27), XP55033574, Retrieved from the Internet: URL:http://en.wikipedia.org/w/index.php?title=Titanium_nitride&oldid=416234382 [retrieved on 2012-07-23] the whole document -----	1-20

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2012/026914

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