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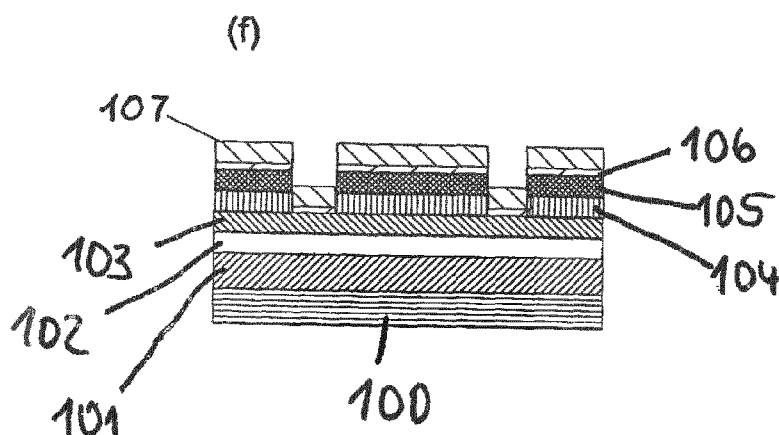
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(54) Title: METHOD OF MANUFACTURING AN ORGANIC ELECTRONIC DEVICE AND ORGANIC ELECTRONIC DEVICE



(57) Abstract: The present disclosure relates to a method of manufacturing an organic electronic device, comprising providing a layered device structure, the layered device structure comprising a plurality of electrodes and an electronically active region being provided in electrical contact with at least one of the plurality of electrodes, said providing of the layered device structure comprising steps of providing an organic semiconducting layer, applying a structuring layer to the organic semiconducting layer, the structuring layer having a first region and a second region, the first region being covered by a layer material, applying a contact improving layer to the structuring layer by depositing at least one of an organic dopant material and an organic dopant-matrix material at least in the first region, depositing a layer material on the contact improving layer at least in the first region, and removing the structuring layer at least in the second region. Furthermore, an organic electronic device is provided.



Method of manufacturing an organic electronic device and organic electronic device

The invention refers to a method of manufacturing an organic electronic device and an organic electronic device.

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Background

The compatibility of organic materials and device concepts to high resolution, cost-effective patterning techniques exhibits a major requirement in order to warrant their commercial success. In particular, down-scaling and high density integration of organic field effect transistors (OTFTs) is essential to overcome current performance limitations and to make OTFTs become a prospective device for applications e.g. in active matrix displays or organic microprocessors.

With respect to the production of organic electronic devices having an electronically active region which is being made at least in part from an organic material and which is in contact with one or more electrodes. Various methods for structuring the organic semiconductor layers were proposed, e.g. shadow mask deposition, laser ablation, inkjet printing, or nano-imprinting. However, they are either lacking in their throughput capacitance, accessible feature size, or their compatibility with the organic compounds themselves. Photolithography on the other hand is a very powerful technique which is currently adopted as a standard patterning approach for inorganic electronic industry. However, except of some limited cases (cf. Balocco et al., Org. Electron. 7, 500 (2006), Huang et al., J. Mat. Chem. 17, 1043 (2007)), conventional photo-resist, developer, and solvent compounds (using e.g. tuluol and alkaline solvents) are not applicable to organic materials.

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Summary

It is an object of the invention to provide technologies for organic electronic devices having an improved operation functionality.

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According to one aspect, a method of manufacturing an organic electronic device according to claim 1 is provided. According to another aspect, an organic electronic device according to claim 11 is provided. Advantageous developments are disclosed in the dependent claims.

- 5 A method of manufacturing an organic electronic device is provided, the method comprising providing a layered device structure, the layered device structure comprising a plurality of electrodes and an electronically active region being provided in electrical contact with at least one of the plurality of electrodes. The step of providing the layered device structure comprises a step of providing an organic semiconducting layer steps of applying a structuring layer on the organic
10 semiconducting layer, the structuring layer being provided with a first region to be covered by the layer material and a second region not to be covered by the layer material, applying a contact improving layer on the structuring layer by depositing an organic dopant material and / or an organic dopant-matrix material at least in the first region, depositing a layer material on the contact improving layer at least in the first region, and removing the structuring layer at least in the second region, but not in the first region.
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According to another aspect, an organic electronic device is provided, the device comprising

- a layered device structure, the layered device structure comprising a plurality of electrodes and an electronically active region being provided in electrical contact with at least one of the plurality of electrodes,
20
- in the layered structure, an organic semiconducting layer comprising a first region treated in a photo lithography process, and
- a layer stack deposited on the first region, the layer stack comprising a structured layer and a contact improving layer provided between and in contact with the first region and the structured layer.
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After the step of removing the structuring layer the layer material with the underlying contact improving layer remains at least in the first region, thereby, providing coverage of at least the first region, but not the second region, with the layer material.

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By the contact improving layer, an electrical contact may be improved at an interface between the organic semiconducting layer and the structured layer produced above the organic semiconducting layer in the layered structure.

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The structuring process may be used several times in the process of producing the layered device structure.

10 The electronically active region, besides the contact improving layer, may comprise one or more organic layers made of at least one organic semiconducting material, preferably an organic small molecule semiconductor different from organic polymers.

15 The contact improving layer may be provided in between and in contact with layers both made of an electrically non-doped material. The contact improving layer may improve the electrical contact at the interface of the two non-doped layers.

The organic semiconducting layer and / or the contact improving layer may be provided either by vacuum deposition or by a solution-based deposition process.

20 By the process comprising said applying the structuring layer on the organic semiconducting layer, said applying the contact improving layer on the structuring layer, said depositing the layer material on the contact improving layer, and said removing the structuring layer at least in the second region, a structured layer made of a layer material is provided on the organic semiconducting layer.

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The method may further comprise a lift-off structuring process. The lift-off structuring process may be used several times in the process of producing the layered device structure. The lift-off structuring process may comprise the steps of applying the structuring layer on the organic semiconducting layer, applying the contact improving layer on the structuring layer, depositing the

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layer material on the contact improving layer, and removing (lifting-off) the structuring layer at least in the second region.

5 The step of providing the structuring layer may further comprise a step of using a photo lithographic process.

10 The using the photo lithographic process may further comprise steps of depositing a photo resist cover on the organic semiconducting layer and structuring the photo resist cover, said structuring comprising steps of illuminating and removing the photo resist cover, thereby, at least partially removing the photo resist cover in at least the second region, but not the first region. The photo resist cover may be removed by etching. The photo resist cover may be a single layer or a multi-layer cover. For example, a plurality of layers made from different photo resist materials may be provided. Different layers may be provided for implementing different functions in the lift-off structuring process.

15 The step depositing the photo resist cover may further comprise steps of depositing a protection layer on the organic semiconducting layer, and depositing a photo resist layer on the protection layer. The protection layer may provide protection for the underlying layer against wet materials used, for example, for the structuring of the photo resist layer, e.g. by etching. The protection layer may be transparent to oxygen. The step of structuring the photo resist cover may comprise removing at least the photo resist layer in at least the first region, but not the second region. In addition, the protection layer may at least partially be removed.

25 The etching of the photo resist cover may further comprise a step of providing a non-closed residual layer made from non-removed residuals of the photo resist cover in the first region. The non-removed residuals may be made of the material of the protection layer and / or photo resist layer. It may only partially cover the underlying organic semiconducting layer.

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There may be a step of providing a structured electrode layer made of an electrode material. For example, one or more top electrodes may be produced, the top electrode(s) being provided on top of the electronically active region. Said providing of the structured electrode layer may part of the process of providing the structured layer.

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There may further be a step of providing a structured non-electrode layer made of a non-electrode material. Said providing of the structured non-electrode layer may part of the process of providing the structured layer.

10 The photo lithographic process may be performed by using a fluorine based photo lithography.

The contact improving layer may be provided with a layer thickness of about 1 nm to about 100 nm.

15 The providing the layered device structure may comprise a step of providing a device selected from the following group: organic field effect transistor, an organic circuit assembly, organic light emitting device, and organic photovoltaic device.

Description of preferred embodiments

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In the following, embodiments will be described in further detail, by way of example, with reference to figures. The figures show:

Fig. 1a to 1d a schematic representation of a process for producing a layered structure of an organic semiconducting device using a photo-lithographic process,

25 Fig. 2 optical microscope images of layered structures comprising an organic semiconducting layer,

Fig. 3 graphical representations for the transfer characteristic and current-voltage curves (inset) of a lithographically structured OTFT in comparison to a reference device,

- Fig. 4 graphical representation of a transistor resistance $R_{\text{Ch}+2\text{C}}$ (channel + contact) of lithographically produced OTFTs for different channel lengths ($V_{\text{DS}}=2\text{V}$),
- Fig. 5a and 5b graphical representations of XPS measurements of the C 1s signal of a C_{60} film after removing Ortho 310 in comparison to a C_{60} film as evaporated (Fig. 5a) and the F 1s signal of a C_{60} film after removing Ortho 310 (Fig. 5b), respectively,
- Fig. 6 a graphical representation of the luminance of a green OLED for different gate-source voltages at a fixed drain-source voltage of 12V,
- Fig. 7a to 7h a schematic representation of a procedure for manufacturing a complementary inverter employing photo-lithography,
- Fig. 8 a microscope image of an inverter circuit before deposition of electrodes,
- Fig. 9 a graphical representation of input vs. output voltage (switching characteristics) of the complementary organic inverter fabricated by photo-lithography,
- Fig. 10 a schematic representation of a process for producing a layered structure of an OTFT by using a photo-lithographic process,
- Fig. 11a and 11b a graphical representation of the I-V curves and the transfer characteristics of two lithographically structured OTFTs with and without an contact improving layer, and
- Fig. 12 a graphical representation of the contact resistance estimated by transmission line method for lithographically made OTFTs with and without the contact improving layer.

Fluorine based photo-lithography is used for high resolution patterning of p- and n-channel organic field effect transistor (OTFT) (pentacene and C_{60}) under ambient conditions. The OTFT performance is only slightly affected by the structuring procedure, which can be explained by a detailed study including OTFT characterization and X-ray photoelectron spectroscopy (XPS). Hence, fluorine based photo-lithography exhibits a powerful method for structuring of organic semiconductor materials.

It was found that down-scaling of OTFTs may be restricted by injection of charge carriers from the source electrode. This effect leads to deviations from the gradual channel approximation and therefore from OTFT scaling laws.

5 For the use of photo-lithography on organic materials it is proposed using sacrificial protection layer(s). These layers may protect the active material from the wet chemicals during the lithographic process and can be either removed or left as a functional part of the device. This concept may be beneficial owing to its versatility and its potential compatibility to a wide class of organic materials. Here, the process of photo-lithography structuring or patterning is applied to small
10 molecule organic semiconductors.

Photo-resists and solvents used for photo-lithographic patterning may be based on highly fluorinated compounds. Such materials are highly hydrophobic and inert concerning reactions with typical organic semiconductors. These properties enable the use of fluorinated photo-resists as
15 protection layers for organic semiconductors. Furthermore, their hydrophobic character warrants the combination with conventional photo-resist compounds using hydrophilic developer solutions.

Following, the use of a photo-lithography process which allows for structuring OTFTs, especially
20 OTFTs containing one or more layers made of C₆₀ or pentacene, in a top source / drain geometry under ambient conditions is described. Material properties of the organic semiconductors such as layer adhesion, surface roughness, and sensitivity to oxygen and moisture, may affect the photo-lithography process. In the following, the influence of the patterning procedure on the performance of OTFTs is investigated.

25 Structuring on organic materials is performed. The structuring process, for example, may be used for fabrication of OTFTs. A highly doped silicon substrate is used as a gate electrode 2 on a substrate 1. The gate electrode 2 is covered by a gate insulator 3 made of Al₂O₃. The gate insulator 3, for example, may have a thickness of 23nm or 50nm. After substrate cleaning and surface prepa-

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ration, an organic semiconducting layer 4 of either C₆₀ (40nm) or pentacene (25nm, 40nm, and 80nm) is deposited under vacuum conditions (see Fig. 1a).

Subsequently, the samples are taken out of the vacuum chamber, and are exposed to air the first time. A protection layer 5 made of a lift-off resist (Ortho 310 - negative resist, Orthogonal Inc.) is spin-coated (3000rpm, 30s, thickness 1µm) under ambient conditions directly onto the organic semiconducting layer 4 (see Fig. 1b). The lift-off resist Ortho 310 acts as a protective resist since it is based on fluorinated photosensitive polymers which are chemically benign to non-fluorinated organic compounds. It is processed, i.e. deposited, etched, and stripped off, by hydrofluoroether (HFE) solvents.

Worth mentioning, the lift-off resist Ortho 310 only protects the organic semiconductor of the organic semiconducting layer 4 from the wet chemicals, but it is transparent to oxygen. The second role of the protection layer 5 is its use as lift-off resist. This is possible due to the mutual orthogonality of Ortho 310 and non-fluorinated commercial imaging resist. Thus, processing of Ortho 310 does not influence the imaging resist and vice versa.

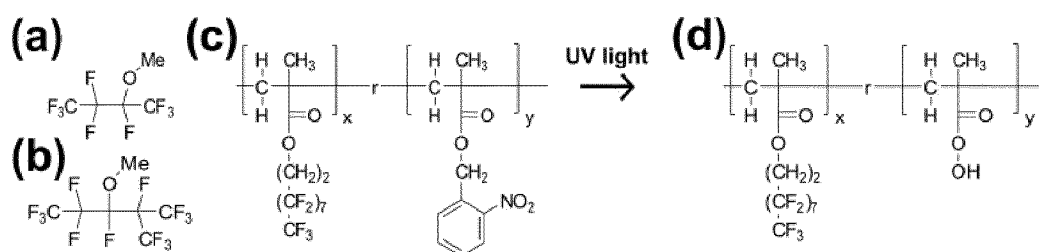
A photo resist layer 6 made of an imaging resist (ma-P1210, positive resist from micro resist technology GmbH, Berlin, thickness 1µm) is spin-coated onto the protection layer 5 using the same procedure and it is exposed by the SF-100 UV broadband exposure system (see Fig. 1b). The exposed parts of the photo resist layer 6 are removed by development in NaOH solution for 17s (see Fig. 1c) and rinsing in deionized water. Afterwards, the photo resist layer 5 serves as an etching mask for Ortho 310. This pattern of the photo resist layer 6 is transferred to Ortho 310 by etching with HFE solvents (see Fig. 1d).

An electrode material 7, namely gold, is deposited through the resist stencil and finally spare gold is removed via lift-off using HFE 7100 in a nitrogen atmosphere (see Fig. 1e and 1f). Apart from the step in Fig. 1f, all other steps of the structuring process are done under ambient conditions in air. The total exposure time to oxygen and moisture is about 30min.

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In an alternative method, only one of the protection layer 5 and the photo resist layer 6 is used. The only layer deposited will provide photo resist functionality.

- 5 Following, the chemical structure of the fluorinated solvent and photo-resist compounds are depicted: (a) HFE 7100, (b) HFE 7300, (c) photosensitive photo-resist (soluble in HFE solvents), and (d) photo-resist after UV light exposure (insoluble in HFE solvents).



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The method may be modified depending on the specific organic material. Since photo-lithography is a multi-step process some conditions may be kept constant in order to identify crucial parameters. In particular, for the described embodiments, resist deposition and development time may remain unchanged. Ideal processing parameters with the highest reliability, independent of layer thickness, are found for C_{60} as:

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- exposure time 0.6s ($40 \text{ mJ} / \text{cm}^2$),
 - development in NaOH for 17s,
 - rinsing by deionized water, and
 - 20 - spin-rinsing by HFE 7100 for 50s (3000rpm).

These conditions allow for a high resolution patterning on C_{60} without a notable influence on the organic layer. Fig. 2a to 2d show optical microscope images of layered structures comprising an organic semiconducting layer after a lift-off process as described above. The images show result for a layered structure comprising C_{60} (40nm) with gold electrodes on top (see Fig. 2a), pentacene

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(80nm) with gold electrodes (see Fig. 2b), pentacene (40nm) with gold electrodes (see Fig. 2c), and pentacene (25nm) (see Fig. 2d).

For pentacene the patterning process was adapted. In particular, the surface roughness and the weak substrate adhesion of pentacene films may need modifications of the photo-lithography recipe. In Fig. 2a to 2d pentacene films of various thicknesses (80nm, 40nm, and 25nm) are shown after the lift-off process using the same procedure as established for C₆₀. There are differences in layer coverage and optical contrast for the different thicknesses.

Especially, for 80nm of pentacene (see Fig. 2b), the layer is non-uniform, contains large defects, and looks perforated. This effect is reduced for 40nm (see Fig. 2c) of pentacene and even vanishes for 25nm (see Fig. 2d) where a uniform layer can be observed. The layer roughness of pentacene films may lie in the range of the layer thickness. This property can explain the different optical contrast obtained in the microscope images.

Furthermore, the layer roughness may lead to a different adhesion of photo-resist and organic semiconductor. In particular, since the layer roughness is increased also the effective contact area between photo-resist and pentacene is increased. Hence, if the HFE solvent creeps underneath the photo-resist in order to lift it off, the photo-resist entrains the pentacene film. This is caused by the fact that owing to the large contact area, the adhesion of pentacene to the photo-resist is larger than the adhesion to the substrate. This influence leads to the appearance of defects as obtained in Fig. 2b. If the pentacene layer is thinner, this effect is reduced which also increases the yield of the lift-off process. In general, for the chosen layer thicknesses the lift-off yield increases from < 20% for 80nm of pentacene to > 80% for 25nm thick films. Hence, for a structuring of pentacene films, the layer thickness should be preferably < 40nm.

However, in view of the roughness of pentacene, also other parameters such as resist treatment, exposure time, and / or etching procedure may be modified. The thickness of the photo-resist may be expected to be larger than for C₆₀ which is related to the better resist adhesion. Therefore, also

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larger exposure durations may be required. In detail, for 25nm thick pentacene films the dose was increased from 0.6s to 0.75s - 0.8s to compensate for the larger resist thickness. Such differences of exposure time are undesired if C₆₀ and pentacene have to be structured on the same substrate as it is required for e.g. complementary circuits. Therefore, different resist treatment processes are tested. An effective reduction of exposure time is achieved in two different ways. First, the samples can be annealed after resist deposition. Heating at 70°C for 1min reduces the exposure time to 0.6s. Unfortunately, such heating steps may not be applied to some organic materials. A second way to reduce the exposure time is to wait for at least 10min after resist deposition. The effect of annealing and waiting is similar. In either case, solvents can desorb of the resist which effectively reduces its thickness and therefore the exposure time.

The last step that may be modified for structuring of pentacene is the etching process. In contrast to C₆₀ where a spin-rinsing process is employed, etching on pentacene may require a less aggressive procedure owing to the enhanced resist adhesion. Thus, instead of this spin-rinsing, the pentacene samples are dipped into HFE 7300 for 4min which is less aggressive than HFE 7100. After this dipping, the samples are again dipped in fresh HFE 7300 for 30s in order to avoid Langmuir-Blodgett film formation on the organic material.

With these modifications of the patterning recipe, pentacene can be structured with a high resolution and a high process yield as known for C₆₀.

Following, the influence of photo-lithographic patterning on the OTFT performance is studied.

The buckyball C₆₀ molecule is chosen for these investigations since this material can be seen as a benchmark material for electron transporting organic semiconductors. Its high symmetry leads to highest mobility values reported for electron transporting organic semiconductors (cf. Zhang et al., J. Appl. Phys. 104, 104504 (2008), Kobayashi et al., Science and Technology of Advanced Materials 4, 371 (2003), Zhang et al., Appl. Phys. Lett. 93, 133305 (2008)). However, C₆₀ has the same tendency as most other electron transporting organic materials: water and oxygen can be

adsorbed easily and can act as trap states for charge carrier transport. To discuss influences of the lithography on OTFT performance, changes in threshold voltage, contact resistance, mobility, and subthreshold-swing in comparison to a reference device structured by shadow mask are discussed.

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Electron mobilities up to $5\text{cm}^2 / (\text{V s})$ have been reported (cf. Kobayashi et al., Science and Technology of Advanced Materials 4, 371 (2003), Zhang et al., Appl. Phys. Lett. 93, 133305 (2008), Virkar et al., Adv. Mat. 19, 1962 (2009)) for C_{60} using special surface treatments or low work function metals for source and drain electrodes. OTFTs prepared are not optimized for
10 highest charge carrier mobility. Nevertheless, charge mobilities obtained are within the state-of-the-art for C_{60} OTFTs. They can be further improved according (cf. Kobayashi et al., Science and Technology of Advanced Materials 4, 371 (2003), Zhang et al., Appl. Phys. Lett. 93, 133305 (2008), Virkar et al., Adv. Mat. 19, 1962 (2009)).

15 OTFT performance can be influenced by lithographic structuring in two ways. First, resist and solvent compounds will interact with the organic semiconductor. Second, there is an influence since the samples are exposed for several minutes to air and moisture before they are covered by the photo-resist. In order to distinguish between these two influences, the reference sample and the lithographically processed devices are exposed to air after the first characterization. After-
20 wards additional annealing steps are performed. In detail, after processing and the first measurement of fresh devices, the samples are exposed to air for one hour without protective resist and are heated afterwards for 1h in a nitrogen glove box at 100°C .

It is well known that C_{60} , which has been exposed to air can be reactivated in an oxygen-free at-
25 mosphere (cf. Fujimori et al., Solid State Comm. 89, 437 (1994), Matsushima et al., Appl. Phys. Lett. 91, 103505 (2007)) (nitrogen glove box or vacuum). Additional heating may reduce the required reactivation time. C_{60} contains two dominant trap levels, namely deep one (0.4eV below the conduction level) and a shallow one (0.2eV below the conduction level) which is mainly caused by physisorption of oxygen and water. These shallow trap states can be healed by heating

under vacuum conditions or inert atmosphere. Accordingly, the post-annealing step should help to remove the residuals of water and oxygen remaining in C₆₀. Thus, changes of OTFT parameters (threshold voltage, contact resistance, mobility) that can be reversed by the annealing procedure are likely caused by the accidental influence of water and oxygen and not by the lithography itself.

Fig. 3 shows graphical representations for the transfer characteristic and current-voltage curves (inset) of a lithographically structured OTFT in comparison to a reference device.

The transfer characteristics ($V_{DS}=8V$) of lithographically (dotted line) and shadow mask patterned (closed line) C₆₀ OTFTs are shown. The transistors have a channel length of 30 μm and a channel width of 300 μm , respectively. The short dotted curve denotes the performances directly after deposition. The short dashed curve shows the OTFT performance after one hour under ambient conditions (measurement in nitrogen) and the dashed line after an annealing of one hour at 100°C in a nitrogen glove box. The inset shows the current-voltage characteristics of the lithographically processed device. The gate-source voltages are: 2V, 3V, 4V, 6V, 8 V. The gate insulator is a 50nm layer of Al₂O₃ (ALD processed).

In general, both devices show typical OTFT performance, which means a clear off-state, a linear regime, and a saturation if V_{DS} exceeds $V_{GS} - V_{th}$. Nevertheless, there are clear differences between reference OTFTs and lithographically structured OTFTs. Obviously, there is a shift in threshold voltage and a reduced on-state current.

In detail, the threshold voltage is shifted between the fresh reference sample ($V_{th}=1.4V$) and lithographically produced sample ($V_{th}=2.3V$) by 0.9V (values are summarized in Table 1 below).

The threshold voltage of the lithographically produced sample further increases to $V_{th}=3.8V$ if the sample is exposed to air for one hour. If the sample is annealed, the threshold voltage decreases again to $V_{th}=3.4V$. Thus, oxygen exposure increases threshold voltage. This effect can be partial-

ly compensated by heating. Focusing on the reference sample, a similar tendency of threshold voltage shift can be obtained. After air exposure, a threshold voltage of 3.3V is measured. This threshold is reduced to 2.3V after annealing. The threshold shift presumably arises because of water absorbed at the dielectric interface. These states, acting also a trap states, are not removable by the simple annealing procedure done here. They are caused by strongly bound hydroxyl groups at the insulator material. Utilizing highly hydrophobic gate dielectrics as e.g. polymers might help to reduce this effect. Differences in total values of threshold voltage likely arise from the fact that OTFTs produced by lithography have been exposed to air for a longer time and no annealing has been employed after structuring.

Table 1

	V_{th} (V)	Contact Resistance			Mobility ($cm^2/(Vs)$)	SS-Swing (mV/dec)
		(kΩcm)				
		$V_{GS} = 4V$	$V_{GS} = 6V$	$V_{GS} = 8V$		
Reference						
fresh	1.4±0.1	8.9 ± 0.8	6.8 ± 0.8	6.1 ± 0.5	0.17±0.02	580 ± 20
1h air	3.3±0.1	22.3 ± 1.6	14.0 ± 1.2	11.4 ± 1.1	0.14±0.02	600 ± 20
1h at 100°C	2.3±0.1	14.4 ± 1.4	10.5 ± 1.2	8.3 ± 0.7	0.15±0.02	610 ± 20
Lithography						
fresh	2.3±0.1	43.7±12.5	34.5 ± 8.5	30.1 ± 3.4	0.13±0.02	510 ± 20
1h air	3.8±0.1	96.5±11.7	46.8 ± 5.6	30.7 ± 3.6	0.10±0.02	280 ± 40
1h at 100°C	3.4±0.1	71.6 ± 6.1	38.2 ± 3.8	22.7 ± 4.1	0.11±0.02	250 ± 40

With respect to Table 1, the following parameters are depicted: threshold voltage, contact resistance, mobility, and subthreshold-swing (SS-swing) for reference C₆₀ OTFTs and the lithographically processed transistors. The mobility and threshold voltage are determined for long channel devices (channel length 30 μm). Mobility is taken from the slope of the transfer curve at $V_{GS} = 5V$. The standard deviations are taken from variations of three OTFTs for each channel length and from fitting using the transmission line method, respectively.

Furthermore, a comparison of the transfer curves and on-state currents suggests that the transfer curve of the lithographically produced sample is merely parallel shifted for $V_{GS} > 5V$. Accordingly, mobility determined in this OTFT geometry is only slightly influenced (see Table 1). This fact indicates that the transport properties of C_{60} are only slightly affected and annealing is sufficient to remove oxygen and water related trap states in C_{60} . Apart from this, for $V_{GS} < 5V$ a steeper rise of the transfer curve is observed for lithographically produced samples. This increase in subthreshold-swing becomes more pronounced for larger threshold voltages (see Table 1).

- 10 In contrast, the subthreshold-swing of the reference device (fresh, 1h air, annealing at 100°C for 1h) is slightly affected (580mV/dec, 600mV/dec, 610mV/dec) in comparison to lithographically generated samples. However, assuming that the threshold shift is the only influence of lithographic structuring, changes in subthreshold-swing cannot be explained consistently. This is caused by the fact that an increased number of interface states would lead to an increased threshold voltage and an increased subthreshold-swing. The subthreshold-swing for the reference devices, however, is constant which implies that qN_{IT} is larger than C_i (this means $N_{IT} > 10^{12}cm^{-2}$) (q - elementary charge, N_{IT} - density of interface states ($1/(cm^2 eV)$), C_j - specific capacitance of the gate insulator).
- 20 In case of lithographically prepared OTFTs, the subthreshold-swing is lowered by annealing which suggests, in contradiction to the reference devices, a reduced number of interface states. As it will be pointed out, this discrepancy can be explained by the fact that lithographic structuring leads to an increase of contact resistance.
- 25 Following, studies on the relation of contact resistance and mobility are described.

The on-state current for lithographically made samples is smaller than for the reference sample. Besides mobility, an important parameter which may affect the on-state of the field-effect transistor is the contact resistance (R_C). R_C is determined using a transmission line model (cf. Necliudov

et al., Solid State Electron. 47, 259 (2003)) for all tested types of devices.

Fig. 4 shows a transistor resistance $R_{\text{Ch}+2\text{C}}$ (channel + contact) of lithographically produced OTFTs for different channel lengths ($V_{\text{DS}}=2\text{V}$). The curves denote different gate-source voltages: $V_{\text{GS}}=4\text{V}$ (40), $V_{\text{GS}}=6\text{V}$ (41), and $V_{\text{GS}}=8\text{V}$ (42). The contact resistance R_{C} (inset) is estimated from the intersection at zero channel length.

The contact resistance is evaluated from a channel length variation between $30\mu\text{m}$ and $100\mu\text{m}$. The gate-source voltage dependence (inset) of contact resistance indicates a field dependent injection mechanism. Table 1 shows that lithographically prepared samples exhibit a stronger field dependence of contact resistance than the reference. Furthermore, a contact resistance four to five times larger than for the reference devices is obtained for the lithographically patterned OTFTs. Lithographically made OTFTs exhibit a contact resistance above these previously reported values.

For low gate-source voltage, significant differences in contact resistance of lithographically produced samples are obtained for different post-treatment steps. These differences presumably arise because of the threshold voltage shift for the various post-treatment steps. However, for a gate-source voltage of 8V , the contact resistance of lithographically produced OTFTs is almost independent of the post-treatment step. In consequence, since for all post-treatment steps similar values of contact resistance are obtained for $V_{\text{GS}}=8\text{V}$, it can be deduced that there is almost not effect of air and water related trap states in C_{60} on R_{C} . Accordingly, the increased R_{C} is a direct consequence of the lithographic patterning.

Fig. 5a and 5b show graphical representations of XPS measurements of the C 1s signal of a C_{60} film after removing Ortho 310 in comparison to a C_{60} film as evaporated (Fig. 5a) and the F 1s signal of a C_{60} film after removing Ortho 310 (Fig. 5b), respectively. The spectra are fitted with multiple peaks, assuming a full width at half maximum (FWHM) in the range of 1.0 to 2.0eV and

a Lorentzian to Gaussian contribution (L/G) between 20 and 40. A Shirley background is subtracted in all graphs.

This effect presumably appears because of resist residuals between the semiconductor and the source / drain electrode. This assumption is confirmed by the XPS investigations. In particular, an XPS signal is obtained that can be attributed to fluorine, a main component of photo-resist and solvent used here. Consequently, there are partial solvent / resist residuals on the C₆₀ film.

For comparison, Fig. 5a and 5b also show the carbon related XPS signal for a pristine C₆₀ film and a C₆₀ film processed by lithography. In detail, the signal of the C 1s core level of the pristine C₆₀ film can be fitted with one main peak at 284.8eV, which is generally attributed to pure carbon compounds. Moreover, the spectrum contains also several shake peaks generally observed for C₆₀. In comparison, the signal of the C₆₀ film after removing Ortho 310 has lightly changed. One additional peak at 292.1eV is observed, which lies in the range of reported CF₂ and CF₃ bonds and hence it can be attributed to carbon which is directly bound to fluorine. The main peak is broadened indicating that two states are present: one again at 284.8eV and a second with a small chemical shift of 0.2eV. This shifted peak can be assigned to carbon atoms in the resist which are not directly bound with fluorine but affected by its strong electronegativity. Due to this fact and presence of fluorine signal, it can be concluded that there is still some resist left after removal. However, the presence of an unaffected C-C signal, attributed to the pristine C₆₀, indicates that the thickness of these residuals should be in the range of a few monolayers. Nevertheless, XPS investigations clearly disclose the presence of resist residuals on the C₆₀ film. Such residuals cause the increased contact resistance for lithographically made devices as summarized in Table 1. Beside its influence on contact resistance, the effect of resist residuals can be seen in the determined value of mobility which is slightly lower for lithographically made OTFTs than for the reference devices (see Table 1).

The problem of resist residuals is known as such for photo-lithography procedures. Such residuals are typically removed by a descum oxygen plasma etch process. Unfortunately, in the present

case such processing cannot be directly applied to organic semiconductors, due to oxidation of C₆₀.

In summary, lithographically manufactured OTFTs show an increased threshold voltage shift arises because of water and oxygen related trap states at the dielectric interface. Furthermore, a sufficient healing of C₆₀ by vacuum / glovebox annealing can be deduced. This can be seen in an almost unaffected mobility (parallel shifted transfer curve for $V_{GS} > 5V$). However, an increased contact resistance caused by resist residuals on C₆₀ is obtained. A strong field dependence of contact resistance for lithographically prepared samples likely causes a steeper subthreshold-swing.

With respect to photo-lithographic patterning of organic semiconductors, in the following two applications for organic TFTs are discussed: inverter circuits and OTFTs as drivers in OLED displays.

Lithographically patterned OTFTs were found suitable for both applications. However, some limitations for the usage of OTFTs may apply in such circuits. These limitations which are not specific to lithographically made devices may arise from the low transconductance of organic thin-film transistors. This leads either to considerable power losses in case of display drivers or to low switching frequencies in case of organic inverters. The low transconductance can be seen as a direct consequence of the low charge carrier mobility in organic materials and the limited scalability of OTFTs as discussed in the previous subsection. These performance restrictions are not only relevant for lithographically structured OTFTs having an enlarged contact resistance; it can be shown that an equivalent performance to shadow mask patterned OTFTs may be reached, for example, if a special electrode preparation is employed.

Following, OTFTs for OLED display drivers are considered. A green OLED driven by a lithographically produced OTFT was prepared. The layer stack and the OLED performance as such are described in (cf. He et al., Proc. SPIE 26, 5464 (2004), He et al., Appl. Phys. Lett. 85, 3911 (2004)).

A transistor comprising C_{60} with a channel length of $30\mu\text{m}$ and a channel width of 24mm is employed. The ratio between the active area of the OLED and the driving transistor is larger than 4 in this case (including OTFT contact pads). This ratio can be increased for smaller feature sizes since the photolithography technique enables to scale down the OTFT size.

Fig. 6 shows results for an OLED driven by a C_{60} OTFT. Curve 60 shows the current through the OLED for different voltages applied across the OLED. Curve 61 displays the luminance of the OLED driven by the OTFT for different gate-source voltages. The inset shows external quantum efficiency (EQE, open circles) and power efficiency (P_{eff} , closed rectangles) for different luminance values.

Fig. 6 depicts the luminance of the green OLED for different gate-source voltages at a fixed drain-source voltage of 12V . The higher drain-source voltage, in contrast to Fig. 1, is required to obtain the saturation regime of the OTFT with the OLED in series. Nevertheless, the highly efficient OLED used here guarantees a minimum of driving voltage: a luminance of 1000cd/m^2 is achieved for voltages less than 4V (voltage drop across the OLED). As shown in Fig. 6, an increase in luminance is obtained for increasing gate-source voltage and 1000cd/m^2 are exceeded at 9V . This clearly shows that even without aggressive scaling of driving OTFTs, sufficient luminance of OLED pixels can be achieved. Unfortunately, a comparison of the power efficiency P_{eff} of OLED driven by the OTFT and the pure OLED (60 lm/W , compare (cf. He et al., Appl. Phys. Lett. 85, 3911 (2004))), exhibits that 55 to 70% (depending on the luminance) of the provided electrical power is consumed by the driver.

Following, a combination of two transistors within an inverter circuit is considered as a second application for organic thin-film transistors.

In this context, the patterning of source and drain electrodes on top of organic materials may be applied for fabrication of unipolar inverters. In particular, in order to design such inverters, pho-

- 20 -

to-lithography can help matching the characteristics of the individual OTFTs which significantly improves the inverter gain. Moreover, as a consequence of the increased inverter gain for matching OTFTs, the integration density of transistors can be increased. These points exhibit a clear and strong advantage in comparison to shadow mask fabrication. However, this is not the only advantage of photo-lithographic patterning of inverters since photo-lithography can also be employed to design complementary inverters. Such complementary circuits are superior to unipolar and pseudo-complementary circuits since they offer a higher gain or the inverters, a higher integration density, and less effort in terms of circuit design.

In Fig. 7a to 7h, a procedure for manufacturing a complementary inverter employing fluorine based photo-lithography is depicted.

A two-step procedure was used. In a first step, after substrate cleaning and HMDS treatment, on a gate layer 71 (n-Si-substrate 70) and a gate insulator layer 72 an organic semiconducting layer 73 made of a thin layer of pentacene serving as p-channel material is deposited (see Fig. 7a). The organic semiconducting layer 73 is covered by photo-resist layers 74 and 75 and structured by photo-lithography as explained above. After the development of photo-resist, the organic semiconducting layer 73 is removed from the uncovered areas by e.g. an oxygen plasma etch process (radio-frequency plasma) (see Fig. 7d).

In a second deposition step, a further organic semiconducting layer 76 made of C_{60} is deposited as n-channel material (see Fig. 7e). To remove spare C_{60} the sample is dipped in HFE 7300 in nitrogen atmosphere (see Fig. 7f). In this way, the organic semiconducting layer 73 (pentacene) and the further organic semiconducting layer 76 (C_{60}) can be structured on the same substrate with a high spatial resolution. The latter aspect is of particular importance for fabrication of high-frequency devices. To finalize the inverter structure, a second lithography step as described above is employed to pattern source and drain electrodes 77 (see Fig. 7g, 7h - coating, exposure, and development of Ortho 310 and ma - P1210, and gold deposition and lift-off in HFE 7300).

A microscope image of the inverter circuit before deposition of the electrodes is shown in Fig. 8. Fig. 8 shows a microscope image of a photo-resist pattern of two OTFTs on pentacene and C₆₀. The channel length of both devices is 20 μm.

- 5 Fig. 9 shows a graphical representation of input vs. output voltage (switching characteristics) of the complementary organic inverter fabricated by fluorine based photo-lithography.

The channel length is 50 μm for the p-channel transistor and 62 μm for the n-channel OTFT, respectively. The right axis shows the gain of the inverter. The n- and p-channel OTFT have the
10 same channel width, however, the channel length is chosen with respect to the individual OTFT performance in order to guarantee a switching of the inverter at $V_{DD}/2$. In detail, the channel length of the pentacene p-channel transistor is 50 μm, while the C₆₀ n-channel transistor has a channel length of 62 μm for the inverter shown in Fig. 9. As can be seen in Fig. 9, caused by this adjustment of channel length, the inverter switches at $V_{DD}/2$ showing an inverter gain above 4.

15 Although this inverter shows a reasonable on/off swing, apparently it does not reach V_{DD} for $V_{in} = 0$. This can be attributed to the fact that even if the inverter is balanced, the pentacene transistor is not perfectly in the off-state for $V_{in} = 0$ (the threshold voltage is slightly negative). Thus, this yields a static current flow across the p-channel transistor for $V_{in} = 0$ and consequently, V_{out} does
20 not reach V_{DD} for $V_{in} = 0$. A further consequence of the asymmetry of threshold voltage is the fact that both transistors are not working perfectly in the linear regime at $V_{in} = V_{DD}/2$ (the resistances of both OTFTs in the linear regime are not perfectly matching). This discrepancy leads also to a static current flow and consequently to a reduced inverter gain. In particular, the inverter gain is inversely proportional to the difference between the resistances of both transistors and
25 minute variations of the inverter balance can cause significant differences in the inverter gain.

Photo-lithographically structured OTFTs as discussed above may be restricted in their performance by the increased contact resistance which is equivalent to an enlarged transfer-length. Such possible restrictions, however, may at least in part be compensated by a special preparation

of electrode(s), e.g. source and drain electrodes, namely “molecular interface doping”. The same method can analogously be employed, for example, to n-channel OTFTs and other organic electronic devices for which a lift-off structuring process is used.

- 5 According to Fig. 10a to 10c, on a substrate 100 a gate layer 101 and a gate insulator layer 102 are deposited. On the gate insulator layer 102 an organic semiconducting layer 103 made of an organic semiconductor material is deposited. In order to structure e.g. source and drain electrodes of an organic thin-film transistor a lithographic patterning as described e.g. in Fig. 1 is employed. In the present example a bilayer photo-resist structure of Ortho 310 (104) and ma-P 1210 (105) is deposited onto the organic layer 103. According to Table 1, Fig. 4 and Fig. 5 charge carrier injection from the electrode into the organic semiconductor material may be hindered by residuals of photoresist. To improve the injection in the OTFT, a contact improving layer 106 (thickness: 1nm) of the strong acceptor compound F₆-TCNNQ is deposited on the organic semiconducting layer 103 which in turn is at least partially covered with a residual layer made of residual photo resist material left over from a former photolithographic process. In order to avoid a doping effect of the acceptor compound F₆-TCNNQ on the channel area provided in the organic semiconducting layer 103, the contact improving layer 106 is patterned by the resist mask (layers 104 and 105) used for deposition for source and drain electrode 107 (see Fig. 10f and 10g).
- 20 Fig. 11a and 11b show the I-V-curves and the transfer characteristics of two lithographically structured OTFTs with and without interface doping. Fig. 11a shows the transfer characteristics (V_{DS} = -6V), and Fig. 11b shows I-V-curves of two pentacene OTFTs structured by fluorine based photo-lithography (channel length 100μm, channel width 1mm, 50nm Al₂O₃ serves as the gate insulator). Closed lines show the performance of the transistor with interface doping and dashed lines without interface doping. The gate source voltage for Fig. 11b are provided within the Figure.
- 25

As shown there, the thin contact improving layer (injection layer) significantly improves the transistor performance. In particular, the off-state current and the threshold voltage are unaffected

which means that no free charge carriers are present in the channel. Hence, the dopant merely influences the interface at source and drain electrode.

This effect of interface doping can be seen in the on-state current of the transistor. More specifically, the on-state current for $V_{GS} > V_{th}$ is strongly increased for doped devices whereas the sub-threshold regime is only weakly affected. Within the subthreshold regime, the OTFT performance is not governed by injection of charge carriers, but dominated by the interface properties in the channel. In contrast, above the threshold-voltage, the OTFT behaviour is restricted by the number of charge carriers injected from the source electrode. Hence, since interface doping can effectively reduce injection barriers for charge carriers, a larger on-state current is measured for doped devices. Furthermore, this experiment on interface doping shows in an unambiguous way that the performance of organic thin-film transistor is restricted by charge carrier injection even for long channel devices. For the devices shown in Figure 106 (long channel devices $L=100\mu m$), the current-voltage curves suggest an increased charge carrier mobility for doped devices ($0.1 cm^2 / (Vs)$ doped, $0.19 cm^2 / (Vs)$ doped, measured at $V_{GS}=V_{DS} = -6V$). Since the channel region is undoped, this has to be seen as an effect of the increased charge carrier density in devices with an injection layer.

To quantify the improvement of charge carrier injection, the contact resistance is measured using the transmission line method. Results of a lithographically patterned OTFT with and without interface doping and a reference OTFT structured by a shadow mask are shown in Fig. 12 which shows the contact resistance estimated by transmission line method for lithographically made OTFTs with (rectangles) and without interface doping (circles). Furthermore, the contact resistance for shadow mask produced OTFT (same layer thickness, geometry, and substrate, without doping) is shown (triangles). The applied source-drain voltage is $-1V$.

As can be seen, the contact resistance is effectively lowered if “interface doping” (contact improving layer(s)) is employed. Moreover, doped OTFTs can even beat the reference device produced by shadows mask.

Although there are resist residuals on the pentacene, the dopant can effectively provide charge carriers to the matrix. Since this is may not be expected for a closed layer of photo-resist covering the pentacene, it may be concluded that the thin photo-resist film covers the pentacene only partially and hence dopant molecules are in direct contact to the semiconductor material.

It was shown that the high-mobility small molecule organic materials, for example, pentacene and C60, are compatible to photo-lithographic processing under ambient conditions. This may be accomplished by using, for example, a highly fluorinate photo-resist and solvents which are chemically benign to these materials. A reliable lithography process is established. The process proposed also accounts for the different film properties of the organic materials, in particular for the layer roughness of pentacene films.

Organic thin-film transistors are fabricated using this lithography protocol and their performance is compared to reference devices patterned by shadow masks. In this way, influences arising from the lithography procedure and the accidental effects caused by air exposure can be distinguished. Latter ones affect the threshold voltage of the OTFTs, but not charge carrier transport in general. In this context, thermal annealing may help in recovering the transistor performance, and hence a similar charge carrier mobility is observed for lithographically made OTFTs and reference devices. Nevertheless, resist residuals may increase the contact resistance in lithographically patterned OTFTs. In consequence, down-scaling of such OTFTs does not follow the prediction as formulated within the gradual channel approximation. Most notably, the transistor performance is predominantly governed by the transfer length if the channel length is less than $30\mu\text{m}$. This enlarged transfer length can be directly associated to the large contact resistance.

Lithographically made OTFTs are suitable for applications as e.g. driving transistors in OLED displays or as switches in inverter circuits. In particular, the good scalability of photo-lithography exhibits a considerable advantage in comparison to state-of-the-art structuring techniques as e.g.

- 25 -

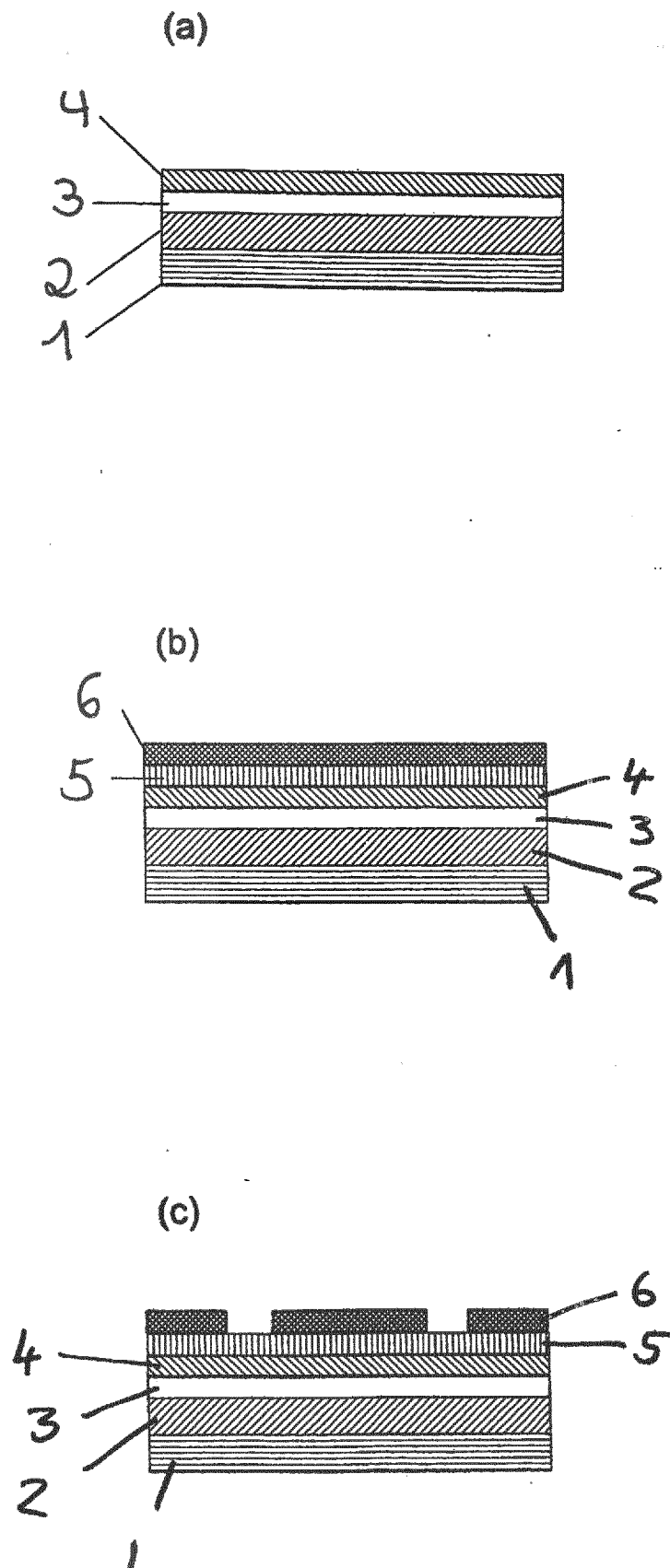
shadow mask patterning. Interface doping may be used as a method for reducing the contact resistance and improving the performance of lithographically patterned OTFTs.

5 The features disclosed in this specification, the figures and / or the claims may be material for the realization of the invention in its various embodiments, taken in isolation or in various combinations thereof.

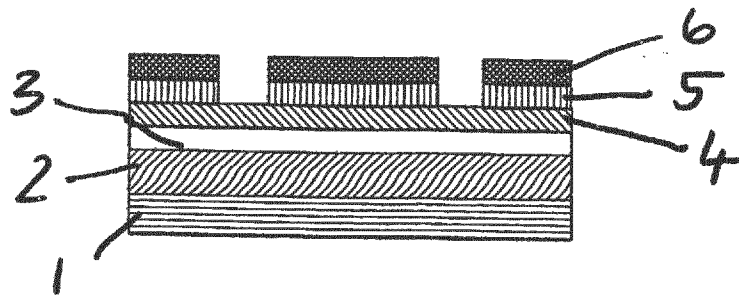
Claims

1. A method of manufacturing an organic electronic device, comprising:
 - providing a layered device structure, the layered device structure comprising a plurality of electrodes and an electronically active region being provided in electrical contact with at least one of the plurality of electrodes, said providing of the layered device structure comprising steps of
 - providing an organic semiconducting layer,
 - applying a structuring layer to the organic semiconducting layer, the structuring layer having a first region and a second region, the first region being covered by a layer material,
 - applying a contact improving layer to the structuring layer by depositing at least one of an organic dopant material and an organic dopant-matrix material at least in the first region,
 - depositing a layer material on the contact improving layer at least in the first region, and
 - removing the structuring layer at least in the second region.
2. Method according to claim 1, further comprising a lift-off structuring process.
3. Method according to claim 1 or 2, wherein said providing the structuring layer further comprises using a photo lithographic process.
4. Method according to claim 3, wherein said using the photo lithographic process further comprises:
 - depositing a photo resist cover on the organic semiconducting layer and
 - structuring the photo resist cover, said structuring comprising steps of illuminating and removing the photo resist cover, thereby at least partially removing the photo resist cover in at least the second region, but not the first region.
5. Method according to claim 4, wherein said depositing the photo resist cover further comprises:
 - depositing a protection layer on the organic semiconducting layer, and

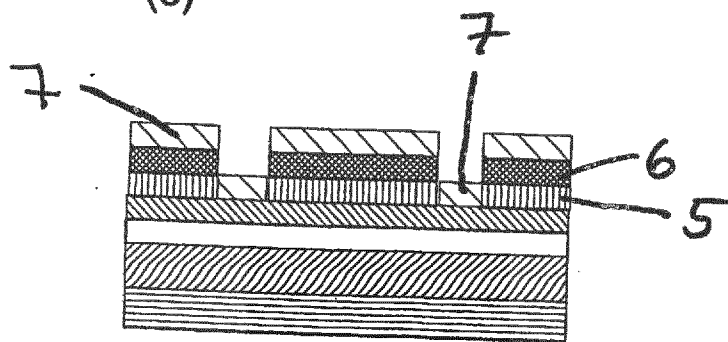
- depositing a photo resist layer on the protection layer.
6. Method according to claim 4 or 5, wherein said etching of the photo resist cover further comprises providing a non-closed residual layer made from non-removed residuals of the photo resist cover in the first region.
5
 7. Method according to one of the preceding claims, further comprising a step of providing a structured electrode layer made of an electrode material.
 - 10 8. Method according to one of the claims 1 to 5, further comprising a step of providing a structured non-electrode layer made of a non-electrode material.
 9. Method according to claim 3 or one of the claims 4 to 8, referring to claim 3, wherein the photo lithographic process is performed by using a fluorine based photo lithography.
15
 10. Method according to one of the preceding claims, wherein the contact improving layer is provided with a layer thickness of about 1 nm to about 100 nm.
 11. Method according to one of the preceding claims, wherein said providing the layered device structure comprises providing a device selected from the following group: organic field effect transistor, an organic circuit assembly, organic light emitting device, and organic photovoltaic device.
20
 12. An organic electronic device, comprising
25
 - a layered device structure, the layered device structure comprising a plurality of electrodes and an electronically active region being provided in electrical contact with at least one of the plurality of electrodes,
 - in the layered structure, an organic semiconducting layer comprising a first region treated in a photo lithography process, and
30
 - a layer stack deposited on the first region, the layer stack comprising a structured layer and a contact improving layer provided between and in contact with the first region and the structured layer.



(d)



(e)



(f)

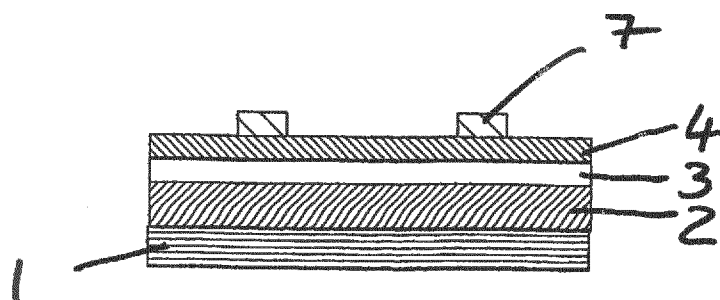


Fig. 1

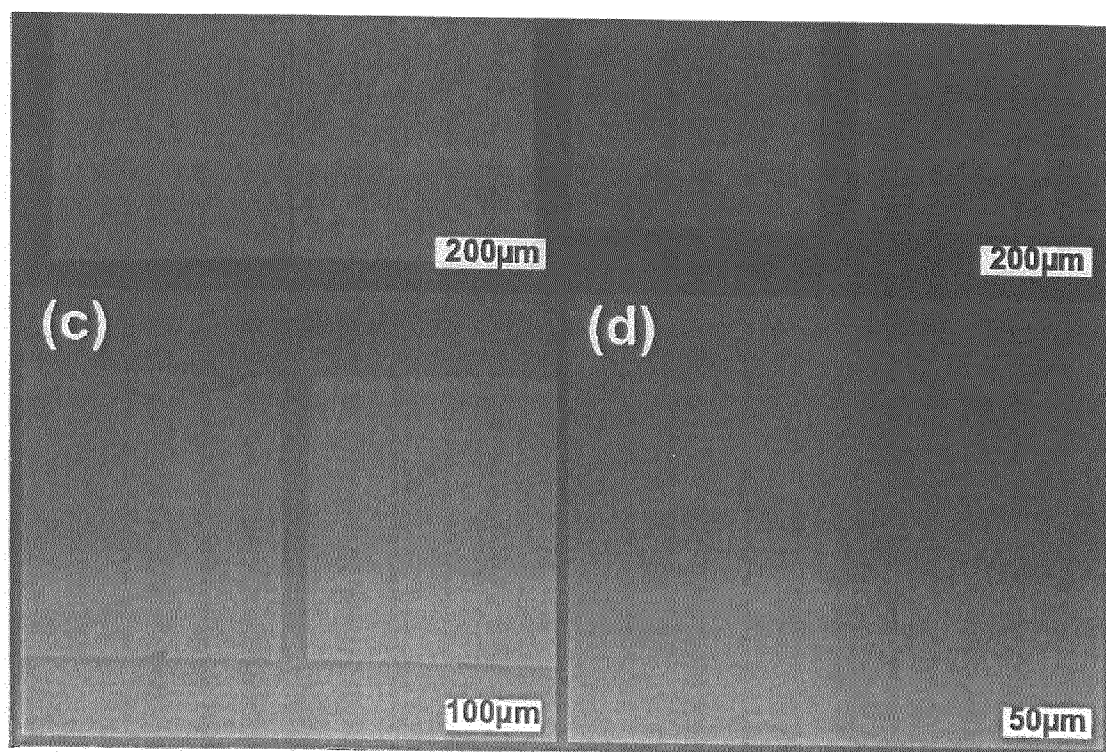


Fig. 2

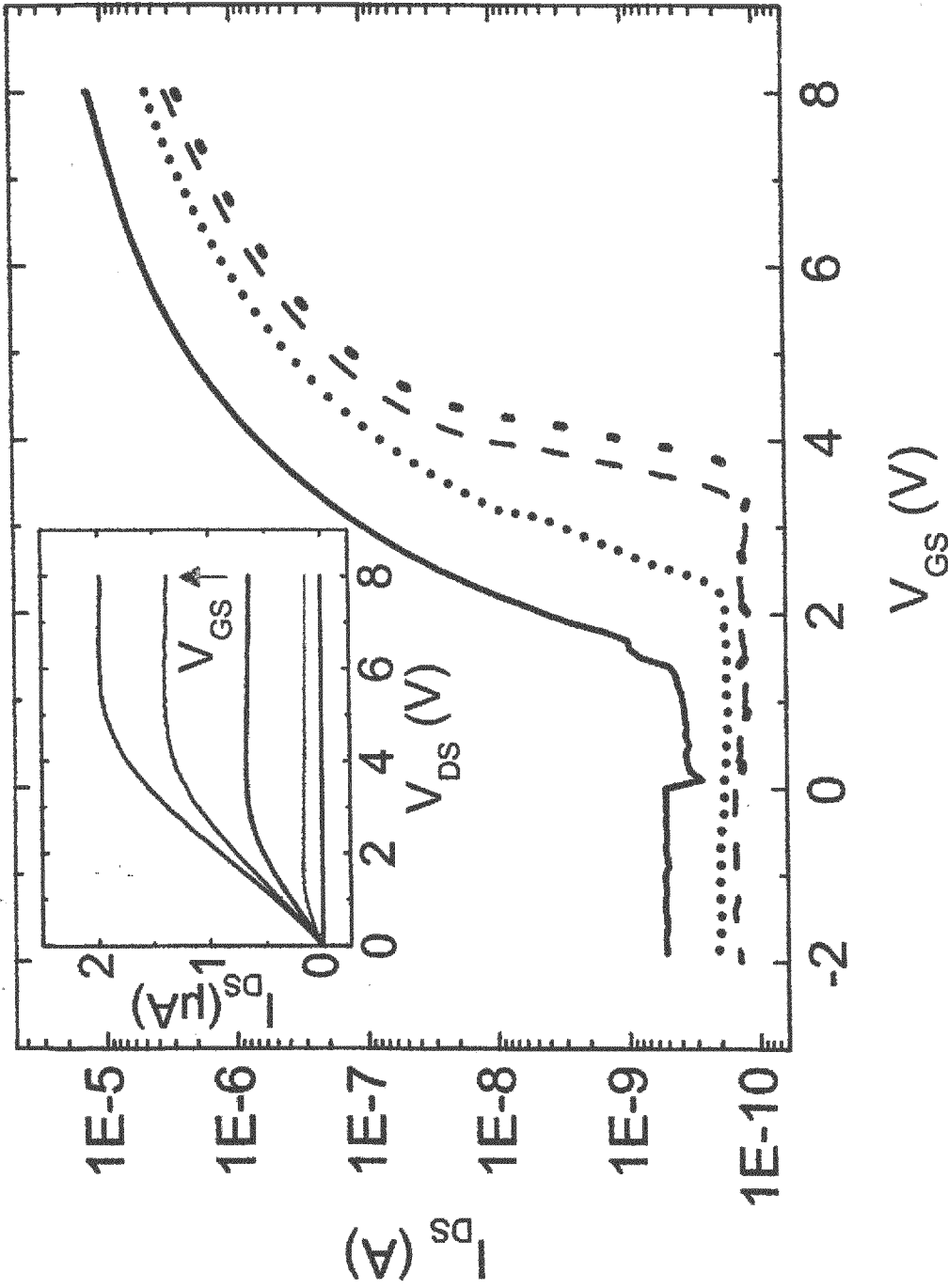


Fig. 3

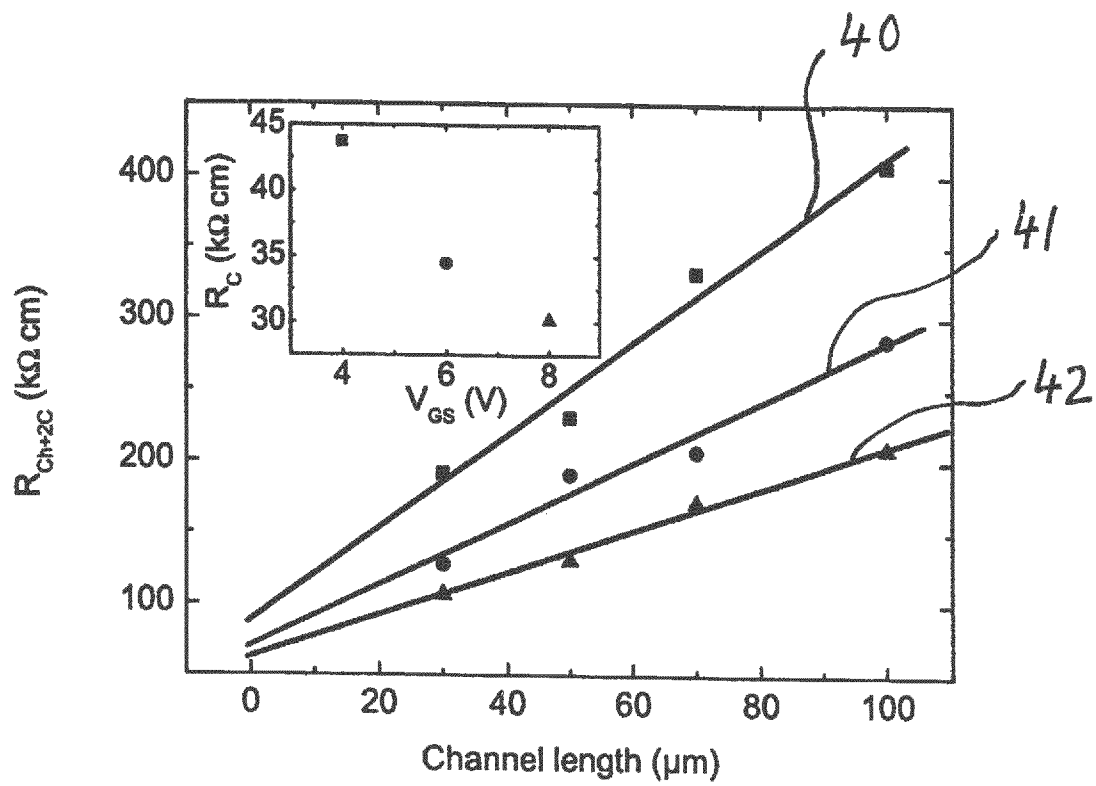
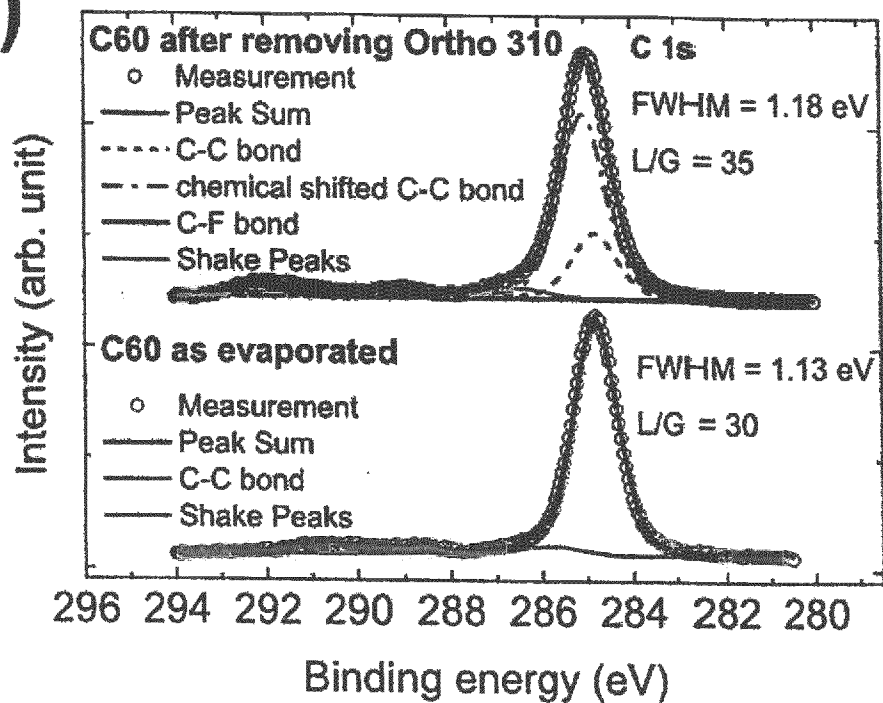


Fig. 4

(a)



(b)

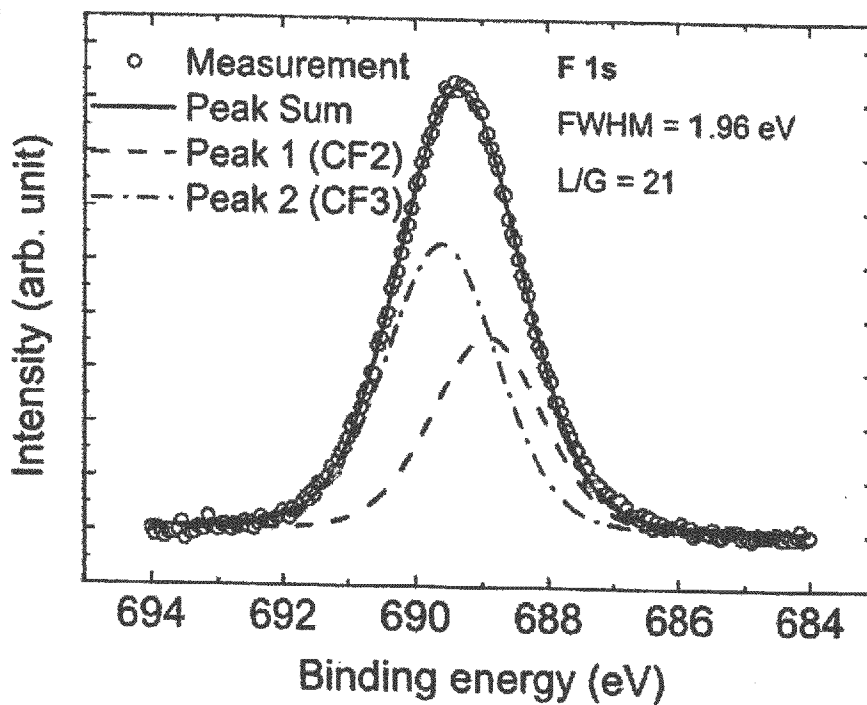


Fig. 5

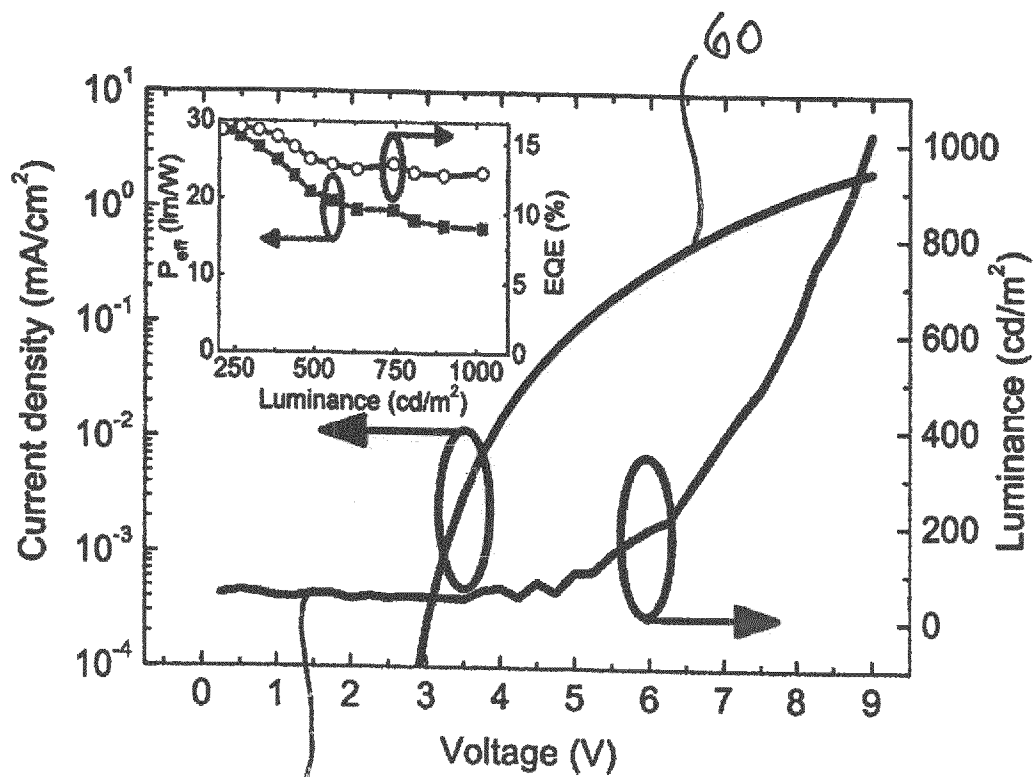


Fig. 6

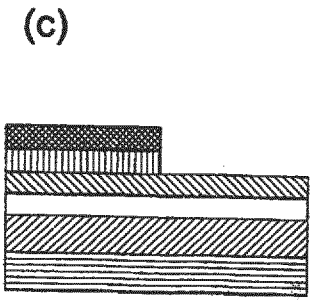
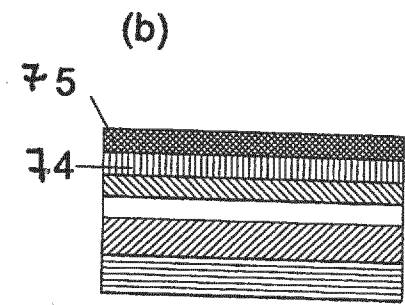
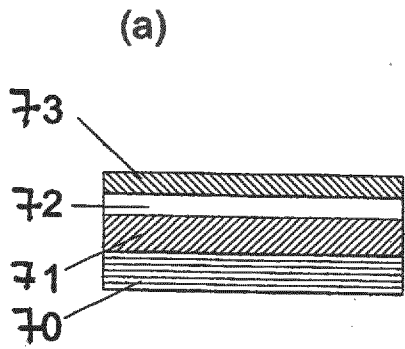
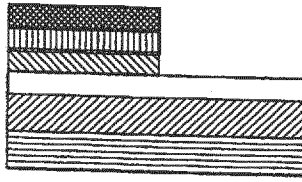
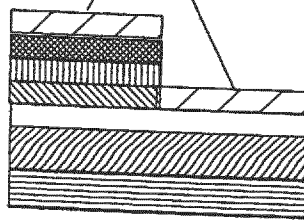


Fig. 7

(d)



(e) 76



(f)

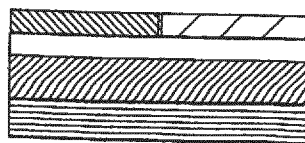
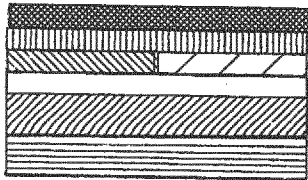


Fig. 7

(g)



(h)

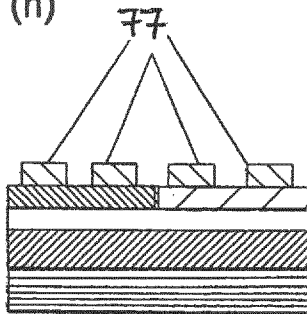


Fig. 7

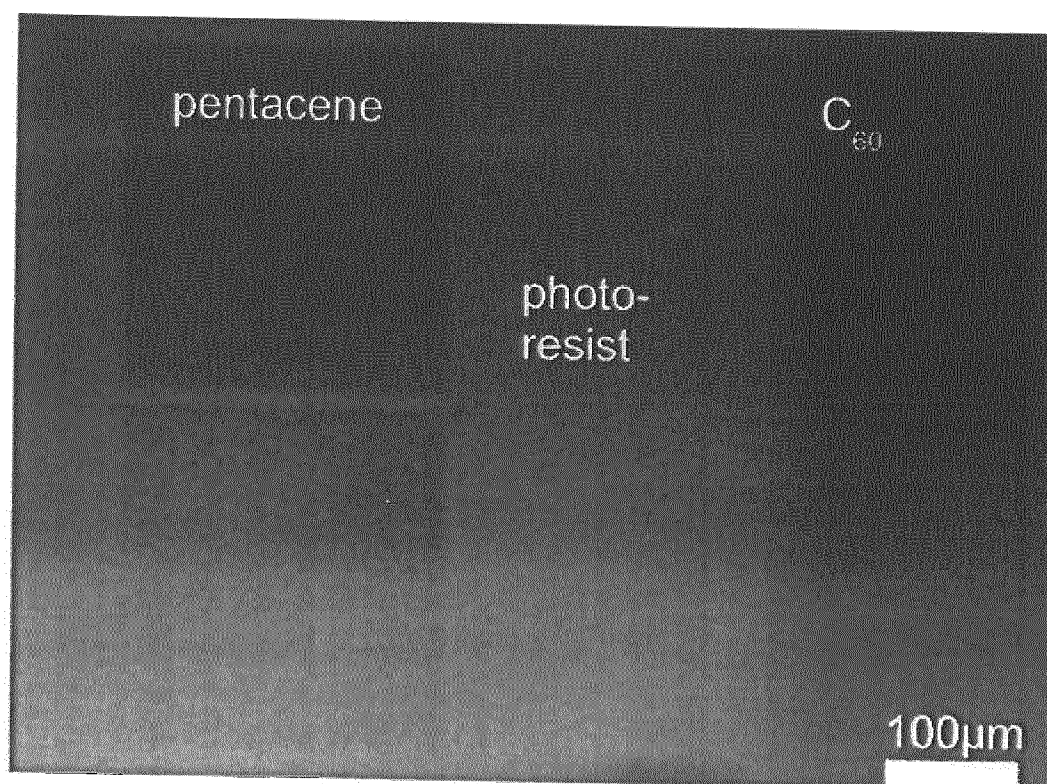


Fig. 8

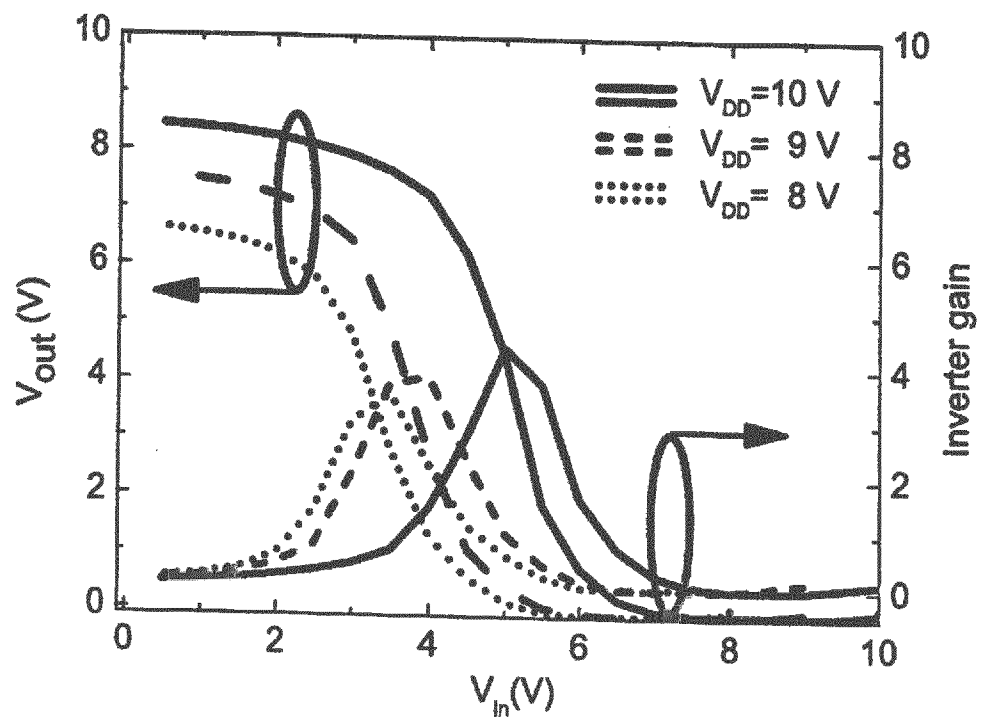
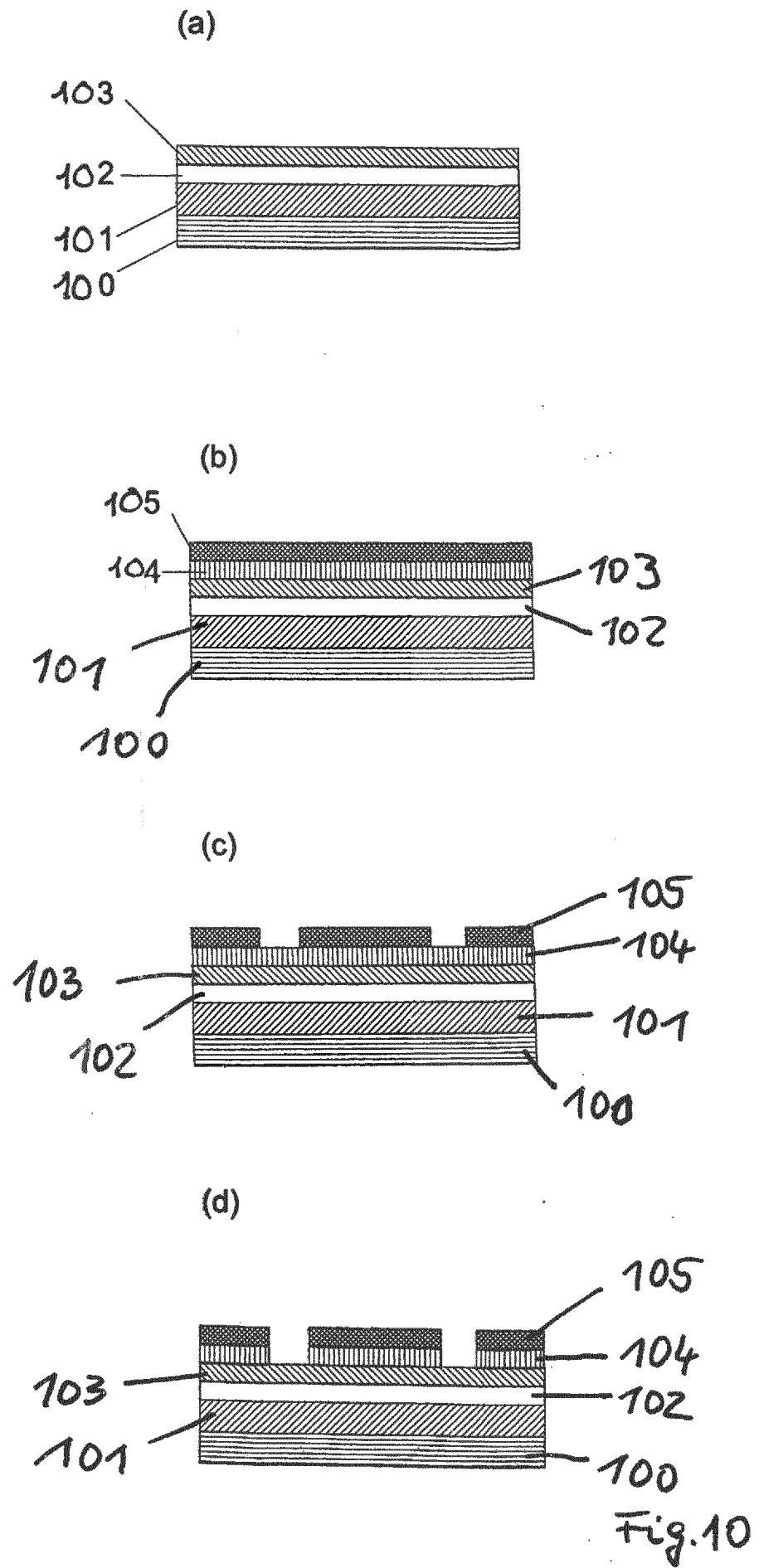
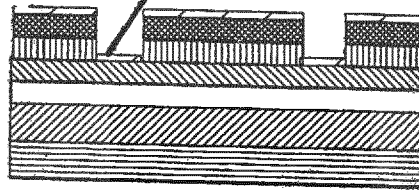


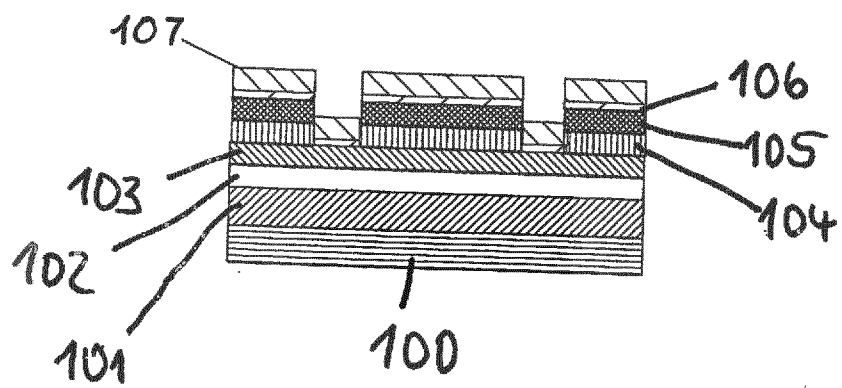
Fig. 9



(e) 106



(f)



(g)

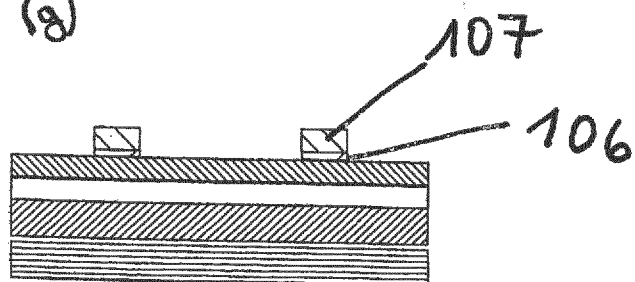


Fig. 10

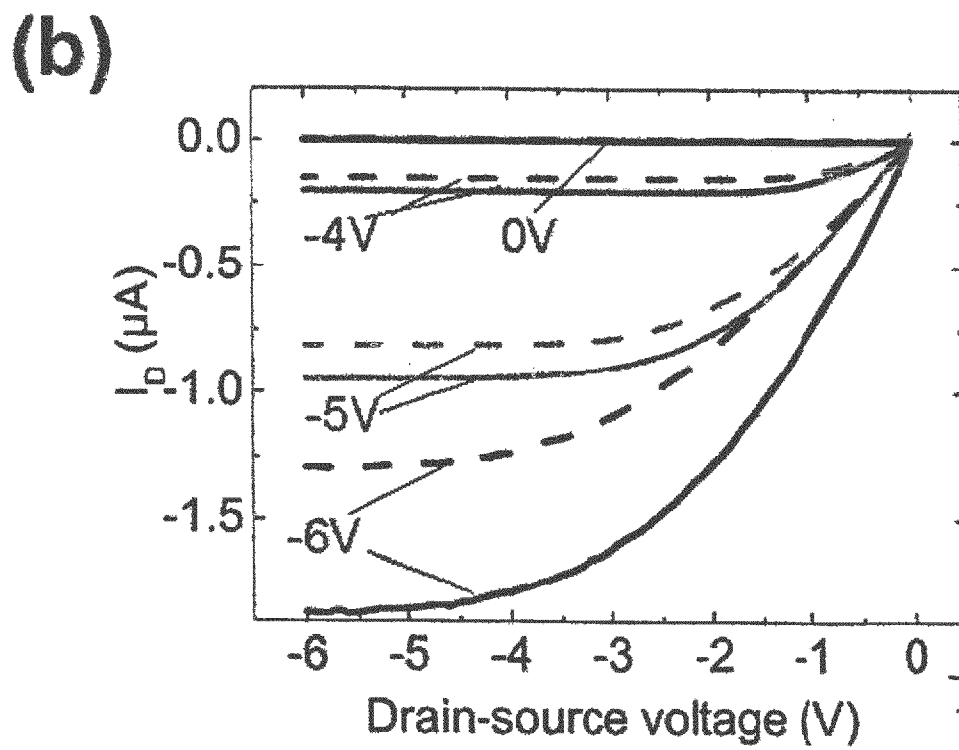
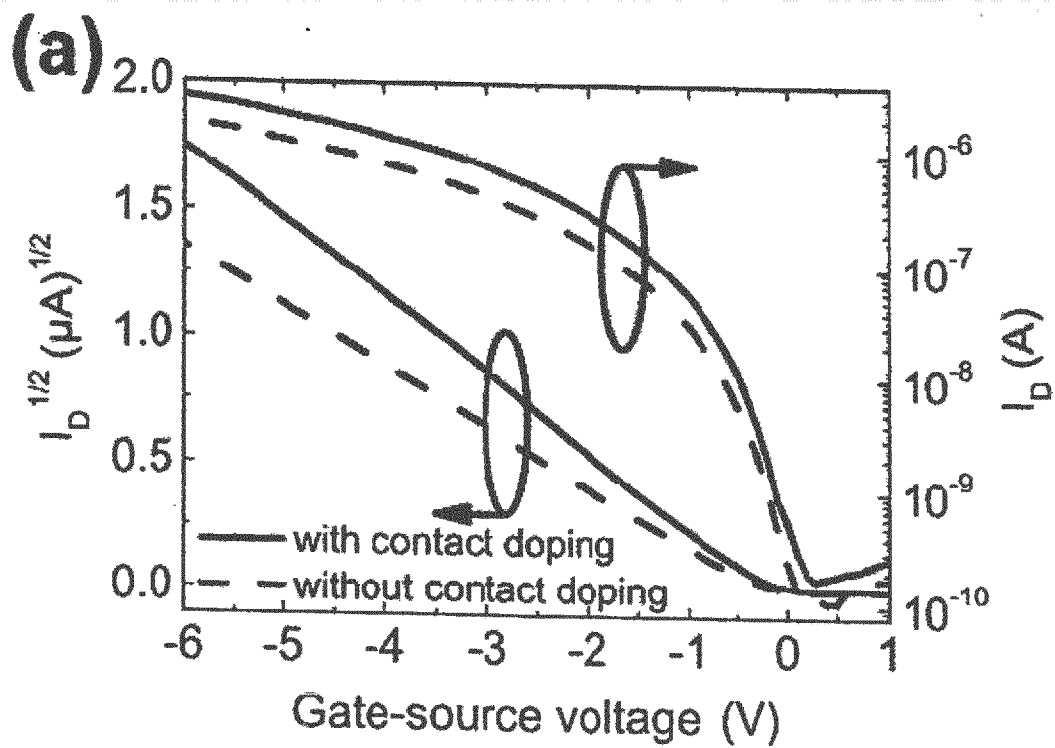


Fig. 11

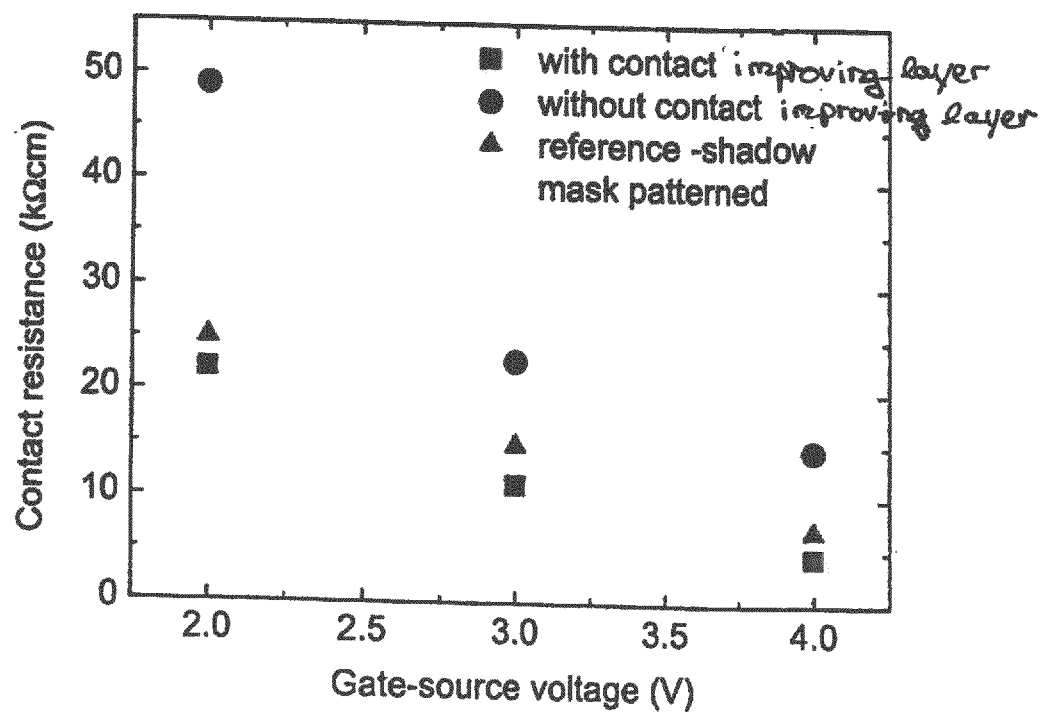


Fig. 12

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2014/055976

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L51/00 H01L51/10
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2010/219402 A1 (KATSUHARA MAO [JP] ET AL) 2 September 2010 (2010-09-02) paragraphs [0033] - [0066], [0153] - [0161]; figures 1A,1B,12A-12D ----- -/--	1-8, 10-12 9



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

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INTERNATIONAL SEARCH REPORT

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