(12) PATENT ABRIDGMENT   (11) Document No **AU-B-22022/92**
(19) AUSTRALIAN PATENT OFFICE   (10) Acceptance No. **656794**

(57) Claim

1.   A terminating station for a synchronous multiplex transmission network, wherein a frame of a plurality of rows and a plurality of columns is transmitted through the network, said columns being divided into a first field for carrying a transport overhead and a second field for carrying a plurality of virtual tributary path data, said rows and columns defining a plurality of timeslots, the terminating station comprising:

a bit pattern generator for generating a virtual tributary path idle (VTPI) pulse sequence;

means for inserting said VTPI pulse sequence into a portion of said first field of the frame; and

timeslot interchange means for interchanging timeslots of said frame, said timeslot interchange means copying contents of said first field of said frame into at least one column of the second field of said frame where virtual tributary path data is not present.

AUSTRALIA
PATENTS ACT 1990   **656 7 5**

COMPLETE SPECIFICATION

FOR A STANDARD PATENT

ORIGINAL

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Invention Title:	Virtual Tributary Path Idle Insertion Using Timeslot Interchange

The following statement is a full description of this invention, including the best method of performing it known to me/us:-

Virtual Tributary Path Idle Insertion Using Timeslot Interchange

Background of the Invention

The present invention relates generally to synchronous transmission systems, and more specifically to the insertion of a virtual tributary path idle (VTPI) code into a multiplex signal.

According to CCITT Recommendation G709, it is specified that a virtual tributary path idle (VTPI) signal be inserted to a STS-1 (synchronous transport signal level-1) frame if at least one of the virtual tributaries of the frame carries no data signals. A conventional technique for the VTPI insertion involves the use of a set of a VTPI generator and a selector for each virtual tributary for generating a VTPI and combining it with data bits.

Since the current approach needs as many sets of VTPI generator and selector as there are virtual tributaries, it results in circuit complexity and an increase in terminal equipment size and cost.

Summary of the Invention

It is therefore an object of the present invention to provide a VTPI insertion technique which requires a single VTPI insertion circuit for multiple virtual tributary paths.

The present invention is based on the fact that a portion of a frame where a transport overhead has been inserted is not used by the current technique when timeslots are interchanged. To minimize the number of VTPI insertion circuits, the present invention uses this portion of a frame as a temporary storage area for a VTPI signal and allows the timeslot interchanging function to copy the stored signal into other portions of the frame which are assigned to idle virtual tributaries.

According to a broadest aspect of the present invention, there is provided a terminating station for a synchronous multiplex transmission network, wherein a frame of a plurality of rows and a plurality of columns is transmitted through the network, said columns being divided into a first field for carrying a transport overhead and a second field for carrying a plurality of virtual tributary path data, said rows and columns defining a plurality of timeslots, the terminating station comprising:

a bit pattern generator for generating a virtual tributary path idle (VTPI) pulse sequence;

means for inserting said VTPI pulse sequence into a portion of said first field of the frame; and

timeslot interchange means for interchanging timeslots of said frame, said timeslot interchange means copying contents of said first field of said frame into at least

one column of the second field of said frame where virtual tributary path data is not present.

The invention further discloses a terminating station for a synchronous multiplex transmission network, wherein a frame of a plurality of rows and a plurality of columns is transmitted through the network, said columns being divided into a first field for carrying a transport overhead and a second field for carrying a plurality of virtual tributary path data, said rows and columns defining a plurality of timeslots, the terminating station comprising:

a controller;

a plurality of transport overhead extraction circuits, each of the transport overhead extraction circuits receiving an incoming frame and extracting a transport overhead (TOH) therefrom and supplying the extracted transport overhead to said controller;

a plurality of virtual tributary path idle (VTPI) insertion circuits connected respectively to outputs of said transport overhead extraction circuits, each of the VTPI insertion circuits receiving a TOH-extracted frame from the corresponding TOH extraction circuit, each of the VTPI circuits generating a virtual tributary path idle (VTPI) pulse sequence and inserting said VTPI pulse sequence into a portion of said first field and producing a VTPI-containing frame, and producing a frame not containing said VTPI when all columns of the second field of the received frame carry virtual tributary path data;

a switching network having a plurality of inlet terminals connected respectively to said VTPI insertion circuits and a plurality of outlet terminals, said switching network being responsive to a control signal from said controller for providing timeslot interchanging on the VTPI-containing frame and on the frame not containing the VTPI, and switching the timeslot-interchanged frame to said outlet terminals, said switching network copying contents of the first field of the VTPI-containing frame into at least one column of the second field of the VTPI-containing frame where virtual tributary path data is not present; and

a plurality of transport overhead insertion circuits coupled respectively to the outlet terminals of said switching network for rewriting the first field of each of frames from the switching network with a transport overhead supplied from said controller.

Brief Description of the Drawings

The present invention will be described in further detail with reference to the accompanying drawings, in which:

1   Fig. 1 is a block diagram of a terminating station of a synchronous

2   optical network according to the present invention;

3   Fig. 2 is a block diagram of a VTPI insertion circuit;

4   Figs. 3A to 3D show contents of the transport overheads of several

5   frames of a multiframe structure when they are inserted by VTPI insertion

6   circuit; and

7   Fig. 4A shows an STS-1 frame in which the VTPI-containing columns of

8   each frame are transferred to several columns of the synchronous payload

9   envelope (SPE) by the TST switch, and Fig. 4B shows another STS-frame in

10   which the VTPI-containing columns of the frame are copied to several

11   columns of the SPE using a multicast function.

12   DETAILED DESCRIPTION

13   Referring now to Fig. 1, there is shown a line terminating station of a

14   synchronous optical network (SONET) according to the present invention.

15   As illustrated, the line terminating station of this invention comprises a

16   plurality of optoelectric converters 1 to which incoming fiber optic

17   transmission lines are respectively terminated. Each optoelectric converter

18   receives an optical signal level-1 (OC-1) and translates it into a

19   corresponding electrical signal known as synchronous transport signal

20   level-1 (STS-1). According to the frame format of the STS-1 signal, each

21   frame consists of 9 rows of 90 bytes (columns) each and the first to third

22   columns of the frame are occupied by a transport overhead, and the

23   remaining 87 columns of the frame is known as a synchronous payload

24   envelope (SPE) to carry 87 x 9 bytes of STS-1 information payload

25   including a column of path overhead (POH).

26   The outputs of O/E converters 1 are coupled respectively to

27   corresponding TOH (transport overhead) extraction circuits 2 which are

28   associated with an operations (synchronization), administration and

29   maintenance (OAM) controller 7. Each TOH extraction circuit 2 reads a

30   transport overhead out of the first to third columns of the incoming STS-1

frame into the OAM controller 7 for network operations, administration and maintenance purposes and reads an STS information payload out of the remaining columns of the frame.

According to this invention, virtual tributary path idle (VTPI) insertion circuits 3 are provided corresponding to TOH extraction circuits 2. Each VTPI insertion circuit 3 is connected to the output of the corresponding TOH extraction circuit 2 to receive the STS information payload bytes. The output of each VTPI insertion circuit 3 is connected to one of inlet terminals of a time-space-time switch 4 (or digital cross-connect switch or add-drop multiplexer). To the outlet terminals of the switch 4 are connected TOH insertion circuits 5 whose outputs are connected via electrooptic converters 6 to outgoing fiber optic transmission lines. Each of the TOH insertion circuit 5 is associated with the OAM controller 7 to permit insertion of a transport overhead into an outgoing STS-1 frame.

In a well known manner, TST switch 4 provides timeslot interchange within each incoming frame (where the timeslot is defined as a slot for carrying a byte of data and identified by a particular row and a particular column of the frame), provides space switching on a timeslot basis between the inlet terminals and outlet terminals of the switch to form outgoing STS-1 frames, and provides timeslot interchange within each outgoing frame. Switching control signals for this purpose are supplied from the OAM controller 7.

As shown in Fig. 2, each VTPI insertion circuit 3 comprises a data buffer 10, a VTPI generator 11, a selector 12 and a timing circuit 13. Each frame from the corresponding TOH extraction circuit 2 is stored into buffer 10 and supplied to selector 12 under the control of timing circuit 13. A VTPI (virtual tributary path idle) pulse sequence is generated by VTPI generator 11 in response to a timing signal from circuit 13 when at least one of the virtual tributaries of a frame carries no data signal and applied to selector 12 where it is combined with the information payload for form an STS-1 frame. Selector 12 receives TOH timing pulses from timing circuit 13 to insert the

1 VTPI bit sequence into one of the timeslots of the transport overhead of

2 each frame and 0-bit sequences into the other timeslots of the transport

3 overhead. Typical examples of transport overheads for multiframe

4 transmission are shown in Fig. 3A to 3D, where a path overhead byte J1

5 indicates 64-kbps channel used to repetitively send a 64-byte fixed-length

6 string so a receiving terminal can continuously verify the integrity of a path,

7 and a path overhead byte H4 is a multiframe indicator for payloads

8 needing frames that are longer than a single STS frame when packing

9 lower rate channels (virtual tributaries) into the SPE. V_1, V_2, V_3 and V_4 are

10 virtual tributary path idle sequences, and where V_1 is typically represented

11 by a sequence of "01101100" and V_2, V_3 and V_4 are set equal to all zero's.

12 To facilitate the transport of lower rate digital signals, the SONET

13 standard uses sub-STS-1 payload mappings referred to as virtual tributary

14 (VT) structure as shown in Fig. 4A. This mapping divides the SPE field of

15 each STS-1 frame into 7 subframes or VT blocks with 12 columns in each

16 so that the subframes account for 84 columns ~~with~~ plus one column for the path overhead

17 (column number 1) and two unused columns (column numbers 30 and

18 59). The 84 columns are therefore partitioned by the unused columns into

19 three groups of 28 columns each, with the first group accounting for

20 column numbers 2 to 29, the second group for column numbers 31 to 58,

21 and the third group for column numbers 60 to 87. Corresponding 28

22 columns of different groups are assigned to virtual tributaries #1 through

23 #28, respectively.

24 According the present invention, the OAM controller 7 controls the

25 TST switch 4 to provide timeslot interchange on the incoming STS-1 frame

26 with a VTPI contained in its transport overhead by ~~transferring~~ copying the contents

27 of the transport overhead to idle virtual tributary columns of the SPE field.

28 If virtual tributary #1 is idle, the contents of the first, second and third

29 columns of the transport overhead ~~to~~ are copied into the virtual tributary columns #1, i.e.,

30 column numbers 2, 31 and 60, respectively, of the SPE field, as indicated
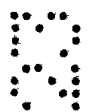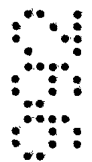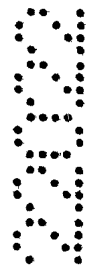
1   by hatchings and arrows in Fig. 4A. If more than one virtual tributary is

2   idle, a multicasting function of the TST switch is used to advantage. For

3   example, if virtual tributaries #1 and #2 are idle, the contents of the first,

4   second and third columns of the transport head are copied into the virtual
                        of the

5   tributary columns #1 and #2, first, second and third groups, respectively,

6   as shown in Fig. 4B. After the usual switching processes, VTPI-containing

7   STS-1 frames appear at appropriate TOH insertion circuits 5 where their
             overheads

8   transport heads are overwritten with new TOH bytes supplied from the

9   OAM controller 7.

10   It is seen from the foregoing that the present invention takes advantage

11   of the timeslot switching function of a digital cross-connect switch or add-

12   drop multiplexer for copying or writing the contents of the first to third

13   columns of an STS-1 frame into idle virtual tributaries.

The claims defining the invention are as follows:

1.   A terminating station for a synchronous multiplex transmission network, wherein a frame of a plurality of rows and a plurality of columns is transmitted through the network, said columns being divided into a first field for

5   carrying a transport overhead and a second field for carrying a plurality of virtual tributary path data, said rows and columns defining a plurality of timeslots, the terminating station comprising:

      a bit pattern generator for generating a virtual tributary path idle (VTPI) pulse sequence;

10   means for inserting said VTPI pulse sequence into a portion of said first field of the frame; and

      timeslot interchange means for interchanging timeslots of said frame, said timeslot interchange means copying contents of said first field of said frame into at least one column of the second field of said frame where virtual tributary path data is not

15   present.

2.   A terminating station as claimed in claim 2, wherein said frame is a synchronous transport signal level-1.

3.   A terminating station for a synchronous multiplex transmission network, wherein a frame of a plurality of rows and a plurality of columns is

20   transmitted through the network, said columns being divided into a first field for carrying a transport overhead and a second field for carrying a plurality of virtual tributary path data, said rows and columns defining a plurality of timeslots, the terminating station comprising:

      a controller;

25   a plurality of transport overhead extraction circuits, each of the transport overhead extraction circuits receiving an incoming frame and extracting a transport overhead (TOH) therefrom and supplying the extracted transport overhead to said controller;

      a plurality of virtual tributary path idle (VTPI) insertion circuits connected

30   respectively to outputs of said transport overhead extraction circuits, each of the VTPI insertion circuits receiving a TOH-extracted frame from the corresponding TOH extraction circuit, each of the VTPI circuits generating a virtual tributary path idle (VTPI) pulse sequence and inserting said VTPI pulse sequence into a portion of said first field and producing a VTPI-containing frame, and producing a frame not

35   containing said VTPI when all columns of the second field of the received frame carry virtual tributary path data;

      a switching network having a plurality of inlet terminals connected respectively to said VTPI insertion circuits and a plurality of outlet terminals, said switching

network being responsive to a control signal from said controller for providing timeslot interchanging on the VTPI-containing frame and on the frame not containing the VTPI, and switching the timeslot-interchanged frame to said outlet terminals. said switching network copying contents of the first field of the VTPI-containing frame into at least

5 one column of the second field of the VTPI-containing frame where virtual tributary path data is not present; and

a plurality of transport overhead insertion circuits coupled respectively to the outlet terminals of said switching network for rewriting the first field of each of frames from the switching network with a transport overhead supplied from said controller.

10 4. A terminating station as claimed in claim 3, wherein the incoming frame received by each of said transport overhead extraction circuits is a synchronous transport signal level-1.

DATED this Twentieth Day of October 1994
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Virtual Tributary Path Idle Insertion Using Timeslot Interchange
ABSTRACT OF THE DISCLOSURE

In a terminating station for a synchronous multiplex transmission network in which a frame of (i) rows and (j) columns is transmitted,
5 the (j) columns of the frame is divided into (k + m) columns, with the (k) columns carrying a transport overhead and the (m) columns carrying an information payload. The (m) columns are subdivided into (k) groups of (n) columns each, and each of the corresponding (n) columns of each group carries a virtual tributary traffic. In the terminating station,
10 a virtual tributary path idle (VTPI) pulse sequence is generated and inserted into the (k) columns of each frame. A timeslot interchanger (4), which provides the usual timeslot interchange within the frame, copies the contents of the (k) columns of the frame into one or more of the (n) columns of the (k) groups, respectively, of the same frame.

Figure 1

FIG. 1

FIG. 2

VTPI Insertion Circuit 3
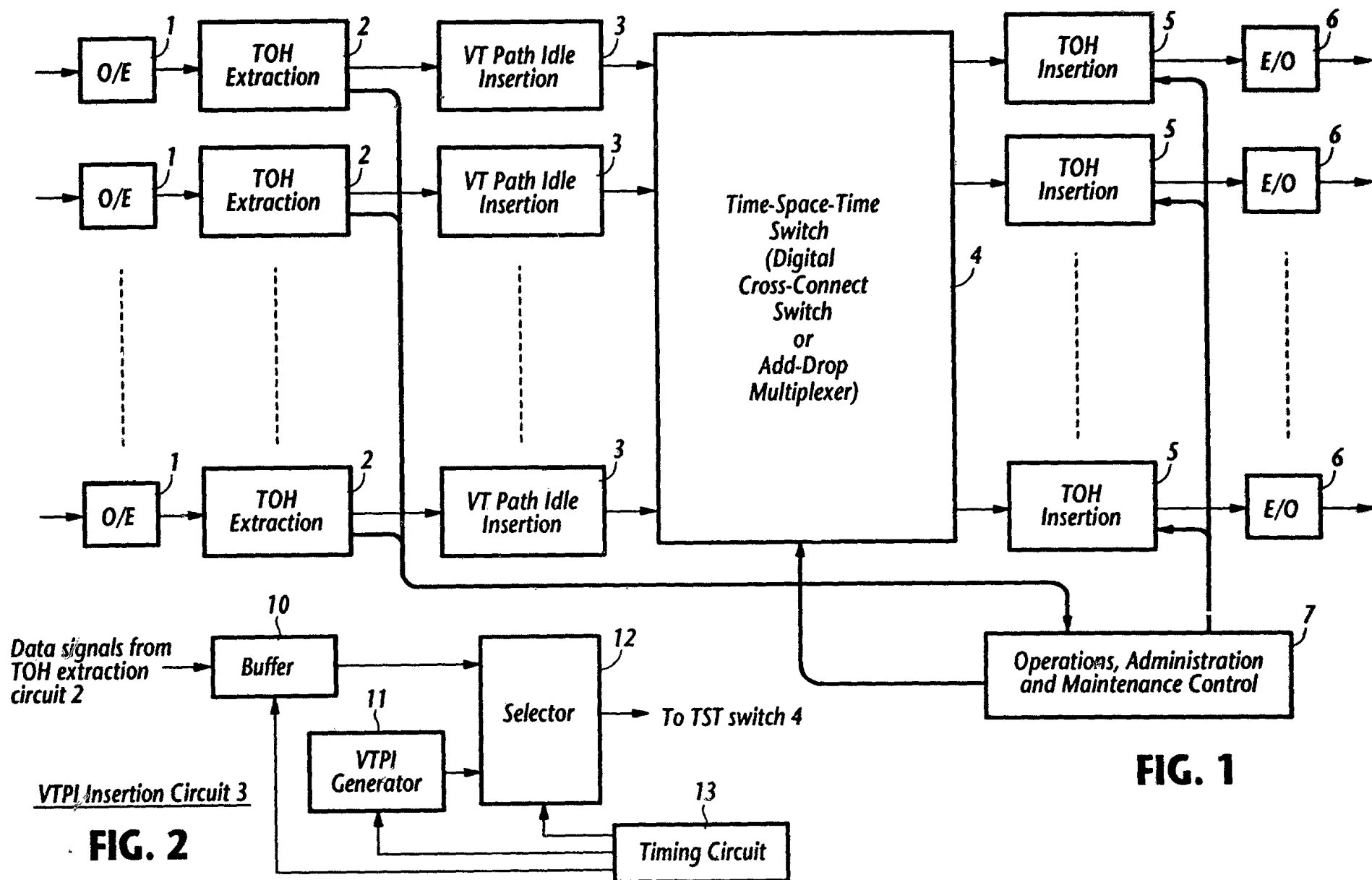
FIG. 3A

Frame #1

$V_1 = 0 1 1 0 1 1 0 0$
$0 = 0 0 0 0 0 0 0 0$

0	0	0	
0	0	0	
0	0	0	
V_1	0	0	J1
0	0	0	
0	0	0	
0	0	0	
0	0	0	
0	0	0	H4

____ TOH ____/ \POH \ _____ SPE _____

FIG. 3B

Frame #2

$V_2 = 0 0 0 0 0 0 0 0$

0	0	0	
0	0	0	
0	0	0	
V_2	0	0	J1
0	0	0	
0	0	0	
0	0	0	
0	0	0	
0	0	0	H4

FIG. 3C

Frame #3

$V_3 = 0 0 0 0 0 0 0 0$

0	0	0	
0	0	0	
0	0	0	
V_3	0	0	J1
0	0	0	
0	0	0	
0	0	0	
0	0	0	
0	0	0	H4

FIG. 3D

Frame #4

$V_4 = 0 0 0 0 0 0 0 0$

0	0	0	
0	0	0	
0	0	0	
V_4	0	0	J1
0	0	0	
0	0	0	
0	0	0	
0	0	0	
0	0	0	H4

FIG. 4A

		#1	#2	-------	#27	#28		#1	#2	-------	#27	#28		#1	#2	--------	#27	#28
1	Z3	0	D		D	D		0	D		D	D		0	D		D	D
2	Z4	0	D		D	D		0	D		D	D		0	D		D	D
3	Z5	0	D		D	D		0	D		D	D		0	D		D	D
4	J1	0	D		D	D	U	0	D		D	D	U	0	D		D	D
5	B3	0	D		D	D	n	0	D		D	D	n	0	D		D	D
6	C2	0	D		D	D	u	0	D		D	D	u	0	D		D	D
7	G1	0	D		D	D	s/e/d	0	D		D	D	s/e/d	0	D		D	D
8	F2	0	D		D	D		0	D		D	D		0	D		D	D
9	H4	0	D		D	D		0	D		D	D		0	D		D	D

1	2	3	1	2	3	-------	28	29	30	31	32	-------	57	58	59	60	61	---------	86	87

$\underbrace{\qquad}_{TOH}$ (POH) (SPE Column Number)

SPE

0 = 0 0 0 0 0 0 0 0
D = Data byte

FIG. 4B

0 = 0 0 0 0 0 0 0 0
D = Data byte