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Foley

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[54] **PRINT CONTROL SYSTEM FOR HIGH SPEED PRINTERS**

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[51] **Int. Cl.** **B41j 9/12**

[58] **Field of Search** ..... 101/91, 93 C, 96; 317/137; 340/172.5, 347, 365; 178/23

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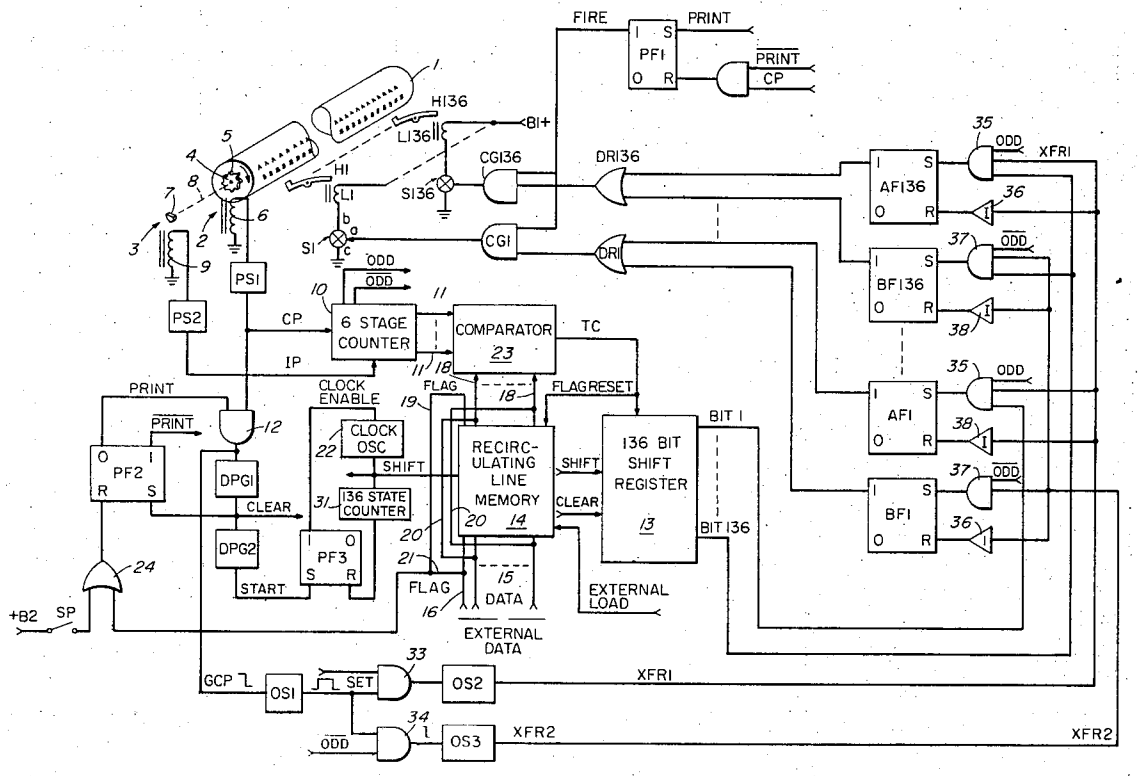
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[57] **ABSTRACT**

A print control system for line printers of the type including a recirculating line memory adapted to be loaded with digital signals representing the characters to be printed on a line. Character pulses, one for each character that can be printed, each program a search of the memory for a different associated character, and load a first register with print signals for each column for which that character is to be printed. Odd character pulses direct loading of a second set of registers, one for each column, with the contents of the first register representing the results of the search for each odd character, and even character pulses direct loading of a third set of registers, one for each column, with the contents of the first register representing the results of the search for each even character. The second and third registers are alternately latched for predetermined intervals by overlapping timed firing pulses, and either register, when latched in the print cycle, enables a gate to provide driving current to the hammer driver for that column.

12 Claims, 2 Drawing Figures



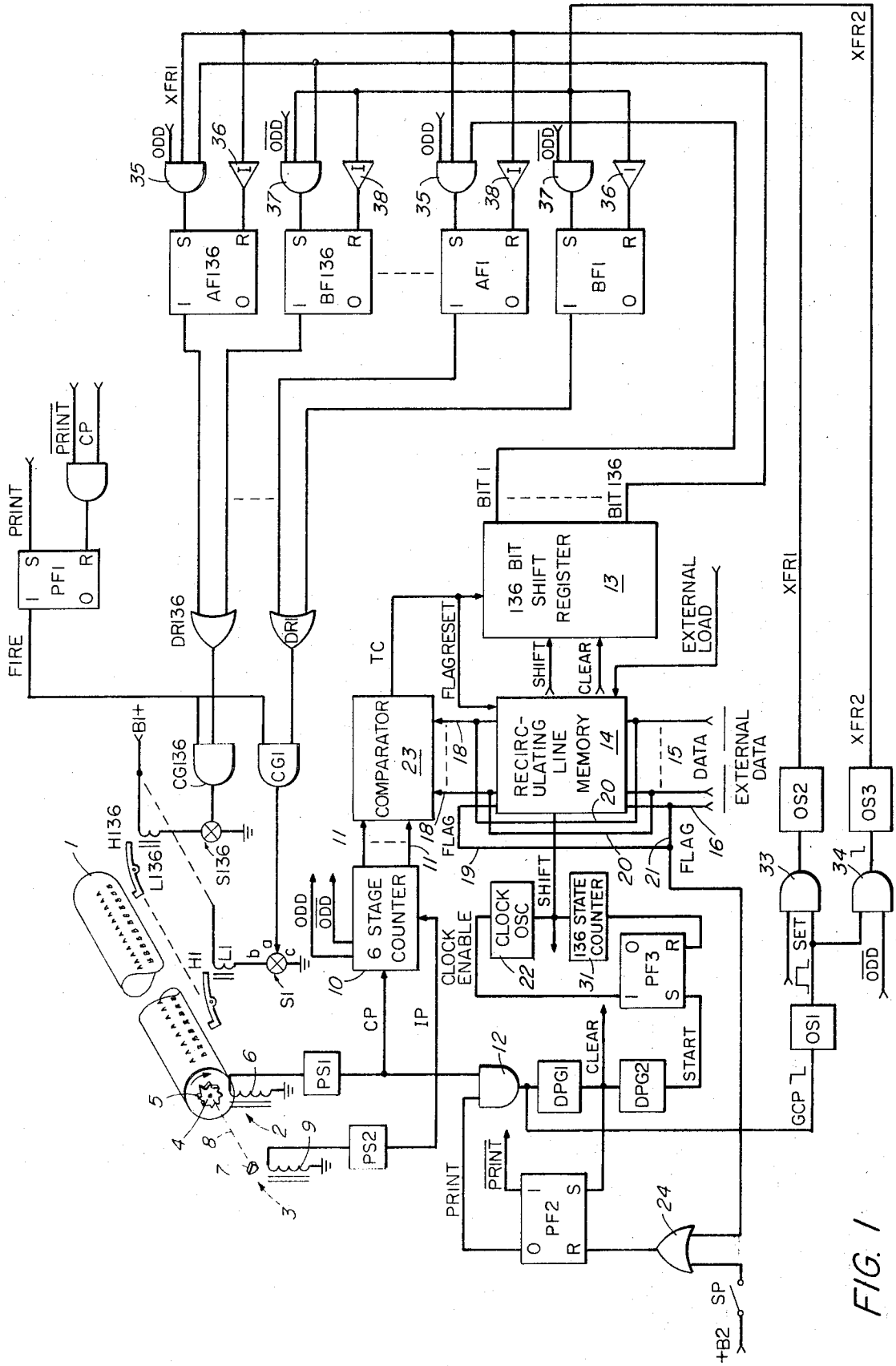

XFR1
XFR2
ODD
AF136
BF136
AF1
BF1
DRI136
DRI
PRINT
CP
PFI
FIRE
BIT 1
BIT 136
136 BIT SHIFT REGISTER 13
EXTERNAL LOAD
SHIFT
CLEAR
TC
FLAGRESET
COMPARATOR 23
RECIRC-ULATING LINE MEMORY 14
DATA
EXTERNAL DATA
FLAG
BI+
CGI136
CGI
H136
L136
S136
HI
LI
SI
6 STAGE COUNTER
CLOCK ENABLE
CLOCK OSC
136 STATE COUNTER
PF3
START
CP
IP
PSI
PS2
DPG1
DPG2
CLEAR
PF2
OS1
OS2
OS3
SET
GCP
SP
+B2

FIG. 1

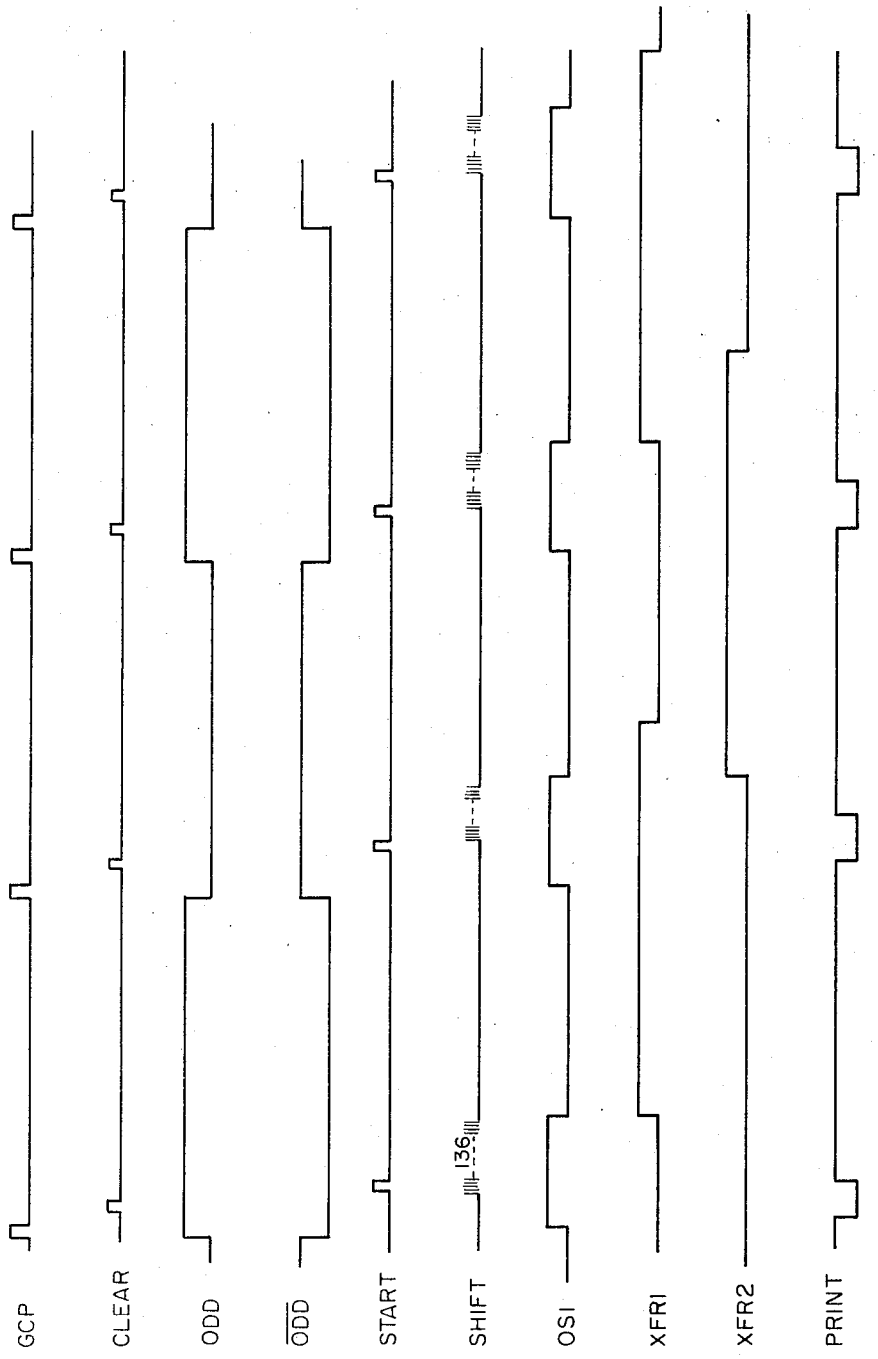

GCP
CLEAR
ODD
$\overline{ODD}$
START
SHIFT
136
OSI
XFR1
XFR2
PRINT

FIG. 2

PRINT CONTROL SYSTEM FOR HIGH SPEED PRINTERS

My invention relates to high speed printers, and particularly to a novel print cycle control system.

In U.S. Pat. No. 3,656,427, granted to me on Apr. 18, 1972 for Print Control System for High Speed Printers, and assigned to the assignee of this application, I have disclosed and claimed a print control system in which one standardized image control pulse is employed to direct and control the firing of all of those hammers which are to be fired at a time, to print a given character in selected columns of a line to be printed. This system has the advantage that only one precision pulse generator is required to maintain uniform print quality, while each of a hundred or more of print hammers are delivered equal amounts of energy, whether one or all of them are to be fired at once. However, one firing pulse is required for each of the several characters that may be printed in a given line, i.e., typically **64** of such pulses per line as a maximum. Thus, the line rate of printing is limited by the product of the maximum number of characters that can be printed in a line and the minimum duration of the precision firing pulse of current that must be delivered to each hammer driver circuit in order to ensure good print quality with a given print hammer assembly. The object of my invention is to increase the line rate of printing of high speed printers of the line-at-a-time type without materially increasing the cost and complexity of the print hammers and their hammer driver circuits.

Briefly, the above and other objects of my invention are attained by a novel print hammer control system in which a plurality of precision fire control signals are provided, although far less than one per print hammer, and preferably only two for all of an even number of print hammers. These signals may each direct the supply of current to a given hammer driver for a longer duration that the interval between character pulses, so that two or more characters may be printed at successive times with energy supplied during overlapping intervals.

My invention is organized about the concept that for any given column, only one character will be printed for each line, and directed by the thought that for each character to be printed, a fixed interval of driving current, depending on the parameters of the image forming device, is necessary. For any particular line that is to be printed, a given print hammer may be required to print either an odd character or an even character in the font, but not both; and, once fired, it will not be fired again during the printing of that line. The apparatus of my invention is arranged to take advantage of those considerations by beginning the firing of the hammer or hammers for the next odd, or even, character to be printed, while the hammer or hammers for the even or odd character being printed is still receiving drive energy.

More particularly, the apparatus of my invention comprises novel data processing apparatus, under the control of conventional character and index pulse generators, connected between a conventional printer buffer and the image forming devices of the printer to carry out the several functions required of the printer following even character pulse. The apparatus includes a shift register, capable of containing a signal for each column indicating whether or not the image forming

device for that column is to be activated. Two banks of latches are provided, each containing one latch for each column.

Following each odd character pulse (counting from any desired character in the font), and after the shift register has been loaded, an odd timing signal is generated which transfers the contents of the shift register into one bank of latches. The latches of that bank which correspond to columns in which that odd character is to be printed then start the flow of driving energy to their associated image forming devices, and continue the supply of energy for a predetermined time.

Meanwhile, the next even character pulse starts a scan of memory, and loads the shift register with signals indicating whether or not the next character is to be printed. An even timing signal is then generated, which transfers the contents of the shift register into the other bank of latches. That begins the timing of the flow of driving energy to the selected image forming devices which are to print the even character, while any image forming devices printing the previous odd character are still being energized.

The manner in which the apparatus of my invention is constructed, and its mode of operation, will best be understood in the light of the following detailed description, together with the accompanying drawings, of a preferred embodiment thereof.

In the drawings,

FIG. **1** is a schematic block and wiring diagram of a print control system in accordance with my invention, and

FIG. **2** is a timing chart illustrating the operation of the system of FIG. **1.**

Referring now to FIG. **1,** I have shown my invention in a particular and exemplary embodiment in which it comprises the print control system for a high speed impact drum printer. Application of the invention in its broader aspects to printers of other forms will be apparent to those skilled in the art as the description proceeds. Those aspects of the printer which may be of conventional construction, and will be understood by those versed in the art, will be but briefly alluded to, and, except in the respects to be detailed hereinafter, the apparatus can be the same as that shown and described in my above cited U.S. Pat. No. 3,656,427.

In FIG. **1,** the printer is shown to comprise a movable type carrier in the form of a print drum **1** on which rows of characters are engraved in a conventional manner. Conventional means, not shown, are provided to rotate the drum **1** at constant speed. In a typical configuration, there would be 64 different characters available for printing in each of 136 columns. The like characters, such as the A's, are arranged in straight rows parallel to the axis of the drum so that all like characters come into printing position, with respect to a bank of print hammers **H1** through **H136,** at the same time.

Each of the print hammers, such as the hammers **H1** and **H136** shown, is arranged to be actuated by an actuating solenoid having a winding, such as the winding **L1** for the hammer **H1** and the winding **L136** for the hammer **H136.** The showing of the hammers and their actuating windings is intended as a functional schematic diagram. In practice, any conventional hammer and actuating assembly can be employed, such as those cited as preferable in my above cited patent.

Each of the windings is provided with an independent actuating circuit extending from a power supply termi-

nal at a potential +B1, through the winding such as L1, and through an electronic switch such as S1 to ground. The corresponding actuating circuit for the winding L136 extends through a switch S136 to ground. The switches such as S1 and S136 may be conventional electronic switches having load terminals, such as *b* and *c* for the switch S1, and a control terminal such as *a*. Particular suitable forms which these switches may take are shown and described in my above cited patent.

Each of the switches such as S1 and S136 is arranged to be closed when a logic 1 signal appears on an output terminal of an associated AND gate such as gate CG1 for the switch S1 and a gate CG136 for the switch S136. Suitable gates are described in my above cited patent.

Each of the AND gates such as CG1 and CG136 has two input terminals, one of which is connected to the output terminal of a conventional flip-flop PF1. When set, the flip-flop PF1 produces a level labelled FIRE that enables all of the gates GC1 through CG136.

The second input terminal of each of the gates such as CG1 is connected to the output terminal of a different one of a set of conventional OR gates OR1 through OR136. Each of these gates OR1 through OR136, when supplied with a logic 1 signal at either of its two input terminals, produces a logic 1 output signal that will cause the associated AND gate such as CG1 to produce a logic 1 output signal, if the FIRE level is present, for a time interval determined by the duration of the logic 1 signal produced by the OR gate such as OR1.

When the FIRE level is produced, and the gates such as OR1 supply logic 1 output signals to the corresponding gates such as CG1, the corresponding switch such as S1 will be closed to pass current through the winding such as L1, for the duration of the logic 1 signal produced by the gate such as OR1, and cause the hammer such as H1 to strike toward the print driver, engaging conventional intermediate paper and ribbon, not shown, to produce an image.

Each of the OR gates OR1 through OR136 has two input terminals, each connected to the logic 1 output terminal of a different one of a pair of latches, here shown as conventional DC flip-flops, there being one each pair of such latches for each column in the line to be printed. In particular, the OR gate OR1 has one input terminal connected to the logic 1 output terminal of an odd character flip-flop AF1, and a second input terminal connected to the logic 1 output terminal of an even character flip-flop BF1. Similarly, the other OR gates, such as the gate OR136, have one input terminal connected to the logic 1 output terminal of an odd character flip-flop such as AF136, and a second input terminal connected to the logic 1 output terminal of an even character flip-flop such as BF136.

During the printing cycle, each time a different odd character, such as A, C, etc., comes into printing position, the 136 odd character registers AF1 through AF136 are each set or not set accordingly as that character is to be, or is not to be printed, respectively, in the corresponding column. If set, these registers remain set for a predetermined firing interval. Similarly, each time a different even character, such as B, D, comes into printing position, the 136 even character registers BF1 through BF136 are each set or not set according as the even character is or is not to be printed in the corresponding column.

As will appear, each of the even character registers, when set, remains set for the same predetermined interval as the odd character registers, and these intervals may overlap the times during which the odd character registers are set, as will be described next.

Basic timing in the print cycle is provided by a conventional character pulse generator generally designated 2, and a conventional index pulse generator generally designated 3. While these generators may take that variety of forms known to those skilled in the art, as here shown the character pulse generator 2 comprises a toothed ferromagnetic disc 4 having a tool such as 5 for each different character that can be printed.

The teeth such as 5 cooperate with a magnetic circuit including a stationary pickoff coil 6 to produce a pulse in the coil 6 each time a character approaches printing position. Similarly, the index pulse generator may comprise a single tooth 7 of ferromagnetic material, fixed to the shaft 8 on which the drum 1 is carried to produce a pulse in a coil 9 once for each revolution of the print drum.

The pulses produced by the coil 6 are applied to a conventional pulse shaping circuit PS1 to produce a character pulse CP for each pulse induced in the coil 6. Similarly, the pulses induced in the coil 9 are applied to a conventional pulse shaping circuit PS2 to produce an index pulse IP for each revolution of the print drum 1.

The character pulses CP are applied to the input terminal of a six stage counter 10. The counter 10 may be a conventional electronic binary counter producing a digital output signal on six output leads such as 11 that has a different one of 64 values for each of the 64 different characters that can be printed. The index pulse IP is applied to reset the counter once each revolution, so that the counter output always accurately represents the character next coming into position after the character then coming into position has passed through the printing position and is being printed, or not, in the selected columns.

The character pulses CP are also applied to one input terminal of a two input terminal AND gate 12. The gate 12 receives a second input signal, labeled PRINT, from a flip-flop PF1, to be described. When the PRINT signal is present at logic 1, and a character pulse CP is present, the gate 12 produces a gated character pulse labeled GCP. This pulse is applied to a conventional delayed pulse generator DPG1 of any conventional design.

The delayed pulse generator DPG1 produces a pulse labeled CLEAR, delayed from the pulse GCP in the manner shown in FIG. 2. The CLEAR pulse sets the flip-flop PF2, and performs other functions to be described.

The CLEAR pulse is applied to a conventional 136 bit shift register 13, to be described, to reset the shift register so that each of its 136 bits are at logic 0. The CLEAR pulse is also applied to a delayed pulse generator DPG2, which produces a START pulse following the CLEAR pulse as illustrated in FIG. 2.

The START pulse is applied to the set input terminal of a conventional flip-flop PF3 to set the flip-flop and thereby produce a logic 1 signal, labeled CLOCK ENABLE, at its logic 1 output terminal.

The apparatus includes a conventional recirculating line memory **14** of any conventional construction. It essentially comprises a conventional 136 stage, 7 bit per stage shift register that is connected for data rotation. The memory **14** may be of conventional MOS construction, or may be a core plane or the like, and includes 136 word storage locations of seven bits each. Suitable gating, reading and writing circuits are provided for entering external digital data on seven input leads, including six data leads **15**, of which the first and last are shown, and a lead **16** on which there is a logic 1 flag bit for each six bit character signal entered on the leads **15**.

The signals on the leads **15** and **16** are entered into a first seven bit location in the memory in response to an EXTERNAL LOAD pulse supplied to a lead **17**. The next character represented by signals on the leads **15** and **16** is loaded into the first memory location by the subsequent EXTERNAL LOAD pulse, which also effects transfer of the first character into the second location. That action proceeds until 136 characters have been entered into the memory with the first character entered in the 136th location in position to be read out on six output data leads **18**, of which the first and last are shown, and an output flag lead **19**. A set of leads **20** interconnects **18** and the leads **15**, and a lead **21** interconnects the leads **16** and **19**.

After the memory **14** is loaded, a SHIFT pulse, at times provided by a clock oscillator **22** in a manner to be described, causes the contents of each seven bit location in the memory **14** to be transferred into the next location. The signals representing the first character, entered into the memory in location **136**, and appearing on the leads **18**, are transferred over to the leads **20** to be entered into the first location of the memory.

As each set of data signals on the leads **18** is read out of the memory **14**, it is supplied to a conventional six bit comparator **23**, in which the data on the leads **18** is compared with the data on the six output leads **11** of the six stage counter **10**. When the character represented by the six bit code on the leads **18** agrees with the character represented by the six bit code on the leads **11**, a "true compare" bit TC is produced.

When a true-compare pulse TC is produced, it is applied as a FLAG RESET signal to erase the flag bit associated with the character signal that produced it. Thus, as a character is read out of the 136th location in the memory into the comparator, and at the same time over the leads **20** to be loaded into the first character location, if a flag reset and true-compare pulse is produced, the flag bit will be erased.

When a flag bit is produced on lead **19** as the corresponding character is read into the comparator and back into the first location of the memory, it is also applied to one input terminal of a conventional OR gate **24**. The output terminal of the gate **24** is connected to the reset input terminal of a conventional flip-flop PF2. A flag bit on lead **19** accordingly resets the flip-flop PF2 and causes it to produce the PRINT signal at logic **1** at its logic **0** output terminal. The flip-flop PF2 is arranged to be set by the CLEAR pulse, as described above.

The OR gate **24** has a second input terminal connected through means schematically shown as a switch SP to a suitable source of potential +B2. The switch SP is momentarily closed at the end of a cycle of paper movement to reset the flip-flop PF2. The closing of the switch SP represents the conventional "start print" signal produced in a conventional manner as well understood by those skilled in the art.

When enabled by the CLOCK ENABLE signal produced by the flip-flop PF3 in its set state, the clock oscillator **22** produces a series of **136** shift pulses that are applied to the memory **14**, and to the shift register **13**. The shift pulses from the oscillator **22** are also applied to the input terminal of a conventional **136** state counter **31**. After **136** such pulses are applied to the counter, it produces an output signal that resets the flip-flop PF2.

The shift register **13** comprises **136** stages of storage, which may be flip-flops or the like, connected as a shift register. A first stage is connected to the output of the comparator **23** to receive the pulses TC. The first stage has an output lead labeled BIT **1** on which a signal representing the contents of the first stage appears. Subsequent stages in the shift register also have corresponding output terminals. For example, the last stage **136** has an output lead on which a signal labeled BIT **136**, representing its contents, appears.

When **136** clock pulses are applied by the clock oscillator to the shift register **13**, at each shift pulse that causes a character to be supplied from the memory to the comparator **23** that produces a pulse TC, a logic 1 is entered into the shift register. If a pulse TC is not produced, a logic 0 is loaded into the register. The contents of that stage are transferred to the next stage with the succeeding shift pulse, until **136** storage locations in the shift register have been loaded with logic 1's for each pulse TC representing that the character is to be printed in the corresponding column. Thus, at the end of each of the **136** shift pulses, the shift register **13** contains a train of signals, one for each of the **136** columns of the printer, and each indicating by a logic 1 state that the character represented by the current state of the six stage counter **10** is to be printed, or by a logic 0 state that is not to be printed, in the corresponding column.

Each of the **136** leads labeled BIT **1** through BIT **136** is connected to gates for either of a pair of flip-flops associated with the corresponding column, as selected by circuits to be described. In particular, for each odd character coming into printing position, such as A, a bank of flip-flops (or other conventional latch circuits) AF1 through AF136 is enabled to be set by the corresponding register in the shift register **13**. For each even character coming into printing position, such as B, a second bank of flip-flops BF1 through BF136 is enabled.

In order to select the odd or even bank of flip-flops to receive the contents of the register **13**, the trailing edge of each gated character pulse GCP from the gate **12** triggers a conventional one-shot multivibrator OS1 to produce a positive pulse labeled SET. The SET pulse is applied to one input terminal of each of two conventional AND gates **33** and **34**.

The AND gate **33** has another input terminal connected to the first stage of the counter **10**, which changes state at each character pulse CP, to receive a signalled labeled ODD when the next character coming into printing position is in the odd set A, C, E, etc. Similarly, the AND gate **34** has a second input terminal connected to the complementary side of the first stage of the counter **10** to receive a logic one level labeled $\overline{\text{ODD}}$

when the next character coming into printing position is in the even set such as B, D, etc.

When the SET pulse is produced, the gate **33** or **34** that is selected by the ODD or $\overline{\text{ODD}}$ level currently present produces an output signal that triggers one of two precision one-shot multivibrators OS2 and OS3 to produce a timed firing pulse of predetermined duration, such as 1.3 milliseconds in a particular embodiment of my invention. Such a pulse is produced as a logic 1 level labeled XFR1 by the multivibrator OS2 when the gate **33** produces an output signal. Similarly, the multivibrator OS3 produces such a pulse, labeled XFR2, when the gate **34** produces an output signal. As shown in FIG. **2**, the XFR1 and XFR2 pulses may overlap, i.e., if the interval between character pulses is 1.23 milliseconds, the pulses XFR1 and XFR2 may each be 1.3 milliseconds in duration, as in the example described above.

The XFR1 pulses are each applied to one input terminal of 136 three-input terminal AND gates **35**. A second input terminal of each of the gates **35** receives the level ODD. A third input terminal of each of the gates **35** receives a different one of the 136 output signals from the 136 stages of the shift register **13**, labeled BIT1 through BIT**136**, each at logic 1 when a character is to be printed in the corresponding column **1** through **136**.

The output terminal of each of the gates **35** is connected to the set input terminal S of a different one of the odd flip-flops AF1 through AF**136**. Each of these flip-flops is thus set when and only when the ODD level, the XFR1 pulse, and the corresponding print command signal BIT1 through BIT**136**, are all at logic 1. The XFR1 pulse is also applied, through **136** inverters **36**, to the reset input terminals R of each of the flip-flops AF1 through AF**136**. By this arrangement, and referring to FIG. **2**, any of the flip-flops AF1 through AF**136** can be set during the ODD intervals, but not during the $\overline{\text{ODD}}$ intervals, and, if set, remains set during the XFR1 pulse.

A corresponding arrangement permits the setting of any of the even flip-flops BF1 through BF**136** selected by a logic **1** on the associated lead BIT1 through BIT**136** when the level $\overline{\text{ODD}}$ is present and the pulse XFR2 is produced. When set, any of the flip-flops BF1 through BF**136** remain set for the duration of the timed XFR2 pulse. For that purpose, the signals XFR2, $\overline{\text{ODD}}$ and the corresponding lead BIT1 through BIT**136** are connected to the three input terminals of each of a set of **136** AND gates **37**. Each of the gates **37** has an output terminal connected to the set input terminal S of a different one of the even flip-flops BF1 through BF**136**. Also, the XFR2 pulse is applied, through a set of **136** inverters **38**, to the next input terminals R of the flip-flops BF1 through BF**136**.

As noted above, when the FIRE level is present at logic 1, and any of the flip-flops AF1 through AF**136** or BF1 through BF**136** is set, the corresponding hammer driver coil L1 through L**136** is energized, for a time determined by the current pulse XFR1 or XFR2. The FIRE level is produced by the flip-flop PF1 when the latter is set by the PRINT signal, initially produced by the start-print signal SP. This PRINT signal is present when a character pulse CP is produced as long as a FLAG bit remains in the memory **14**, i.e., until the last character in the line to be printed has been printed. When that occurs, the next character pulse CP will be produced when the level PRINT is present. Those signals, applied to an AND gate **39**, reset the flip-flop PF1 and terminate the print cycle, removing the FIRE level to prevent any false printing during the following "move paper" cycle. The signal $\overline{\text{FIRE}}$, produced at the logic 0 output terminal of the flip-flop PF1, may also serve as an indication that the paper can be moved into position for the next line to be printed, and that the memory **14** can be reloaded with the information to be printed on the next line.

While not shown, it is preferred that there be an operational amplifier included between the logic 1 output terminal of the flip-flop PF1 and the paralleled input terminals of the gates CG1 through CG**136**, for the purpose described in my above cited U.S. Pat. No. 3,656,427 of producing a FIRE level that will not be appreciably changed despite the number of gates that may be enabled to supply current to it.

However, this level does not determine the duration of the firing intervals, as in my above cited patent, the duration being determined by the pulses XFR1 and XFR2. Other particular features described in my above cited patent, where applicable, are of course to be employed, and their description is incorporated herein by reference.

Operation of the apparatus of my invention will next be described with reference to FIGS. **1** and **2**. Referring to FIG. **1**, assume that the flip-flops AF1 through AF**136**, BF1 through BF**136**, PF1 and PF3 are reset, and that the flip-flop PF2 is set. The print drum **1** is assumed to be rotated at a constant speed such that character pulses CP are being produced at intervals of 1.23 milliseconds, with index pulses IP being produced at intervals of 78.9 milliseconds. Assume that the memory **14** has been loaded with **136** six-bit characters on the leads **15**, by application of EXTERNAL LOAD pulses to shift them into the memory, each signal on the leads **15** being accompanied by a logic **1** FLAG bit applied on the lead **16**. Assuming the storage location assignments shown, the character signal for column **1** would be loaded into the memory first, and the character signal for column **136** would be that last loaded into the memory over the leads **15** and **16**.

Next, assume that a start print signal is given by momentarily closing the switch SP to reset the flip-flop PF2 through the OR gate **24**. The PRINT signal will now be produced, enabling the gate **12** to respond to the next character pulse CP to produce a gated character pulse CGP. The PRINT signal will set the flip-flop PF2 to produce the FIRE level.

The first gated character pulse GCP produced by the gate **12** will cause the delayed pulse generator DPG1 to produce the CLEAR pulse, as shown in FIG. **2**. The CLEAR pulse will clear the shift register **13**, and will set the flip-flop PF2 to remove the level PRINT and produce the level $\overline{\text{PRINT}}$. The CLEAR pulse also actuates the delayed pulse generator DPG2 to produce the START signal as illustrated in FIG. **2**. That signal will set the flip-flop PF3.

With the flip-flop PF3 set, producing the signal CLOCK ENABLE, the clock oscillator **22** will begin to produce SHIFT pulses, which advance the **136** state counter **31**. The SHIFT pulses will cause the contents of the memory **14** to be supplied one at a time to the comparator **23**, and restored to the memory over the leads **20** and **21**.

In the comparator **23,** the characters supplied from the memory are compared with the signal on leads **11** from the counter **10.** During each set of **136** SHIFT pulses, the contents of the counter **10** remain at the state set by the last character pulse CP that produced the pulse GCP.

As each character of the memory **14** is supplied to the comparator **23,** a pulse TC is produced or not produced according as the corresponding character is the same as or different from the character in the counter **10,** respectively. Thus, if the character code supplied by the counter **10** represents the character A, and the memory had a line of characters all of which are A's, **136** TC pulses would be strobed into the shift register **13.** On the other hand, if none of the characters were A's, **136** logic 0's would be supplied to the shift register **13.** At the end of the **136** pulses, the shift register **13** is loaded with logic 1's in each location in which the character in the counter **10** is to be printed, and logic 0's in each location in which it is not to be printed. In response to the last of the **136** SHIFT pulses, the counter **31** will reset the flip-flop PF2 and disable the oscillator **22.**

As the first and each following SHIFT pulse is applied to the memory **14,** and a character is read out of the memory **14** to the comparator, the corresponding FLAG bit on the lead **19** is applied to the gate **24** and resets the flip-flop PF2. Each TC pulse that is produced causes a FLAG RESET signal to be applied to the memory to erase the corresponding FLAG bit. Thus, the result following the first pulse GCP in the print cycle will be that the first SHIFT pulse will cause the first FLAG bit in the memory to reset the flip-flop PF2 and restore the PRINT signal. Subsequent FLAG bits will produce no change because the flip-flop PF2 is already reset.

The trailing edge of each gated character pulse GCP triggers a conventional one-shot multivibrator OS1 to produce a pulse labeled SET which is, as shown in FIG. **2,** of sufficient duration to bridge the **136** shift pulses that program the search of the memory as just described. This SET pulse is applied to the gates **33** and **34,** one of which is enabled by the ODD or $\overline{\text{ODD}}$ pulse currently produced by the first stage of the counter **10.** The trailing edge of the set pulse accordingly triggers the selected precision one-shot multivibrator OS2 or OS3 to produce a timed pulse XFR1 or XFR2 as described above.

If the pulse XFR1 is produced, the corresponding A latches AF1 through AF136 that have print command signals applied to them by the register **13** will be set to turn on the corresponding current supplies for the associated hammer driver coils L1 through L136 for the duration of the pulse XFR1. In the mean time, the next character pulse CP that is produced, assumed to be for an even character, will advance the counter **10** and enable the gate **12** to produce another pulse GCP. When the subsequent transfer pulse XFR2 is produced by the precision pulse generator OS3, the contents of the shift register **13** will be transferred into the flip-flops BF1 through BF136. These flip-flops will thus be set or not set depending on whether or not the character represented by the counter **10** and now coming into printing position is to be printed in the corresponding column. Since the XFR1 and XFR2 pulses can overlap, as shown in FIG. **2,** the flow of current to the hammer drivers that are to print one character can begin before the flow of current to the hammer drivers that are printing the preceding character is interrupted, although the image forming impacts are still spaced by the interval between characters arriving at the print station.

During some memory scan cycle, which may be the first cycle, the 64th cycle, or any intermediate cycle, the last character in the memory **14** will be found to agree with the character in the counter **10,** and the last FLAG bit will be erased from the memory. The FLAG bit will be erased, after it has reset the flip-flop PF2 to produce the PRINT level, unless the PRINT level is already present, by using the FLAG RESET signal to prevent the FLAG bit from being rewritten into the memory. The character which occasioned the last TC pulse will be printed clearing the ensuing pulse XFR1 or XFR2.

The next character pulse CP will produce a GCP pulse and a CLEAR pulse. The latter will reset the flip-flop PF2 to produce the level $\overline{\text{PRINT}}$. Since there are no characters left in the memory **14,** this level will not be removed. The following character pulse CP will accordingly reset the flip-flop PF1 through the gate PF1, and produce the $\overline{\text{FIRE}}$ level to end the print cycle.

The printer will then enter the cycle in which paper is moved and another line of characters is loaded into the memory. No further operation of the apparatus of my invention will take place until the next start print signal is produced by momentarily closing the switch SP.

While I have described my invention with respect to the details of a preferred embodiment thereof, many changes and variations will occur to those skilled in the art upon reading my description, and such can obviously be made without departing from the scope of my invention.

Having thus described my invention, what I claim is:

1. In combination with a high speed printer having a character pulse generator for producing character pulses at first intervals determined by the intervals between arrival of a series of characters in printing position, memory means for storing a sequence of character signals representing the characters in a line to be printed, means responsive to each character pulse for scanning said memory means and producing a sequence of binary signals each determining whether or not a character is to be printed in a different column following that character pulse, means for sequentially registering said sequences, timing signal generating means responsive to said character pulses for alternately producing a first or a second timing pulse following each memory scan, an image forming device for each binary signal in said sequence, and means controlled by said registering means and said timing signal generating means for energizing each of said image forming devices for a time determined by said timing pulses when said registering means is storing a binary signal indicating that a character is to be printed by that image forming device and one of said timing signals is present.

2. In a high speed printer comprising means for producing character pulses at intervals *t*1 and a series of printing means, each actuable to print characters in response to energy applied at a substantially constant rate for an interval *t*2, where *t*2 is greater than *t*1, means for alternately producing first and second overlapping tim-

ing signals each having a duration $t2$, means for registering a first or a second signal for each image forming device following each character pulse, and means responsive to each first signal and either of said timing signals that is present for energizing the corresponding printing means for the duration of the timing signal that is present.

3. In a high speed printer comprising memory means for storing a sequence of character signals each representing a character in a line to be printed, register means for storing a sequence of binary signals, one for each column in a line to be printed, each binary signal having a first or a second truth value according as a character is or is not to be printed in the associated column, means for producing a character pulse each time a character approaches printing position, means responsive to each character pulse for scanning said memory means and loading said register means with a sequence of binary signals each having a truth value determined by whether or not the character approaching printing position is to be printed in the corresponding column, means responsive to said character pulses for alternately producing first and second timing signals of equal duration greater than the intervals between said character pulses, printing means for each column in a line to be printed, and means controlled by said timing signals and said register means for actuating each printing means when the corresponding signal in said register means indicates that a character is to be printed for the interval of the timing signal that is present.

4. In combination with a high speed printer having more than three image forming devices each requiring energization for an interval $t1$ and print signal registering means loaded at intervals $t2$ less than t1 with signals indicating whether or not each image forming device is to be energized in response to character pulses produced at intervals $t2$, timing signal generating means for alternately producing first and second timing signals of duration $t1$, and means controlled by said registering means and said timing signal generating means for activating each of said image forming devices for the duration of either of said timing signals that is present when said print signal registering means indicates that that image forming device is to be energized.

5. In a high speed printer of the line at a time type having an image printing device for each column in a line to be printed and a character pulse generator for producing a character pulse each time a different character approaches printing position, memory means for storing a sequence of character signals, one for each column in the line to be printed, register means having a storage location for each column in the line to be printed, comparator means responsive to each character pulse for scanning said memory means and storing a sequence of signals in said register means each determining whether or not the character approaching printing position is or is not to be printed in a corresponding column, means for producing a first timing signal following every other character pulse, means for producing a second timing signal following every character pulse not followed by a first timing signal, and means controlled by said register means and said timing signals for energizing each image forming device for the duration of each timing signal produced when the signal in the corresponding location of said register means indicates that the character coming into position is to be printed.

6. The apparatus of claim **5,** in which the duration of said first timing signals is equal to the duration of said second timing signals and greater than the interval between said character pulses.

7. The apparatus of claim **5,** in which said means for energizing each image forming device comprises first and second latch means each enabled by a signal in the corresponding location of said register means indicating that the character coming into printing position is to be printed and set to energize the corresponding image device for an interval corresponding to the duration of a different one of said timing signals.

8. The apparatus of claim **7,** in which the duration of said first timing signal is equal to the duration of said second timing signals and greater than the interval between said character pulses.

9. Apparatus for supplying printing energy to the image forming devices of a high speed printer having a character pulse generator producing character pulses at intervals $t1$ for intervals $t2$ longer than the intervals $t1$ between character pulses, comprising first and second latch means for each image forming device, a register for each image forming device set to a first state or a second state following each character pulse according as said image forming device is or is not to be energized, respectively, means responsive to said character pulses for alternately producing first and second timing signals having equal durations $t2$, and means controlled by each of said registers and by said timing signals when present for energizing the corresponding image forming device when the said register is in its first state for the duration of the timing signal that is present.

10. A print control system for line printers having a line memory adapted to be loaded with digital signals representing the characters to be printed on a line and means for moving a font of characters past each of a bank of image forming devices, one for each column in a line to be printed, comprising means for producing a character pulse each time a different character approaches printing position, means responsive to each character pulse for searching the memory for the character then approaching printing position, a first register, means responsive to each character pulse for loading said first register with a print signal for each column in which the associated character is to be printed, means responsive to each character pulse for detecting the parity of the character pulse in a predetermined sequence, a first bank of latches, one for each image forming device, a second bank of latches, one for each image forming device, means responsive to each character pulse and to said parity detecting means for producing a first or a second timing pulse for each character pulse in accordance with the parity of that character pulse, means responsive to said first timing pulse for actuating said first bank of latches to a first state or a second state in accordance with the contents of said first register to set the corresponding latch of said first bank of latches to its first state for the interval of said first pulse when the corresponding character print signal is present in said first register, means responsive to said second timing pulse for actuating said second bank of latches to a first state or a second state in accordance with the contents of said first register to set the corresponding latch of said second bank to its first state for the interval of said second pulse when the corresponding character print signal is present in said first register,

and means controlled by said banks of latches in their first states for energizing said image forming devices.

11. The apparatus of claim **10,** in which said timing pulses are of equal duration greater than the intervals between character pulses.

12. In a high speed printer having the capacity to print in more than three columns, means for producing character pulses, a register having the capacity to store a signal for each column to be printed, means for loading said register at each character pulse with signals indicating whether or not the corresponding character is to be printed in each column, first and second timing pulse generators each operable to produce a timing signal having a predetermined duration longer than the interval between character pulses, said timing pulses overlapping, first and second latch means, an image forming device for each column to be printed, and means controlled by said timing pulse generators, said latch means, and said register for energizing each image forming device each time a corresponding signal in said register indicates that a character is to be printed when a timing signal is produced for the duration of the timing signal.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,855,923 Dated December 24, 1973

Inventor(s) _____

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

On the title page, after inventors' names insert --[73] Assignee: Data Printer Corporation, Cambridge, Massachusetts--.

Signed and sealed this 15th day of April 1975.

(SEAL)
Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents
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