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(54) ELECTRICAL INTERCONNECTION AND THIN FILM TRANSISTOR FABRICATION METHODS, AND INTEGRATED CIRCUITRY

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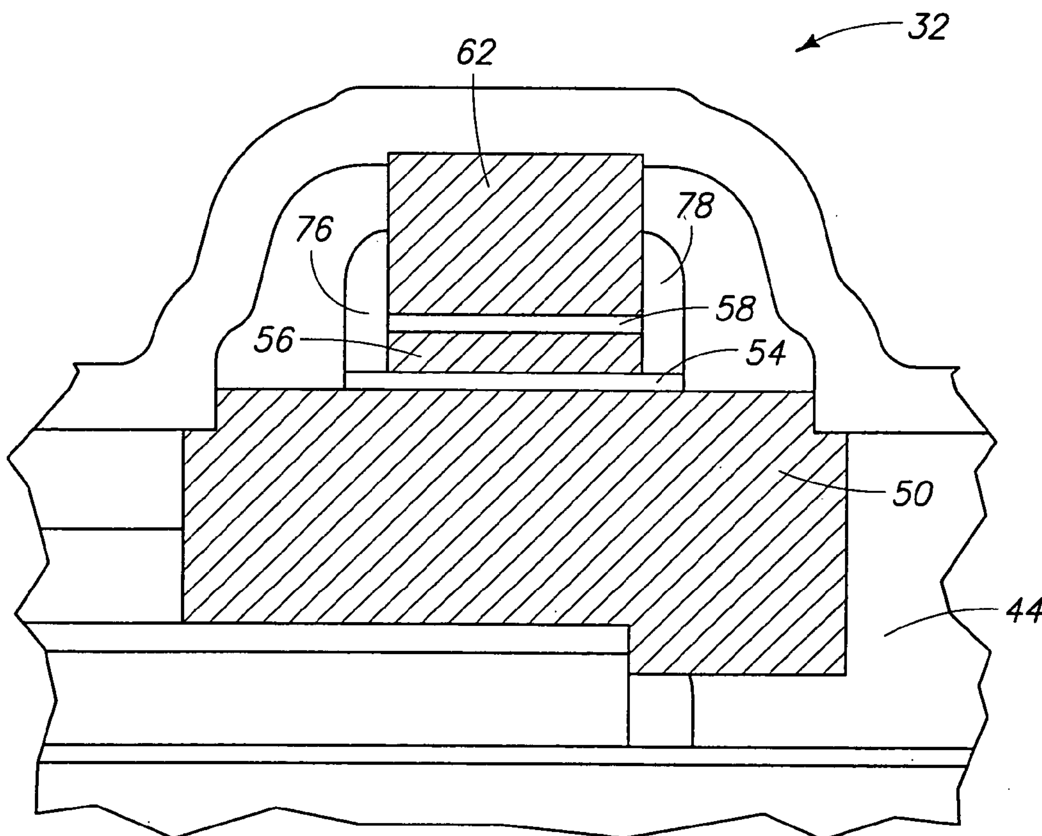
(57) ABSTRACT

An electrical interconnection method includes: a) providing two conductive layers separated by an insulating material on a semiconductor wafer; b) etching the conductive layers and insulating material to define and outwardly expose a sidewall of each conductive layer; c) depositing an electrically conductive material over the etched conductive layers and their respective sidewalls; and d) anisotropically etching the conductive material to define an electrically conductive sidewall link electrically interconnecting the two conductive layers. Such is utilizable to make thin film transistors and other circuitry.



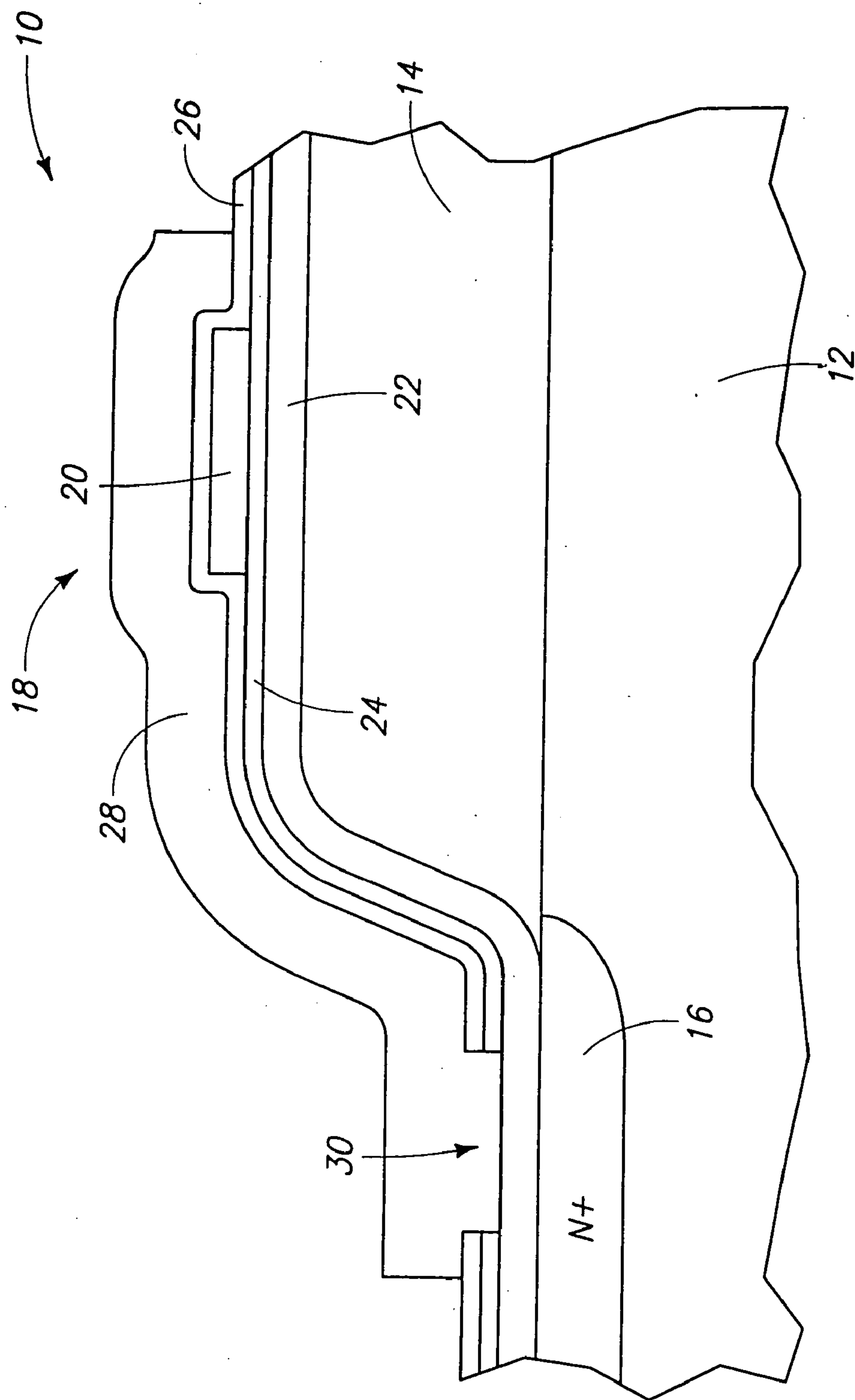
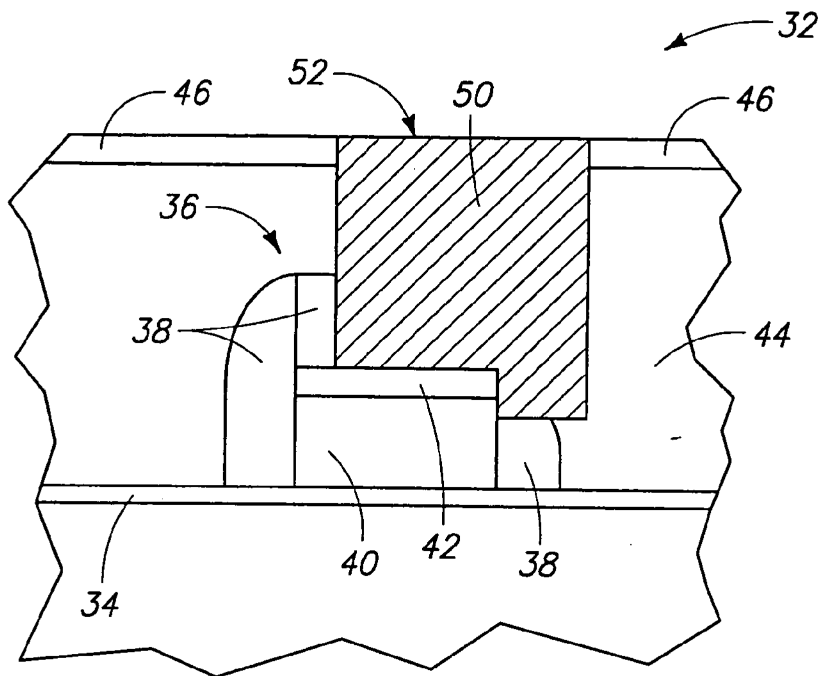


FIG 1
PRIOR ART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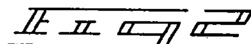
Fig 2

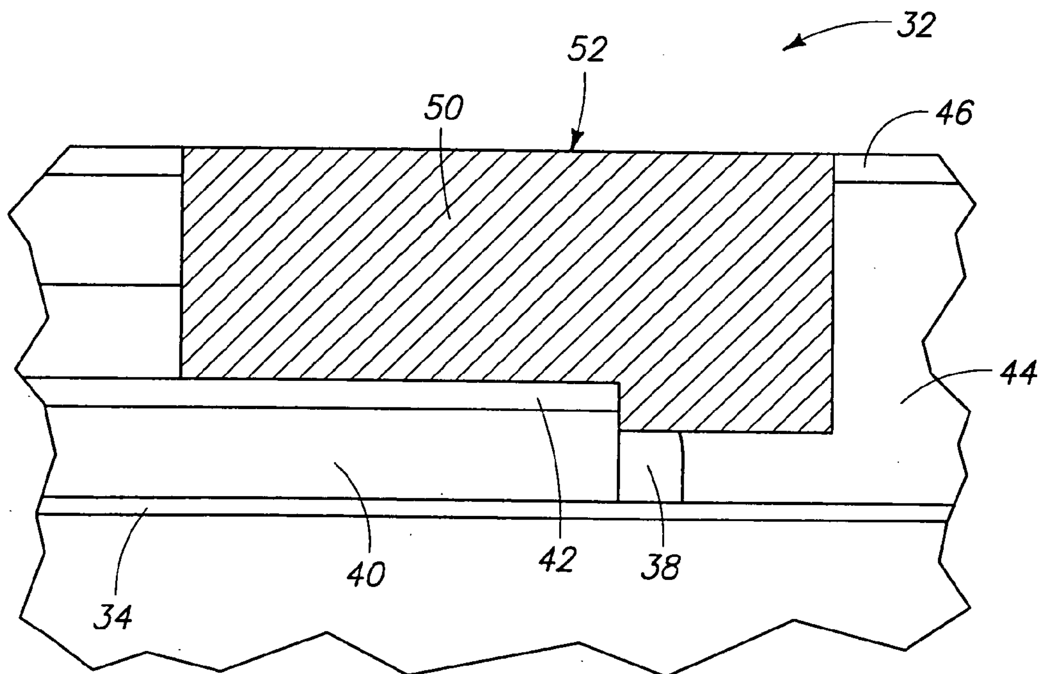
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Fig 3

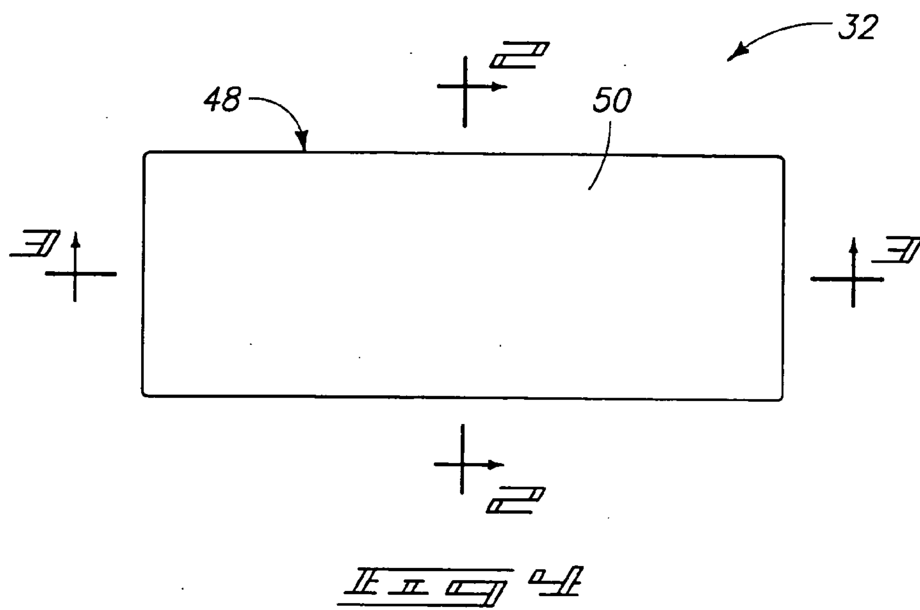


Fig 4

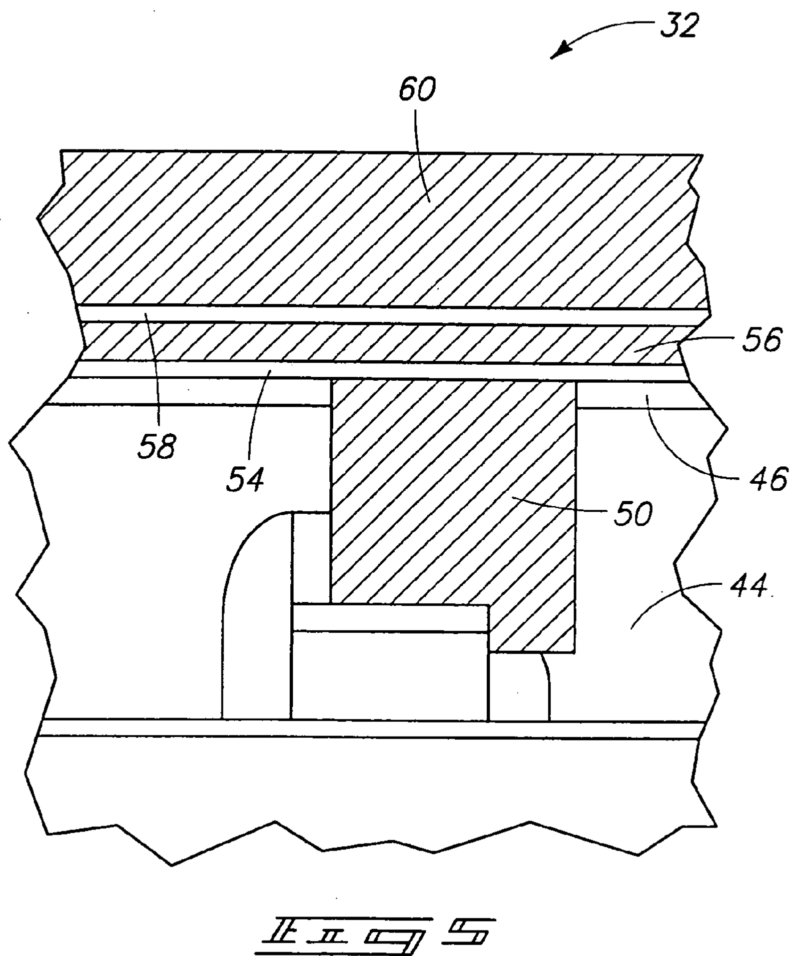


Fig 5

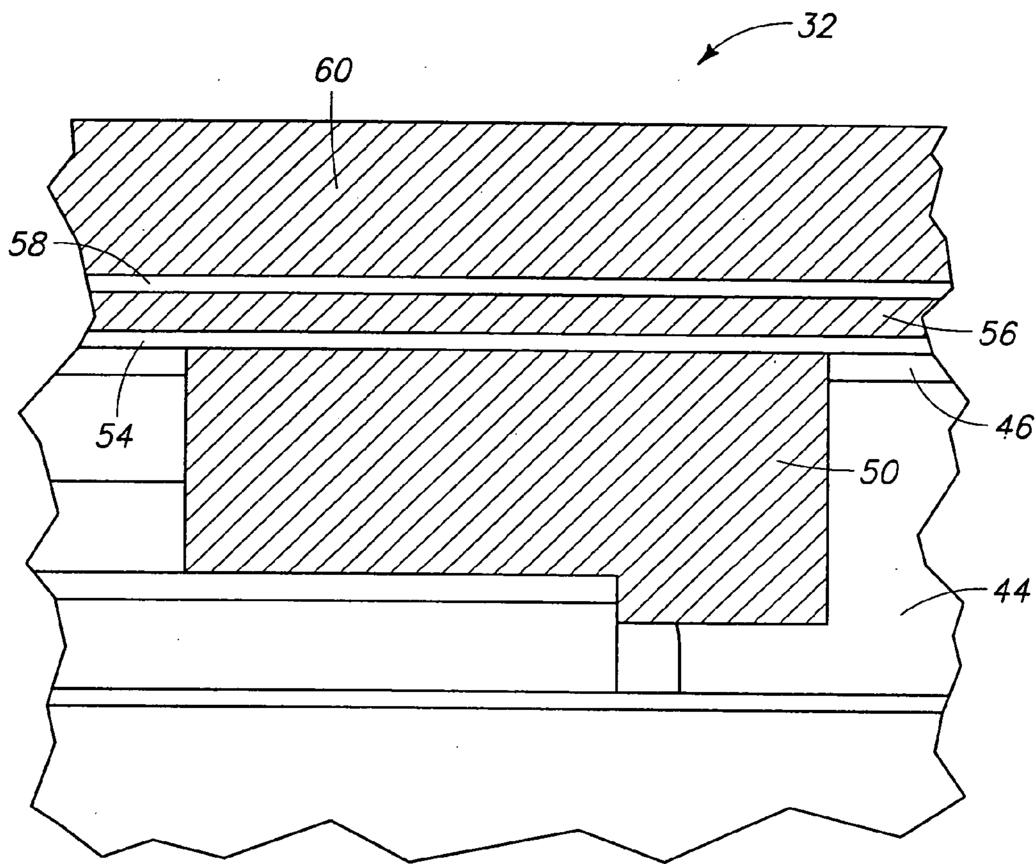


Fig 6

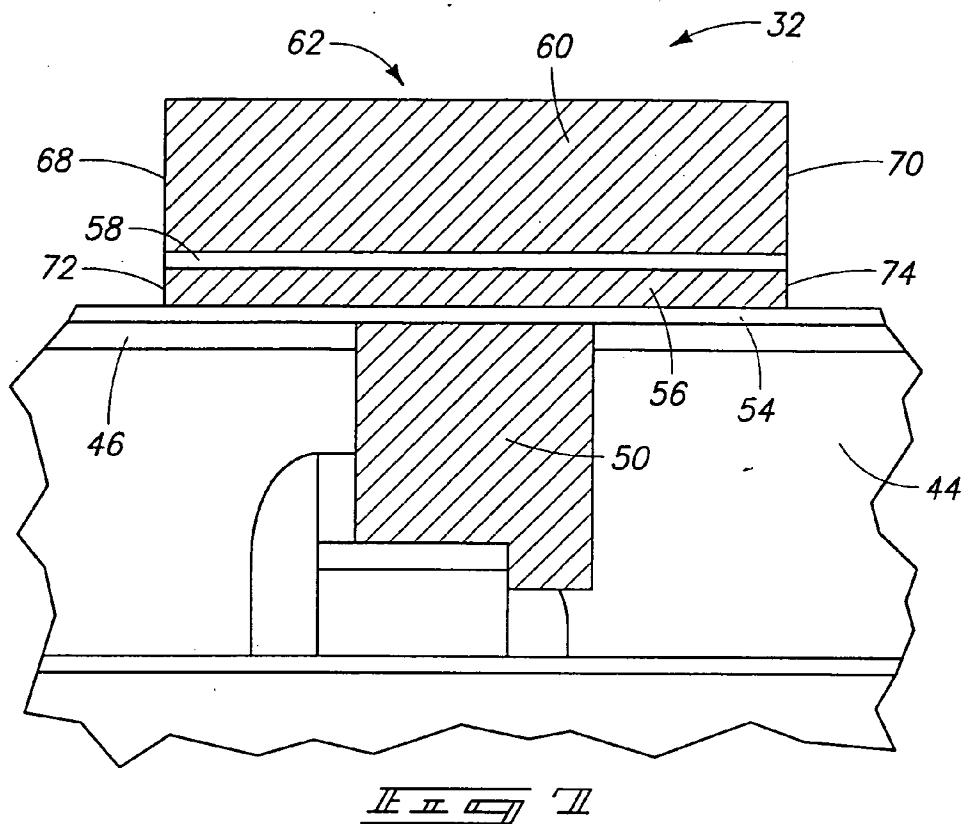


Fig. 7

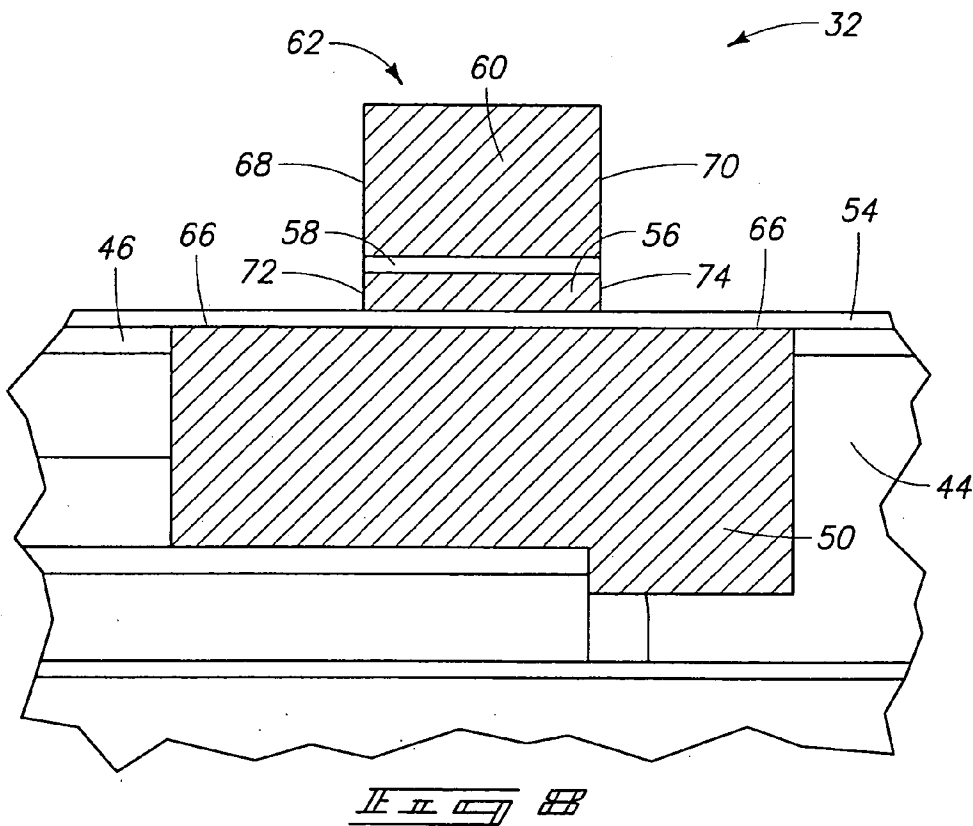


Fig. 8

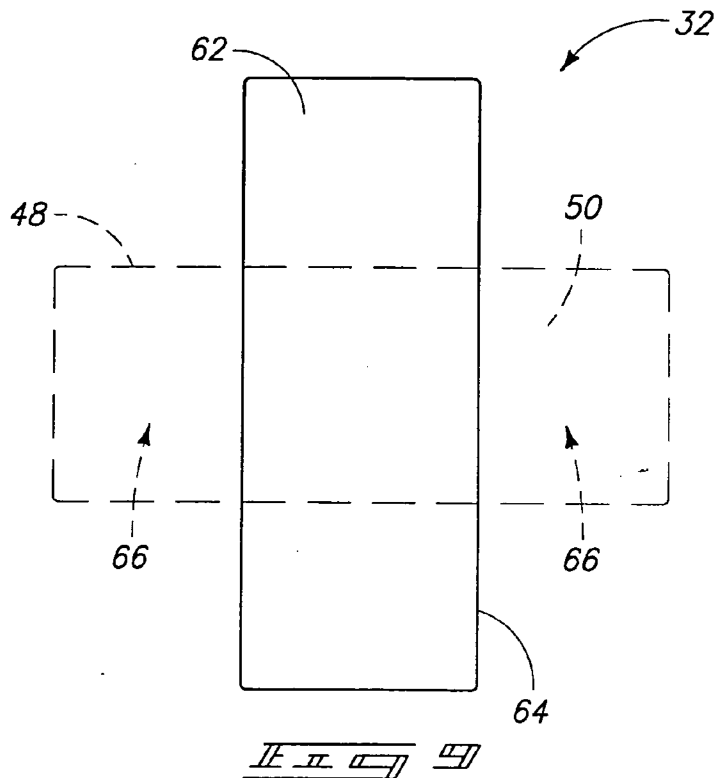
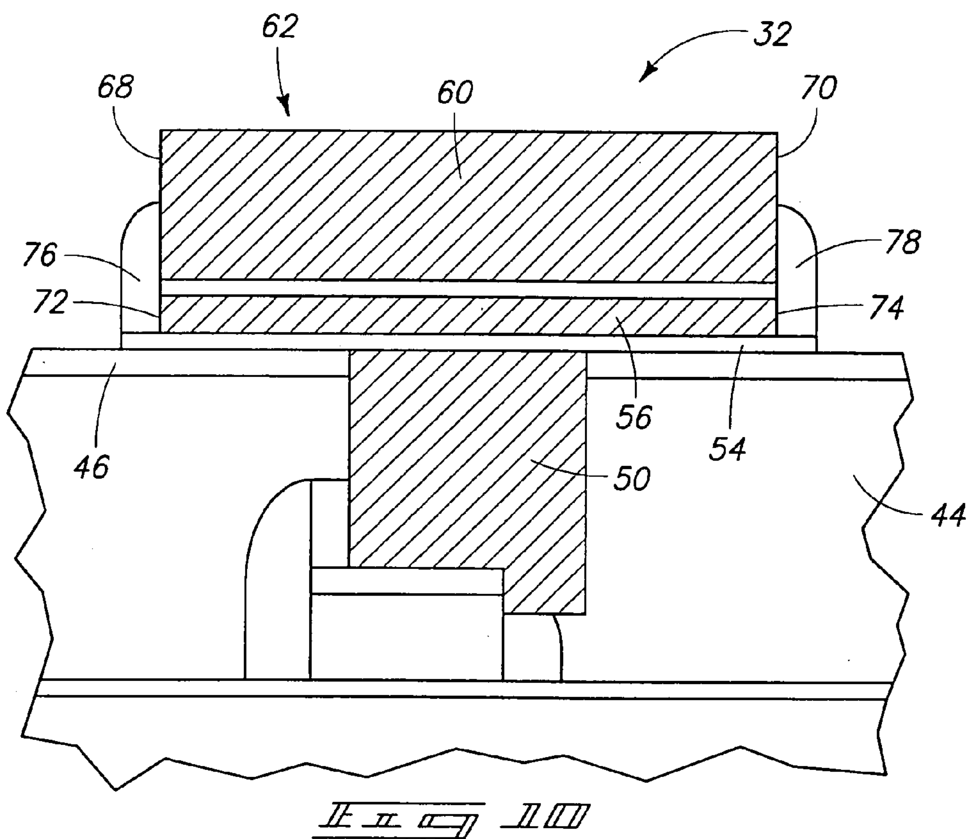


Fig 9



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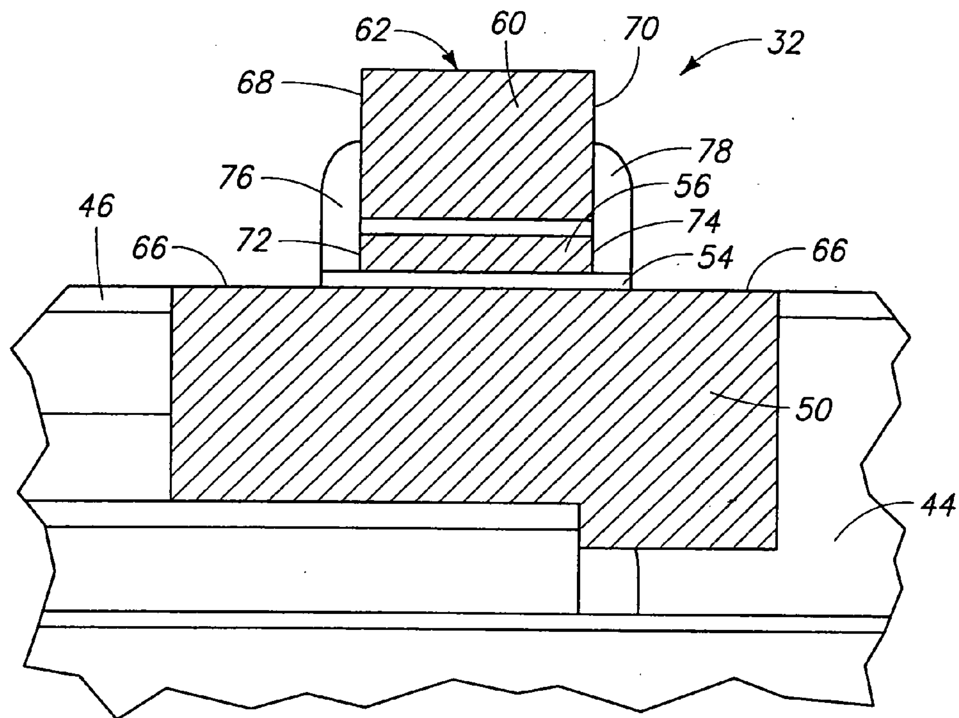


Fig 11

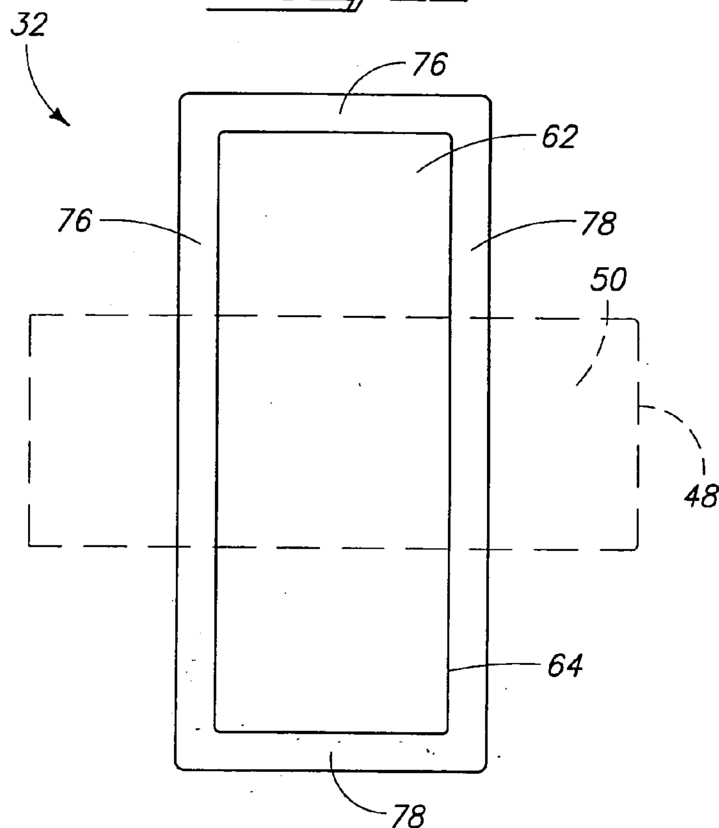


Fig 12

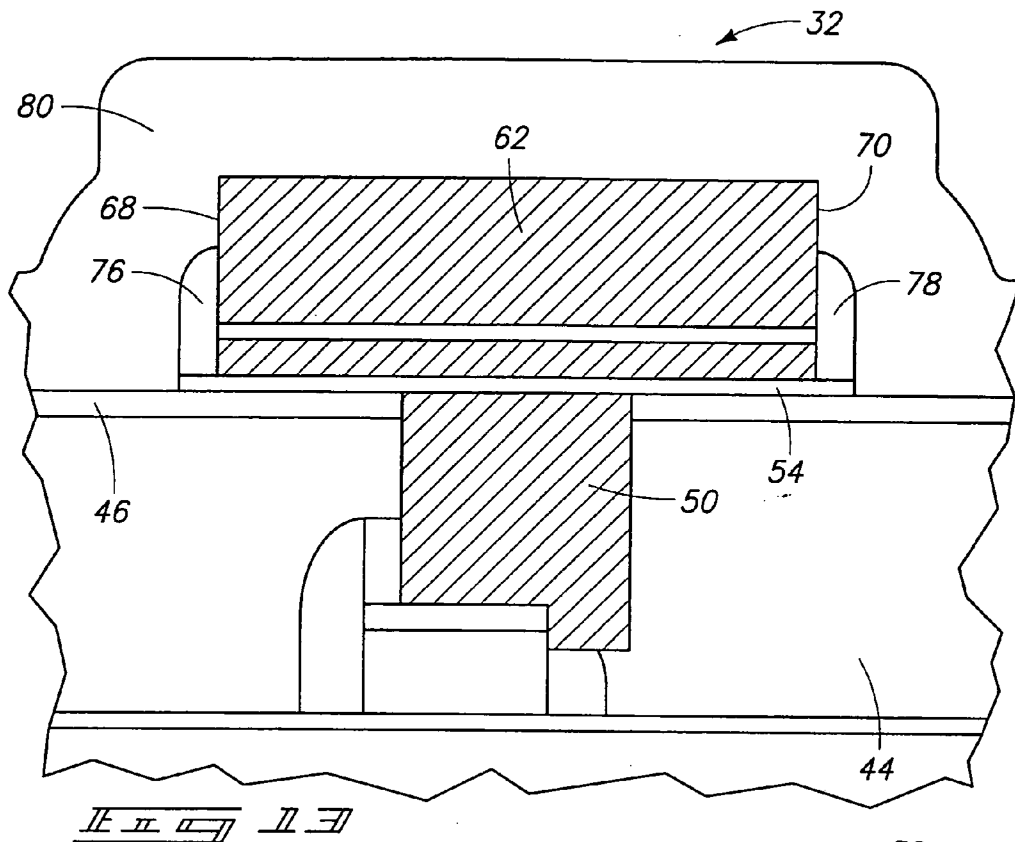


Fig 13

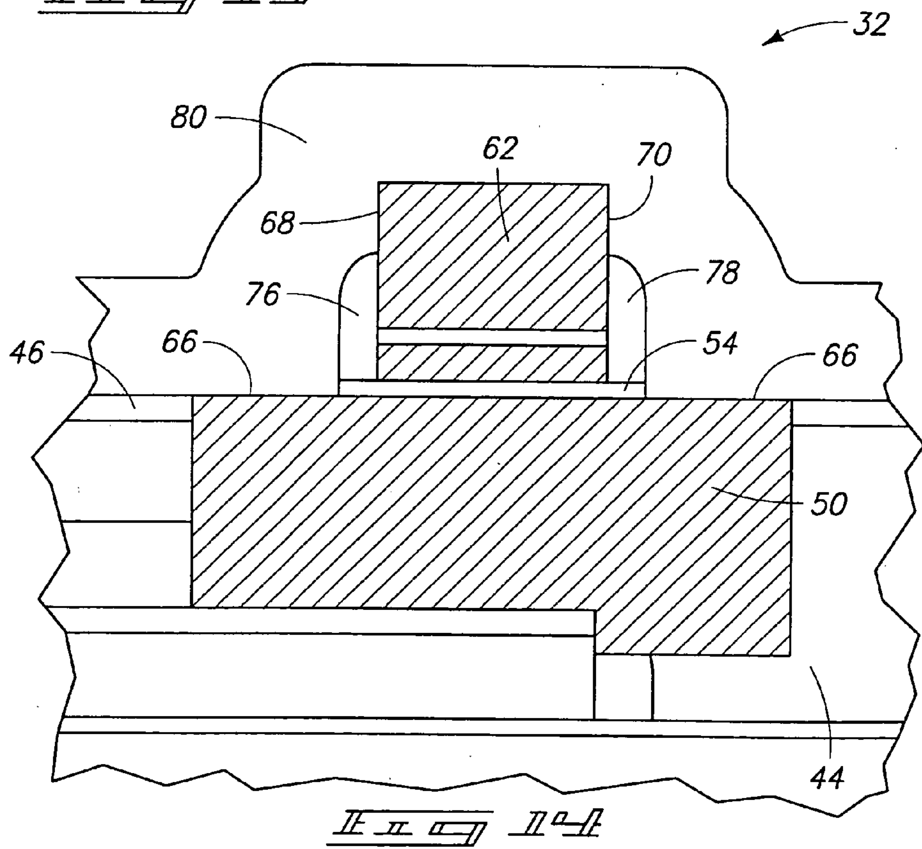


Fig 14

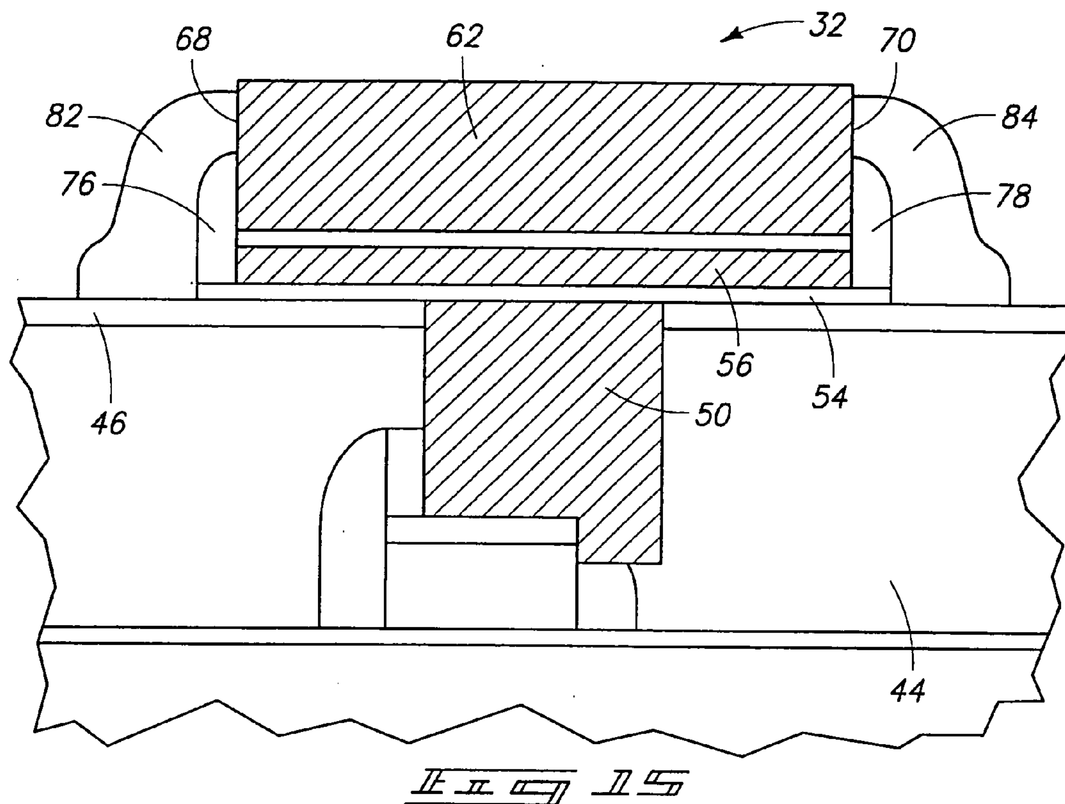


Fig 15

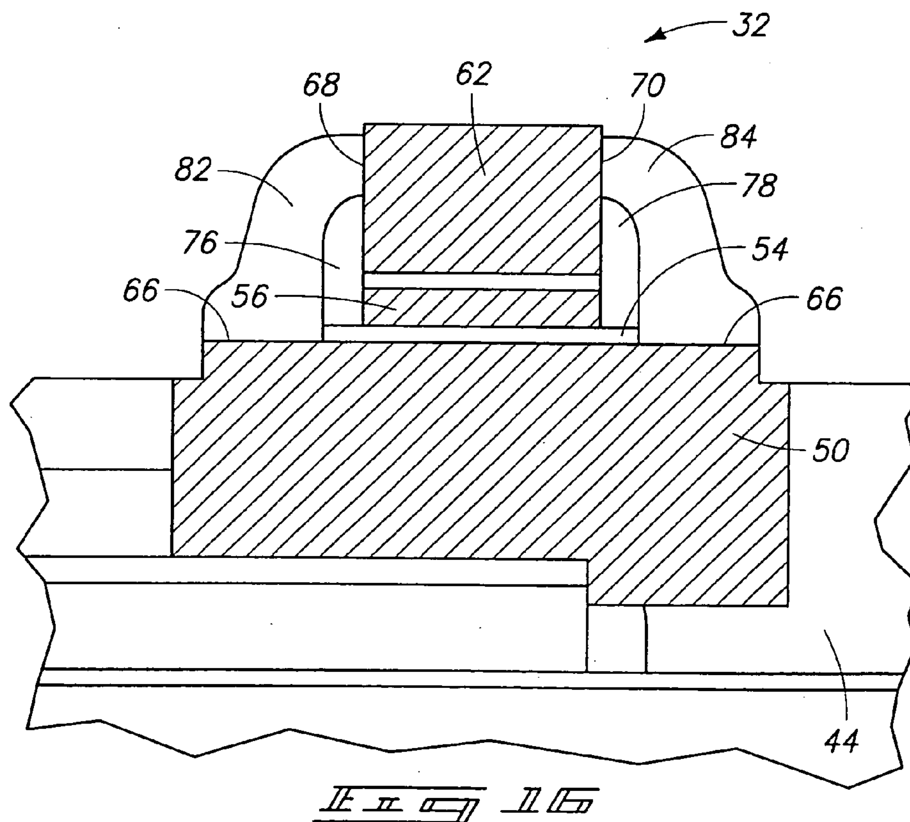


Fig 16

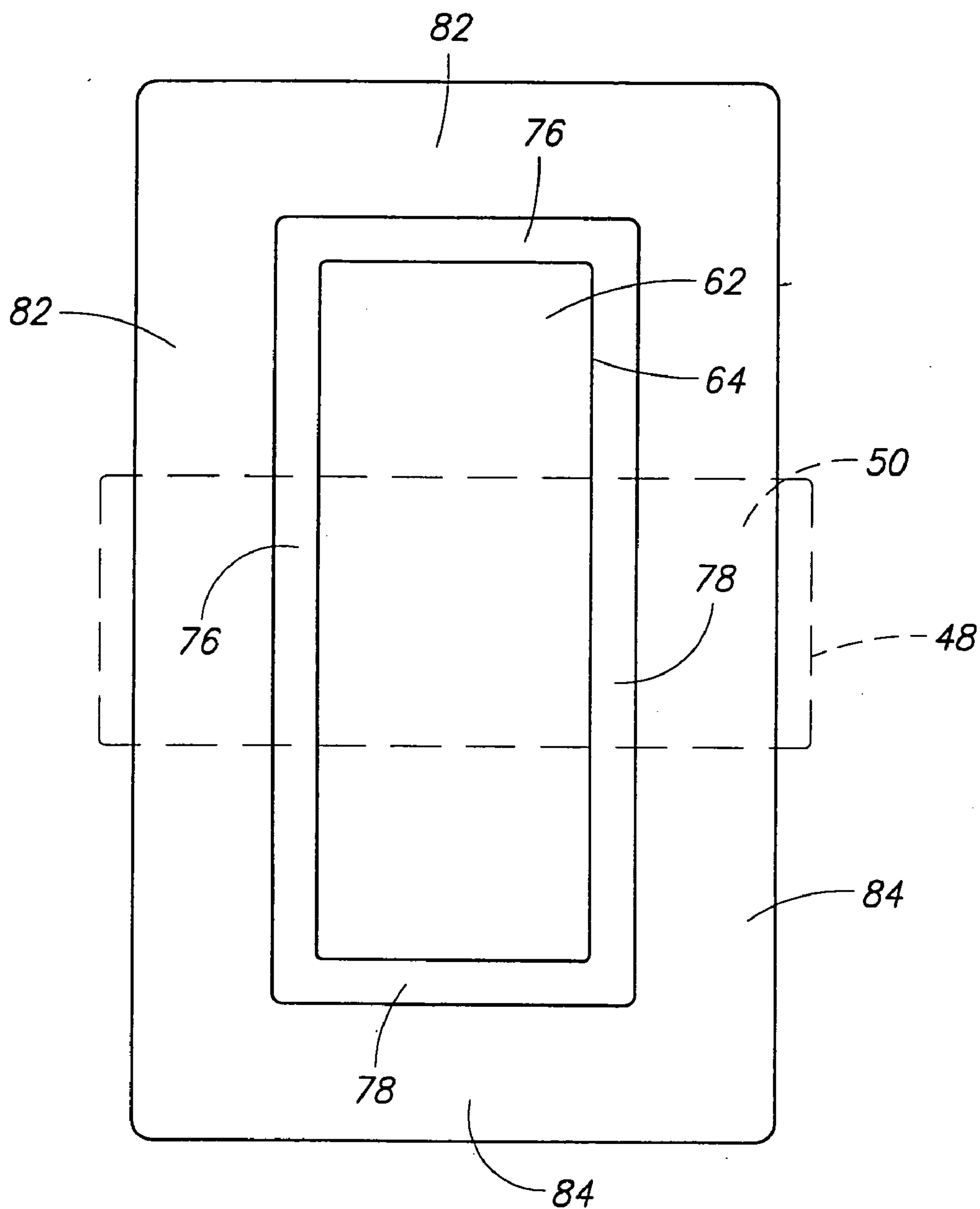


Fig 17

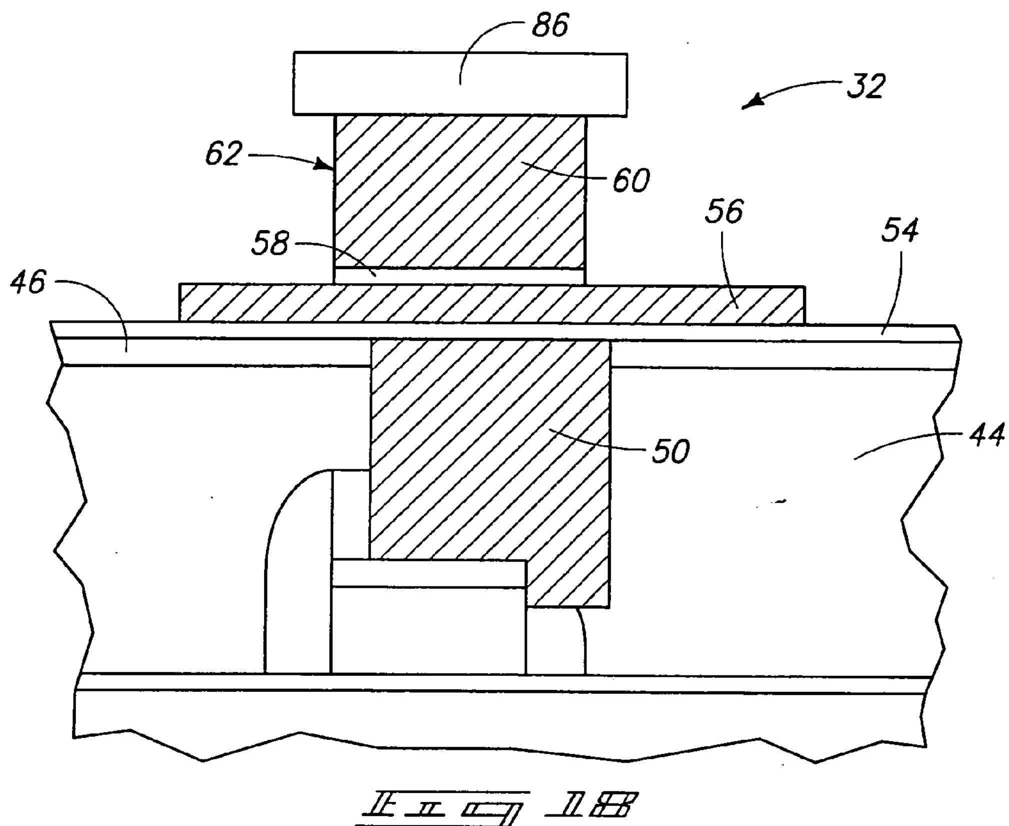
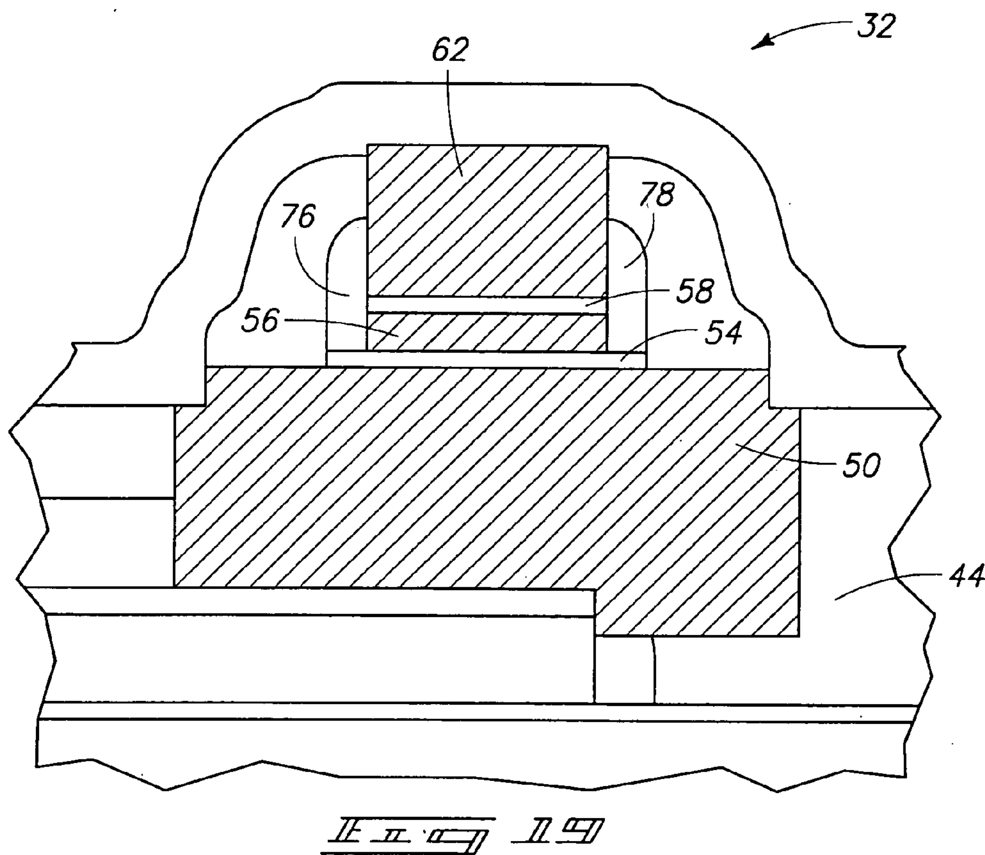


Fig 18



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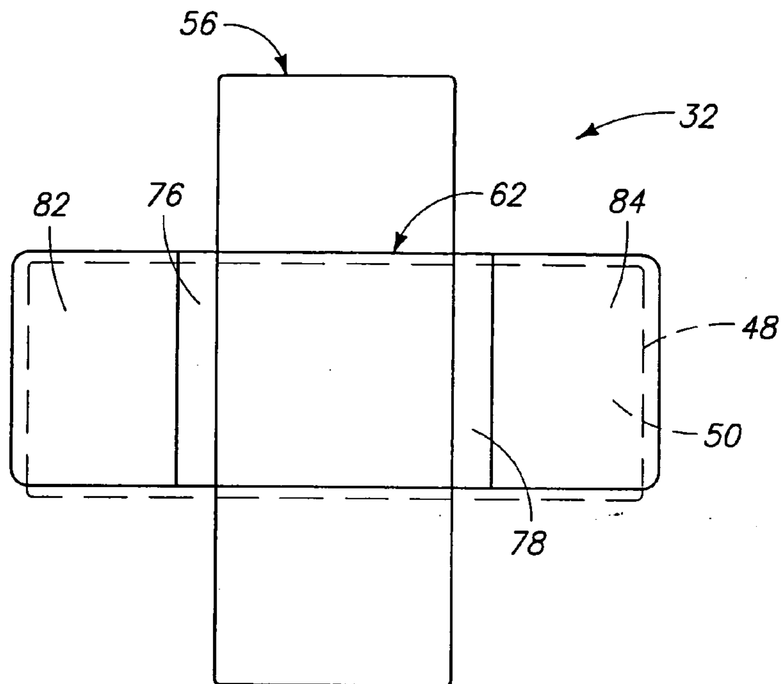
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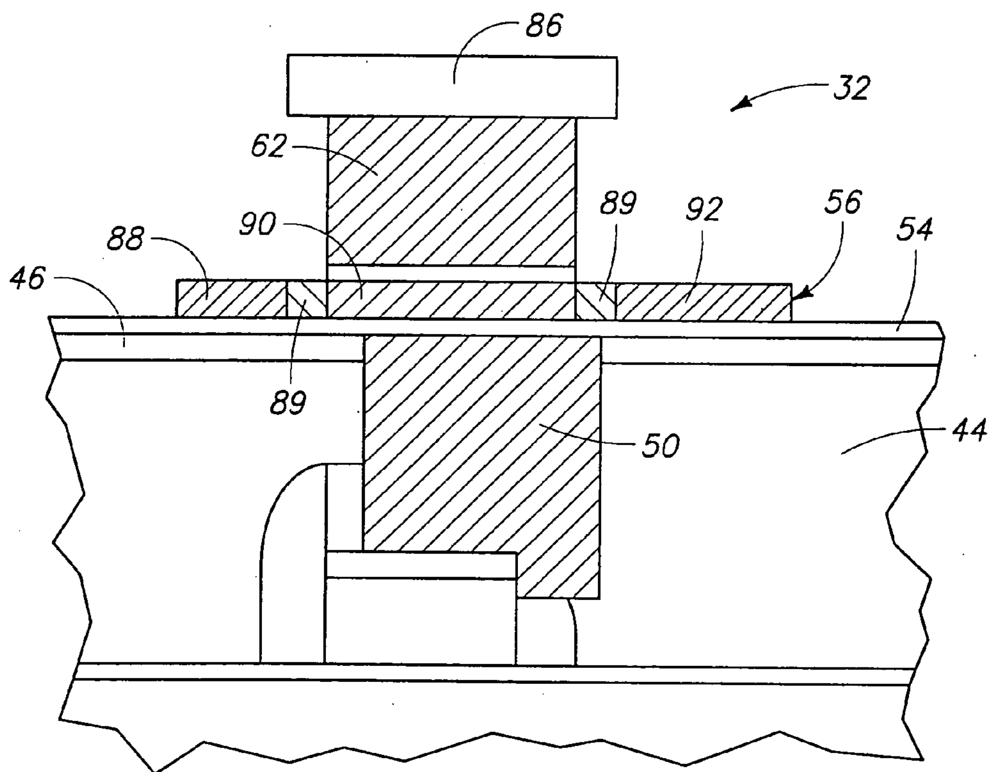
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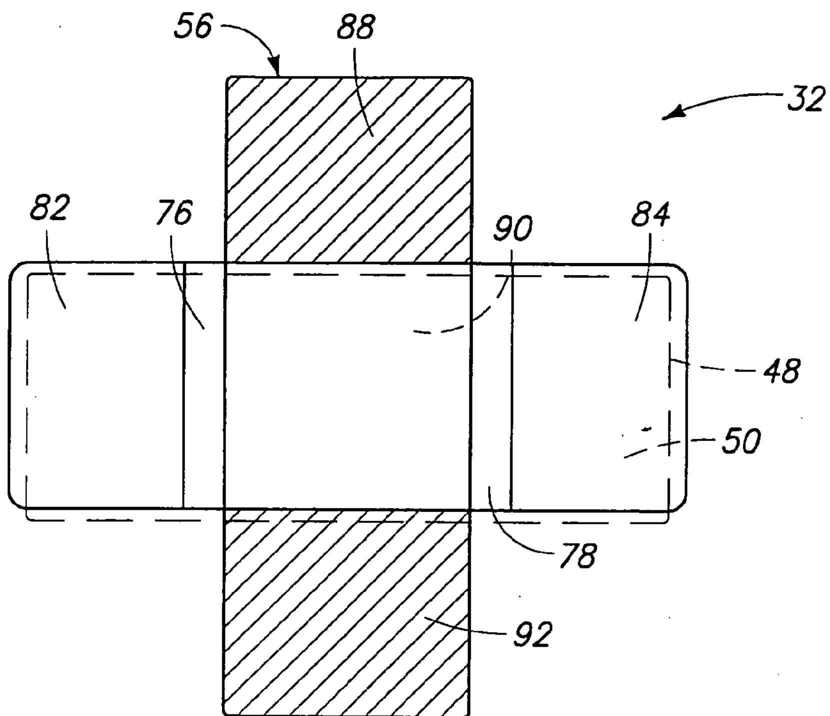
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Fig 22

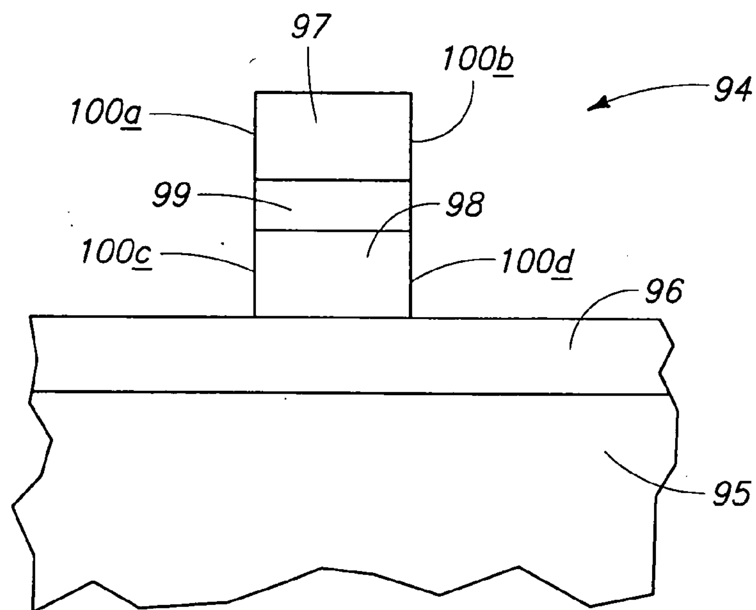
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Fig 23

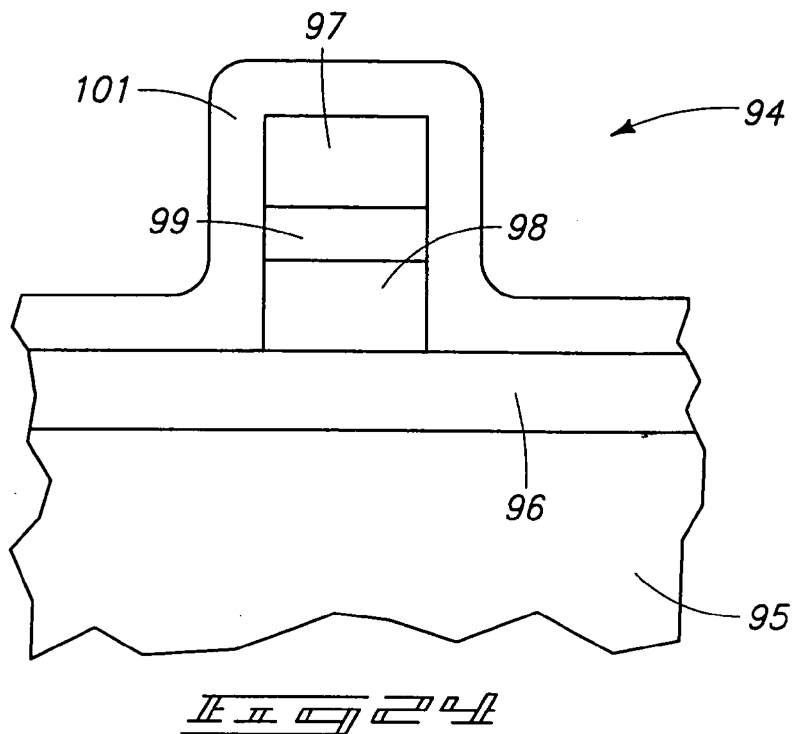

Fig 24

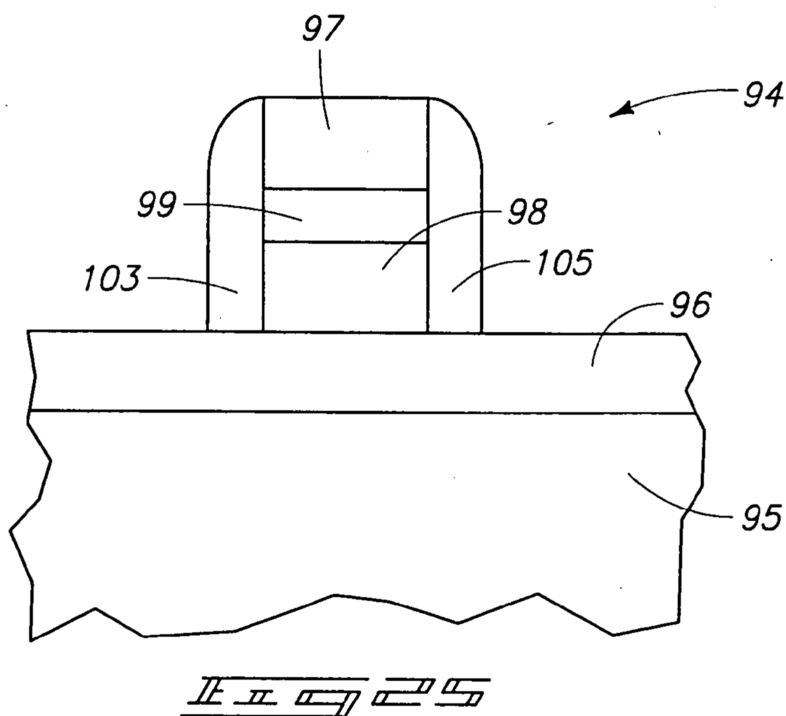

Fig 25

ELECTRICAL INTERCONNECTION AND THIN FILM TRANSISTOR FABRICATION METHODS, AND INTEGRATED CIRCUITRY

TECHNICAL FIELD

[**0001**] This invention relates to electrical interconnection and thin film transistor fabrication methods, and to integrated circuitry having electrically interconnected layers.

BACKGROUND OF THE INVENTION

[**0002**] The invention grew out of needs associated with thin film transistors (TFTs) and their usage in high-density static random access memories (SRAMs). A static memory cell is characterized by operation in one of two mutually exclusive and cell-maintaining operating states. Each operating state defines one of the two possible binary bit values, zero or one. A static memory cell typically has an output which reflects the operating state of the memory cell. Such an output produces a "high" voltage to indicate a "set" operating state. The memory cell output produces a "low" voltage to indicate a "reset" memory cell operating state. A low or reset output voltage usually represents a binary value of zero, and a high or set output voltage represents a binary value of one.

[**0003**] A static memory cell is said to be bi-stable because it has two stable or self-maintaining operating states, corresponding to two different output voltages. Without external stimuli, a static memory cell will operate continuously in a single one of its two operating states. It has internal feedback to maintain a stable output voltage, corresponding to the operating state of the memory cell, as long as the memory cell receives power.

[**0004**] The operation of a static memory cell is in contrast to other types of memory cells, such as dynamic cells, which do not have stable operating states. A dynamic memory cell can be programmed to store a voltage which represents one of two binary values, but requires periodic reprogramming or "refreshing" to maintain this voltage for more than very short time periods. A dynamic memory cell has no feedback to maintain a stable output voltage. Without refreshing, the output of a dynamic memory cell will drift toward intermediate or indeterminate voltages, effectively resulting in loss of data.

[**0005**] Dynamic memory cells are used in spite of this limitation because of the significantly greater packaging densities which can be attached. For instance, a dynamic memory cell can be fabricated with a single MOSFET transistor, rather than the six transistors typically required in a static memory cell. Because of the significantly different architectural arrangements and functional requirements of static and dynamic memory cells and circuits, static memory design has developed along a different path than has the design of dynamic memories.

[**0006**] Ongoing efforts in SRAM circuitry to improve active loads has brought about the development of TFTs in attempts to provide low leakage current as well as high noise immunity. While the invention grew out of needs associated with TFTs of SRAM circuitry, the artisan will appreciate applicability of the invention to other types of circuitry.

[**0007**] Some recent TET technology employs fully surrounded field effect transistor (FET) gate regions, such as shown in **FIG. 1**. Such illustrates a semiconductor wafer fragment **10** comprised of a bulk substrate **12** and overlying insulating layer **14**. Bulk substrate **12** includes an n+ active area **16** which electrically connects with a gate of a thin film transistor, which is generally indicated by numeral **18**. Such transistor includes a channel region **20**. The adjacent source and drain of such transistor would be into and out of the plane of the paper on which **FIG. 1** appears. A first or bottom gate conductive layer **22** is provided over insulating layer **14** and extends to electrically connect with active area **16**. A bottom gate oxide dielectric layer **24** is provided atop bottom gate layer **22** and contacts with the bottom of transistor channel region **20**. A top gate layer **26** overlies bottom dielectric layer **24** and the top of transistor channel region **20**. An electrically conductive top gate layer **28** is provided and patterned over top gate oxide dielectric layer **26**. A contact opening **30** is provided through top and bottom gate oxide layers **26, 24** respectively, over active area **16** prior to top gate layer **28** deposition. Such results in electrical interconnection of top gate **28** with a bottom gate **22**. Thus, channel region **20** is surrounded by conductive gate material for switching transistor **18**"on".

[**0008**] The above described construction requires photolithography and etch steps for producing contact opening **30**, and separate patterning of top gate electrode **28**. It would be desirable to provide methods of forming thin film transistors which minimize photolithography and etching steps.

BRIEF DESCRIPTION OF THE DRAWINGS

[**0009**] Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

[**0010**] **FIG. 1** is a diagrammatic section of a semiconductor wafer fragment processed in accordance with prior art methods, and is described in the "Background" section above.

[**0011**] **FIG. 2** is a diagrammatic section of a semiconductor wafer fragment processed in accordance with the invention. Such view is a section of the wafer fragment taken along a position relative to line Y-Y in **FIG. 4**.

[**0012**] **FIG. 3** is a view of the **FIG. 2** wafer fragment taken at a same processing step as that illustrated by **FIG. 2**. Such view is a section of the wafer fragment taken along a position relative to line X-X in **FIG. 4**.

[**0013**] **FIG. 4** is a diagrammatic top plan view of the **FIG. 2** wafer fragment taken at the same processing step as that illustrated by **FIG. 2**.

[**0014**] **FIG. 5** is a view of the **FIG. 2** wafer fragment taken at the same relative position as **FIG. 2**, but at a process step subsequent to that illustrated by **FIG. 2**.

[**0015**] **FIG. 6** is a view of the **FIG. 2** wafer fragment taken at the same relative position as **FIG. 3**, but at a process step subsequent to that illustrated by **FIG. 3** and corresponding in process sequence to that of **FIG. 5**.

[**0016**] **FIG. 7** is a view of the **FIG. 2** wafer fragment taken at the same relative position as **FIG. 2**, but at a process step subsequent to that illustrated by **FIG. 5**.

[**0017**] **FIG. 8** is a view of the **FIG. 2** wafer fragment taken at the same relative position as **FIG. 3**, but at a process

step subsequent to that illustrated by **FIG. 6** and corresponding in process sequence to that of **FIG. 7**.

[**0018**] **FIG. 9** is a top plan view of the **FIG. 2** wafer fragment taken at the same processing step as that illustrated by **FIG. 7**.

[**0019**] **FIG. 10** is a view of the **FIG. 2** wafer fragment taken at the same relative position as **FIG. 2**, but at a process step subsequent to that illustrated by **FIG. 7**.

[**0020**] **FIG. 11** is a view of the **FIG. 2** wafer fragment taken at the same relative position as **FIG. 3**, but at a process step subsequent to that illustrated by **FIG. 8** and corresponding in process sequence to that of **FIG. 10**.

[**0021**] **FIG. 12** is a top plan view of the **FIG. 2** wafer fragment taken at the same processing step as that illustrated by **FIG. 10**.

[**0022**] **FIG. 13** is a view of the **FIG. 2** wafer fragment taken at the same relative position as **FIG. 2**, but at a process step subsequent to that illustrated by **FIG. 10**.

[**0023**] **FIG. 14** is a view of the **FIG. 2** wafer fragment taken at the same relative position as **FIG. 3**, but at a process step subsequent to that illustrated by **FIG. 10** and corresponding in process sequence to that of **FIG. 13**.

[**0024**] **FIG. 15** is a view of the **FIG. 2** wafer fragment taken at the same relative position as **FIG. 2**, but at a process step subsequent to that illustrated by **FIG. 13**.

[**0025**] **FIG. 16** is a view of the **FIG. 2** wafer fragment taken at the same relative position as **FIG. 3**, but at a process step subsequent to that illustrated by **FIG. 14** and corresponding in process sequence to that of **FIG. 15**.

[**0026**] **FIG. 17** is a top plan view of the **FIG. 2** wafer fragment taken at the same processing step as that illustrated by **FIG. 15**.

[**0027**] **FIG. 18** is a view of the **FIG. 2** wafer fragment taken at the same relative position as **FIG. 2**, but at a process step subsequent to that illustrated by **FIG. 15**.

[**0028**] **FIG. 19** is a view of the **FIG. 2** wafer fragment taken at the same relative position as **FIG. 3**, but at a process step subsequent to that illustrated by **FIG. 16** and corresponding in process sequence to that of **FIG. 18**.

[**0029**] **FIG. 20** is a top plan view of the **FIG. 2** wafer fragment taken at the same processing step as that illustrated by **FIG. 18**.

[**0030**] **FIG. 21** is a view of the **FIG. 2** wafer fragment taken at the same relative position as **FIG. 2**, but at a process step subsequent to that illustrated by **FIG. 18**.

[**0031**] **FIG. 22** is a top plan view of the **FIG. 2** wafer fragment taken at the same processing step as that illustrated by **FIG. 21**.

[**0032**] **FIG. 23** is a diagrammatic section of an alternate wafer fragment at a processing step in accordance with another aspect of the invention.

[**0033**] **FIG. 24** is a view of the **FIG. 23** wafer fragment taken at a processing step subsequent to that illustrated by **FIG. 23**.

[**0034**] **FIG. 25** is a view of the **FIG. 23** wafer fragment taken at a processing step subsequent to that illustrated by **FIG. 24**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[**0035**] This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

[**0036**] In the context of this document, "electrically conductive material" signifies a material which is inherently conductive as deposited, or capable of being rendered electrically conducted by subsequent processing steps or applications of conventional operational electric fields.

[**0037**] In accordance with one aspect of the invention, a method of fabricating a bottom and top gated thin film transistor comprises the following steps:

[**0038**] providing an electrically conductive bottom thin film transistor gate electrode layer on a semiconductor substrate, the bottom gate electrode layer having a planarized outer surface, the outer surface having a surface area;

[**0039**] providing a bottom gate dielectric layer over the bottom gate electrode layer;

[**0040**] providing a thin film transistor body layer over the bottom gate layer;

[**0041**] defining source, drain and channel regions within the thin film body layer;

[**0042**] providing a top gate dielectric layer over the thin film transistor body layer;

[**0043**] providing an electrically conductive too transistor gate electrode layer over the top gate dielectric layer;

[**0044**] etching the composite top gate electrode, top gate dielectric, and body layers in a pattern which defines a top gate electrode, top gate dielectric and body outline which is received only partially within the bottom gate electrode outer surface area, the bottom gate electrode outer surface area including a portion extending outwardly beyond the outline, the etching defining outwardly exposed top gate electrode and body sidewalls;

[**0045**] providing a layer of insulating dielectric over the etched top gate electrode and outwardly exposed sidewalls;

[**0046**] anisotropically etching the insulating dielectric layer to define an insulating sidewall spacer, the sidewall spacer leaving the top gate electrode sidewall outwardly exposed;

[**0047**] outwardly exposing bottom gate electrode surface area extending outwardly beyond the outline;

[**0048**] providing a layer of electrically conductive material over the outwardly exposed top gate electrode sidewall and outwardly exposed bottom gate electrode surface area; and

[0049] anisotropically etching the layer of conducting material to define an electrically conductive sidewall link electrically interconnecting the top gate electrode sidewall and bottom gate electrode outer surface.

[0050] In accordance with another aspect of the invention, an electrical interconnection method comprises:

[0051] providing two conductive layers separated by an insulating material on a semiconductor wafer;

[0052] etching the conductive layers and insulating material to define and outwardly expose a sidewall of each conductive layer;

[0053] depositing an electrically conductive material over the etched conductive layers and their respective sidewalls; and

[0054] anisotropically etching the conductive material to define an electrically conductive sidewall link electrically interconnecting the two conductive layers.

[0055] In accordance with still a further aspect of the invention, an electrical interconnection method comprises:

[0056] providing inner and outer conductive layers separated by an insulating material on a semiconductor wafer;

[0057] etching the conductive layers and insulating material to define and outwardly expose a sidewall of the outer conductive layer and to outwardly expose the inner conductive layer;

[0058] depositing an electrically conductive material over the etched conductive layers, the electrically conductive material contacting the outer conductive layer exposed sidewall and exposed inner conductive layer; and

[0059] anisotropically etching the conductive material to define an electrically conductive sidewall link electrically interconnecting the two conductive layers.

[0060] The invention also contemplates integrated circuitry formed in accordance with the above methods, and well as other integrated circuitry.

[0061] More specifically and referring initially to **FIGS. 2-4**, a semiconductor wafer fragment is indicated generally by reference numeral **32**. Such comprises a gate oxide layer **34** and word line **36**. Bulk substrate would exist below gate oxide **34**, and is not shown for clarity. Word line **36** is comprised of insulating regions **38**, electrically conductive polysilicon region **40**, and overlying electrically conductive silicide region **42**. An insulating oxide layer **44** and subsequent insulative nitride layer **46** are provided over word line **36**. Layers **46** and **44** have been photo-patterned and etched to produce a bottom electrode contact outline **48** **(FIG. 4)** which extends inwardly to expose and ultimately provide electrical connection silicide region **42** of word line **36**. The etch is timed such that silicide region **42** is reached with minimal over-etch such that the adjacent substrate is not reached. Subsequently, a layer of electrically conductive material, preferably polysilicon, is deposited atop the wafer to a thickness sufficient to completely fill bottom thin film transistor gate electrode outline **48**. Such layer is then chemical-mechanical polished (CMP) to isolate and define an electrically conductive bottom thin film transistor gate electrode **50** on a semiconductor substrate. Such electrode has a planarized outer surface **52** and an outer surface area defined by outline **48**. A more detailed description of forming such a construction id described in our co-pending U.S. patent application Ser. No. 08/061,402, filed on May 12, 1993, and entitled "Fully Planarized Thin Film Transistor (TFT) and Process To Fabricate Same", which is hereby incorporated by reference.

[0062] Referring to **FIGS. 5 and 6**, a bottom gate dielectric layer **54** is provided over bottom gate electrode layer **50**. Such preferably comprises SiO_2 deposited to a thickness of from about 100 Angstroms to about 500 Angstroms. A thin film transistor body layer **56** is provided over bottom gate layer **54**. Such is preferably amorphous silicon as-deposited, which is then transformed to polycrystalline silicon by solid phase crystallization technique. Such preferably is provided to a thickness of from about 100 Angstroms to about 700 Angstroms. A conventional V_t n− adjust implant into layer **56** would then preferably be provided. A top gate dielectric layer **58** is provided over thin film transistor body layer **56**. Such preferably comprises SiO_2 deposited to a thickness of from about 100 Angstroms to about 500 Angstroms. An electrically conductive top transistor gate electrode layer **60** is provided over top gate dielectric layer **58**. Such preferably comprises in situ conductively doped polysilicon deposited to a thickness of about 2,000 Angstroms. Thus, and for purposes of the continuing discussion, inner and outer conductive layers **50** and **60** respectively, are provided on a semiconductor wafer. Such are separated by an insulating material in the form of dielectric layers **54** and **58**, and the insulative nature of semiconductor material **56**.

[0063] Referring to **FIGS. 7-9**, composite top gate electrode, top gate dielectric, and body layers **60**, **58**, and **56** respectively, are etched in a pattern which defines an electrically conductive top gate electrode **62**, top gate dielectric and body outline **64** which is received only partially within bottom gate electrode outer surface area **48**. Preferably and as shown, such composite etching is preferably conducted to be selective to bottom gate dielectric layer **54**. Bottom gate electrode outer surface area **48** **(FIG. 9)** includes portions **66** which extend outwardly beyond outline **64**. For purposes of the continuing discussion, such composite etching defines an opposing pair of outwardly exposed top gate electrode sidewalls **68**, **70**, and an opposing pair of body sidewalls **72** and **74**.

[0064] Referring to **FIGS. 10-12**, a layer of insulating dielectric, such as SiO_2, is provided over etched top gate electrode **62** and outwardly exposed sidewalls **68**, **70**, **72** and **74**. Such layer is anisotropically etched to define insulating sidewall spacers **76** and **78** which leaves top gate electrode **62** outer sidewalls **68** and **70** outwardly exposed. Most preferably, such anisotropic etching is conducted without any photomasking relative to spacers **76** and **78** formation, to outwardly expose approximately 800 Angstroms of sidewalls **76** and **78** elevation. Photomasking might occur elsewhere with respect to the wafer, but preferably not for the purposes of forming such sidewall spacers. Most preferably, no photomasking occurs during this etching step. As shown, such insulating layer is preferably etched to form spacers **76** and **78** which partially overlap outwardly exposed top gate

electrode sidewalls **68** and **70**, yet provide outwardly exposed portions as well. Such etching is also conducted to etch bottom gate dielectric layer **54** to outwardly expose bottom gate electrode upper surface area portions **66** which extend outwardly beyond outline **64**. Thus, bottom gate electrode surface area **66** extending outwardly beyond outline **64** is outwardly exposed. Further, inner and outer conductive layers **50** and **52** respectively are thus etched to outwardly expose a sidewall of outer conductive layer **60**, and to outwardly expose inner conductive layer **50**. Alternately considered, thin film transistor body layer **56** can be considered as a mid-conductive layer, or more accurately a conductive capable layer, which is electrically isolated from and positioned between inner and outer conductive layers **60** and **50**, respectively. Mid-conductive layer **56** thus includes sidewalls **72** and **74** which are covered by an insulating material in the form of spacers **76** and **78**. The preferred thickness of the layer from which spacers **76** and **78** are formed is about 150 to 400 Angstroms, leaving the width of spacers **76** and **78** at preferably about 100 to 350 Angstroms.

[**0065**] Referring to **FIGS. 13 and 14**, a layer **80** of electrically conductive material is provided over the outwardly exposed top gate electrode **62**, sidewalls **68** and **70**, and over insulating spacers **76** and **78**, and over outwardly exposed bottom gate electrode surface area portions **68**. Layer **80** preferably comprises in situ, conductively doped polysilicon provided to a thickness of about 1,000 Angstroms. As will be appreciated by the artisan, electrical interconnection has thus been made between top gate electrode **62** and bottom gate electrode **50** without the typical added associated photo lithography step for connecting such electrodes as is shown by **FIG. 1**.

[**0066**] Referring to **FIGS. 15-17**, layer **80** is anisotropically etched to define electrically conductive sidewall links **82** and **84** which electrically interconnect top gate electrode sidewalls **68**, **70**, and bottom gate electrode surface area portions **66**. Such anisotropic etching is again preferably conducted without any photomasking relative to the sidewall link formation, while photomasking might occur elsewhere on the wafer. Most preferably, no photomasking occurs during this etching step.

[**0067**] Referring to **FIGS. 18-20**, a layer of photoresist **86** is deposited and patterned, and top electrode layer **60** subsequently etched to provide the illustrated offset of top gate electrode **62** relative to bottom gate electrode **50**. Preferably, the etch of polysilicon **60** is terminated in an isotropic undercut etch to optionally enable a p− LDD implant into a region between p+ source/drain regions and transistor body region **56**.

[**0068**] Referring to **FIGS. 21 and 22**, the masked wafer is subjected to a p+ implant (with resist layer **86** still in place) for definition of source and drain regions **92, 88** respectively. Such also effectively defines a channel region **90** within thin film transistor body layer **56**. Channel region overlaps with the bottom gate electrode, and has an insulated sidewall (**FIG. 19**). Thus in accordance with the above described method, source/drain and channel regions are effectively defined by anisotropic etching of the layer of conductive material utilized to form sidewall interconnecting links **82** and **84**. Preferably, top gate electrode **62** underlaps bottom gate electrode **50** on the source and overlaps bottom gate electrode **50** on the drain side, as is shown. If desired, the illustrated resist overhang can be utilized for providing a blanket p− implant **89** after the p+ implant is done with resist still in place, and then the resist is stripped off (to provide a PMOS LDD structure).

[**0069**] Further aspects of the invention are described with reference to **FIGS. 23-25**. Such illustrates a semiconductor wafer fragment **94** comprised of a bulk substrate **95** and overlying insulating region **96**. Two conductive layers **97** and **98**, separated by an insulating material layer **99**, are provided atop insulating layer **96**. Such conductive and insulating materials are etched, as shown, to define an opposing pair of outwardly exposed sidewalls **100***a,* **100***b*, and **100***c*, **100***d,* for each conductive layer.

[**0070**] Referring to **FIG. 24**, a layer **101** of an electrically conductive material is deposited over etched conductive layers **97** and **98** and their respective sidewalls **100***a,* **100***b* and **100***c,* **100***d.* The preferred material for conductive layer **101** is in situ conductively doped polysilicon.

[**0071**] Referring to **FIG. 25**, layer **101** is subjected to an anisotropic etch to define a pair of electrically conductive sidewall links **103** and **105** which effectively electrically interconnect conductive layers **97** and **98**. Such anisotropic etching is most preferably conducting without photomasking relative to the sidewall link formation, while other areas of the wafer might be masked. Most preferably, no photomasking occurs during this etching step.

[**0072**] In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is co be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

1-41. (canceled)

42. A semiconductor construction comprising:

a first conductive layer over a substrate;

a second conductive layer over the first conductive layer;

a third conductive layer over the second conductive layer; and

a fourth conductive layer in electrical communication with the first and third conductive materials and electrically insulated from the second conductive layer.

43. The semiconductor construction of claim 42 wherein the fourth conductive layer is a conductive sidewall spacer.

44. The semiconductor construction of claim 42 wherein the first, second, third and fourth conductive layers are comprised by a transistor device.

45. The semiconductor construction of claim 42 wherein the third conductive layer overlaps the first conductive layer on a first side and underlaps the first conductive layer on a second side.

46. The semiconductor construction of claim 42 wherein the fourth conductive layer comprises conductively doped polysilicon.

47. The semiconductor construction of claim 42 wherein the second conductive layer is separated from the fourth conductive layer by an insulative sidewall spacer having a thickness of from about 100 Angstroms to 350 Angstroms. conductive layer is separated from the fourth conductive layer by an insulative sidewall spacer having a thickness of from about **100** Angstroms to **350** Angstroms. S:WI**2228**O**5**MOi .doc **5**

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