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[54] CONTINUOUS DIGITAL RATEMETER

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[51] **Int. Cl.** **G01r 23/02**

[58] **Field of Search** ..... 235/150.31, 150.3; 328/165, 328/108, 109, 120; 324/78 D

[56] **References Cited**

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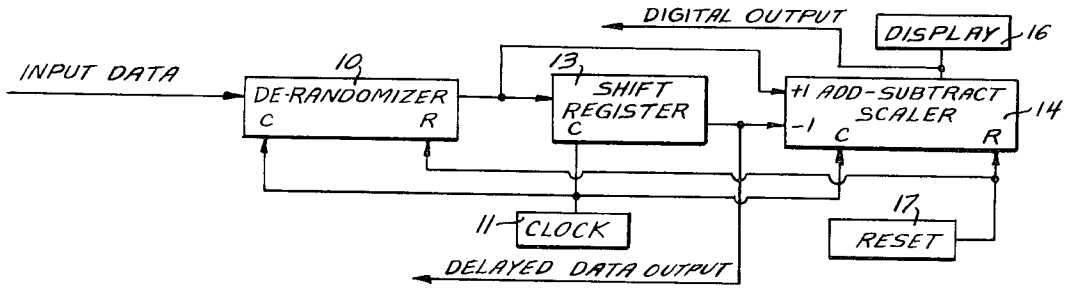
[57] **ABSTRACT**

A continuous ratemeter having a digital output is described. The ratemeter has relatively long integration periods while producing a substantially continuous output. The ratemeter develops a delayed replica of the input pulse train and can indicate differential as well as integral count rates.

6 Claims, 3 Drawing Figures



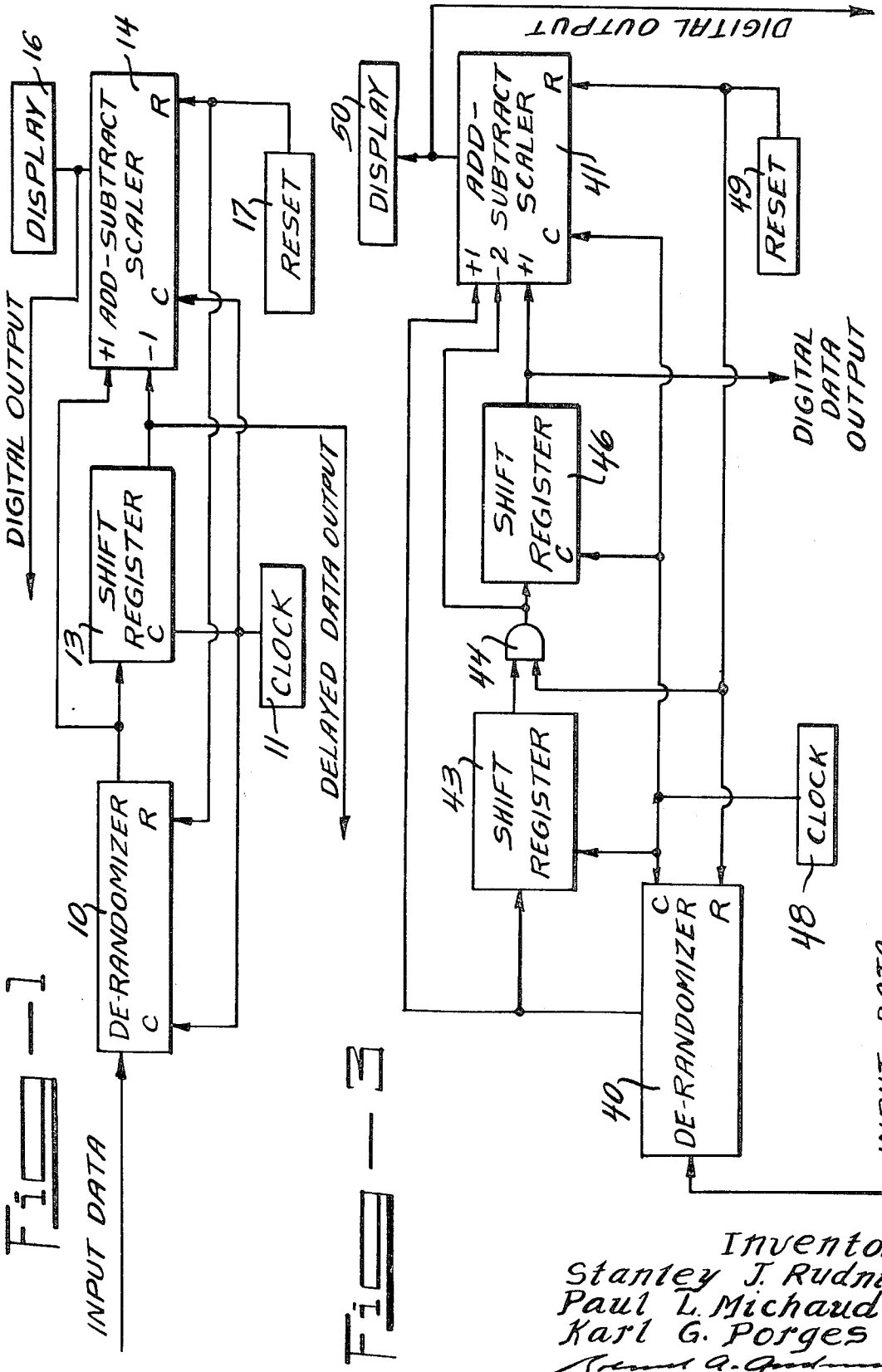


Fig. 1

Fig. 2

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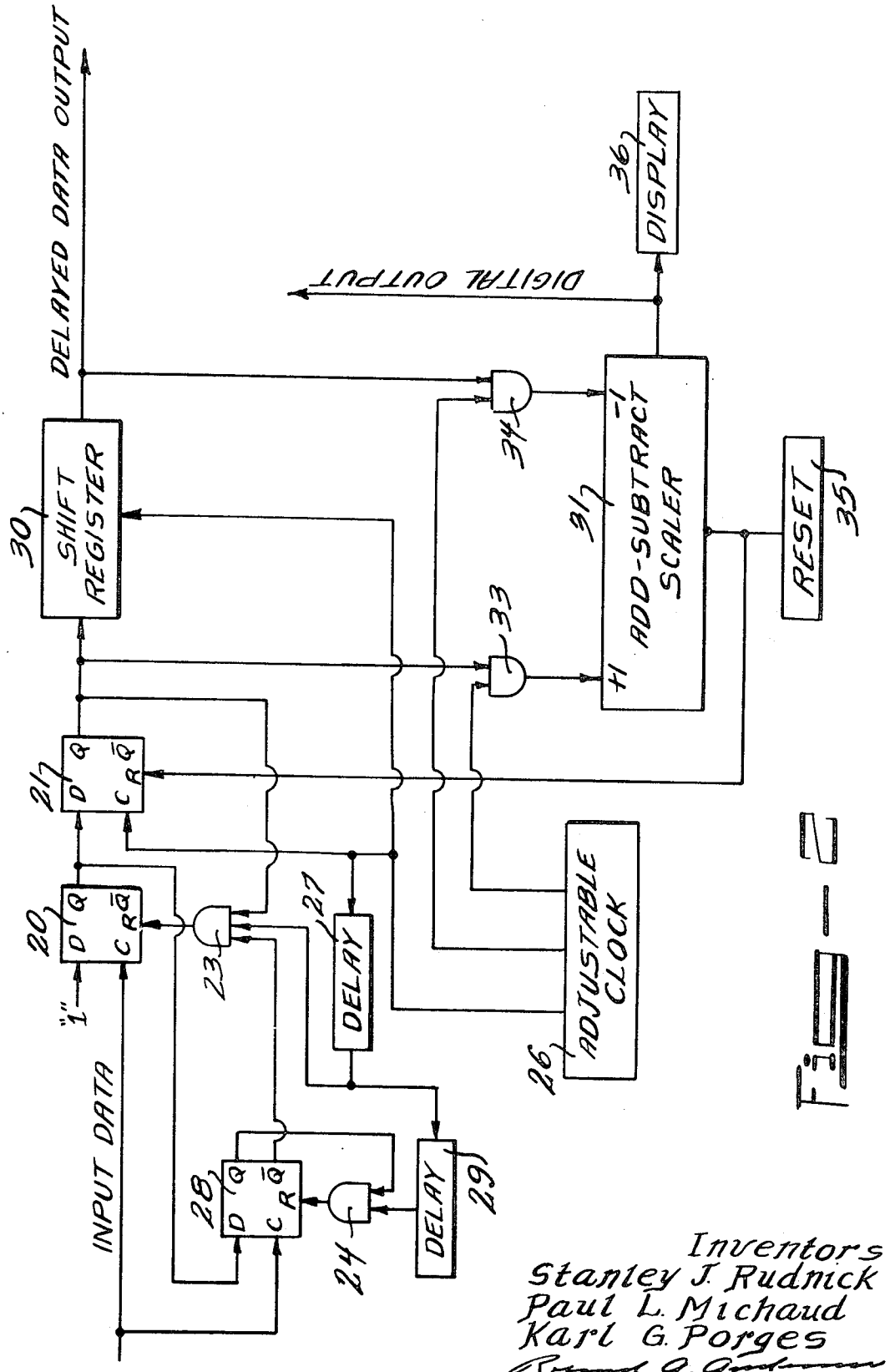

FIG. 2

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CONTINUOUS DIGITAL RATEMETER

CONTRACTUAL ORIGIN OF THE INVENTION

The invention described herein was made in the course of, or under, a contract with the UNITED STATES ATOMIC ENERGY COMMISSION.

BACKGROUND OF THE INVENTION

Ratemeters are widely used in reactor instrumentation, alarm systems and other nuclear applications. While a large number of stable analog ratemeter designs are available, the input to a ratemeter is digital and an output which is also digital is often required, for example, when the ratemeter is used in conjunction with an alarm level discriminator. Furthermore, digital computers are increasingly employed to monitor, diagnose and correct power levels of reactors and feed rates of processing plants. With existing analog ratemeters it is necessary to develop an analog function from the digital output of a count channel and then develop a digital signal from the analog output for alarm system or computer input.

A number of digital ratemeters of the cyclic count and dump type have been described and are commercially available. These cyclic count and dump circuits produce outputs only at the end of each count interval and respond to step inputs in a manner determined not only by the choice of counting periods but also by the particular phase of the count cycle at the instant the step occurs.

It is therefore an object of this invention to provide a continuous digital ratemeter having relatively simple logic.

Another object of this invention is to provide a continuous digital ratemeter which produces a delayed replica of the input pulse train.

Another object of this invention is to provide a continuous digital ratemeter which is capable of differential counting.

Another object of this invention is to provide a continuous digital ratemeter having an output which is always present and in which the response to a step change in input begins immediately.

SUMMARY OF THE INVENTION

In practicing this invention, a continuous digital ratemeter is provided for receiving random input pulses and for developing an output representative of the input pulse rate. The ratemeter includes a clock for developing a clock signal having a frequency f. A derandomizer receives the random input pulses and acts to develop only a single pulse output during a period $1/f$ in response to at least one random input pulse being received during the period $1/f$. A shift register is coupled to the clock means and has an input coupled to the derandomizer for receiving the pulse outputs therefrom. An add-subtract scaler has an add input mode coupled to the derandomizer and a subtract input mode coupled to the shift register. Each input pulse from the derandomizer adds one to the count in the add-subtract scaler. Each pulse output from the shift register subtracts one from the add-subtract scaler. Thus the number of counts in the scaler is always exactly equal to the number of pulses in the shift register.

The derandomizer may be used to reduce errors which occur when more than one data input pulse is received during a period $1/f$. The ratemeter may also be constructed to provide a differential count rate to detect sudden changes in the count rate while excluding longtime changes. The information stored in the shaft register is a delayed replica of the input pulse train. This information may be read out to show how a particular count in the add-subtract scaler was produced.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is illustrated in the drawings, of which:

FIG. 1 is a block diagram of the continuous digital ratemeter of this invention.

FIG. 2 is a block diagram of the continuous digital ratemeter of FIG. 1, showing a derandomizer which reduces errors caused by multiple input pulses during the count period.

FIG. 3 is a block diagram of a continuous digital ratemeter which develops a differential count.

DETAILED DESCRIPTION OF THE INVENTION

Referring to FIG. 1, there is shown a block diagram of the continuous digital ratemeter of this invention. The input data is applied to the input of the derandomizer **10**. Clock **11** is coupled to derandomizer **10** to control the operation of the derandomizer. The clock signals from clock **11** have a frequency f with a period $1/f$. Derandomizer **10** acts to produce no more than one output pulse during the period $1/f$, provided at least one input pulse is received during this period. This prevents additional input pulses during the period $1/f$ from being counted improperly to develop count errors. Since the input pulses are random, it is possible for two or more pulses to occur during the period $1/f$. Since the second pulse would not be counted, an error would result. The circuit in FIG. 2 acts to reduce this error and its operation will be explained in a subsequent portion of this specification.

The output pulses from derandomizer **10** are coupled to shift register **13** and the add-subtract scaler **14** in the add mode. Thus, every pulse developed by derandomizer **10** acts to add one to the count in add-subtract scaler **14**. Clock **11** steps the pulses through shift register **13** and the output pulses from shift register **13** are coupled to add-subtract scaler **14** in the subtract mode. As a result, the number of counts in the add-subtract scaler **14** is always exactly equal to the number of pulses in the shift register. This number equals the number of input pulses in the preceding time interval m/f and has an average value mn/f, where m = the number of bits in the shift register, f = the clock frequency and n = the mean input rate.

In an example of a digital ratemeter of this type, the shift register **13** had a capacity of 20,000 bits and the clock frequency was 1 MHz. The count in add-subtract scaler **14** can be displayed by display unit **16** or coupled to other devices such as a computer as desired. Since the count in add-subtract scaler **14** is exactly the same as the count in shift register **13**, the input data which produces a particular count in the add-subtract scaler **14** can be read out and analyzed as desired. This is particularly important in a nuclear safety device wherein a count of a predetermined magnitude within the add-subtract scaler **14** would cause the reactor to shut down or make other changes. The input data which cause this action may then be examined without the necessity for providing permanent storage of all input data received. A reset circuit **17** provides resetting pulses to initialize add-subtract scaler **14** and shift register **13**.

Referring to FIG. 2, there is shown a derandomizer circuit which reduces the error caused when more than one pulse is received during the period $1/f$. Input data pulses are received by primary buffer (D-type bistable multivibrator) **20** which produces an output upon receipt of the first pulse in the period $1/f$. With the primary buffer set in the Q state, a Q output is developed from synchronizer **21** at the proper time in the clock cycle. The Q output from synchronizer **21** is coupled to AND-gate **23** to provide an enabling signal for the AND-gate. The Q output of primary buffer **20** enables auxiliary buffer **28**. If no further pulses are received during the period $1/f$, a clock pulse from adjustable clock **26**, delayed for a time equal to or greater than the propagation delay through synchronizer **21** by delay **27**, acts to develop an output signal from AND-gate **23**, resetting primary buffer **20**.

If, however, a second pulse is received during the period $1/f$, the pulse sets enabled auxiliary buffer **28**. With auxiliary buffer **28** in the set state, the $\overline{Q}$ output, which is coupled to AND-gate **23**, is removed, blocking the AND gate. If a third pulse is received during the period $1/f$, this pulse is discarded and is lost, producing an error. The probability that three or more pulses will be received during the period $1/f$ is very much

less than the probability that one or two pulses will be received. Thus, the circuit decreases the error caused by discarding pulses. If required, additional auxiliary buffers of the same design could be used to further reduce the error.

When AND-gate **23** is disabled by the output from auxiliary buffer **28**, the clock pulse from adjustable clock **26** will not reset primary buffer **20**. Auxiliary buffer **28** is reset by the clock pulse delayed by both delay **27** and delay **29**, whose delay must be equal to or greater than the duration of the pulse from delay **27**. Thus, during the following period $1/f$, primary buffer **20** is in the set state, as if it had received a pulse during that period. If a pulse is received during that period, it is registered in auxiliary buffer **28**, as previously described. If, however, a second pulse is received during the subsequent period, it is discarded. The probability that two consecutive periods will each have two or more pulses is very low. Therefore, the use of the single auxiliary buffer stage acts to decrease significantly the errors caused by discarding pulses. Additional auxiliary buffer stages can be added to further reduce the errors, if this is required.

The output of synchronizer **21** is coupled to shift register **30** and the add input of add-subtract scaler **31** through AND-gate **33**. The output of shift register **30** is coupled to the subtract input of add-subtract scaler **31** through AND-gate **34**. AND-gates **33** and **34** are enabled at the desired time by signals from adjustable clock **26**. Reset **35** and display **36** are as previously described in FIG. **1**. The operation of shift register **30** and add-subtract scaler **31** is the same as previously described. The clock rate of clock **26** can be adjusted as desired to change the period $1/f$, and consequently the overall delay and time constant.

Referring to FIG. **3**, there is shown a continuous digital ratemeter having a circuit which provides a differential count rate. In some nuclear applications the count rate itself is not significant, since the count rate gradually increases over a long period of time. An example might be found in the radioactivity of the primary sodium coolant which will increase as the reactor is operated. However, if a fuel rupture occurs, the radioactivity will increase suddenly and it is important to detect this sudden increase rather than the absolute magnitude of the input data rate. In FIG. **3**, the data is applied to derandomizer **40** which acts in the manner previously described. The output of the derandomizer is coupled to the add-subtract scaler **41** to add one to the scaler. The output of derandomizer **40** is also coupled to shift register **43**. The output of shift register **43** is coupled through AND-gate **44** to shift register **46** and add-subtract scaler **41**. The output from shift register **43** acts to subtract two from the count in the add-subtract scaler **41**. The output of shift register **46** is coupled to add-subtract scaler **51** and acts to add one to the count therein. Thus, the count in add-subtract scaler **41** is equal to the difference between the counts in shift register **43** and shift register **46** (count in shift register **43** minus the count in shift register **46**). The count in shift register **46** represents the data bits received during the time period T_1 equal to m/f, where m is the number of stages in the shift register and f is the clock frequency of clock **48**. The count in shift register **43** represents the number of input data bits received in the period T_2 (equal to m/f) which follows T_1. Thus the difference between the counts of shift registers **43** and **46** represents the change in the input data rate in consecutive timer periods and is independent of long-term changes. Reset **49** and display **50** are as previously described.

The embodiments of the invention in which exclusive property or privilege is claimed are defined as follows:

1. A continuous digital ratemeter for receiving random input pulses and for developing an output representative of the pulse rate thereof, including in combination, clock means for developing a clock signal having a frequency f, input means for receiving the random input pulses and coupled to said clock means, said input means acting to develop only a single pulse output during a period $1/f$ in response to at least one random input pulse being received during said period $1/f$, shift register means coupled to said clock means and further having an input coupled to said input means for receiving said pulse outputs therefrom and an output, an add-subtract scaler having an add input mode and a substrate input mode, one of said add and subtract input modes being coupled to said input means, the other of said add and subtract input modes being coupled to said shift register means output, the total count in said add-subtract scaler being a measure of the pulse rate of the random input pulses.

2. The continuous digital ratemeter of claim **1** wherein, said add input mode is coupled to said input means and said subtract input mode is coupled to said shift register means output.

3. The continuous digital ratemeter of claim **2** wherein, said clock frequency f is adjustable.

4. The continuous digital ratemeter of claim **3** wherein, said input means includes first buffer means and second buffer means each adapted to receive the random input pulses, said first buffer means having an output coupled to said second buffer means, said first buffer means being responsive to the first random input pulse during said period $1/f$ to develop said single pulse output, said single pulse output acting to enable said second buffer means whereby a second random input pulse during said period $1/f$ is entered into said second buffer means, said second buffer means being responsive to the second random input pulse to develop a disabling signal, control means coupled to said clock means a said second buffer means and said first buffer means, said control means being responsive to said disabling signal to prevent resetting of said first buffer means at the end of said period $1/f$, whereby the second random input pulse is counted during the time period subsequent to said $1/f$ time period.

5. The continuous digital ratemeter of claim **3** wherein, said shift register means includes a first shift register coupled to said clock means and having an input coupled to said input means for receiving said pulse outputs therefrom and an output, a second shift register coupled to said clock means and having an input coupled to said output of said first shift register and an output, said add-subtract scaler having an add 1 input mode coupled to said input means, an add 1 input mode coupled to said output of said second shift register and a subtract 2 input mode coupled to said output of said first shift register, whereby the count in said add-subtract scaler is equal to the count in said first shift register minus the count in said second shift register.

6. The continuous digital ratemeter of claim **2** wherein, said add input mode of said add-subtract scaler adds 1 to the count therein and said subtract input mode of said add-subtract scaler subtracts 1 from the count therein.

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