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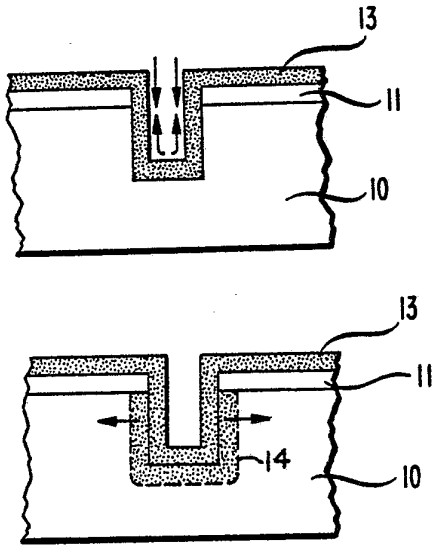
(54) Title: METHOD FOR CONTROLLED DOPING TRENCH SIDEWALLS IN A SEMICONDUCTOR BODY



(57) Abstract

For trench isolation technology or trench capacitor type memory cells it is necessary to controllably dope the steep sidewalls of the trench. A thin transfer layer (13) of polysilicon is deposited in the trench to conformally coat the sidewalls as well as the bottom of the trench and the top surface surrounding the trench. An impurity is implanted into the polysilicon at the bottom of the trench and around the top surface. Upon heating, the impurity diffuses rapidly along the polysilicon layer upwardly and downwardly along the sidewalls. It then diffuses into the sidewalls.

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METHOD FOR CONTROLLED DOPING TRENCH SIDEWALLS IN A SEMICONDUCTOR BODY

Background of the Invention

This invention relates to a process for improving the controllability of the doping of various portions of semiconductor devices. Semiconductor integrated circuit devices are built essentially in two dimensions, i.e., on the surface of a substrate. As the size of these devices continues to shrink, fundamental limitations on further size reductions are approached. An apt example is the capacitor in semiconductor memory devices. It has been reduced in size to the point where the charge capacity barely exceeds charge levels produced by noise mechanisms, e.g., alpha particle noise. It is inevitable that future devices will be constructed in three dimensions, opening a new horizon for microcircuit technology. One such approach has already been proposed and, in principle, built. See U. S. Patent No. 4,353,086. See also IEEE Electron Device Letters, Vol. EDL-4, No. 11, November, 1983, Morie et al. The essence of the approach is to build the memory cell capacitor vertically into the substrate. This so-called trench or wall capacitor has a predominant portion of the storage plate extending into rather than along the chip surface. The amount of surface area consumed is only the area of the trench at the surface.

One feature of such structures is a vertical sidewall that is doped selectively in a controlled shallow region. Doping such a sidewall by chemical diffusion from an impurity rich vapor is straightforward but does not afford the degree of control over the impurity level and distribution (including depth) that is required for many current devices. Doping a vertically extending sidewall by ion implantation, a process that normally does afford the desired shallow depth and controlled concentration, is difficult because the ion implanting beam is highly directional and does not effectively impact the sidewall.

Statement of the Invention

According to this invention a transfer layer is deposited over the entire trench, i.e., the top (the surface of the substrate immediately surrounding the trench), the bottom, and the sidewalls of the trench. The desired ions are then implanted into the transfer layer at the top or bottom (or both) of the trench. These regions extend horizontally and are easily implanted. The portion of the transfer layer covering the sidewalls will be largely devoid, at this point, of impurities. The structure is then heated to diffuse the impurities downwardly from the top and/or upwardly from the bottom of the trench into the sidewall portion of the transfer layer. Further heating causes the impurities in the sidewall portion of the transfer layer to diffuse into the sidewall of the trench itself creating the desired impurity region. The transfer layer comprises a material in which the diffusion rate of impurities is high (e.g. 5X) relative to the rate in single crystal silicon. The preferred material is polysilicon or amorphous silicon in which these rates differ by more than an order of magnitude. Another recommended material is refractory metal silicide, e.g. $TaSi_2$ or WSi_2.

Brief Description of the Drawings

FIGS. 1-6 are schematic representations of steps in a process for doping sidewalls in accordance with the invention;

FIG. 7 shows a further step in a different embodiment of the invention, and

FIGS. 8 and 9 illustrate a further variation of the invention.

Detailed Description

FIG. 1 illustrates a semiconductor substrate 10 having a trench 12 formed therein by any of a variety of known techniques. Most typically the substrate 10 is silicon and, for example, is p-type. A layer 11, of e.g., SiO_2, covers the substrate surface. The trench can be formed by applying a masking layer 11, opening a window in

layer 11 by reactive ion etching (RIE) and RIE etching the substrate anisotropically to form trench 12. Anisotropic dry etching processes, using for example RIE, are known in the art and are capable of forming trenches with nearly vertical sidewalls and aspect ratios, depth to width, greater than one. See, e.g., U. S. Patent No. 4,104,086. For the purposes of this invention "vertical" is intended to mean 90° to the surface ±20°, and suitable aspect ratios are of the order of one or more. (Generally, trenches with smaller aspect ratios can be sidewall doped using known processes.)

Subsequent to formation of the trench, a transfer layer 13, preferably polysilicon or amorphous silicon, is deposited covering the entire trench, FIG. 2. This layer is advantageously formed by CVD to insure coverage of the sidewalls of the trench. Thickness of layer 13 is not crictical but typically is at least 500Å to ensure wall coverage. In this embodiment layer 11 is shown interposed between the polysilicon layer 13 and the substrate surface to prevent doping of the substrate top surface. However, applications may be found where doping of the top surface is desirable in which case layer 11 is absent or removed prior to depositing the polysilicon layer.

The structure shown in FIG. 2 is then ion implanted, FIG. 3, to deposit impurities in the layer 13. Due to the directional nature of the ion beam, relatively few impurities deposit in the sidewall portions of layer 13. If the device being made is a storage capacitor for an n-channel access transistor, the substrate 10 will be p-type and a recommended implant is arsenic or phosphorus at 1E14/cm^2. The implanted structure is then heated to diffuse the implanted impurities upwardly from the bottom and/or downwardly from the top as shown schematically in FIG. 4. Impurities such as phosphorous diffuse rapidly along the sidewall at temperatures of the order of 950°C. Upon further heating substantial doping of the sidewall of the substrate occurs as shown in FIG. 5 thus forming a

desired p-n junction 14. Diffusion time of the order of 30 minutes to 2 hours is adequate to produce this result. As represented in FIGS. 4 and 5 the impurities are shown as diffusing first throughout the layer 13 and thereafter into the substrate 10. Due to the more rapid diffusion of impurities in polysilicon (layer 13) as compared with single crystal silicon (substrate 10), this is (effectively) what occurs and is the basis for the invention. In actuality, the process does not occur in successive, distinct steps, as shown, but occurs simultaneously at different rates, as will be evident to those skilled in the art.

After completion of the doping of the sidewall, doping layer 13 may, if desired, be removed. A preferred way of removing layer 13 is to oxidize it completely, by known thermal techniques. Removal of the resulting oxide layer by known selective etching is straightforward. Alternatively, the oxide layer may remain, to function as the dielectric for the capacitor. Applications may arise for retaining layer 13, e.g. in making diodes, or ohmic contacts to substrate 10. In the case of the latter, boron is suitable as the impurity.

If the structure of FIG. 6 is to be employed as a capacitor in a memory device, a dielectric layer (not shown) is grown or deposited in the trench and a conductive layer is applied thereover, e.g., as described in Patent No. 4,353,086. The dielectric is typcially SiO_2, grown by a thermal growth process and the conductive layer may be aluminum but is preferably polysilicon. The polysilicon layer may be deposited to a thickness that fills the trench to provide an essentially planar topology. The thermal diffusion process illustrated by FIG. 4 and/or 5 can be advantageously effected in conjunction with the growth of the dielectric layer for the memory cell. The dielectric layer may also be produced by oxidation of the transfer layer as indicated earlier.

The trench capacitor arrangement described in

U.S. Patent No. 4,353,086 requires isolation between facing sidewalls. An approach for manufacturing this structure is shown in FIGS. 7 and 8. Isolation at the bottom of the trench is achieved, for example, by etching the trench at 20a of FIG. 7 anisotropically to remove the implanted region at the bottom of the trench.

As described above, doping of the sidewalls results from impurities ascending the sidewall from the bottom of the trench as well as descending from the top. As shown in FIGS. 8 and 9 it can be sufficient to dope the sidewalls primarily from the top of the trench.

Another application of the technique described herein is the making of trench-isolated devices. For an n-channel trench-isolated structure, the sidewall doping is boron at a level of the order of $2 \times 10^{16}/cm^3$. Further details on trench isolation using conventional doping methods can be found in U. S. Patent Nos. 4,104,086 and 4,353,086.

The following is a process sequence suitable for forming trench isolation structures. The sequence follows approximately the steps described in conjunction with FIGS. 1 to 6 except that layer 11 in this example includes a silicon nitride layer deposited on a silicon dioxide layer.

A structure similar to that shown in FIG. 1 is formed by RIE etching a trench 1μ wide and 5μ deep. Layer 11 consists of 175Å of grown oxide covered with 1200Å of silicon nitride. The polysilicon layer 13 is 1000Å thick and is deposited by conventional CVD. The polysilicon layer is capped with 700Å of undoped oxide. The cap is optional (hence is not shown) and is recommended to obtain the desired implant profile in the transfer layer and to minimize evaporation of impurities during subsequent heat treatments.

Boron is then implanted at 40 kev and $10^{13}/cm^2$, followed by a drive-in step in nitrogen at 950°C for 60 minutes. The polysilicon transfer layer

is then oxidized through followed by an anneal at 950°C for 60 minutes.

The transfer layer, now converted to oxide, may remain in place. If desired the trench may be filled with dielectric material as described in U. S. Patent No. 4,104,086.

The doping technique set forth herein has been described in terms of doping a sidewall. However, the essential aspect of the invention is a means for doping a layer or portion of a layer that is relatively inaccessible to the implant beam. Such a layer or region might, for example, be situated underneath another layer, in which case a portion of a transfer layer that is accessible to the beam is implanted and the implanted impurities are thereafter diffused to a region of the transfer layer that is inaccessible to the ion beam. It is contemplated that the region of the transfer layer that is implanted will lie in one dimensional plane, typically normal or approximately normal to the ion implant beam, and the region to which the impurities are to be transferred may be along a vertical, or approximately vertical, plane inaccessible, or largely inaccessible to the ion beam, as in the case of the sidewalls described herein. Or the region to which the impurities are transferred may lie transversely with respect to the beam but inaccessible thereto due to intervening layers.

This transfer of impurities in a dimension transverse to the substrate surface is one important characteristic of the invention. The extent of this transfer can be substantial. Although the transfer of impurities through the thickness of certain layers is known, the thicknesses involved are quite modest, typically of the order of a fraction of a micron. One way of defining the transfer process of the invention to distinguish from the prior known process, is to prescribe a length of transfer that is substantially greater than the thickness of the transfer layer. Typically the

latter will be on the order of a fraction of a micron while the former will be on the order of several microns.

Means for introducing the impurities may be by ion implantation or by predeposit from a gas or vapor source, both cases followed typically by a thermal treatment. The site where the impurities are desired is typically inaccessible, or not conveniently accessible, to the conventional source of impurities. Other situations where the invention is useful are where the site underlies one or more physical layers, making the site inaccessible to either an ion beam or a gas or vapor impurity source.

Difficulties may arise in some applications of the so-called trench technology due to effects occurring at the bottom of the trench. For example, layers deposited or formed at the bottom of the trench may exhibit non-uniformities. Since electric field effects are likely to be non-uniform in the vicinity of the corners of the trench, the potential for dielectric breakdown and other device failures is liable to be increased due to the corners and/or bottom of the trench. Moreover, stress effects within the substrate at these corners may encourage leakage of charge stored in the vicinity of the trench bottom. Therefore, it is sometimes advantageous, depending upon the particular devices being made, to utilize a structure like that shown in FIGS. 7 and 10 in which the storage layer does not extend to, or around, the corners of the trench bottom.

Claims

1. A method for doping a semiconductor body characterized by forming a continuous transfer layer (13) on first (11) and second (10) spaced apart surfaces of a substrate containing said body, said surfaces being transversely oriented with respect to one another, and said second surface being on said body, introducing impurities into said layer at said first surface, and heating said layer and said body for causing diffusion of said impurities to said second surface through said transfer layer and into said body from said layer at said second surface.

2. The method of claim 1 including:

forming a trench (12) in a surface portion of a semiconductor substrate, the sidewall of said recession extending approximately vertically with respect to said surface of the substrate,

depositing the transfer layer in said trench to cover said sidewall and a portion of said substrate extending transversely to said sidewall, said transfer layer comprising a material in which the diffusion rate of said impurities is greater than in said substrate, and

implanting impurities into said transversely extending portion.

3. The method of claim 2 in which the diffusion rate of impurities in the transfer layer is at least five times the diffusion rate in the substrate.

4. The method of claim 2 in which the transfer layer is polysilicon or amorphous silicon.

5. The method of claim 2 in which the layer as deposited is substantially undoped.

6. The method of claim 2 including the additional steps of forming a dielectric layer covering a trench wall and depositing a conductive layer over the dielectric layer to form a capacitor.

7. The method of claim 6 in which the transfer layer is silicon and the dielectric layer is formed by

oxidizing the silicon transfer layer.

8. The method of claim 2 including oxidizing the transfer layer completely through its thickness.

9. The method of claim 8 including subsequently removing the oxidized transfer layer.

10. The method of claim 1 in which the trench is filled with a dielectric material after the diffusion heating step.

1/2

FIG. 1

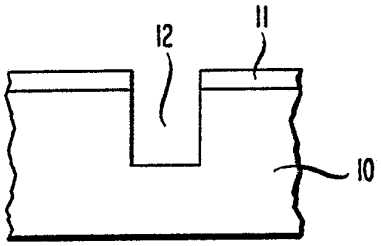


FIG. 2

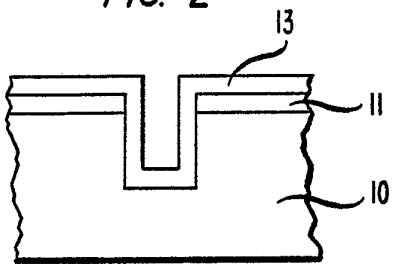


FIG. 3

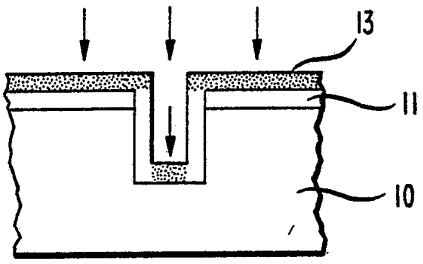


FIG. 4

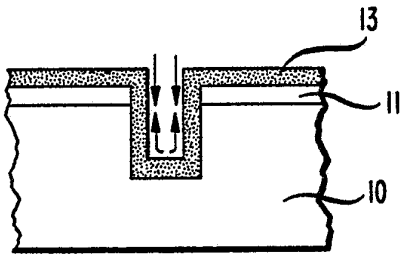


FIG. 5

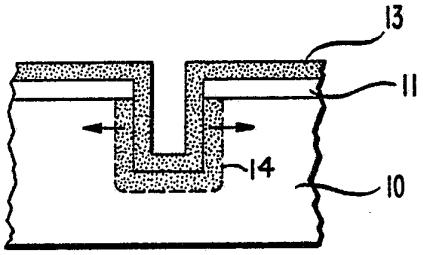


FIG. 6

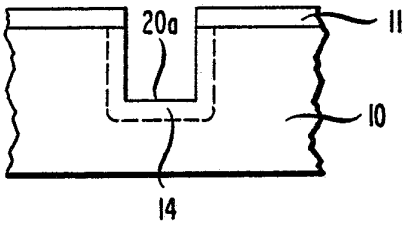


FIG. 7

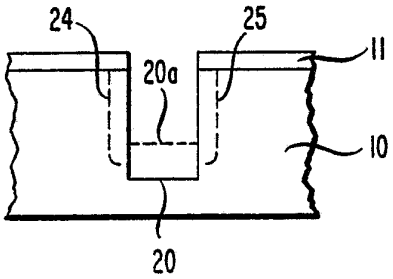


FIG.8

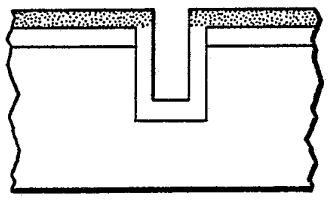
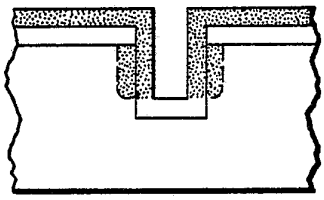


FIG.9



INTERNATIONAL SEARCH REPORT

International Application No PCT/US 85/00503

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: H 01 L 21/225; H 01 L 21/76; H 01 L 29/94

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
Y	DE, A1, 3223842 (K.K. SUWA SEIKOSHA) 13 January 1983 see figures 2a-2d; page 4, lines 14-17, 19-21; page 5, lines 4-8,10-12, 17-27	1,2
A		4,5
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Y	EP, A2, 0044400 (INTERNATIONAL BUSINESS MACHINES CORP.) 27 January 1982 see figure 14; page 7, lines 9-20	1,2
A		8
	--	
A	Nuclear Instruments and Methods in Physics Research, vol. 209/210, part 2, May 1983 (Amsterdam, NL) A.E. Michel et al.: "Ion-implanted polysilicon diffusion sources", pages 719-724, see page 719, section 2	1
	--	
A	Extended Abstracts on the 15th Conference	./.

* Special categories of cited documents: [10]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
21st June 1985	11 JUIL. 1985
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	G.L.M. Kruydenberg

Form PCT/ISA/210 (second sheet) (January 1985)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
	on Solid State Devices and Materials 30 August - 1 September 1983, Tokyo, JP; sponsored by the Japan Society of Applied Physics; T. Morie et al.: "Depletion trench capacitor cell", pages 253-256 see figure 1; page 253, section III "Process Sequence"	1,6,10
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A	FR, A1, 2489041 (GENERAL ELECTRIC COMP.) 26 February 1982 see figure 8; page 9, lines 2-4	1,2

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 85/00503 (SA 9274)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 03/07/85

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Patent document cited in search report	Publication date	Patent family member(s)		Publication date
DE-A- 3223842	13/01/83	JP-A-	58000149	05/01/83
		NL-A-	8202594	17/01/83
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		JP-A-	58000182	05/01/83
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		US-A-	4397075	09/08/83
		CA-A-	1155972	25/10/83
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		US-A-	4325182	20/04/82
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