

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
30 April 2009 (30.04.2009)

PCT

(10) International Publication Number
WO 2009/055384 A1

(51) International Patent Classification:

H01L 21/8239 (2006.01) *H01L 21/336* (2006.01)
H01L 21/8246 (2006.01) *H01L 21/311* (2006.01)
H01L 27/105 (2006.01) *H01L 21/8247* (2006.01)
H01L 27/115 (2006.01) *H01L 21/285* (2006.01)

(21) International Application Number:

PCT/US2008/080636

(22) International Filing Date: 21 October 2008 (21.10.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

11/924,823 26 October 2007 (26.10.2007) US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

[Continued on next page]

(54) Title: SELECTIVE SILICIDE FORMATION USING RESIST ETCH BACK

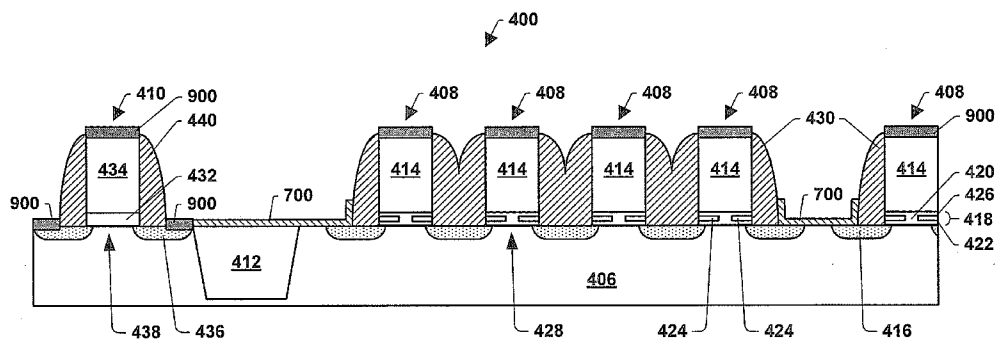


Figure 9

(57) Abstract: Methods of selectively forming metal silicides on a memory device are provided. The methods can include forming a mask layer over the memory device; forming a patterned resist over the mask layer; removing upper portions of the patterned resist; forming a patterned mask layer by removing portions of the mask layer that are not covered by the patterned resist; and forming metal silicides on the memory device by a chemical reaction of a metal layer formed on the memory device with portions of the memory device that are not covered by the patterned mask layer. By preventing silicidation of underlying silicon containing layers/components of the memory device that are covered by the patterned mask layer, the methods can selectively form the metal silicides on the desired portions of the memory device.

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— *with amended claims*

SELECTIVE SILICIDE FORMATION USING RESIST ETCH BACK

TECHNICAL FIELD

Described are methods of selectively forming silicides on memory devices.

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BACKGROUND

Modern computing devices utilize a variety of kinds of memory devices to store and access information. Memory devices include the general classes of random access memories (RAM) and read only memories (ROM). These classes further contain static RAM (SRAM), dynamic RAM (DRAM), programmable ROM (PROM), electrically programmable ROM (EPROM), electrically erasable PROM (EEPROM), as well as FLASH memory, and the like. Most memory devices employ an internal architecture in the form of an array memory of bit cells, containing plural rows and plural intersecting columns.

15 A memory cell is placed at each intersecting row and column in the array. Typically, a particular memory cell is accessed by activating its row and then reading or writing the state of its column. Memory sizes are defined by the row and column architecture. For example, a 1024 row by 1024 column memory array defines a memory device having one megabit of memory cells. The array rows are referred to as word lines and the array columns are referred to as bit lines.

20 The trend in semiconductor memory devices has been toward higher circuit density with higher numbers of bit cells per device, lower operating voltages, and higher access speeds. To achieve these high densities there have been, and continue to be, efforts toward scaling down device dimensions (*e.g.*, at sub-micron levels). However, as scaling down device dimensions, sheet resistivity of electrically conductive component of the memory devices (*e.g.*, gates, drain and source regions, emitters of bipolar transistors, local interconnect regions, and interconnect lines) may limit the speed at which memory devices can operate.

25 To reduce the sheet resistivity of memory devices, a layer of metal silicide can be formed over the surface of electrically conductive component of the memory devices. The resultant silicided components provide the lower resistivity of a metal silicide. While silicides are useful for reducing the sheet resistivity of memory devices,

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formation of silicides may interfere with the operation of analog circuits by providing undesirable junction leakage. Thus, the requirement of small features with close spacing between adjacent features requires sophisticated manufacturing techniques.

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SUMMARY

One aspect of the subject invention provides methods of selectively forming metal silicides on memory devices. The methods can include forming a mask layer over the memory device; forming a patterned resist over the mask layer; removing upper portions of the patterned resist; forming a patterned mask layer by removing portions of
10 the mask layer that are not covered by the patterned resist; and forming metal silicides on the memory device by a chemical reaction of a metal layer formed on the memory device with portions of the memory device that are not covered by the patterned mask layer. By preventing silicidation of underlying silicon containing layers/components of the memory device that are covered by the patterned mask layer, the methods can
15 selectively form the metal silicides on the desired portions of the memory device.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a top view of an exemplary memory device in accordance with an aspect of the subject invention.

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Figure 2 is a schematic illustration of a portion of a memory core such as may include at least part of one of the cores depicted in Figure 1 in a virtual ground type configuration in accordance with an aspect of the subject invention.

Figure 3 is a top view of at least a portion of a memory core, such as may include at least part of one of the cores depicted in Figure 1 in accordance with an aspect
25 of the subject invention.

Figure 4 illustrates a cross sectional view of an intermediate state of a portion of an exemplary memory device in accordance with an aspect of the subject invention.

Figure 5 illustrates forming a mask layer over a memory device in accordance with an aspect of the subject invention.

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Figure 6 illustrates forming a patterned resist over portions of a memory device in accordance with an aspect of the subject invention.

Figure 7 illustrates forming a patterned mask layer in accordance with an

aspect of the subject invention.

Figure 8 illustrates forming a metal layer over a memory device in accordance with an aspect of the subject invention.

Figure 9 illustrates forming metal silicides on portions of a memory device in accordance with an aspect of the subject invention.

Figure 10 illustrates an exemplary methodology of selectively forming metal silicides on a memory device in accordance with an aspect of the subject invention.

DETAILED DESCRIPTION

The innovation described herein provides methods for forming silicided and non-silicided layers/components on silicon containing layers/components of memory devices by utilizing a patterned mask layer. The patterned mask layer is formed on the memory device, and then a metal layer is formed over the memory device. The patterned mask layer cover portions of the memory device, and the covered portions of the memory device are protected from silicide formation. Uncovered portion of the memory device by the patterned mask layer can contact and react with the metal layer, thereby forming metal silicides.

In one embodiment, sidewall spacers adjacent lateral sidewalls of, for example, gates are also employed to prevent silicide formation. When such a sidewall spacer is employed, the mask layer can contain a material that is different from a material of the sidewall spacer. Therefore, after the silicide formation, the patterned mask layer can be removed from the memory device without substantially damaging the sidewall spacer.

The metal silicides formed on bit lines can significantly reduce the contact resistnace to the bit lines. Also, the metal silicides formed on gate electrodes can significantly reduce the resistance of the gate structure, as compared to a polysilicon gate. As a result, the overall conductivity of the gate electrodes can be increased. The innovation described herein therefore effectively addresses the concerns raised by the trend towards the miniaturization of memory devices.

The innovation is now described with reference to the drawings, wherein like reference numerals are used to refer to like elements throughout. In the following description, for purposes of explanation, numerous specific details are set forth in order

to provide a thorough understanding of the innovation. It may be evident, however, that the innovation can be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form in order to facilitate describing the innovation.

5 Although the selective silicide formation can be applied to any type of memory device, the innovation is hereinafter illustrated and described in the context of an exemplary semiconductor device having one or more memory arrays containing dual bit memory cells arranged in a virtual ground type array architecture. Figure 1 illustrates a top view of an exemplary dual bit flash memory device 100. The memory
10 device 100 generally includes a silicon substrate 102 in which one or more high-density core regions 104 and one or more lower-density peripheral regions are formed. The high-density core regions 104 typically include one or more M by N arrays of individually addressable, substantially identical dual bit memory cells. The lower-density peripheral regions on the other hand typically include input/output (I/O)
15 circuitry 106 and programming circuitry for selectively addressing the individual memory cells. The programming circuitry is represented in part by and includes one or more x-decoders 108 and one or more y-decoders 110 that cooperate with the I/O circuitry 106 for selectively connecting a source, gate, and/or drain of selected addressed memory cells to predetermined voltages or impedances to effect designated
20 operations on the respective memory cells (*e.g.*, programming, reading, and erasing, and deriving necessary voltages to effect such operations).

Figure 2 is a schematic illustration of a portion 200 of an exemplary memory core such as may include at least part of one of the M by N array cores 104 depicted in Figure 1. The circuit schematic shows a line of memory cells, which includes memory
25 cells 201 through 204 in a virtual ground type implementation, for example. The respective memory cells 201 through 204 are connected to a word line 206, which serves as a control gate, and pairs of the memory cells share a common bit line. For instance, in the example shown, the memory cell 201 associates bit lines 208 and 209; the memory cell 202 associates bit lines 209 and 210; the memory cell 203 associates
30 bit lines 210 and 211; and the memory cell 204 associates bit lines 211 and 212. As such, cells 201 and 202 share bit line 209, cells 202 and 203 share bit line 210 and cells 203 and 204 share bit line 211, respectively.

Depending upon a signal on the word line and the connection of the bit lines in a memory cell to an electrical source or drain, the memory cells 201 through 204 are capable of writing, reading, and erasing bits at locations 215 through 222. For example, control of the bit at location 215 is achieved through connection of the drain to the bit line 208 and the source to the bit line 209. Similarly, control of the bit at location 216 is achieved through connection of the drain to the bit line 209 and the source to the bit line 208. It will be appreciated that although adjacent memory cells share common bit lines, the adjacent memory cells do not interfere with each other because the memory cells are typically programmed one at a time and in such instances only one memory cell is active at a time while programming.

Figure 3 illustrates a top view of at least a portion 300 of a memory core, such as may include at least part of one of the M by N array cores 104 depicted in Figure 1. The memory core 300 is formed upon a silicon substrate 302 and has a plurality of implanted bit lines 304 extending substantially parallel to one another, and further includes a plurality of formed word lines 306 extending substantially in parallel to one another and at substantially right angles to the plurality of implanted bit lines 304. The word lines 306 are disposed over and separated from the bit lines 304 by a dielectric stack (not shown) in a grid arrangement. The memory core 300 can include a bit line contact region (not shown) between word lines 306. The bit line contact region can be used to establish electrical connection to the bit lines through the dielectric stack. It will be appreciated that the word lines 304 and bit lines 306 have contacts and interconnections (not shown) to programming circuitry such as may be represented, at least in part, by x-decoders and y-decoders.

Referring to Figures 4 to 9, one of many possible exemplary embodiments of forming a memory device is specifically illustrated. Figure 4 illustrates a cross sectional view of an intermediate state of a portion of an exemplary memory device 400. The details of the structure and manufacture of the memory device 400 are not critical to the practice of the methods. The details of the structure and manufacture of the memory device 400 can be found in, for example, commonly-assigned U.S. Pat. No. 7,060,564, issued June 13, 2006, which is hereby incorporated by reference.

The memory device 400 can contain two regions, a core region 402 and a periphery region 404 on a silicon substrate 406. The core region 402 typically contains

memory cells 408. The periphery region 404 typically contains the rest of the chip, for example, transistors 410 such as the controlling logic circuitry (*e.g.*, NMOS and/or PMOS transistors) and the input/output devices. In one embodiment, the core region 402 can include a plurality of double-bit, charge storage dielectric electrically erasable and programmable memory cells 408. The core region 402 can be separated from the peripheral region 404 by, for example, a trench isolation (*e.g.*, shallow trench isolation (STI)) 412. The trench isolation 412 can contain any suitable dielectric material such as oxides (*e.g.*, silicon oxides, high temperature oxides (HTO), and tetraethylorthosilicate (TEOS)).

It is to be appreciated that, while only five double-bit memory cells 408 and a single periphery transistor 410 are shown in Figure 4, a memory device 400 can include a plurality of double-bit memory cells and a plurality of periphery transistors organized in an array of rows and columns. In one embodiment, gate electrodes 414 of each memory cell 408 in a row are coupled together to form a respective word line for that row. In addition, sources and drains for each memory cell 408 are coupled to or formed from bit lines 416 for each respective column of the array. Voltage potentials can be applied to corresponding components of each memory cell 408 using the logic circuitry in the periphery region 404.

The silicon substrate 406 contains at least silicon. The silicon substrate 406 may contain any other suitable semiconductor material on which electric devices such as memory cell transistors can be formed. Examples of semiconductor materials include gallium arsenide, indium phosphide, and the like. In one embodiment, the silicon substrate can be doped to have P-type conductivity (*e.g.*, P dopant concentration such as boron).

In the core region 402, the memory cell 408 can contain a charge storage layer 418 on the silicon substrate 406 and the gate electrode 414 on the charge storage layer 418. The silicon substrate 406 can contain a pair of buried bit lines 416 for each memory cell 408. The buried bit line 416 can be doped to have an N-type conductivity (*e.g.*, N⁺ dopant concentration such as arsenic, phosphorous, and antimony). Each of the pair of the buried bit line 416 can function for a memory cell 408 as a source and a drain, respectively, during various programming, reading, and erasing operations. The roles of the source and the drain can be reversed depending on the operation and the

"side" of the memory device 400 on which the operation is conducted. Therefore, the terms "source" and "drain" can be used interchangeably.

The memory cell 408 can contains a charge storage layer 418 containing two charge storage nodes on the silicon substrate 406. The two charge storage nodes are represented by the dashed circle A and the dashed circle B. In one embodiment, the two charge storage nodes are physically separated by a central dielectric 420 in the charge storage layer 418.

The configuration and/or constituent of the charge storage layer 418 may vary and are not critical to the subject invention. The charge storage layer 418 typically contains a first insulating layer 422 (*e.g.*, a bottom dielectric layer or a tunneling dielectric layer), a charge storage dielectric material 424, and a second insulating layer 426 (*e.g.*, a top dielectric layer). The first insulating layer 422 and/or the second insulating layer 426 can contain, for example, silicon oxide (*e.g.*, SiO_2), other standard-K material (*e.g.*, having a relative permittivity below ten), or a high-K material (*e.g.*, having a relative permittivity, in one embodiment, above about ten and, in another embodiment, above about twenty).

The charge storage layer 418 can contain any suitable charge storage dielectric material 424. Examples of charge storage dielectric materials 424 include nitrides (*e.g.*, silicon nitride, silicon oxynitride, and silicon rich nitride), oxides, silicates, a high-k dielectric, for example, having a dielectric constant higher than that of silicon dioxide (SiO_2), and the like. In one embodiment, the charge storage dielectric material 424 contains silicon nitride, silicon oxynitride, and/or silicon rich nitride. In another example, the charge storage material contains oxides or silicates containing Al, Ta, Hf, La, Zr, Ti, Nb, Cr, V, Y, Ce and/or Pr. The charge storage layer 418 can be formed on the silicon substrate 406 by any suitable technique. For example, the charge storage layer 418 can be formed by chemical vapor deposition (CVD), lithography, and etching techniques.

Specific examples of charge storage layer 418 include an oxide/nitride/oxide tri-layer, an oxide/nitride bi-layer, a nitride/oxide bi-layer, an oxide/tantalum oxide bi-layer ($\text{SiO}_2/\text{Ta}_2\text{O}_5$), an oxide/tantalum oxide/oxide tri-layer ($\text{SiO}_2/\text{Ta}_2\text{O}_5/\text{SiO}_2$), an oxide/strontium titanate bi-layer ($\text{SiO}_2/\text{SrTiO}_3$), an oxide/barium strontium titanate bi-layer ($\text{SiO}_2/\text{BaSrTiO}_3$), an oxide/strontium titanate/oxide tri-layer

($\text{SiO}_2/\text{SrTiO}_3/\text{SiO}_2$), an oxide/strontium titanate/barium strontium titanate tri-layer ($\text{SiO}_2/\text{SrTiO}_3/\text{BaSrTiO}_2$), and the like.

In one embodiment, the first and second insulating layers contain oxide dielectrics such as silicon dioxide (SiO_2) and the charge storage dielectric material contains nitride dielectrics such as silicon nitride (Si_xN_y). The oxide-nitride-oxide configuration may be referred to as an ONO layer. Especially, when the nitride layer contains silicon rich nitride, the oxide-nitride-oxide configuration may be referred to as an ORO tri-layer. The oxide-nitride-oxide tri-layer can be fabricated by forming a first silicon oxide layer, forming a silicon nitride layer on the first silicon oxide layer, and forming a second silicon oxide layer on the silicon nitride layer.

In another embodiment, the charge storage layer 418 contains five separate layers, for example, oxide-nitride-polysilicon-nitride-oxide. The oxide-nitride-polysilicon-nitride-oxide configuration may be referred to as an ORPRO layer when the nitride layer contains silicon rich nitride.

When the memory cell 408 has the two charge storage nodes, the memory cell 408 can store two physically distinct bits. In the double-bit memory cell, within the charge storage layer 418, each memory cell 408 includes a first charge storage node represented by the dashed circle A adjacent one of the buried bit lines 416 and a second charge storage node represented by the dashed circle B adjacent the other buried bit line 416. Each bit within the memory cell 408 serves as a binary unit of data (*e.g.*, either 1 or 0) that can be mapped directly to a memory array. Reading or programming one side of charge storage nodes occurs independently of whatever data is stored on the opposite side of the charge storage nodes.

Over the charge storage layer 418, the gate electrode 414 is formed. The gate electrode 414 can control a channel 428 within the silicon substrate 406 interposed between the pair of the buried bit lines 416. In one embodiment, although not shown, a word line can be formed over the gate electrode 414. In another embodiment, a word line is formed over the charge storage layer 418 and the word line functions as a gate electrode 414. The gate electrode 414 and/or the word line typically contain a semiconductor material (*e.g.*, polysilicon, polycrystalline silicon-germanium, etc.) or another suitable material, such as a metal (*e.g.*, tungsten, tantalum, aluminum, nickel, ruthenium, rhodium, palladium, platinum, titanium, molybdenum, etc.) or a metal

containing compound (*e.g.*, titanium nitride, tantalum nitride, etc.).

The memory cell 408 can contain sidewall spacers 430 adjacent lateral sidewalls of the gate electrode 414 and the charge storage layer 418 for use in controlling dopant implantation, device properties, and the like. The spacer 430 of the memory cell 408 can contain any suitable dielectric material. For example, the spacer 430 contains nitrides (*e.g.*, silicon nitrides), oxides (*e.g.*, silicon oxides), and the like.

The periphery transistor 410 can include any suitable type of transistors. For example, the periphery transistor 410 includes a plurality of MOSFETs (metal oxide semiconductor field effect transistor). The periphery transistor 410 can contain a gate dielectric 432, such as silicon oxide (*e.g.*, SiO₂) formed over the periphery region 404 of the silicon substrate 406 and a gate electrode 434 formed over the gate dielectric 432. The gate electrode 434 can contain a semiconductor material (*e.g.*, polysilicon, polycrystalline silicon-germanium, etc.) or another suitable material, such as a metal (*e.g.*, tungsten, tantalum, aluminum, nickel, ruthenium, rhodium, palladium, platinum, titanium, molybdenum, etc.) or a metal containing compound (*e.g.*, titanium nitride, tantalum nitride, etc.).

The silicon substrate 406 of the periphery region 404 can contain a pair of buried bit lines 436 and a channel 438 disposed between the bit lines 436. The bit lines 436 can be formed by implanting ion species within the silicon substrate 406. In one embodiment, the bit line contains an extension region or a lightly doped region and a deep doped region. The periphery transistor 410 can contain sidewall spacers 440 adjacent lateral sidewalls of the gate electrode 434 and the gate dielectric 432. The spacer 440 in the peripheral region 404 can contain any suitable dielectric material. For example, the spacer 440 contains nitrides (*e.g.*, silicon nitrides), oxides (*e.g.*, silicon oxides), and the like.

The spacer 430 of the memory cell 408 and/or the spacer 440 of the transistor 410 can be formed by any suitable method. For example, the spacer 430, 440 can be formed by forming a layer containing the spacer material over the memory device 400 and then removing portions of the spacer material layer not near the side surfaces of the gate 414 of the memory cell 408 and/or the gate 434 of the transistor 410. The layer containing the spacer material can be formed at least over the side surfaces of the gate 414, 434 of the memory cell 408 and /or the transistor 410.

The spacer material layer can be formed by any suitable technique. For example, the spacer material layer is formed using either spin-on or CVD techniques. CVD includes pulsed plasma enhanced chemical vapor deposition (PECVD) and pyrolytic CVD as well as continuous PECVD. PECVD uses continuous radio
5 frequency (rf) power to excite the precursor gases in order to deposit films within the glow discharge region.

Portions of the spacer material layer not near the side surfaces of the gate 414, 434 of the memory cell 408 and /or the transistor 410 can be removed by any suitable technique. For example, the portions of the spacer material layer are removed by
10 etching. In one embodiment, the portions of the spacer material layer are etched by anisotropic etching using, for example, reactive ion etching (RIE) or plasma etching. Examples of etchants include a mixture gas of chlorine, fluorine, and oxygen, a mixture gas of HBr, O₂ and He, and the like.

The memory device 400 can be optionally cleaned by contacting the memory
15 device 400 with any suitable etchant under conditions that the etchant do not substantially remove or damage the components or layers of the memory device 400. In one embodiment, when the sidewall spacers 430, 440 and/or the trench isolation 412 contain nitrides, substantially any oxide on the uppermost surface of the memory device 400 is removed by contacting the memory device 400 with suitable oxide etchants such
20 as hydrofluoric acid. In another embodiment, when the sidewall spacer 430, 440 and/or the trench isolation 412 contain oxides, substantially any nitride on the uppermost surface of the memory device 400 is removed by contacting the memory device 400 with suitable nitride etchants such as phosphoric acid.

Figure 5 illustrates forming a mask layer 500 over the memory device 400.
25 The mask layer 500 is patterned in a subsequent process, and the patterned mask layer 700 is used as a mask for selectively forming silicides. In one embodiment, the mask layer 500 contains any suitable material so that the patterned mask layer can serve as a mask for protecting the covered portions from the subsequent silicidation process. In another embodiment, the mask layer 500 can contain any suitable material so that the
30 mask layer 500 can be patterned by, for example, etching in a subsequent process without substantially damaging other components of the memory cell 408 such as the spacer 430, 440 and the silicon substrate 406. That is, the material of the mask layer

500 can be selected so that there is etch selectivity between the mask layer 500 and the other components of the memory cell 408 such as the sidewall spacer 430, 440 and the silicon substrate 406.

When the memory device 400 contains sidewall spacer 430, 440, the mask layer 500 can contain a material that is different from a material of the sidewall spacer 430, 440. The mask layer material can have a higher etch rate than the sidewall spacer 430, 440 in the subsequent etching process. For example, etching rates of oxide materials are markedly higher than etching rates of nitride materials with respect to oxide etchants. Accordingly, in one embodiment, the mask layer 500 contains oxide materials when the sidewall spacer 430, 440 contains nitride materials. Examples of oxide materials include silicon oxide (*e.g.*, SiO₂). In another embodiment, the mask layer 500 contains nitride materials when the sidewall spacer 430, 440 contains oxide materials since etching rates of nitride materials are markedly higher than etching rates of oxide materials with respect to nitride etchants. Examples of nitride materials include silicon oxynitride, silicon nitride, and the like. In yet another embodiment, diamond-like carbon and/or silicon carbide can be employed as a mask layer 500. The mask layer 500 can be formed by any suitable technique, for example, CVD. In one embodiment, the mask layer 500 is formed in the core region 402 and/or the peripheral region 404. In another embodiment, the mask layer 500 is formed over the entire upper surface of the memory device 400. In yet another embodiment, the mask layer 500 is formed over at least the core region 402 and the peripheral region of the memory device 400.

Figure 6 illustrates forming a patterned resist 600 over portions of the memory device 400. The patterned resist 600 is used as a mask for patterning the mask layer 500 in a subsequent process. The patterned resist 600 can be formed by any suitable manner. For example, the patterned resist 600 is formed by forming a resist by spin-on techniques, spray techniques, CVD, and the like, over the memory device 400; exposing the resist to a pattern of radiation; and developing the resist into the pattern. For example, a resist is deposited over the memory device 400; heat is optionally applied to the resist to remove existing solvents; and when using a positive photoresist, portions of the resist are removed by exposing the resist to radiation in a suitable wavelength range. Examples of various resists include DQN resists (containing

diazonaphthoquinone and a novolac polymer), chemically amplified resists (such containing a photoacid generator and a hydroxystyrene or t-butylacrylate polymer), polymethylmethacrylate resists, polyimide resists, polyester resists, melamine-formaldehyde polymers, polyvinylpyrrolidone, siloxane polymers,

5 poly(p-tert-butoxycarbonyloxy- $\square$ -methylstyrene),
poly(p-tert-butoxycarbonyloxystyrene), poly(tert-butyl p-vinylbenzoate),
poly(tert-butyl p-isopropenylphenyloxyacetate), poly(tert-butyl methacrylate), partially
t-butoxycarbonyloxy substituted poly-p-hydroxystyrene, partially t-butoxycarbonyloxy
substituted poly-3-hydroxyphenyl phenylsiloxane, partially t-butyl substituted

10 polymethacrylate, partially adamantyl substituted polymethacrylate and the like. All possible resist are not listed in the interest of brevity.

In one embodiment, upper portions of the patterned resist 600 are removed. By removing the upper portion of the resist, a desirable height of the resultant patterned resist 600 can be achieved and the patterned resist 600 can cover any suitable portion of

15 the mask layer 500. For example, when a large amount of the upper portion is removed and the resultant patterned resist 600 has a low height, the patterned resist 600 does not cover large areas of features (*e.g.*, the upper surface of the gate 414, 434 of the memory cell 408 and/or transistor 410). On the contrary, when a small amount of the upper portion is removed and the resultant patterned resist 600 has a high height, the patterned

20 resist 600 covers large areas of features (*e.g.*, the substantially entire portion of the memory cell 408 and/or transistor 410).

The upper portion can be removed by any suitable technique. For example, the upper portion is removed by, for example, chemical-mechanical polishing (CMP) and/or etch back techniques. In one embodiment, the upper portion of the resist is

25 removed by contacting the resist with any suitable etchant that does not substantially damage and/or remove other components of the memory device 400. Wet etching and/or dry etching containing isotropic etching and/or anisotropic etching can be employed. Examples of dry etching include reactive ion etching (RIE) using, for example, a mixture gas containing HBr (*e.g.*, HBr and O₂ mixture gas, HBr/NF₃/He and

30 O₂ mixture gas, SF₆, HBr and O₂ mixture gas). The mixture may further include Cl₂.

The patterned resist 600 can cover any suitable portion of the memory device 400. In this example, the patterned resist 600 covers the silicon substrate 406 of the

core region 402 where the memory cells 408 do not locate. In another embodiment, when the memory device 400 contains integrated circuit elements (not shown) such as doped portions of the silicon substrate 406, the patterned resist 600 covers such integrated circuit elements in a core region 402 and/or a peripheral region 404.

5 Any suitable amount of the upper portion of the patterned resist 600 can be removed. As a result, the patterned resist 600 can have any suitable height so that the patterned resist 600 can protect the covered portions of the mask layer 500 from a subsequent mask patterning process. In one embodiment, the height of the uppermost surface of the patterned resist 600 is lower than the heights of the upper surfaces of the
10 gates 414, 434, of the memory cell 408 and/or the transistor 410. In another embodiment, the height of the uppermost surface of the patterned resist 600 is substantially equal to the heights of the upper surfaces of the gates 414, 434, of the memory cell 408 and/or the transistor 410. In yet another embodiment, the height of the uppermost surface of the patterned resist 600 is higher than the heights of the upper
15 surfaces of the gates 414, 434, of the memory cell 408 and/or the transistor 410.

Figure 7 illustrates patterning the mask layer 500, thereby forming a patterned mask layer 700. The mask layer 500 can be patterned by removing portions of the mask layer 500 that are not covered by the patterned resist 600. The exposed portions of the mask layer 500 can be removed by any suitable technique, for example, etching. For
20 example, when the mask layer 500 contains oxides, the exposed portions of the mask layer 500 are removed by contacting the mask layer 500 with any suitable oxide etchant. Examples of oxide etchants include halogen acids such as hydrofluoric acid. In one embodiment, the oxide etchant is a hydrofluoric acid solution. In another embodiment, the oxide etchant is a vapor of hydrofluoric acid. When the mask layer 500 contains
25 nitrides, the exposed portions of the mask layer 500 are removed by contacting the mask layer 500 with any suitable nitride etchant. Examples of nitride etchants include phosphoric acid. The mask layer 500 is contacted with a suitable etchant under conditions that the etchant do not substantially remove or damage other components and/or layers of the memory device 400 such as the sidewall spacer 430, 440. The
30 patterned resist 600 can be removed after forming the patterned mask layer 700 by any suitable technique, for example, etching.

The patterned mask layer 700 can cover any suitable portion of the memory

device 400. In this example, the patterned mask layer 700 covers the silicon substrate 406 of the core region 402 where the memory cells 408 do not locate. In another embodiment, when the memory device 400 contains integrated circuit elements (not shown) such as doped portions of the silicon substrate 406, the patterned mask layer 700 covers such integrated circuit elements in a core region 402 and/or a peripheral region 404.

Figure 8 illustrates forming a metal layer 800 over the memory device 400. The metal layer 800 can contain any suitable metal compound that can be converted to metal silicides in a subsequent process. Examples of metals include refractory metals, such as tungsten, tantalum, molybdenum and the like; and metals of Group VIII of the Periodic Table, such as platinum, palladium, cobalt, nickel, and the like. The metal layer 800 can be converted to form, in a subsequent heat treatment, a metal silicide compound with underlying silicon in, for example, the silicon substrate 406 (*e.g.*, bit lines 416) and/or in the gate electrode 414, 434. The metal layer 800 can be formed by any suitable technique, for example, CVD, physical vapor deposition (PVD), and the like. The metal layer 800 can have any suitable thickness that depends on, for example, a desired thickness of the metal silicide formed in the subsequent process.

Figure 9 illustrates forming metal silicides 900 on portions of the memory device 400 that are not covered with the patterned mask layer 700 and removing unreacted portions of the metal layer 800. When the memory device 400 contains spacers 430, 440, metal silicides can be formed on portions of the memory device 400 that are not covered with the patterned mask layer 700 and the spacers 430, 440. The metal silicides 900 can be formed by any suitable technique. For example, the metal silicides 900 are formed by heating the metal layer 800 to cause a chemical reaction between the metal layer 800 and the underlying silicon containing layer/component of the memory device 400. In one embodiment, the metal silicides 900 are formed by chemical reactions of the metal layer 800 with the silicon of the underlying silicon substrate 406 (*e.g.*, bit lines 416) and/or with the polysilicon of the gate electrodes (*e.g.*, gate electrodes 414 of memory cells 408 and/or gate electrodes 434 of transistors 410). During the salicidation process, the metal of the metal layer 800 can diffuse into the underlying silicon containing layer/component and form the metal silicides 900. At the same time, the patterned mask layer 700 and/or the sidewall spacer 430, 440 can

prevent silicidation of portions of the memory device 400 that are covered by the patterned mask layer 700 and the sidewall spacer 430, 440. As a result, the metal silicides 900 can be selectively formed on the memory device 400. The metal silicides can have any suitable height that depends on, for example, the desired implementations and/or the memory device 400 being fabricated.

Choice of suitable conditions and parameters (*e.g.*, temperature, duration of heat treatment, and the like) of the silicidation process depends on, for example, the desirable dimensions (*e.g.*, height) of the metal silicides 900, the configuration and/or constituent of the metal layer 800 and/or the underlying silicon containing component/layer, the desired implementations and/or the memory device 400 being fabricated, and the like. For example, the metal silicides are formed by rapid thermal annealing (RTA).

Portions of the metal layer 800 over the patterned mask layer 700 remain unreacted and can be removed by, for example, etching. When the memory device 400 contains sidewall spacers 430, 440, portions of the metal layer 800 over the sidewall spacer 430, 440 also remain unreacted and can be removed by, for example, etching. The unreacted portions of the metal layer 800 can be removed by contacting the unreacted metal portions with any suitable metal etchant that does not substantially affect or damage the integrity of other layers/components of the memory device 400 such as the metal silicides 900, the memory cells 408, the transistors 410, the sidewall spacers 430, 440, and the like. Examples of metal etchants include an oxidizing etchant solution. Examples of oxidizing etchants include an acidic solution containing, for example, $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$, $\text{HNO}_3/\text{H}_2\text{O}_2$, $\text{HCl}/\text{H}_2\text{O}_2$, $\text{H}_2\text{O}_2/\text{NH}_4\text{OH}/\text{H}_2\text{O}$, H_3PO_4 , HNO_3 , CH_3COOH , and the like. Other metal etchants can also be used as long as they are capable of removing the unreacted portions of the metal layer 800 selective to other components/layers of the memory device 400.

The silicidation process and the unreacted metal removing process can be performed at any suitable number of times. For example, when using cobalt, in a first silicidation process, cobalt silicides are formed by reacting portions of a cobalt layer and the underlying silicon containing layer/component of the memory device 400. Subsequently the non-reacted cobalt is removed by a selective wet etch process. Thereafter, in a second silicidation process with a higher temperature than the

temperature of the first silicidation process, the cobalt silicides can be transformed into low-ohmic cobalt disilicides.

Although not shown in Figure 9, the patterned mask layer 700 and/or the sidewall spacer 430, 440 can be removed from the memory device 400 after the silicidation process. In one embodiment, removing the sidewall spacer 430, 440 may be advantageous to allow other structural arrangements that increase device performance. For example, removing the sidewall spacers containing silicon dioxide or silicon nitride and forming an interlayer dielectric (ILD) containing low k dielectric material can enhance device performance, by reducing, for example, overlap capacitance between the gate and source and between the gate and drain.

In one embodiment, when the memory device 400 contains sidewall spacers 430, 440, the patterned mask layer 700 and the sidewall spacer 430, 440 have the substantially same etch selectivity. For example, the patterned mask layer 700 and the sidewall spacer 430, 440 contain oxides (*e.g.*, silicon oxides) and can be removed by oxide etchants at the same time. Alternatively, the patterned mask layer 700 and the sidewall spacer 430, 440 contain nitrides (*e.g.*, silicon nitrides) and can be removed by nitride etchants at the same time. In another embodiment, the patterned mask layer 700 has an etch selectivity substantially different from an etch selectivity of the sidewall spacer 430, 440. For example, the patterned mask layer 700 contains oxides and the sidewall spacer 430, 440 contains nitrides. The oxide patterned mask layer 700 can be removed selectively by using oxide etchants without substantially damaging (*e.g.*, removing, ablating) the nitride sidewall spacer 430, 440. Alternatively, the patterned mask layer 700 contains nitrides and the sidewall spacer 430, 440 contains oxides. The nitride patterned mask layer 700 can be removed selectively by using nitride etchants without substantially damaging the oxide sidewall spacer 430, 440.

The metal silicides 900 can have a significantly lower sheet resistance than silicon and polysilicon, even if heavily doped. The metal silicides 900 formed on the polysilicon containing gate 434 is generally referred to as a polycide gate, which significantly reduces the resistance of the gate structure, as compared to a polysilicon gate. As a result, the overall conductivity of the gate electrode 414, 434 may be increased. Since many of the metals mentioned above exhibit the characteristic of reacting with silicon but substantially do not react with the mask layer such as silicon

dioxide, the process may be considered "self-aligned," especially as the non-reacted metal may be readily removed selectively to the metal silicides 900 and selectively to silicon and silicon oxide.

Figure 10 illustrates an exemplary methodology of selectively forming metal silicides on a memory device. At 1000, a mask layer is formed over the memory device. At 1002, a patterned resist is formed over the mask layer. At 1004, upper portions of the patterned resist are removed. At 1006, a patterned mask layer is formed by removing portions of the mask layer that are not covered by the patterned resist. At 1008, metal silicides are formed on the memory device by a chemical reaction of a metal layer formed over the memory device with portions of the memory device that are not covered by the patterned mask layer. Metal silicides are not formed where the metal layer is not contacted with silicon containing layers/components of the memory device due to the patterned mask layer. In one embodiment, the memory device contains spacers (*e.g.*, sidewall spacers). When the memory device contains sidewall spacers, the patterned mask layer contains a material that is different from a material of the spacer, and after forming the metal silicides, either of the patterned mask layer or the spacer can be independently removed by, for example, etching.

Although not shown in Figure 10, the methodology may include any suitable memory device fabrication processes. General examples of memory device fabrication processes include masking, patterning, etching, cleaning, planarization, thermal oxidation, implant, annealing, thermal treatment, and deposition techniques normally used for making memory devices.

The resultant memory device formed herein can be employed for central processing units (CPUs); volatile memory devices such as DRAM devices, SRAM devices, and the like; input/output devices (I/O chips); and non-volatile memory devices such as EEPROMs, EPROMs, PROMs, and the like.

The resultant memory device formed herein is useful in any electronic device. For example, the resultant memory device is useful in computers, appliances, industrial equipment, hand-held devices, telecommunications equipment, medical equipment, research and development equipment, transportation vehicles, radar/satellite devices, and the like. Hand-held devices, and particularly hand-held electronic devices, achieve improvements in portability due to the small size and lightweight of the memory

devices. Examples of hand-held devices include cell phones and other two way communication devices, personal data assistants, Palm Pilots, pagers, notebook computers, remote controls, recorders (video and audio), radios, small televisions and web viewers, cameras, and the like.

5 What has been described above includes examples of the subject invention. It is, of course, not possible to describe every conceivable combination of components or methodologies for purposes of describing the subject invention, but one of ordinary skill in the art may recognize that many further combinations and permutations of the subject invention are possible. Accordingly, the subject invention is intended to
10 embrace all such alterations, modifications and variations that fall within the spirit and scope of the appended claims. Furthermore, to the extent that the term “includes” and “involves” are used in either the detailed description or the claims, such terms are intended to be inclusive in a manner similar to the term “comprising” as “comprising” is interpreted when employed as a transitional word in a claim.

15

INDUSTRIAL APPLICABILITY

The structures and methods described herein are useful in the field of semiconductor processing including non-volatile semiconductor memory fabrication and processing.

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CLAIMS

What is claimed is:

1. A method of selectively forming metal silicides on a memory device,
5 comprising:
forming a mask layer over the memory device;
forming a patterned resist over the mask layer;
removing upper portions of the patterned resist;
forming a patterned mask layer by removing portions of the mask layer that are
10 not covered by the patterned resist; and
forming metal silicides on the memory device by a chemical reaction of a metal
layer formed on the memory device with portions of the memory device that are not
covered by the patterned mask layer.
- 15 2. The method of claim 1, wherein the metal silicides are formed on gates
and portions of a silicon substrate of the memory device that are not covered by the
patterned mask layer.
- 20 3. The method of claim 1 further comprising, prior to forming the mask
layer, removing substantially any oxide on the uppermost surface of the memory device.
4. The method of claim 1, wherein upper portions of the patterned resist are
removed by an etch back process.
- 25 5. A method of selectively forming metal silicides on a memory device,
comprising:
forming spacers adjacent side surfaces of gate electrodes on a silicon substrate
of the memory device;
forming a patterned mask layer over the memory device;
30 forming a metal layer over the memory device; and
forming metal silicides on the memory device by a chemical reaction of the
metal layer with portions of the memory device that are not covered by the spacer or the
patterned mask layer;

wherein the spacer has a substantially different etch selectivity from the patterned mask layer.

6. The method of claim 5, wherein forming the patterned mask layer over
5 the memory device comprises:

forming a mask layer over the memory device;
forming a patterned resist over the mask layer;
removing upper portions of the patterned resist; and
removing portions of the mask layer that are not covered by the patterned resist.

10 7. The method of claim 5, wherein the spacers are formed adjacent side surfaces of gate electrodes of at least one of memory cells, transistors, or combinations thereof.

15 8. The method of claim 5, wherein the metal silicides are formed on gates and portions of the silicon substrate that are not covered by the spacer or the patterned mask layer.

20 9. The method of claim 5, wherein the patterned mask layer comprises silicon dioxide and the spacer comprises nitride and the patterned mask layer comprises oxide.

25 10. The method of claim 6 further comprising
prior to forming the mask layer, removing substantially any oxide on the uppermost surface of the memory device; and
removing the patterned mask layer without substantially damaging the spacer or removing the spacer without substantially damaging the patterned mask layer.

AMENDED CLAIMS

received by the International Bureau on 03 April 2009 (03.04.2009)

What is claimed is:

1. A method of selectively forming metal silicides on a memory device (400), comprising:
 - forming a mask layer (500) over the memory device (400), the mask layer comprising a single layer of either an oxide material or a nitride material;
 - forming a resist (600) over the mask layer (500);
 - patterning the resist (600) by removing portions of the resist (600) to selectively expose at least one of: gate surfaces of a memory cell (408), gates of a transistor (410), or portions of a silicon substrate (406) of the memory device (400);
 - forming a patterned mask layer (700) by removing portions of the mask layer (500) that are not covered by the patterned resist (600), wherein the portions of the mask layer (500) are removed by wet acid etching procedures; and
 - forming metal silicides (900) on the memory device (400) by a chemical reaction of a metal layer (800) formed on the memory device (400) with portions of the memory device (400) that are not covered by the patterned mask layer (700).
2. The method of claim 1, wherein the metal silicides (900) are formed on gates (408) and portions of a silicon substrate (406) of the memory device (400) that are not covered by the patterned mask layer (500).
3. The method of claim 1 further comprising, prior to forming the mask layer (500), removing substantially any oxide on the uppermost surface of the memory device (400).
4. The method of claim 1, wherein portions of the resist (600) are removed by an etch back process.

memory device (400), comprising:

forming spacers (430) adjacent side surfaces of gate electrodes on a silicon substrate of the memory device (400);

forming a patterned mask layer (700) over the memory device (400) wherein the patterned mask layer (400) comprises a single layer of either an oxide material or a nitride material;

forming a metal layer (800) over the memory device (400); and

forming metal silicides (900) on the memory device (400) by a chemical reaction of the metal layer (800) with portions of the memory device (400) that are not covered by the spacer (430) or the patterned mask layer (700);

wherein the spacer has a substantially different etch selectivity from the patterned mask layer (700).

6. The method of claim 5, wherein forming the patterned mask layer (700) over the memory device (400) comprises:

forming a mask layer (500) over the memory device (400), wherein the mask layer (500) comprises a single layer of either an oxide material or a nitride material;

forming a resist (600) over the mask layer (500);

patterning the resist (600) by removing portions of the resist (600) to selectively expose at least one of: gate surfaces (408) of a memory cell, gates of a transistor (410), or portions of a silicon substrate of the memory device (600); and

utilizing wet acid etching procedures to remove portions of the mask layer (500) that are not covered by the patterned resist (600).

7. The method of claim 5, wherein the spacers (430) are formed adjacent side surfaces of gate electrodes (414) of at least one of memory cells (408), transistors (410), or combinations thereof.

formed on gates (408) and portions of the silicon substrate (406) that are not covered by the spacer (430) or the patterned mask layer (700).

9. The method of claim 5, wherein the patterned mask layer (700) comprises silicon dioxide and the spacer (430) comprises nitride.

10. The method of claim 6 further comprising:
prior to forming the mask layer(500), removing substantially any oxide on the uppermost surface of the memory device (400);
removing the portion of the mask layer (500) without substantially damaging the spacer (430) or removing the spacer (430) without substantially damaging the mask layer (500).

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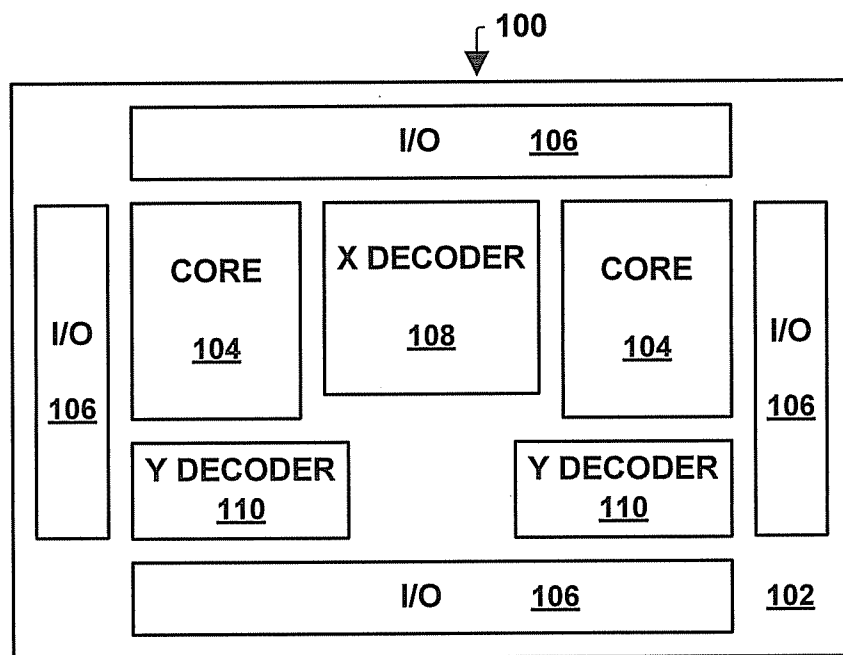


Figure 1

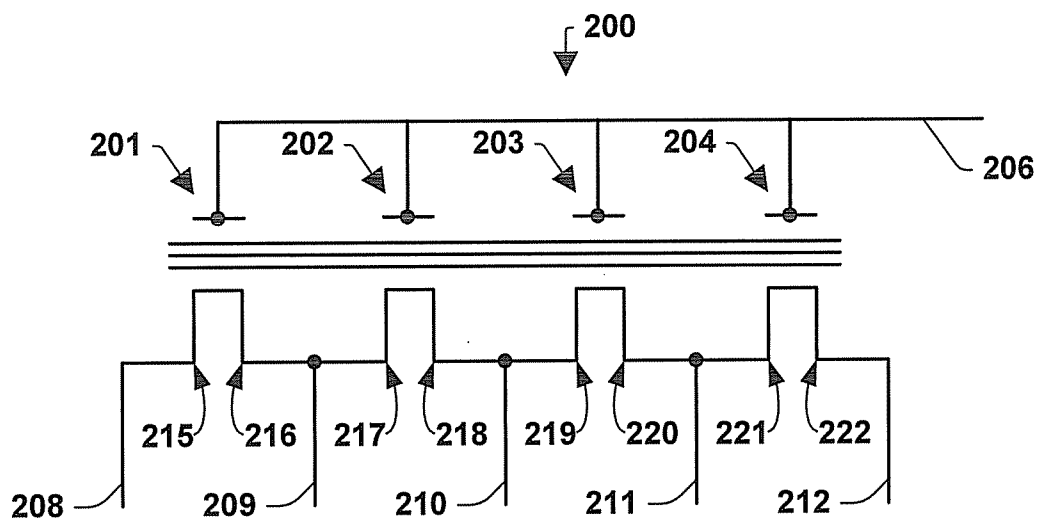


Figure 2

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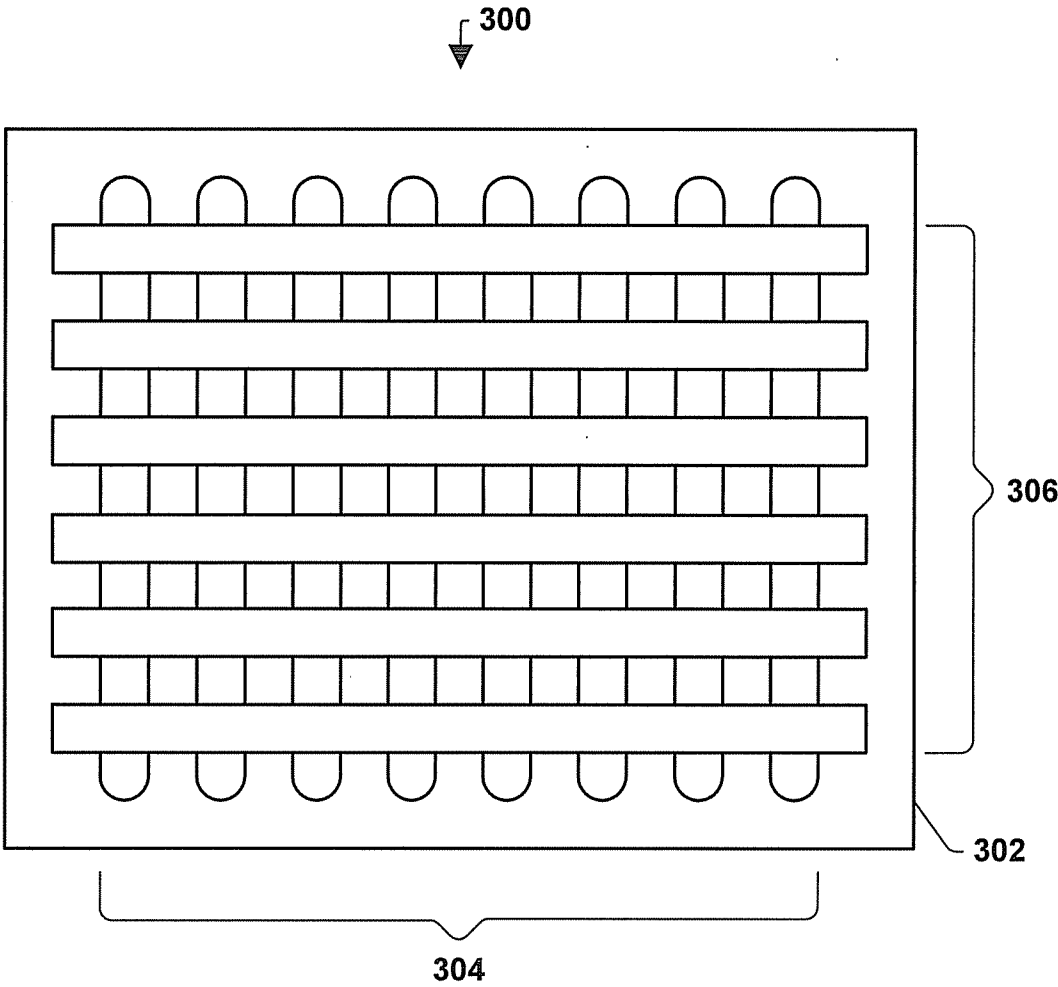


Figure 3

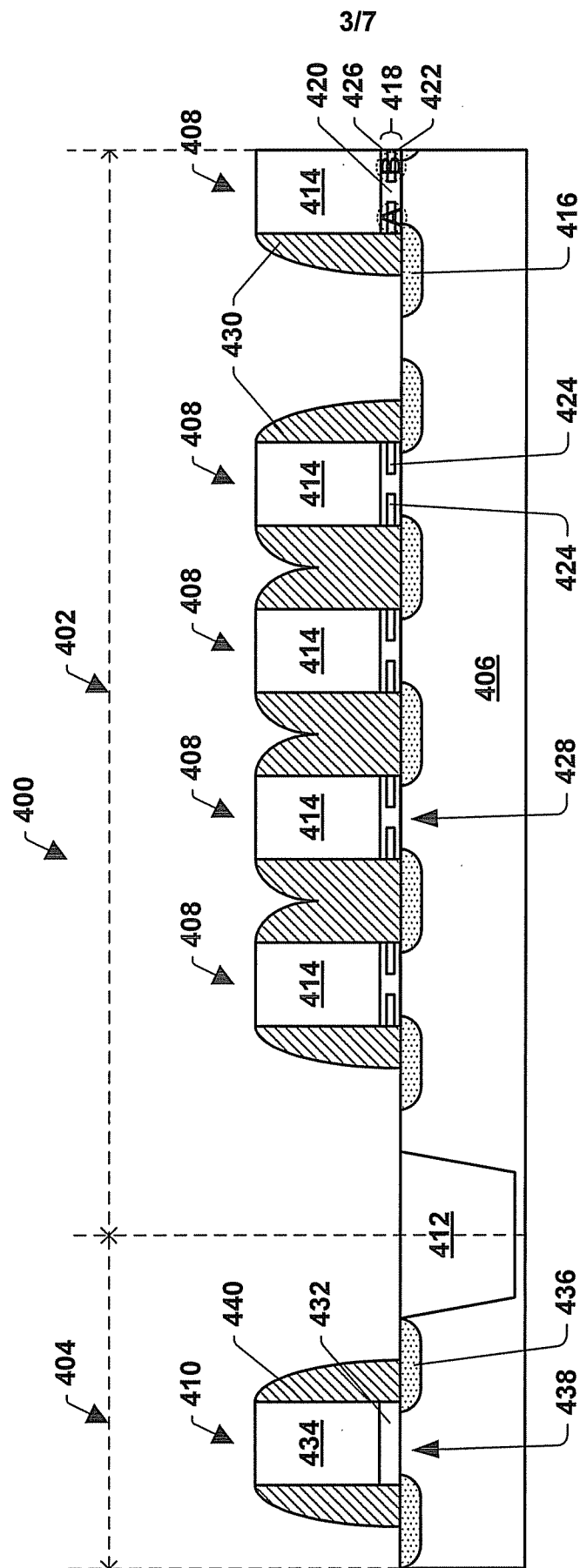


Figure 4

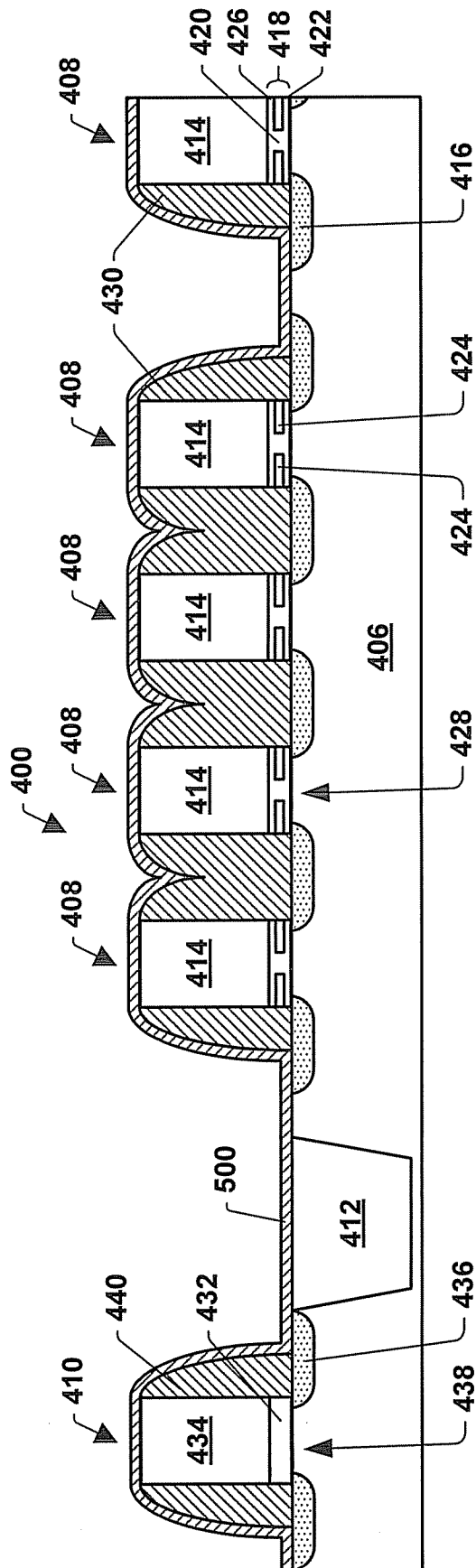


Figure 5

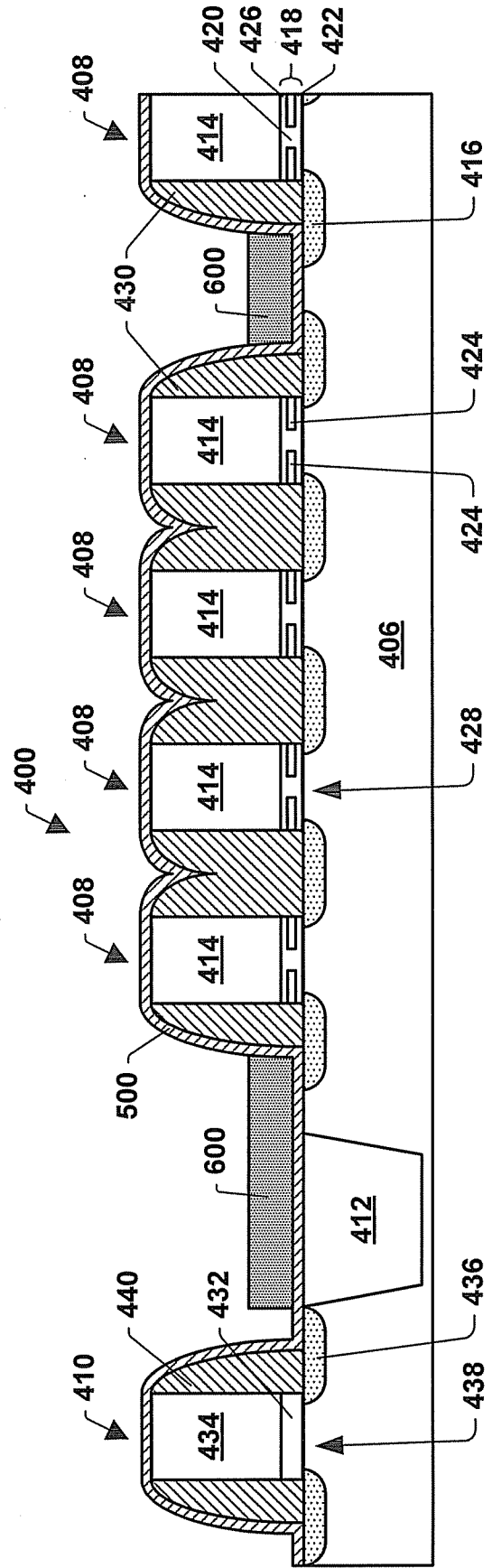
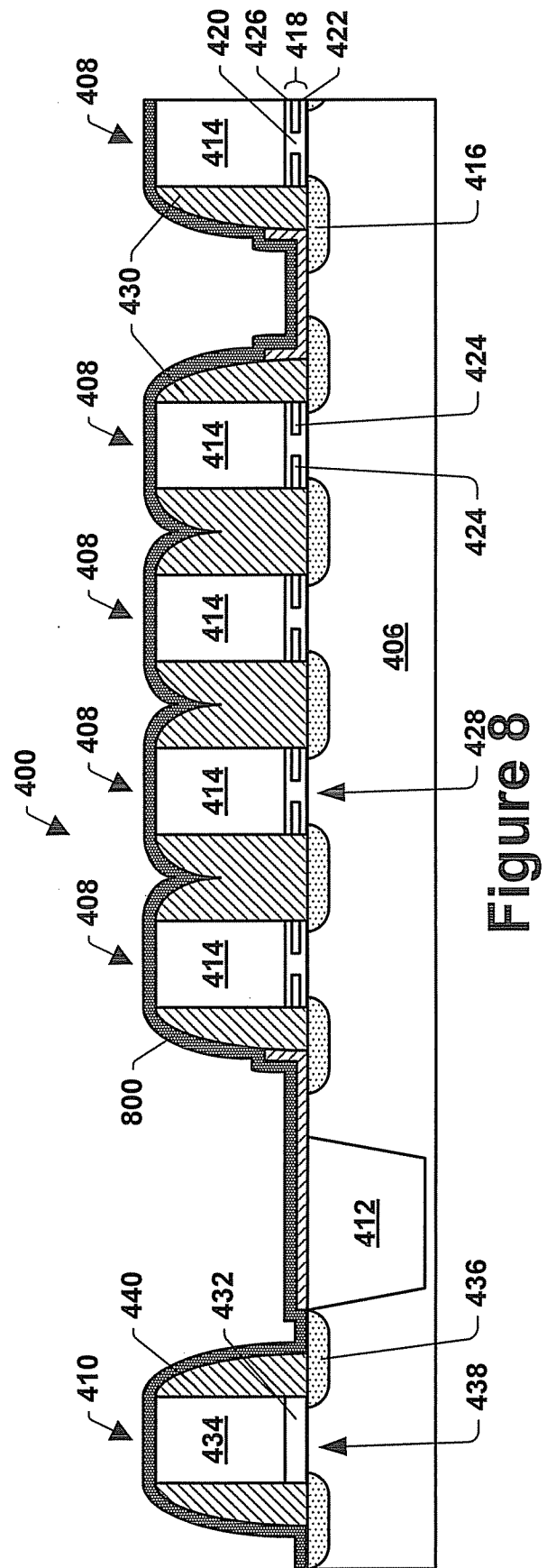
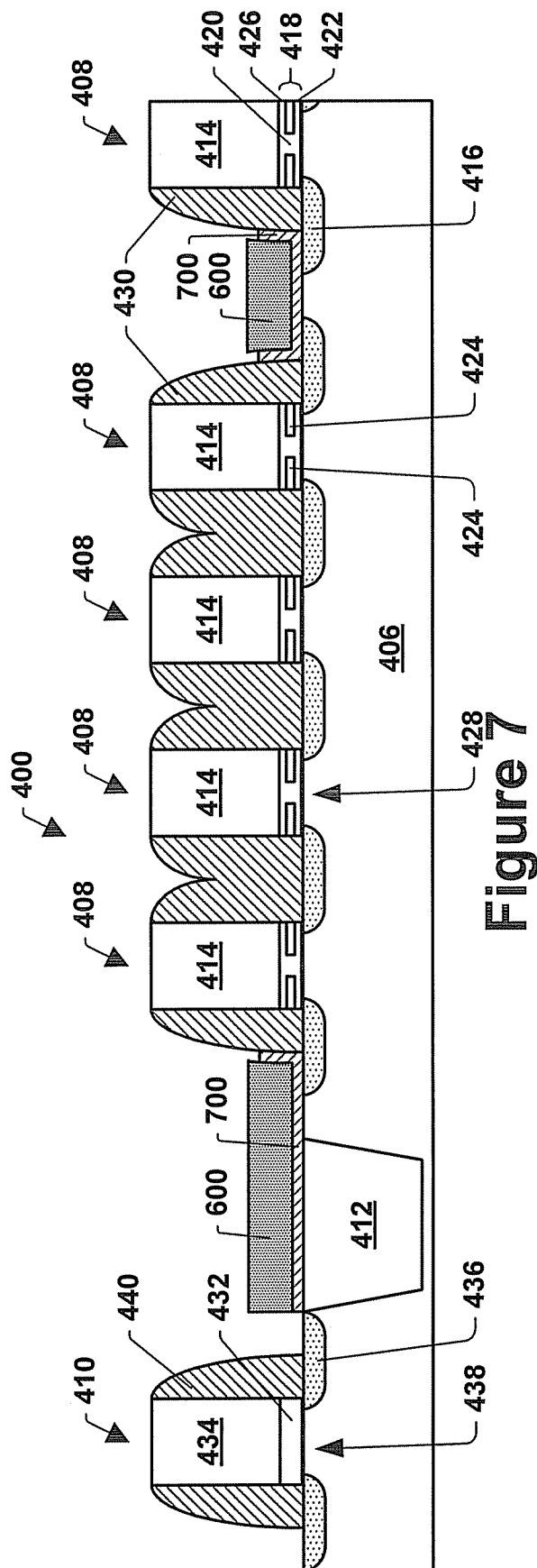


Figure 6



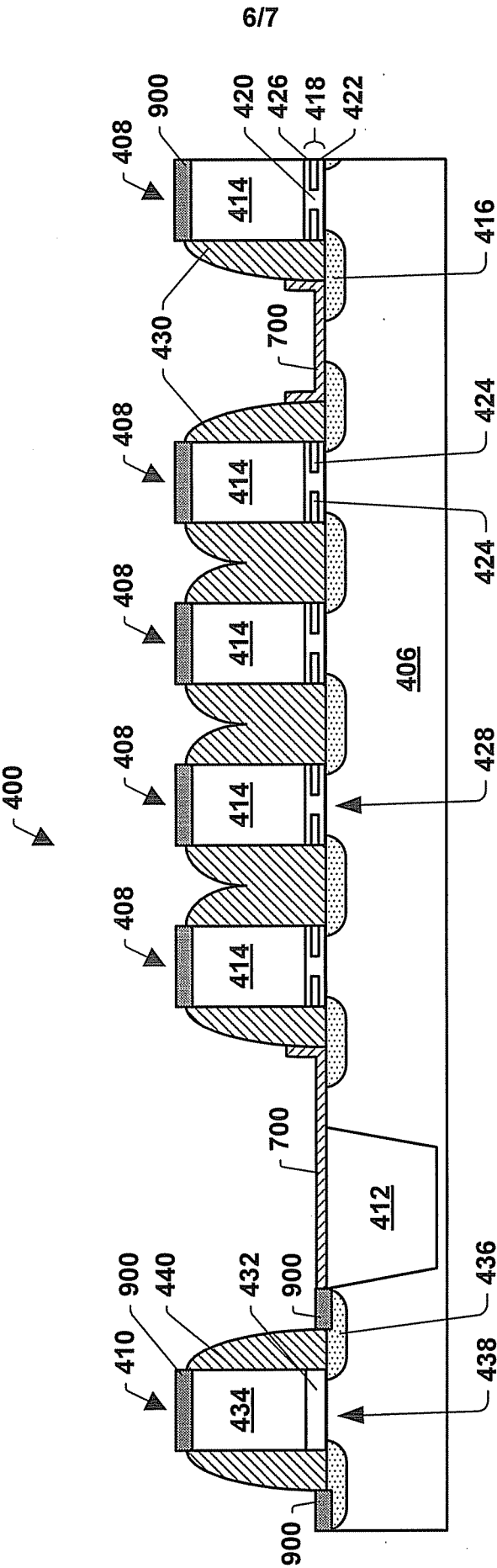
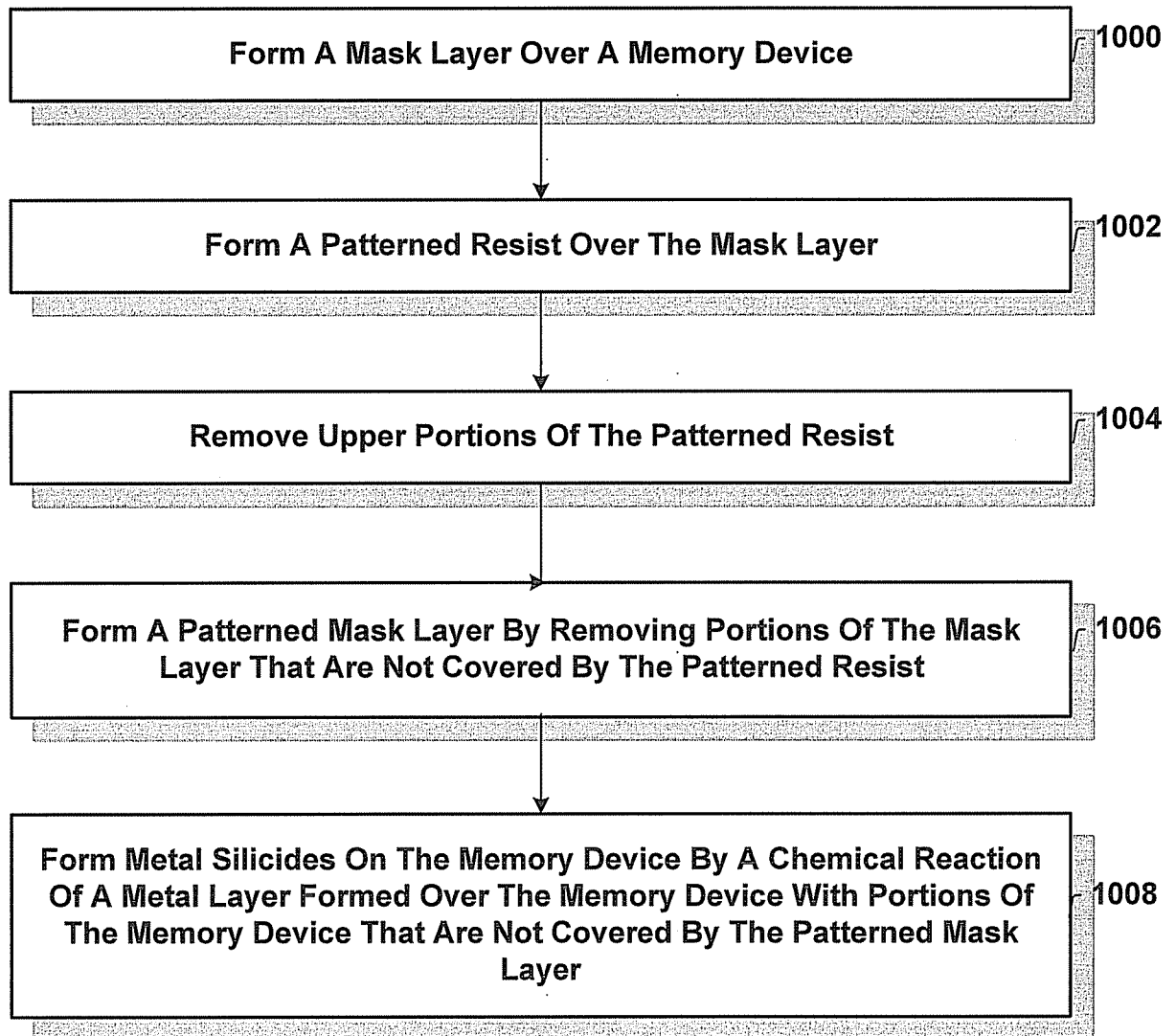


Figure 9

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**Figure 10**

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2008/080636

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L21/8239 H01L21/8246 H01L27/105 H01L27/115 H01L21/336
H01L21/311
ADD. H01L21/8247 H01L21/285

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 025 267 A (PEY KIN-LEONG [SG] ET AL) 15 February 2000 (2000-02-15)	5,7-9
Y	column 3, line 48 - column 6, line 54; figures 1-7	1-4,6,10
Y	EP 0 928 023 A (SIEMENS AG [DE]) 7 July 1999 (1999-07-07) paragraph [0016] - paragraph [0019]; figures 1-9	1-4,6,10
A	US 2002/132430 A1 (WILLER JOSEF [DE] ET AL) 19 September 2002 (2002-09-19) paragraph [0046] - paragraph [0078]; figures 1-11	1-10
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☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

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- *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
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Date of the actual completion of the international search

23 January 2009

Date of mailing of the international search report

30/01/2009

Name and mailing address of the ISA/

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Authorized officer

Albrecht, Claus

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2008/080636

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 975 020 A (ST MICROELECTRONICS SRL [IT]) 26 January 2000 (2000-01-26) paragraph [0009] - paragraph [0030]; figures 1-23 -----	1-10
A	US 2004/014328 A1 (MAKI TATSUICHIRO [JP]) 22 January 2004 (2004-01-22) FIG. 12 is a graph showing the relationship between the pressure inside the reaction chamber and each of the etching rates and the etching selectivity, when the ratio of the space required for the film to be etched is 20%. paragraph [0055] - paragraph [0080]; figures 10-21C -----	1-10

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2008/080636

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 6025267	A	15-02-2000	SG	72872 A1	23-05-2000
EP 0928023	A	07-07-1999	CN	1223469 A	21-07-1999
			JP	11284063 A	15-10-1999
			TW	406351 B	21-09-2000
			US	6960818 B1	01-11-2005
			US	5940717 A	17-08-1999
US 2002132430	A1	19-09-2002	AU	2002338242 A1	15-10-2002
			CN	1502134 A	02-06-2004
			DE	10110150 A1	19-09-2002
			WO	02080275 A2	10-10-2002
			EP	1364409 A2	26-11-2003
			JP	2004530296 T	30-09-2004
			TW	540141 B	01-07-2003
EP 0975020	A	26-01-2000	US	6251728 B1	26-06-2001
US 2004014328	A1	22-01-2004	JP	2004055610 A	19-02-2004