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- (71) **Applicant:** VARIAN SEMICONDUCTOR EQUIPMENT ASSOCIATES, INC. [US/US]; 35 Dory Road, Gloucester, MA 01930 (US).
- (72) **Inventors:** ZHANG, Ying; 4501 Carlyle Court, Apt. 1310, Santa Clara, CA 95054 (US). SHERMAN, Steven; 409 Newtonville Avenue, Newton, MA 02458 (US).
- (74) **Agent:** DAISAK, Daniel, N.; Kacvinsky Daisak Bluni PLLC, 3120 Princeton Pike, Suite 303, Lawrenceville, NJ 08648 (US).
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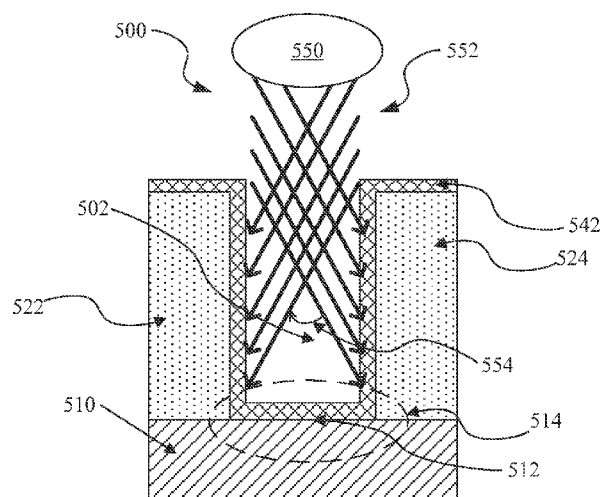
(54) **Title:** PROCESS FLOW FOR REPLACEMENT METAL GATE TRANSISTORS

FIG. 5A

(57) **Abstract:** A replacement metal gate transistor and methods of forming replacement metal gate transistors are described. Various examples provide methods of manufacturing a replacement metal gate transistor that includes depositing a dielectric layer into a trench, wherein the dielectric layer is deposited onto the bottom of the trench and the sidewalls of the trench, depositing a first metal layer into the trench, wherein the first metal layer is deposited onto the bottom of the trench and the sidewalls of the trench over the dielectric layer, depositing a second metal layer into the trench, wherein the second metal layer is deposited onto the bottom of the trench and the sidewalls of the trench over the first metal layer, removing at least a portion of the second metal layer from the sidewalls of the trench, and depositing a conducting layer into the trench. Other embodiments are disclosed and claimed.

PROCESS FLOW FOR REPLACEMENT METAL GATE TRANSISTORS

Field of the Disclosure

[0001] Embodiments of the present disclosure generally relate to semiconductor manufacturing, and more particularly to manufacturing a replacement metal gate transistor.

Background of the Disclosure

[0002] A typical process flow for manufacturing replacement metal gate (RMG) transistors may include removing a temporary gate (sometimes referred to as a dummy gate), leaving a trench where various layers of material are deposited to form the RMG. For example, a dielectric layer may be deposited into the trench, followed by a first metal layer, a second metal layer, and a conductor layer. As will be appreciated, when each layer is deposited into the trench, material may be deposited onto the bottom of the trench as well as the sidewalls. The material build-up on the sidewalls, however, is not required for the RMG transistor to function properly. In some cases, the material build-up on the sidewalls may actually reduce the performance of the transistor. For example, some high-k dielectric build-up on the sidewalls of the trench may increase the parasitic capacitance within the RMG transistor and cause cross-talking with adjacent contacts.

[0003] As device structures and sizes are scaled down, the width of transistor gates also decreases. As such, the width of the trench described above for an RMG transistor also decreases. With each layer of material being deposited into the trench, the material build-up on the sidewalls of the trench further decreases the trench opening for

subsequent layer depositions. Furthermore, each layer of material requires a minimum thickness to properly function. Accordingly, there are theoretical limits to the minimum gate width, the number of layers and each layers respective minimum thickness.

[0004] Additionally, as will be appreciated, deposition may be affected by the aspect ratio of the trench. A trenches aspect ratio is often represented as the ratio of the trench height to trench width. Deposition may be non-uniform at higher aspect ratios, which may manifest as thicker deposition higher on the sidewalls and thinner deposition lower on the sidewalls and at the bottom of the trench. With each successive deposition of a layer in the RMG, the aspect ratio of the trench will increase, possibly further exacerbating the non-uniformity of the deposition and further decreasing the trench width.

[0005] As such, there is a need to remove at least some portion of the material deposited on the sidewalls of the trench, in order to improve the transistor device performance, reduce the aspect ratio of the trench, improve quality and uniformity of depositions, and to allow devices with smaller gate widths to be manufactured.

Summary

[0006] This Summary is provided to introduce a selection of concepts in a simplified form that are further described below in the Detailed Description. This Summary is not intended to identify key features or essential features of the claimed subject matter, nor is it intended as an aid in determining the scope of the claimed subject matter.

[0007] In general, various embodiments of the present disclosure provide a method for forming a replacement metal gate transistor comprising depositing a first layer into a

trench, wherein the first layer is deposited onto a bottom of the trench and onto sidewalls of the trench, depositing a second layer into the trench, wherein the second layer is deposited onto over the first layer and onto the bottom and sidewalls of the trench, and removing at least a portion of the second layer from the sidewalls of the trench.

[0008] As an alternative example, some embodiments disclose a method for forming a replacement metal gate transistor comprising depositing a dielectric layer into a trench, wherein the dielectric layer is deposited onto the bottom of the trench and the sidewalls of the trench, depositing a first metal layer into the trench, wherein the first metal layer is deposited onto the bottom of the trench and the sidewalls of the trench over the dielectric layer, depositing a second metal layer into the trench, wherein the second metal layer is deposited onto the bottom of the trench and the sidewalls of the trench over the first metal layer, removing at least a portion of the second metal layer from the sidewalls of the trench, and depositing a conducting layer into the trench.

[0009] Further embodiments include a replacement metal gate transistor comprising a dielectric layer disposed on a substrate and on inner sidewalls of a trench, wherein the dielectric layer has a bottom section and sidewall sections, a first metal layer disposed on the bottom section of the dielectric layer, a second metal layer disposed on the bottom section of the first metal layer, and a conductor layer disposed on the second metal layer and the sidewall sections of the dielectric layer.

Brief Description of the Drawings

[0010] By way of example, various embodiments of the disclosed device will now be described, with reference to the accompanying drawings, in which:

[0011] **FIGS. 1A – 1E** are block diagrams of an RMG gate transistor;

[0012] **FIGS. 2A – 2C** are a block diagrams of an RMG transistor manufactured according to at least some embodiments of the present disclosure;

[0013] **FIGS. 3A – 3B** are a block diagrams of another RMG transistor manufactured according to at least some embodiments of the present disclosure;

[0014] **FIGS. 4A – 4B** are a block diagrams of another RMG transistor manufactured according to at least some embodiments of the present disclosure;

[0015] **FIGS. 5A – 5D** are a block diagrams of another RMG transistor manufactured according to at least some embodiments of the present disclosure;

[0016] **FIG. 6** is a block diagram of another RMG transistor manufactured according to at least some embodiments of the present disclosure;

[0017] **FIG. 7** is a flow chart illustrating a method of cleaning an RF source, all arranged in accordance with at least some embodiments of the present disclosure.

Detailed Description

[0018] As described above, a typical process for manufacturing an RMG transistor may include removing a temporary gate, leaving a trench; and then filling in the trench by depositing layers of material to form the RMG. In general, the RMG may be formed using any number of suitable thin film deposition techniques (*e.g.*, atomic layer deposition, plasma deposition, ion deposition, or the like) or process flows.

[0019] **FIG. 1A** illustrates a block diagram of an RMG transistor 100 part way through its fabrication process, after the temporary gate (not shown) has been removed. As depicted, the RMG transistor 100 includes a trench 110 formed between sidewalls 122, 124, which are built up on substrate 130. The trench 110 includes a bottom 112 and inner sidewalls 114, 116; and has an initial width 118a (sometimes referred to as “gate width.”) In some examples, the substrate 130 may be silicon and the sidewalls 122, 124 may be silicon dioxide, silicon nitride, or some other silicon-based dielectric material. As will be appreciated, the materials referenced herein to describe the RMG transistor 100, are given for illustrative purposes only and are not intended to be limiting. Other materials may be substituted without departing from the scope of the present disclosure.

[0020] **FIG. 1B** illustrates a block diagram of the RMG transistor 100, having a first layer 142 deposited into the trench 110. As depicted, the first layer 142 has been deposited onto the bottom 112 and inner sidewalls 114, 116 of the trench 110. As will be appreciated, due to the deposition of the first layer 142 onto the inner sidewalls 114, 116, the initial width of the trench opening 118a has been reduced to the width 118b. In general, the initial width 118a will be reduced by approximately twice the thickness of the first layer 142. Thus, the aspect ratio of the trench 110 will be increased. In some examples, the first layer 142 may be formed from a dielectric material. In further examples, the first layer 142 may be formed from a high-k dielectric material (*e.g.*, hafnium silicate, zirconium silicate, hafnium dioxide, or zirconium dioxide).

[0021] **FIG. 1C** illustrates a block diagram of the RMG transistor 100, having a second layer 144 deposited into the trench 110. As depicted, the second layer 144 has been deposited onto the bottom 112 and inner sidewalls 114, 116 of the trench 110 and

over the first layer 142. As described above, deposition may be affected by the aspect ratio of the trench 110. For example, at higher aspect ratios, the uniformity of the deposition may decrease, resulting in increased deposition thickness near the top of the trench 110 and reduced deposition thickness near the bottom of the trench 110. More specifically, this non-uniformity may manifest as corners 144a, 144b. Additionally, as will be appreciated, due to the deposition of the second layer 144 onto the inner sidewalls 114, 116, the width 118b has been reduced (*e.g.*, by approximately twice the thickness of the second layer 144) to width 118c. Thus, the aspect ratio of the trench 110 has again been increased. In some examples, the second layer 144 may be formed from a material having a substantially low conductivity (*e.g.*, titanium nitride).

[0022] FIG. 1D illustrates a block diagram of the RMG transistor 100, having a third layer 146 deposited into the trench 110. As depicted, the third layer 146 has been deposited onto the bottom 112 and inner sidewalls 114, 116 of the trench 110 and over the second layer 144. The third layer 146 is depicted as having less uniform deposition than either the first layer 142 or the second layer 144, represented by corners 146a, 146b. Additionally, as will be appreciated, due to the deposition of the third layer 146 onto the sidewalls 114, 116, the width 118c has been reduced (*e.g.*, by approximately twice the thickness of the third layer 146) to width 118d. Thus, the aspect ratio of the trench 110 has again been increased.

[0023] FIG. 1E illustrates a block diagram of the RMG transistor 100, having the trench 110 filled in with a “contact layer,” 148. In general, the contact layer 148 serves as the main path of electrical conduction along the length of the trench. As such, material for the contact layer 148 is chosen from materials having relatively low electrical

resistivity (e.g. tungsten or aluminum). As depicted, the contact layer 148 has been deposited into the remaining portion of the trench 110, overlaying the third layer 146, forming RMG stack 140.

[0024] The speed of an integrated circuit (IC) built with transistors such as the one illustrated in **FIG. 1** is limited by the electrical resistance along the filled trench 110, and also by the electrical capacitance between two such filled trenches. Therefore the performance of such an IC can be improved by removing at least some of the RMG layers (e.g., the first layer 142, the second layer 144, or the third layer 146) from the trench sidewalls 114, 116. Removing these RMG layers, which typically have relatively high electrical resistivity will make more space for the contact layer 148 which has relatively low electrical resistivity, resulting in a RMG transistor 100 with lower overall electrical resistance. Second, removing the first layer 142, which typically has a high dielectric constant, will reduce the electrical capacitance between two such RMG transistors.

[0025] As will be appreciated, each layer of the RMG 140 may have a corresponding minimum thickness (e.g., 2 nanometers, or the like) in order to function properly.

Accordingly, as device sizes continually scale down, the gate width may not be sufficient to allow for the proper deposition of the various layers of the RMG 140. For example, the gate width may have a theoretical minimum limit of approximately

$2 \cdot N_{\text{layers}} \cdot \text{Thick}_{\text{min}}$, where N_{layers} equals the number of layers in the RMG 140 and

$\text{Thick}_{\text{min}}$ equals the minimum thickness per layer. Furthermore, as illustrated in **FIGS.**

1A – 1E, the width 118 near the top of the trench 110 may decrease quicker than the

width 118 near the bottom 112 of the trench 110. As such, deposition of the contact layer 148 on the bottom 112 of the trench 110 may be difficult using conventional techniques.

[0026] It is to be appreciated, that the RMG transistor 100 described with reference to **FIGS. 1A – 1E** is provided for illustrative purposes only and is not intended to be limiting. Various embodiments of the present disclosure may be applied to processing an RMG transistor having a composition similar to that depicted with reference to **FIGS. 1A – 1E**. Alternatively, various embodiments of the present disclosure may be applied to processing an RMG transistor having a composition different (*e.g.*, having a different number of layers, different material of manufacture, or the like) than that depicted with reference to **FIGS. 1A – 1E**. For example, an RMG transistor may have more or fewer layers than described above. More particularly, an RMG transistor may have only three total layers such as the layers 142, 144, and 146 depicted in **FIG. 1**, or it may have additional layers not shown in **FIG. 1**. Although the following example embodiments reference an RMG transistor having three layers, it is to be appreciated that this is done for purposes of clarity and is not intended to be limiting.

[0027] As introduced above, various embodiments of the present disclosure may be applied to reduce the aspect ratio of trench during manufacturing of an RMG transistor. For example, various embodiments of the present disclosure may be applied to reduce the aspect ratio of the trench 110 shown in **FIGS. 1A – 1E**. The aspect ratio of the trench 110 may be reduced, by, for example, removing portions of the layers (*e.g.*, the layer 142, 144, and/or 146) from the sidewalls 114, 116. With at least some embodiments of the present disclosure, portions of the layers may be removed using an angled ion beam,

which may be configured to etch, sputter, or otherwise remove portions of the layers from the inner sidewalls.

[0028] Some embodiments of the present disclosure will now be described in greater detail with reference to various illustrative examples. It is to be appreciated that these examples are given for illustration only and are not intended to be limiting.

Illustrative Example 1

[0029] **FIG. 2A** illustrates a block diagram of an RMG transistor 200, arranged according to at least some embodiments of the present disclosure. As depicted, the RMG transistor 200 is shown prior to deposition of a contact layer, which typically has a relatively low electrical resistivity for the purpose of reducing the electrical resistance of the gate line. The RMG transistor includes a first layer 242 deposited into a trench 202 formed between sidewalls 222, 224 and substrate 210. In some examples, the first layer 242 may be referred to as a dielectric layer. Second and third layers 244, 246 are also shown. In some examples, the second and third layers 244, 246 may be referred to as first and second metal layers respectively. An ion source 250 generating angled ion beams 252 is also shown. The angled ion beams 252 are incident upon the layers 242, 244, and 246 built-up on the sidewall 222. In general, the angled ion beams 252 may be used to at least partially remove (*e.g.*, via sputtering, etching, or the like) material from the layers 242, 244, and/or 246 that are built-up on the sidewall 222. In some examples, the angle 254a of the angled ion beams 252 (shown measured relative a line 256 perpendicular to the bottom 212) may be selected such that the ion beams are incident upon the sidewall 222, but not the bottom 212. More specifically, the angle 254a may be

selected such that the material on the bottom 212 (*e.g.*, shown by dashed area 214) is substantially not removed by the angled ion beams 252 because the ion beams 252 are shadowed by sidewall 224. In some embodiments, the ion beam 252 assists a reactive ion etch where substantially all of the etched material is chemically volatilized, as opposed to the ion beams 252 sputtering the material where a substantial amount of the sputtered material is physically and may re-deposit inside the trench. Re-deposition of removed material inside the trench may be undesirable because the RMG transistor's performance is sensitive to the composition of the various layers as well as the condition of their surfaces and interfaces.

[0030] FIG. 2B illustrates a block diagram of the RMG transistor 200, arranged according to at least some embodiments of the present disclosure. As depicted, the RMG transistor is shown after material from the layers 242, 244, and 246 built-up on the sidewall 222 has been removed. The angled ion beams 252 are incident upon the layers 242, 244, and 246 built-up on the sidewall 224. In general, the angled ion beams 252 may be used to at least partially remove (*e.g.*, via sputtering, etching, or the like) material from the layers 242, 244, and/or 246 that are built-up on the sidewall 222. In some examples, the angle 254b of the angled ion beams 252 (shown measured relative a line 256 perpendicular to the bottom 212) may be selected such that the ion beams are incident upon the wall 222, but not the bottom 212. More specifically, the angle 254b may be selected such that the material on the bottom 212 (*e.g.*, shown by dashed area 214) is substantially not removed by the ion beams 252 because the ion beams 252 are shadowed by sidewall 222. In some examples, the ion source 250 may be moved, adjusted, or rotated from the positioning shown in FIG. 2A, such that the angled ion

beams 252 are incident upon the sidewall 224 as shown in **FIG. 2B**. As used herein, the term “substantially” when referring to ion beam trajectories shall mean less than 10%. For example, **FIGS. 2A** and **2B** show the ion beams 252 incident upon the sidewalls 222, 224 but not the bottom 212. In practice, some ion from the ion beams 252 may be incident upon the bottom 212. As such, the term “substantially” may be used to indicate that a small portion (*e.g.*, 10% or less) of the ions from the ion beams 252 are incident upon the bottom 212.

[0031] **FIG. 2C** illustrates a block diagram of the RMG transistor 200, arranged according to at least some embodiments of the present disclosure. As depicted, angled ion beams 252 have removed material from layers 242, 244, and 246 built-up on the sidewalls 222, 224 of the RMG transistor 200. Additionally, a contact layer 248 is shown having been deposited into the trench and onto the remaining material from the layers 242, 244, and 246. As used herein, the term “substantially” when referring to the thickness of the bottom sections (*e.g.* 214) or the thickness of the sidewall sections of the layers 242, 244, and/or 246 shall mean at least 50%. For example, **FIG. 2C** shows the material on the bottom 212 of the trench 214 including at least 50% of the original material. Conversely, the material on the sidewalls 222, 224 is shown as having greater than 50% removed. Accordingly, as used herein, substantially not removed shall mean at least 50% of the original material remains and substantially removed shall mean at least 50% of the original material is removed.

Illustrative Example 2

[0032] **FIG. 3A** illustrates a block diagram of an RMG transistor 300, arranged according to at least some embodiments of the present disclosure. As depicted, the RMG transistor is shown prior to deposition of the contact layer. The RMG transistor includes a first layer 342 deposited into a trench 302 formed between sidewalls 322, 324 and substrate 310. Second and third layers 344, 346 are also shown. An ion source 350 generating angled ion beams 352 is also shown. In some embodiments, the ion source 350 may be configured to generate angled ion beams 352 such that the angled ion beams are incident upon the sidewalls 322, 324, but not the bottom 312. More specifically, the angle 354 may be selected such that the material on the bottom 312 (*e.g.*, shown by dashed area 314) is substantially not removed by the angled ion beams 352 because the ion beams 352 are shadowed by sidewalls 322, 324.

[0033] With some examples, the ion source 350 may be a plasma ion source. The plasma ion source may include a plasma process chamber having a plasma sheath positioned adjacent to the RMG transistor 300. The shape of the plasma sheath may be modified with an insulating modifier, which influences the incident angles of ions extracted from the plasma relative to the plane of the trench bottom 312. The insulating modifier can create an ion angle distribution such that no ion trajectories are perpendicular to or near perpendicular to the bottom 312 of the RMG transistor 300.

[0034] **FIG. 3B** illustrates a block diagram of the RMG transistor 300, arranged according to at least some embodiments of the present disclosure. As depicted, angled ion beams 352 have removed material from the layers 342, 344, and 346 built-up on the

sidewalls 322, 324 of RMG transistor 300. Additionally, a contact layer 348 has been deposited into the trench and onto the remaining material from the layers 342, 344, and 346.

Illustrative Example 3

[0035] **FIG. 4A** illustrate a block diagram of an RMG transistor 400, arranged according to at least some embodiments of the present disclosure. As depicted, RMG transistor is shown prior to deposition of the contact layer. The RMG transistor includes a first layer 442 deposited into a trench 402 formed between sidewalls 422, 424 and substrate 410. Second and third layers 444, 446 are also shown. An angled ion source, such as, for example, as described above with respect to illustrative examples 1 or 2, may be used to remove material from second and third layers 444, 446, shown by area 404. The angled ion source, however, is not shown in **FIG. 4A** for clarity. In some examples, it may be advantageous to stop removing material from the sidewalls 422, 424 at the first layer 442. For example, removal of the first layer 442 (*e.g.*, via etching or sputtering) may be difficult. Additionally, it may be advantageous to prevent removal of any material from the sidewalls 422, 424. As such, stopping removal of material at the first layer 442 may assist in preventing removal of material from the sidewalls 422, 424. With some embodiments, removal of material from the sidewalls 422, 424 may be stopped when a portion of the first layer (*e.g.*, which may be a dielectric layer) has been exposed.

[0036] **FIG. 4B** illustrates a block diagram of the RMG transistor 400, according to at least some embodiments of the present disclosure. As depicted, the RMG transistor 400 is shown having material from the area 404 shown in **FIG. 4A** removed. Removal of

material from the sidewalls 422, 424 has been stopped at the first layer 442. As such, the first layer 442 is depicted as substantially unchanged from that shown in **FIG. 4A**.

Additionally, a contact layer 448 has been deposited into the trench and onto the remaining material from the layers 442, 444, and 446.

Illustrative Example 4

[0037] In some embodiments, material built-up on the sidewalls after deposition of a particular layer (*e.g.*, the first layer, or the like) may be removed prior to deposition of another layer. For example, **FIG. 5A** illustrates a block diagram of an RMG transistor 500, arranged according to at least some embodiments of the present disclosure. As depicted, the RMG transistor 500 is shown after deposition of a first layer. More specifically, the RMG transistor 500 includes a first layer 542 deposited into a trench 502, the trench 502 being formed between sidewalls 522, 524 and substrate 510.

[0038] An ion source 550 generating angled ion beams 552 is also shown. In some embodiments, the ion source 550 may be configured to generate angled ion beams 552 such that the angled ion beams are incident upon the sidewalls 522, 524, but not the bottom 512. More specifically, the angle 554 may be selected such that the material on the bottom 512 (*e.g.*, shown by dashed area 514) is substantially not removed by the angled ion beams 552; while the material on the sidewalls 522 and 526 is substantially removed by the angled ion beams 552 because the ion beams 552 are shadowed by sidewalls 522, 524. With some examples, the ion source 550 may be configured similar to that described above with respect to **FIGS. 3A – 3B**. As will be appreciated, in practice a portion of the first layer 542 may remain on the sidewalls 522, 524. For

example, substantially all of the first layer 542 may be removed from the sidewalls 522, 524. However, small amounts (*e.g.*, less than 1 nanometer, or the like) of material may remain on the sidewalls 522, 524 after the angled ion beams 552 are used to remove the material. Also as will be appreciated, a portion of the full thickness of the first layer 542 may remain near the bottom of the sidewalls 522, 524.

[0039] **FIG. 5B** illustrates a block diagram of the RMG transistor 500, arranged according to at least some embodiments of the present disclosure. As depicted, the RMG transistor 500 is shown after material from the layer 542 built-up on the sidewalls 522, 524 has been removed. Additionally, a second layer 544 has been deposited into the trench 502. As depicted, the second layer 544 has been deposited over the first layer 542 on the bottom of the trench 512. However, as the first layer 542 has been removed from the sidewalls 522, 524, as described with respect to **FIG. 5A**, the second layer 544 is depicted as being deposited directly onto the sidewalls 522, 524. As stated above, in some examples, small amounts of the first layer 542 may remain on the sidewalls 522, 524. However, these small amount are not shown in **FIG. 5B** for purposes of clarity of presentation.

[0040] The ion source 550, generating angled ion beams 552, is also shown. In some embodiments, the ion source 550 may be configured to generate angled ion beams 552 such that the angled ion beams are incident upon the sidewalls 522, 524, but not the bottom 512. More specifically, the angle 554 may be selected such that the material on the bottom 512 (*e.g.*, shown by dashed area 514) is substantially not removed by the angled ion beams 552; while the material on the sidewalls 522 and 526 is substantially removed by the angled ion beams 552 because the ion beams 552 are shadowed by

sidewalls 522, 524. As will be appreciated, in practice a portion of the second layer 544 may remain on the sidewalls 522, 524. For example, substantially all of the second layer 544 may be removed from the sidewalls 522, 524. However, small amounts (*e.g.*, less than 1 nanometer, or the like) of material may remain on the sidewalls 522, 524 after the angled ion beams 552 are used to remove the material.

[0041] **FIG. 5C** illustrates a block diagram of the RMG transistor 500, arranged according to at least some embodiments of the present disclosure. As depicted, the RMG transistor 500 is shown after material from the layer 544 built-up on the sidewalls 522, 524 has been removed. Additionally, a third layer 546 has been deposited into the trench 502. As depicted, the third layer 546 has been deposited over the second layer 544 on the bottom of the trench 512. However, as the second layer 544 has been removed from the sidewalls 522, 524, as described with respect to **FIG. 5B**, the third layer 546 is depicted as being deposited directly onto the sidewalls 522, 524. As stated above, in some examples, small amounts of the second layer 544 may remain on the sidewalls 522, 524. However, these small amount are not shown in **FIG. 5C** for purposes of clarity of presentation.

[0042] The ion source 550, generating angled ion beams 552, is also shown. In some embodiments, the ion source 550 may be configured to generate angled ion beams 552 such that the angled ion beams are incident upon the sidewalls 522, 524, but not the bottom 512. More specifically, the angle 554 may be selected such that the material on the bottom 512 (*e.g.*, shown by dashed area 514) is substantially not removed by the angled ion beams 552; while the material on the sidewalls 522 and 526 is substantially removed by the angled ion beams 552 because the ion beams 552 are shadowed by

sidewalls 522, 524. As will be appreciated, in practice a portion of the third layer 546 may remain on the sidewalls 522, 524. For example, substantially all of the third layer 546 may be removed from the sidewalls 522, 524. However, small amounts (*e.g.*, less than 1 nanometer, or the like) of material may remain on the sidewalls 522, 524 after the angled ion beams 552 are used to remove the material. Also as will be appreciated, a portion of the full thickness of the first layer 542 may remain near the bottom of the sidewalls 522, 524.

[0043] **FIG. 5D** illustrates a block diagram of the RMG transistor 500, arranged according to at least some embodiments of the present disclosure. As depicted, the first layer 542, second layer 544, and third layer 546 has been deposited into the trench. Material built-up on the sidewalls 522, 524 after the deposition of each layer has been removed (*e.g.*, using an angled ion beam as described above) prior to deposition of subsequent layers, for example, as depicted with respect to **FIGS. 5A – 5C**. Additionally, a contact layer 548 has been deposited into the trench and onto the third layer 546.

Illustrative Example 5

[0044] In some embodiments, material built-up on the sidewalls after deposition of a particular layer (*e.g.*, the second layer, or the like) may be removed prior to deposition of another layer. Additionally, the first layer (*e.g.*, a high-k dielectric layer, or the like) may be used to stop the removal of material from the sidewalls and/or prevent removal of sidewall material. For example, **FIG. 6** illustrates a block diagram of an RMG transistor 600, arranged according to at least some embodiments of the present disclosure. As depicted, a first layer 642 has been deposited into the trench. Additionally, a second layer 644 and third layer 646 has been deposited into the trench. In the RMG transistor shown, after deposition of the first layer 642 and second layer 644, material from the second layer 644 is removed from the sidewalls 622, 624, (*e.g.*, using an angled ion beam as described above), but the material of first layer 642 remains upon the sidewalls 622, 624. Subsequently, the third layer 646 is deposited and material from the third layer 646 is removed from the sidewalls 622, 624, (*e.g.*, using an angled ion beam as described above) resulting in the structure shown. Additionally, a contact layer 648 has been deposited into the trench and onto the third layer 646.

Illustrative Example 6

[0045] **FIG. 7** is a flow chart illustrating a method 700 for forming an RMG transistor, arranged in accordance with at least some embodiments of the present disclosure. In general, the method 700 is described with reference to the RMG transistor 300 and the ion source 350 and angled ion beams 352 of **FIGS. 3A – 3B**.

[0046] The method 700 may begin at block 710. At block 710, a layer of material (*e.g.*, the first layer 442, the second layer 444 and/or the third layer 446) is deposited into the trench. Continuing from block 710 to block 720, at least some of the material deposited into the trench is removed from the sidewalls 422, 424 of the trench. More particularly, the ion source 450 and the angled ion beams 452 are used to remove (*e.g.*, via etching, sputtering, or the like) the material from the deposited layer that is built-up on the sidewalls 422, 424 without substantially removing material deposited onto the bottom 412 of the trench.

[0047] Continuing from block 720 to block 730, a determination is made as to whether all desired layers have been deposited into the trench. If all layers have been deposited, then the process continues to block 740, and a contact layer may be deposited into the trench and then the process may end at block 750. If, however, additional layers are to be deposited, the process may return to block 710, where another layer may be deposited into the trench.

[0048] In some examples, multiple layers may be deposited and then have material from one or more of the deposited layers built-up on the sidewalls 422, 424 removed. With other examples, a single layer may be deposited and then have material from the layer built-up on the sidewalls 422, 424 removed prior to deposition of another layer.

[0049] The present disclosure is not to be limited in scope by the specific embodiments described herein. Indeed, other various embodiments of and modifications to the present disclosure, in addition to those described herein, will be apparent to those of ordinary skill in the art from the foregoing description and accompanying drawings.

Thus, such other embodiments and modifications are intended to fall within the scope of the present disclosure. Furthermore, although the present disclosure has been described herein in the context of a particular implementation in a particular environment for a particular purpose, those of ordinary skill in the art will recognize that its usefulness is not limited thereto and that the present disclosure may be beneficially implemented in any number of environments for any number of purposes. Accordingly, the claims set forth below should be construed in view of the full breadth and spirit of the present disclosure as described herein.

Claims

1. A method for forming a structure in an integrated circuit comprising:
depositing a layer into a trench, wherein material from the layer is deposited onto a bottom of the trench and onto a first and second sidewall of the trench;
removing at least a portion of the material of the layer from the first and second sidewalls of the trench using an angled ion beam, wherein the angled ion beam is configured to remove the material from the first and second sidewalls of the trench without removing the material from the bottom of the trench.
2. The method of claim 1, wherein the layer is a first layer, the method further comprising:
depositing a second layer into the trench, wherein material from the second layer is deposited onto the bottom of the trench and onto the first and second sidewalls of the trench; and
removing at least a portion of the material of the second layer from off the first and second sidewalls of the trench using the angled ion beam, wherein the angled ion beam is configured to remove the material from the first and second sidewalls of the trench without removing the material from the bottom of the trench.
3. The method of claim 2, further comprising depositing a contact layer into the trench, wherein the contract layer is deposited after the portion of the material from the first layer is removed from the first and second sidewalls using the angled ion beam and

after the portion of the material from the second layer is removed from the first and second sidewalls using the angled ion beam.

4. The method of claim 3, wherein removing the portion of the material of the first layer from the first and second sidewalls and removing the portion of the material of the second layer from the first and second sidewalls are performed concurrently.

5. The method of claim 1, wherein removing the portion of the material of the layer comprises:

targeting the angled ion beam at the first and second sidewalls of the trench, wherein the angled ion beam has substantially no ion trajectories perpendicular to the bottom of the trench; and

etching material of the layer from the first and second sidewalls.

6. The method of claim 5, removing the portion of the material of the layer further includes:

determining whether a desired amount of the material of the layer has been etched from the first and second sidewalls; and

stopping the etching based at least in part on the determination that the desired amount of the material of the layer has been etched away.

7. The method of claim 6, wherein the material deposited onto the first and second sidewalls is 50% of the desired amount of material in the trench.

8. The method of claim 3, further comprising depositing a third layer into the trench, wherein the third layer is deposited onto the bottom of the trench and onto the first and second sidewalls of the trench before either the first layer or the second layer is deposited into the trench

9. A method for forming a replacement metal gate transistor comprising:
depositing a dielectric layer into a trench, wherein the dielectric layer is deposited onto a bottom of the trench and sidewalls of the trench;

depositing a first metal layer into the trench over the dielectric layer, wherein the first metal layer has a first portion deposited onto the sidewalls of the trench and a second portion deposited onto the bottom of the trench;

depositing a second metal layer into the trench over the first metal layer, wherein the second metal layer has a first portion deposited onto the sidewalls of the trench and a second portion deposited onto the bottom of the trench;

removing at least some of the first portion of the second metal layer using an angled ion beam without removing the second portion of the second metal layer; and

depositing a conducting layer into the trench over the third metal layer.

10. The method of claim 9, wherein removing at least some of the first portion of the second metal layer using the angled ion beam comprises:

targeting an angled ion beam at the sidewalls of the trench, wherein the angled ion beam has substantially no ion trajectories perpendicular to the bottom of the trench; and

removing at least some of the first portion of the second metal layer.

11. The method of claim 10, wherein removing at least some of the first portion of the second metal layer using the angled ion beam further comprises:

removing at least some of the first portion of the first metal layer.

12. The method of claim 11, wherein removing at least some of the first portion of the second metal layer using the angled ion beam further comprises:

determining that a portion of the dielectric layer is exposed; and

stopping the removing based at least in part on the determination that a portion of the dielectric layer is exposed.

13. The method of claim 9, wherein the dielectric layer has a first portion deposited onto the sidewalls of the trench and a second portion deposited onto the bottom of the trench, the method comprising:

removing at least some of the first portion of the dielectric layer using the angled ion beam prior to depositing the first metal layer into the trench, wherein the angled ion beam is configured to remove some of the first portion of the dielectric layer but not remove the second portion of the dielectric layer.

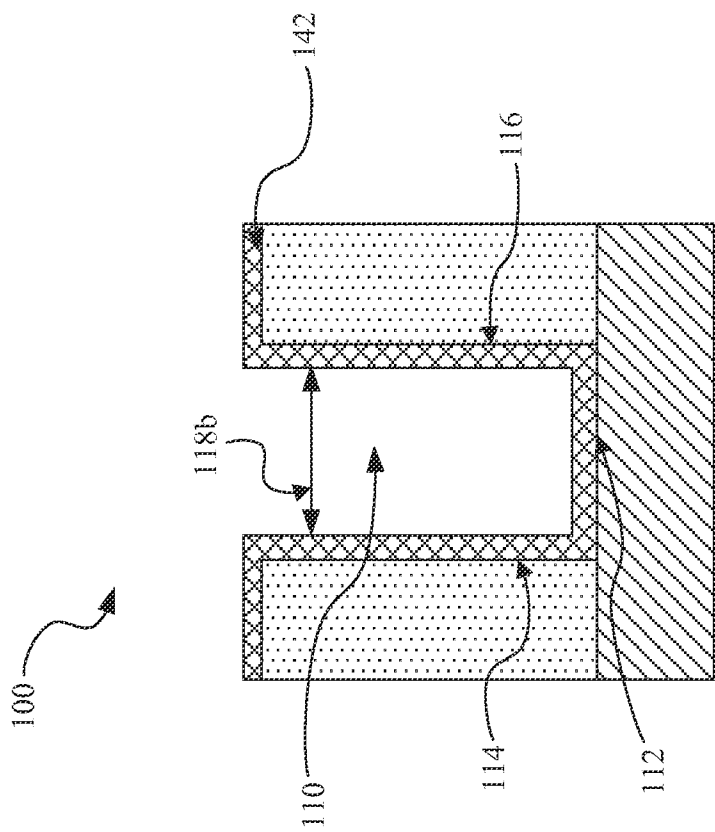


FIG. 1A

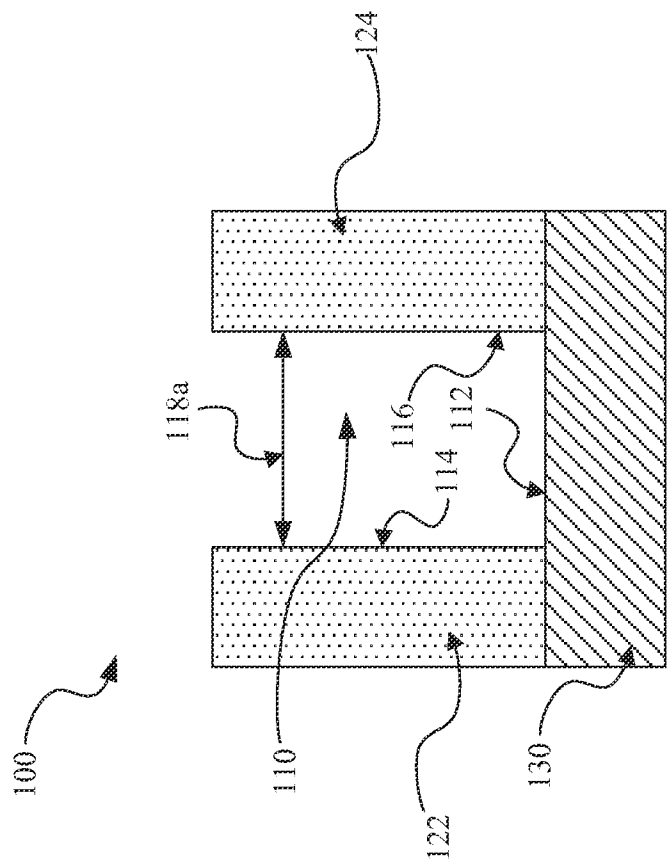


FIG. 1B

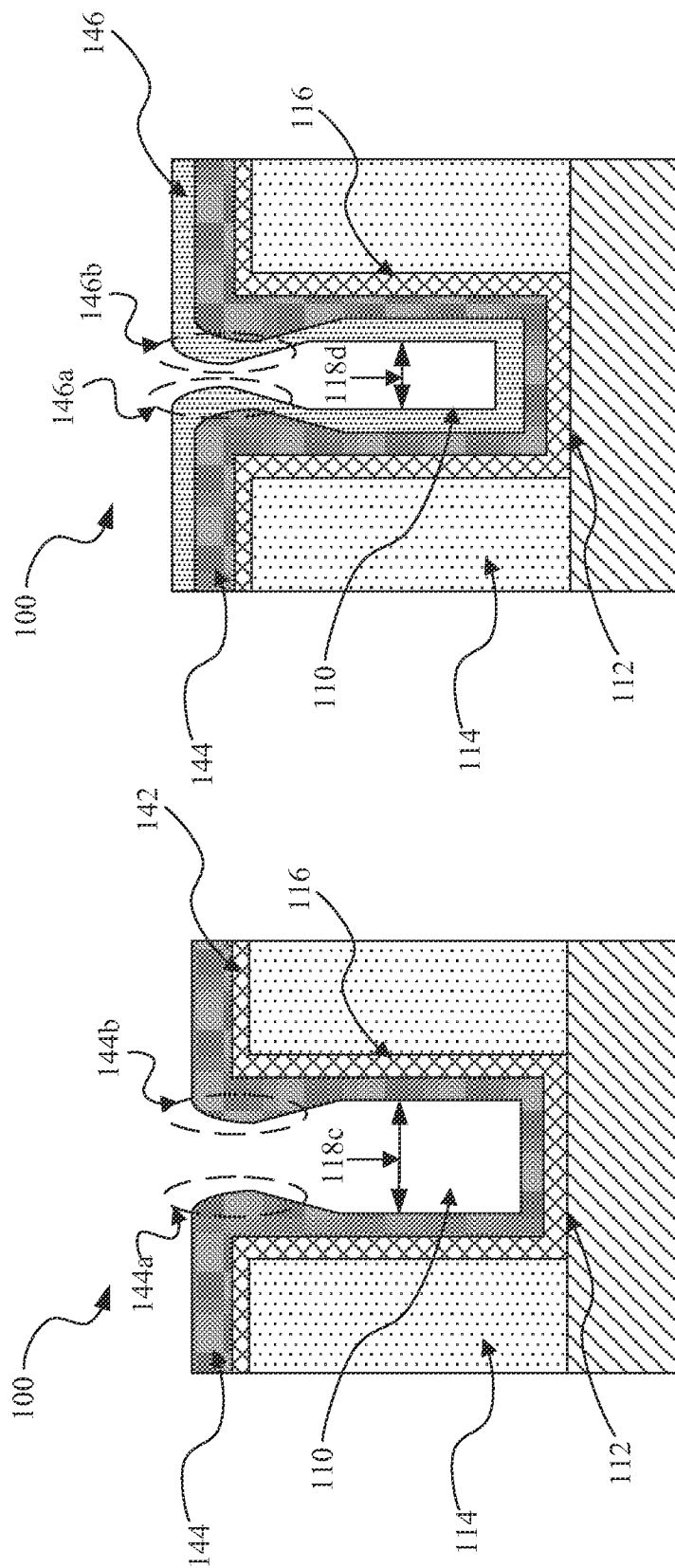


FIG. 10

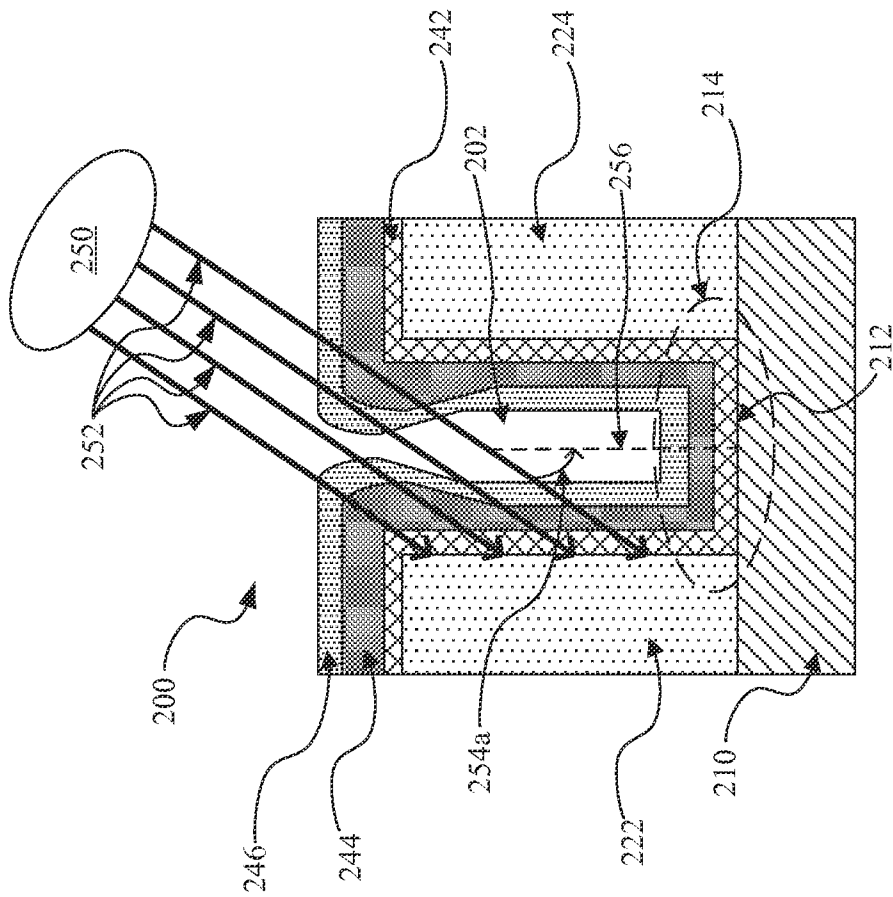


FIG. 2A

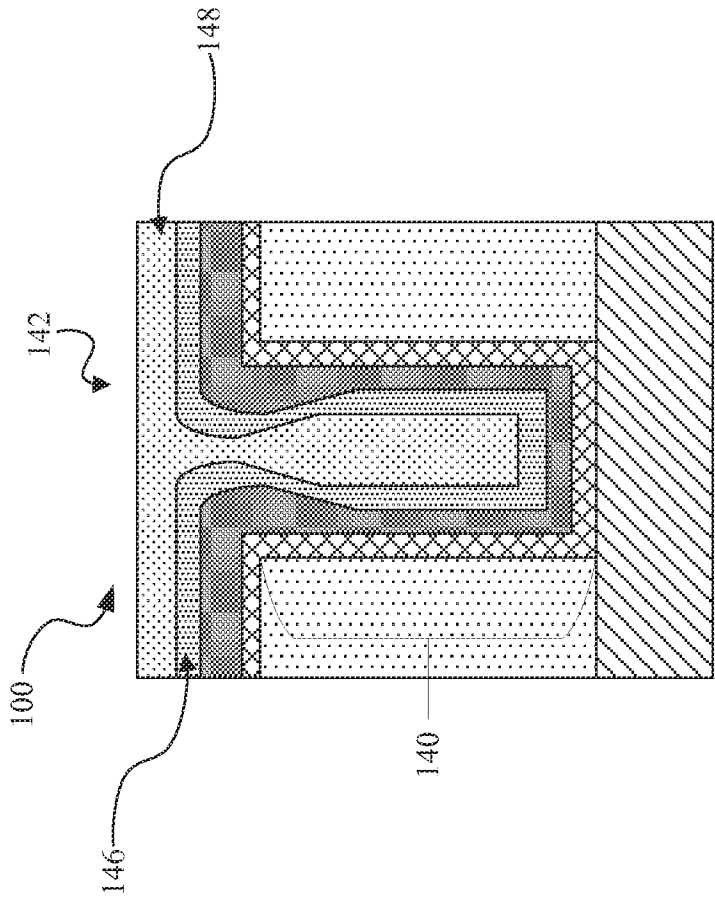


FIG. 1E

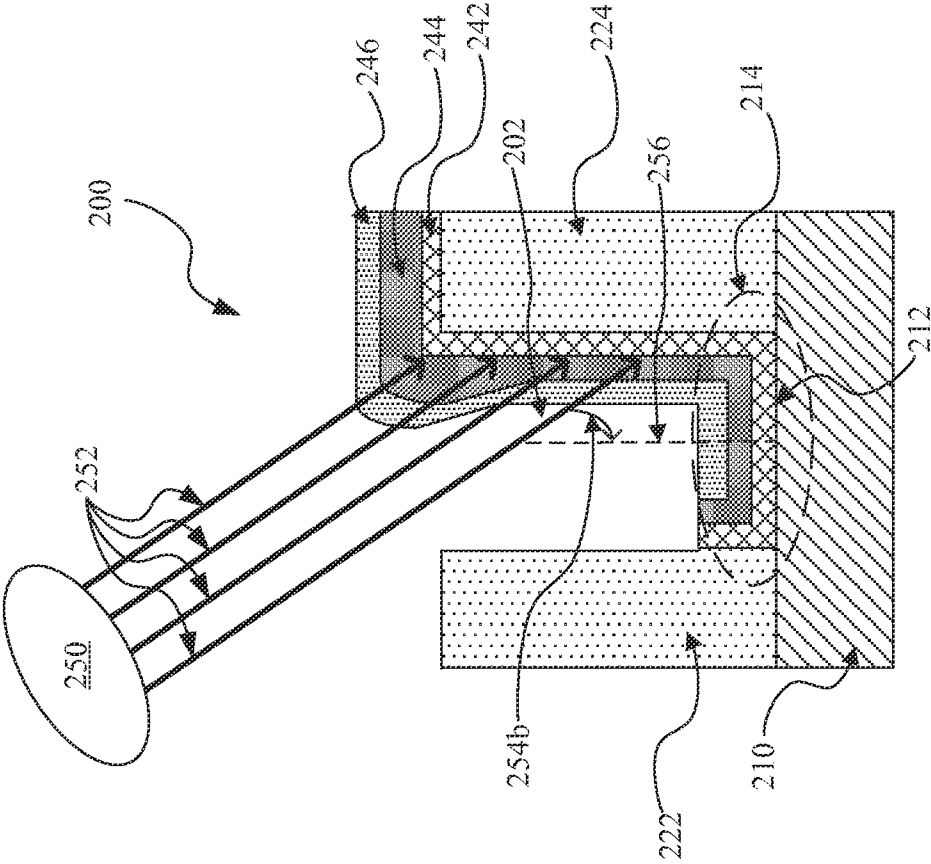


FIG. 2B

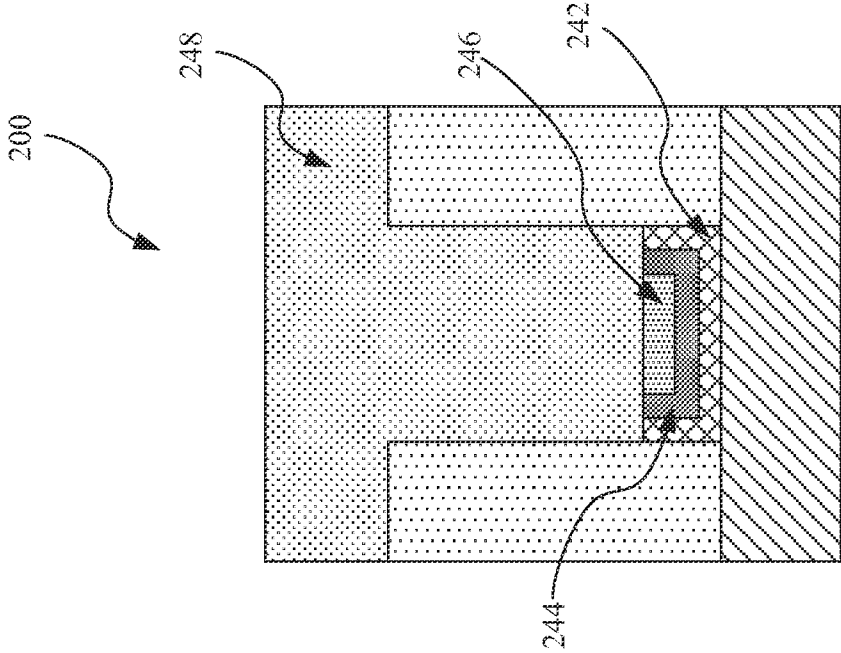


FIG. 2C

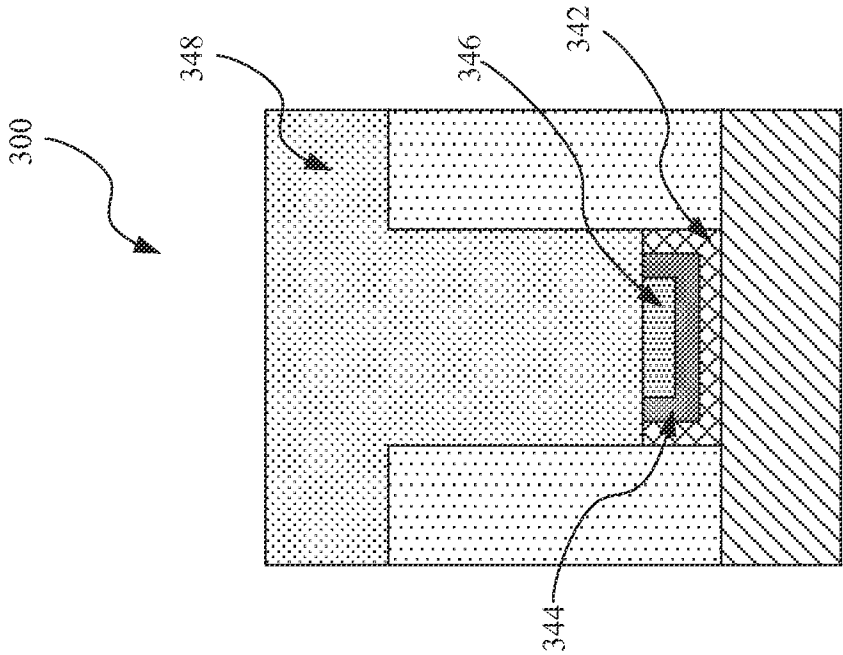


FIG. 3B

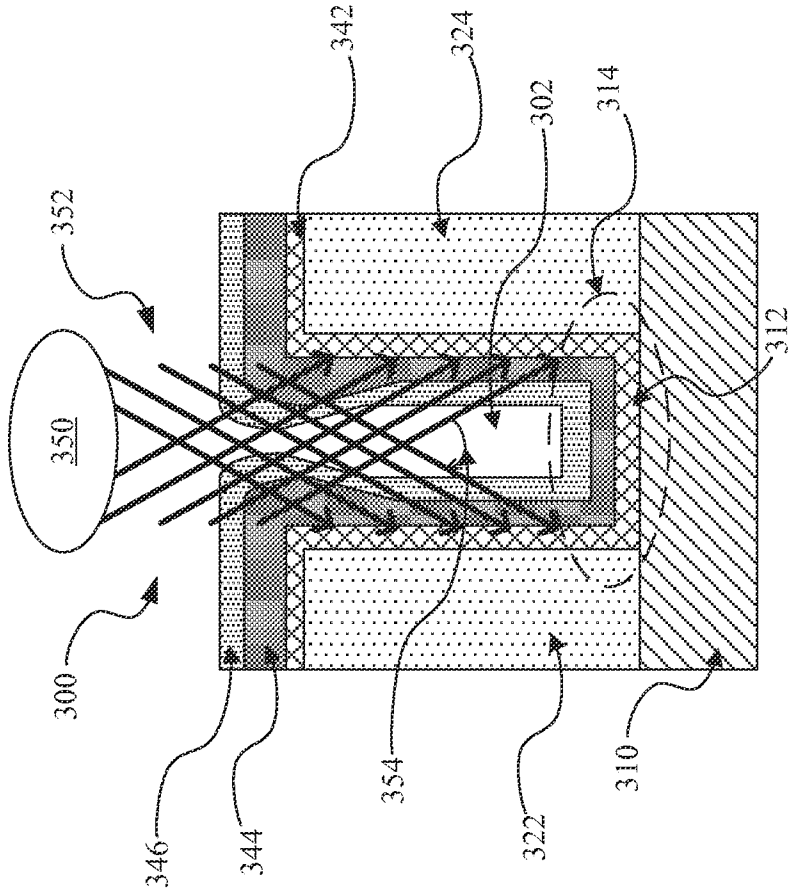


FIG. 3A

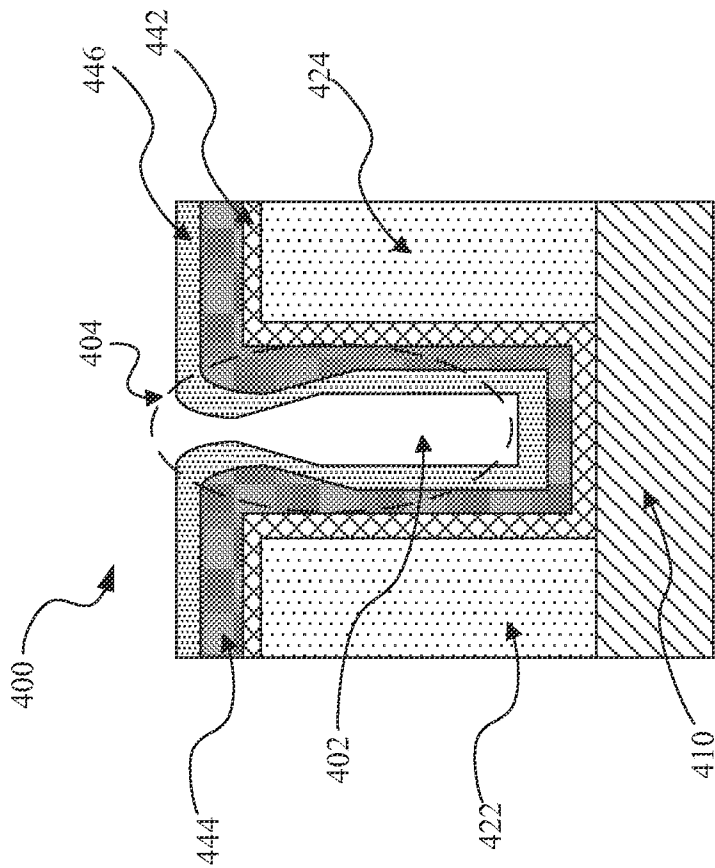


FIG. 4A

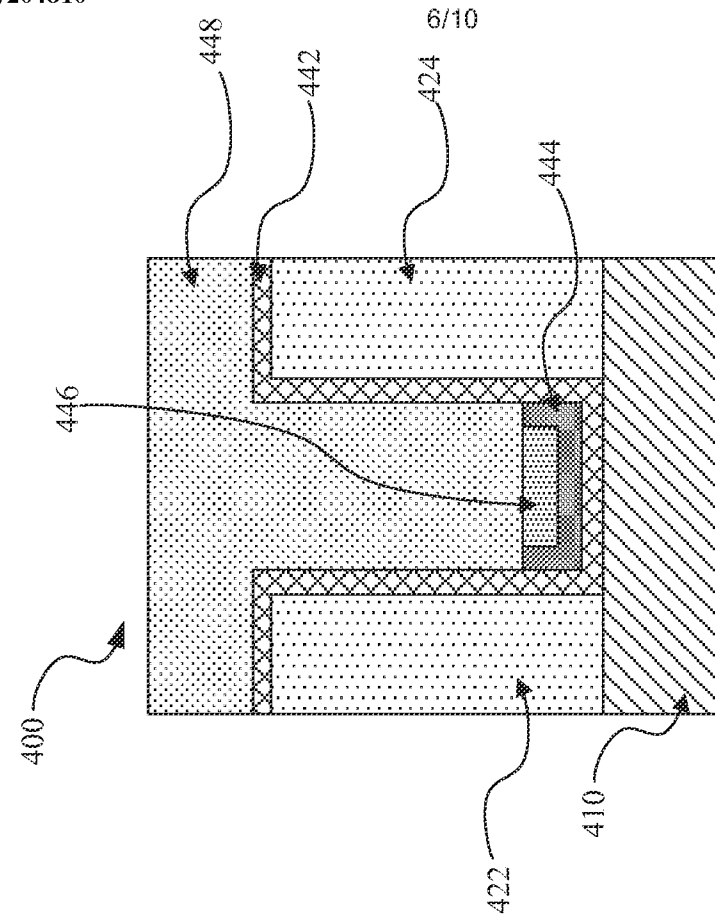


FIG. 4B

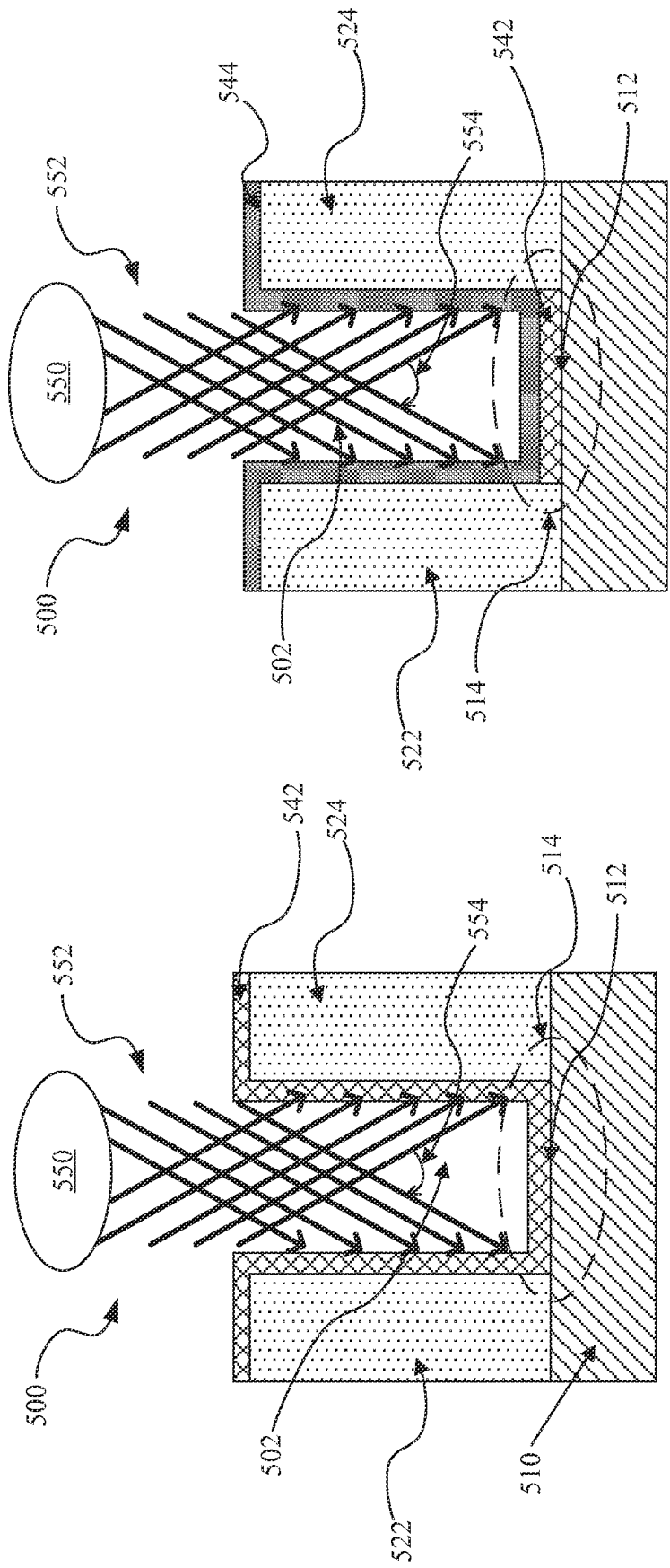


FIG. 5A

FIG. 5B

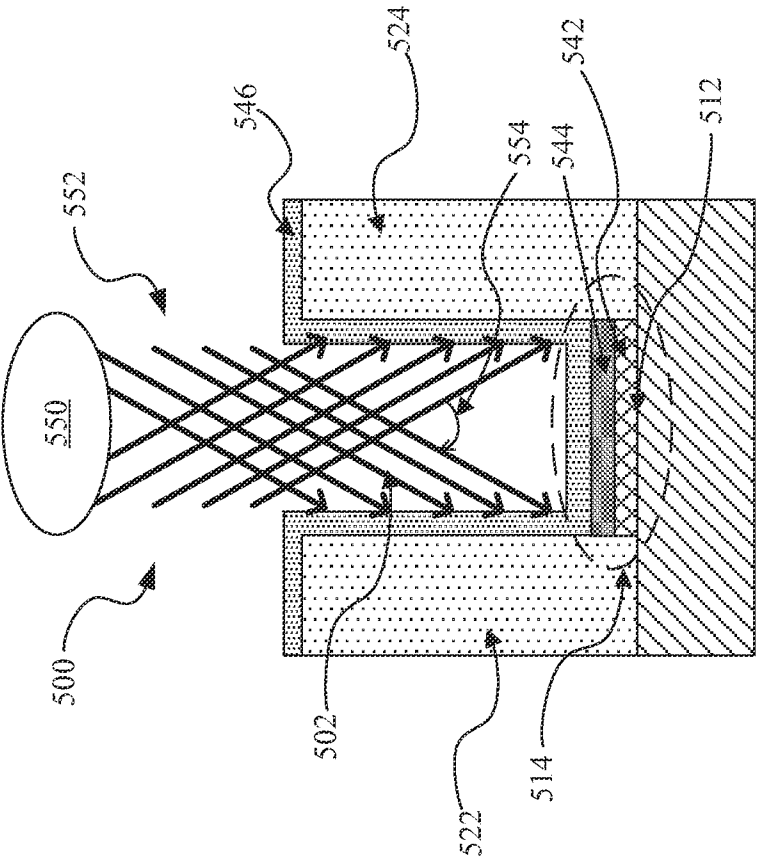


FIG. 5C

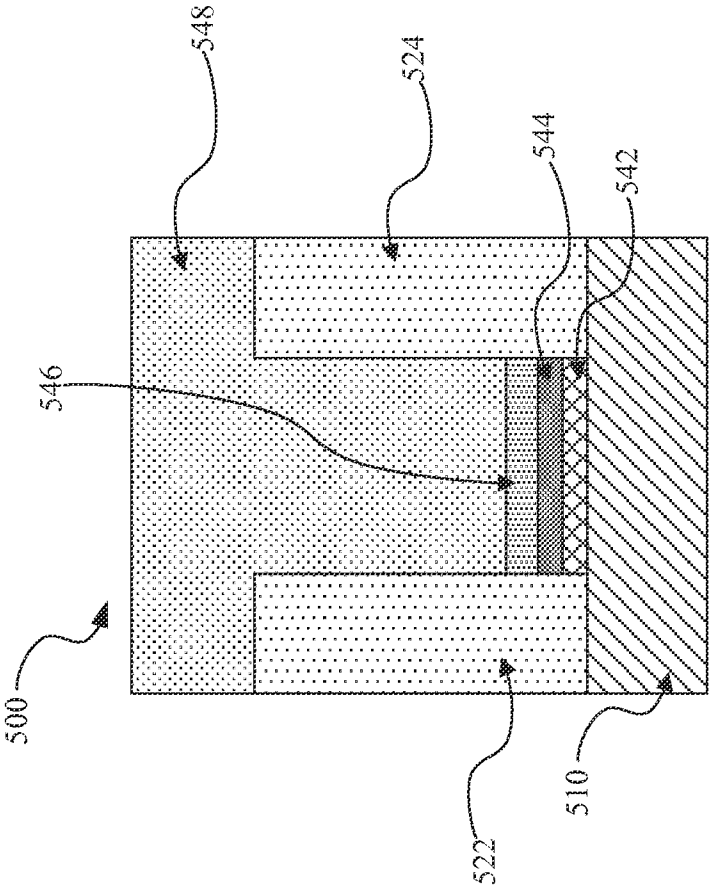


FIG. 5D

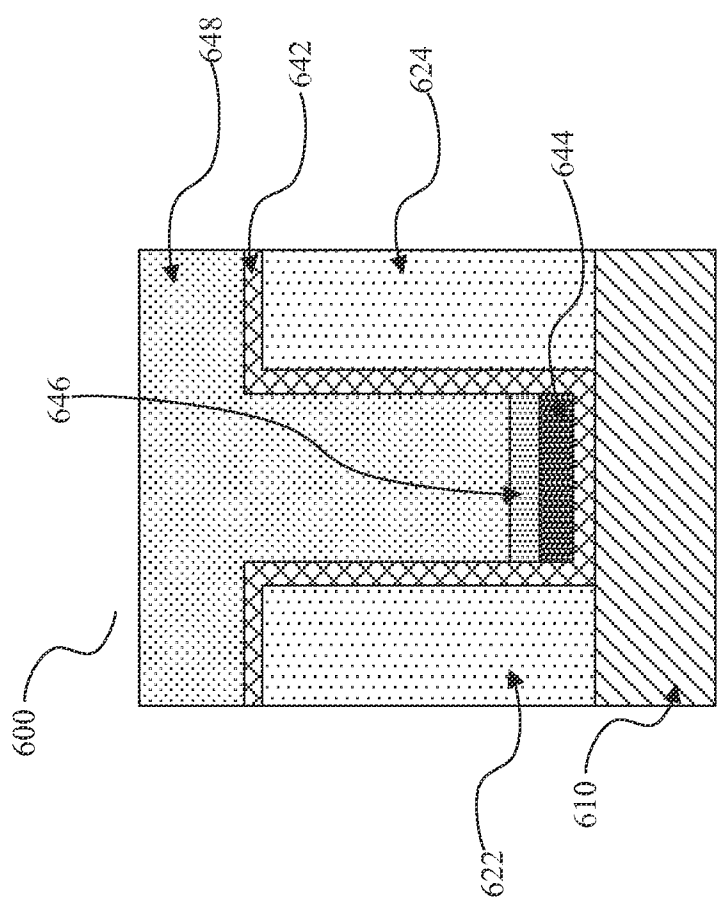
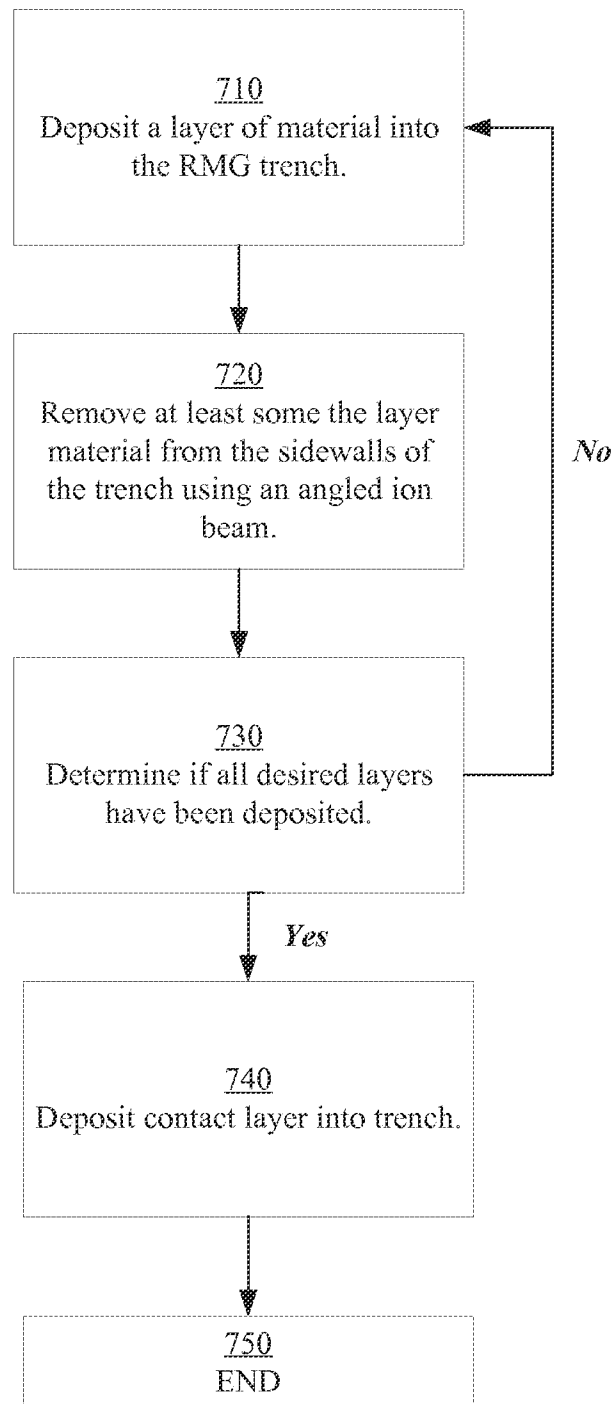


FIG. 6

**FIG. 7**

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/042351**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/336(2006.01)i, H01L 29/78(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/336; H01L 21/28; H01L 21/338; H01L 29/78; G03F 7/00; H01L 21/8242; H01L 29/772

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: trench, sidewall, angle, ion beam, remove and dielectric

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2006-0166419 A1 (KAZUO SHIMOYAMA et al.) 27 July 2006	1,5-7
Y	See paragraphs [0002], [0036]-[0056], claims 1-11 and figures 1A-6B.	2-4,8-13
Y	US 2006-0121678 A1 (JUSTIN K. BRASK et al.) 08 June 2006	2-4,8-13
	See abstract, paragraphs [0025]-[0036] and figures 1i-1q.	
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	See abstract, paragraphs [0060]-[0062] and figure 11.	
A	US 2002-0034708 A1 (HORNG-HUEI TSENG) 21 March 2002	1-13
	See abstract, paragraphs [0023]-[0026] and figures 3-4.	
A	US 2012-0256278 A1 (YING ZHANG et al.) 11 October 2012	1-13
	See abstract, paragraphs [0045]-[0071] and figures 3-7.	



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

28 October 2014 (28.10.2014)

Date of mailing of the international search report

28 October 2014 (28.10.2014)

Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon Metropolitan City, 302-701,
Republic of Korea

Facsimile No. +82-42-472-7140

Authorized officer

CHOI, Sang Won

Telephone No. +82-42-481-8291



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2014/042351

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