Office de la Propriété Intellectuelle du Canada
Un organisme d'Industrie Canada

Canadian Intellectual Property Office
An agency of Industry Canada

CA 2494602 A1 2006/07/08

(21) 2 494 602

(12) DEMANDE DE BREVET CANADIEN
CANADIAN PATENT APPLICATION

(13) A1

(22) Date de dépôt/Filing Date: 2005/01/08

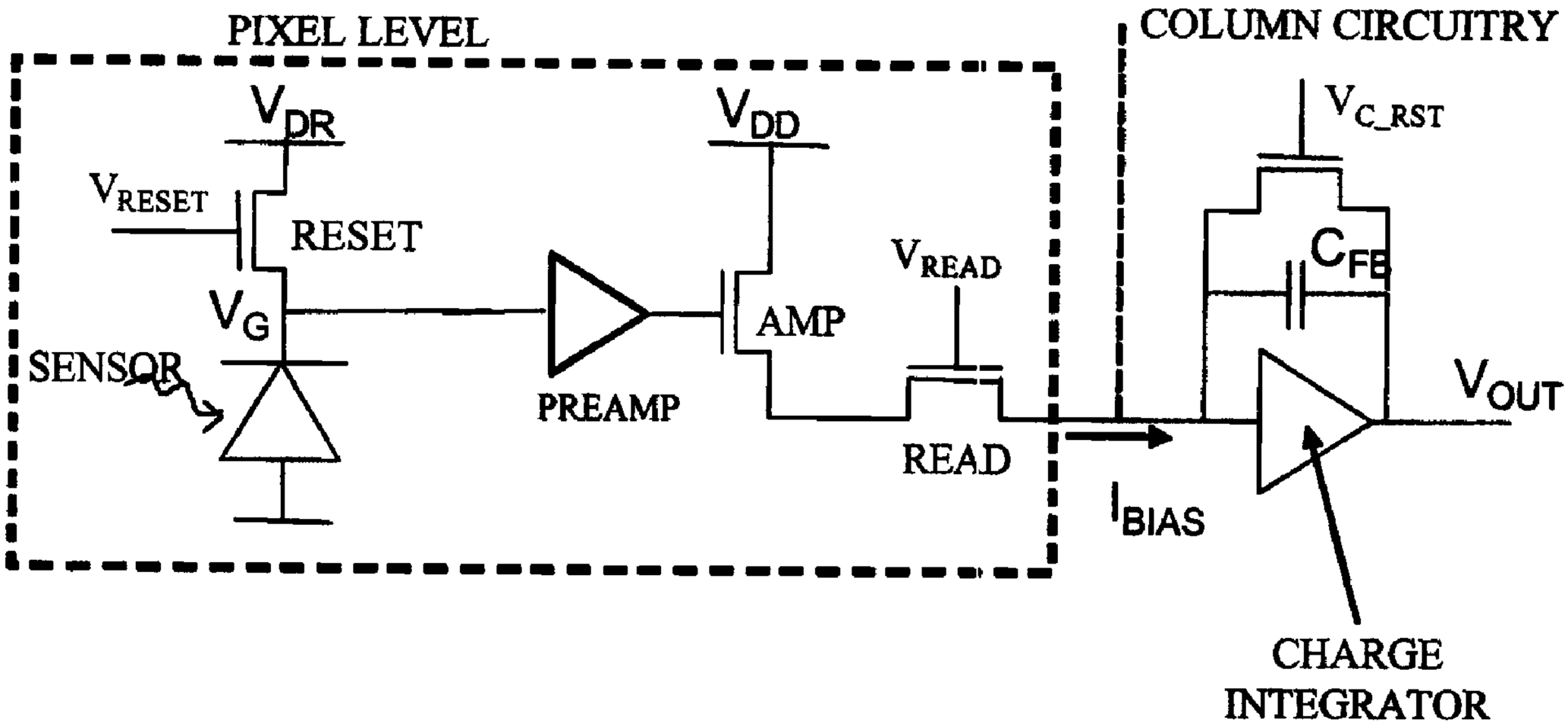
(41) Mise à la disp. pub./Open to Public Insp.: 2006/07/08

(51) Cl.Int./Int.Cl. *H04N 5/335* (2006.01),
H01L 27/146 (2006.01)

(71) Demandeur/Applicant:
KARIM, KARIM S., CA

(72) Inventeur/Inventor:
KARIM, KARIM S., CA

(54) Titre : APPAREIL ET SYSTEME D'IMAGERIE NUMERIQUE
(54) Title: DIGITAL IMAGING APPARATUS AND SYSTEM



DIGITAL IMAGING APPARATUS AND SYSTEM

FIELD OF THE INVENTION

The present invention pertains to the field of digital imaging, and in particular, to digital imaging systems capable of providing large amplification, high dynamic range and fast pixel readout time.

BACKGROUND

Active matrix flat-panel imagers (AMFPIs) have gained considerable significance in digital imaging, and more recently in diagnostic medical imaging applications, in view of their large area readout capability. The pixel, forming the fundamental unit of the active matrix, comprises a detector and readout circuit to efficiently transfer the collected electrons to external electronics for data acquisition. The pixel architecture most commonly used for large area x-ray imaging is the passive pixel sensor (PPS) shown in Figure 1a. Here, a detector, for example, an amorphous selenium (a-Se) based photoconductor or a Cesium Iodide (CsI) phosphor coupled to an amorphous silicon (a-Si:H) p-i-n photodiode, is integrated with a readout circuit comprising an a-Si:H thin-film transistor (TFT) switch. Signal charge is accumulated on the pixel capacitance during an integration cycle and is transferred to an external charge amplifier via the TFT switch during a readout/reset cycle. This capacitance is the p-i-n photodiode capacitance or an integrated storage capacitor for the a-Se photoconductor arrangement. Figure 1b shows a timing diagram for one sequence of operation of a PPS pixel. Cycle **110** and **120** represent the integration cycle and readout/reset cycle, respectively. Other sequences are possible, for example, where double sampling mechanisms are introduced, wherein, double sampling mechanisms are typically used to correct for the effect of non-uniformities within the circuitry. These non-uniformities may comprise process non-uniformities in the form of offsets, and, in the case of a-Si:H technology, non-uniformities in pixel circuit performance due to transistor instability. For example, International Publication Nos. WO9634416 and WO9705659 further disclose flat-panel detectors for radiation imaging using a PPS architecture.

While the PPS has the advantage of being compact and thus amenable to high-resolution imaging, reading a small output signal of the PPS for low input, real-time, large area applications, such as low dose fluoroscopy, requires high performance off-panel column charge amplifiers. These charge amplifiers can potentially introduce noise that degrades the signal-to-noise ratio (SNR) at low signal levels thus undermining the pixel dynamic range. In particular, fluoroscopy can be one of the most demanding applications for flat-panel imaging systems due to the requirement of real-time readout. Real-time x-ray imaging or fluoroscopy is used in many medical interventional procedures where a catheter is moved through the arterial system under x-ray guidance. The technical challenge to be addressed for these types of fluoroscopy is the need for extremely low noise, or alternatively, an increase in signal size before readout. Studies on a-Si:H PPS pixels suggest that an improvement in SNR of an order of magnitude is desirable in order to apply these systems to more advanced imaging applications.

One approach for improved SNR is disclosed in International Publication No. WO02067337 which discloses that the SNR can be increased by employing in-situ, or pixel, amplification via an a-Si:H current-mediated active pixel sensor (C-APS) as depicted in Figure 2a. The gain, linearity and noise results reported show an improvement and indicate that the a-Si:H C-APS, coupled together with an established x-ray detection technology such as a-Se or CsI/p-i-n photodiodes, can meet the stringent noise requirements for digital x-ray fluoroscopy, which is less than 1000 electrons of noise.

To perform amplification of a small, noise vulnerable, input signal, such as in fluoroscopy, the C-APS pixel can be used in three operating cycles; a reset cycle, an integration cycle and a readout cycle. Figure 2b illustrates a timing diagram for a method of operating the C-APS readout circuit employing a double sampling mechanism. In this sequence, during the integration cycle **210**, READ transistor **24** and RESET transistor **21** are kept OFF while AMP_RESET transistor **27** is kept ON. Photons incident upon detector **22** result in the generation of electron-hole pairs that discharge, or charge, the capacitance $C_{DETECTOR}$ at node **201** and thus reduce, or increase, the voltage at node **201**, V_G, by an amount ΔV_G. $C_{DETECTOR}$ mainly comprises the detector **22** capacitance and any storage capacitors that may be used.

The readout cycle **220** follows the integration cycle **210** and during this cycle, READ transistor **24** is turned ON, RESET transistor **21** is kept OFF and the AMP_RESET transistor **27** is turned OFF, resulting in a current, $I_{BIAS} \pm \Delta I_{BIAS}$, that is proportional to $V_G \pm \Delta V_G$ flowing in the AMP transistor **23** and READ transistor **24** branch. The current, $I_{BIAS} \pm \Delta I_{BIAS}$ is then integrated by charge amplifier **25** to obtain and store an output voltage, V_{OUT1}, on the amplifier feedback capacitor **26**.

The reset cycle **230** occurs subsequent to the readout cycle **220** where RESET transistor **21** is pulsed ON and $C_{DETECTOR}$ is charged, or discharged, to reset the voltage at node **201** to V_G while RESET transistor **21** is ON. During this reset cycle, READ transistor **24** is turned OFF and AMP_RESET transistor **27** is turned ON.

To perform the double sampling operation, an additional read cycle **240** follows the reset cycle **230** where again READ transistor **24** is turned ON, RESET transistor **21** is turned OFF and AMP_RESET transistor **27** is turned OFF. I_{BIAS} is integrated by charge amplifier **25** to obtain and store an output voltage, V_{OUT2}, on feedback capacitor **26**. Subtracting V_{OUT1} from V_{OUT2} yields a ΔV_{OUT} that can be free from non-uniformities and is proportional to ΔV_G.

ΔI_{BIAS} is proportional to ΔV_G and is given as:

$$\Delta I_{BIAS} = g_m \Delta V_G$$

where g_m is the transconductance of the AMP transistor **23** and READ transistor **24** readout circuit branch.

The C-APS produces a charge gain, G_i, to amplify the noise vulnerable input signal. The G_i for the C-APS is given as:

$$G_i = (g_m T_S)/C_{DETECTOR}$$

where T_S is the amount of time I_{BIAS} and ΔI_{BIAS} are integrated on the feedback capacitor **26**. As indicated by the equation above, G_i is programmable via g_m, T_S and the choice of an appropriate $C_{DETECTOR}$.

A concern with the C-APS circuit is the presence of a small-signal linearity constraint on the x-ray input signal. Using such a pixel amplifier for real-time fluoroscopy, where the exposure level is small, is feasible since the voltage change at the amplifier input is also small and in the order of mV. However, in applications such as digital chest radiography, mammography or higher dose fluoroscopy, the voltage change at the amplifier input can be much larger due to the larger x-ray exposure levels, which cause the C-APS pixel output to be non-linear thus reducing the pixel dynamic range. Another consequence of a non-linear pixel transfer function is that the standard double sampling mechanism cannot be implemented in hardware due to this non-linearity.

Furthermore, an additional shortcoming of the G-APS pixel is that the presence of a large output current, causes the external or off-panel charge amplifier to saturate. Large pixel output currents can also occur when a large charge gain is required since g_m is proportional to I_{BIAS}.

Another approach disclosed in International Publication No. WO02067337 reports a near-unity gain pixel amplifier, namely, an a-Si:H voltage-mediated active pixel sensor (V-APS). A V-APS architecture is illustrated in Figure 3. READ transistor **34**, AMP transistor **33** and RESET transistor **31** are components of the V-APS pixel and function in a similar manner as in the C-APS pixel. Resistive load **35** is connected to the pixel output node to convert the current in the AMP transistor **33** and READ transistor **34** branch into an output voltage. Resistive load **35** can comprise a resistor load device or a transistor load device. The input signal voltage V_G is translated to a pixel output voltage V_{OUT} with a near unity gain. The V-APS, like the C-APS, can be used in three operating cycles; a reset cycle, an integration cycle and a readout cycle. Like the C-APS, double sampling mechanisms can be applied to the V-APS to correct for the effect of non-uniformities within the circuitry. A problem with the V-APS architecture is that essentially no gain is provided to the input signal. In addition, with current state of the art amorphous silicon technology, it is difficult to achieve real time readout using this architecture when large column bus capacitances are charged and discharged.

Therefore, a pixel design that is able to achieve real-time readout as well as capable of sensing a wider range of input signals is necessary while achieving high gain to detect small noise-vulnerable signals with a large signal-to-noise ratio.

This background information is provided for the purpose of making known information believed by the applicant to be of possible relevance to the present invention. No admission is necessarily intended, nor should be construed, that any of the preceding information constitutes prior art against the present invention.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a digital imaging apparatus and system. In accordance with an aspect of the present invention, there is provided a digital imaging apparatus comprising: a detector for generating a first signal in response to photons incident thereupon; and readout circuitry coupled to said detector for receiving said first signal and for generating a second signal representative of an amplified first signal, said readout circuitry including two or more amplifying stages; wherein said second signal is subsequently output from said digital imaging apparatus.

In accordance with another aspect of the present invention, there is provided a digital imaging apparatus comprising: a detector for generating a first signal in response to photons incident thereupon; and multimode readout circuitry coupled to said detector for receiving said first signal and for generating a second or higher signal representative of said first signal, said multimode readout circuitry switchable between two or more modes of operation, a desired mode of operation determined based on characteristics of said first signal, said readout circuitry including two or more amplifying stages; wherein said second signal is subsequently output from said digital imaging apparatus.

BRIEF DESCRIPTION OF THE FIGURES

Figure 1 illustrates a passive pixel sensor (PPS) according to the prior art.

Figure 1b illustrates an example of a timing diagram for the PPS of Figure 1a.

Figure 2a illustrates a current mediated active pixel sensor (C-APS) according to the prior art.

Figure 2b illustrates an example of a timing diagram for the CAPS of Figure 2a.

Figure 3 illustrates a voltage mediated active pixel sensor (V-APS) according to the prior art.

Figure 4a illustrates a two stage amplifier pixel as one embodiment of the present invention.

Figure 4b illustrates a timing diagram for the embodiment of Figure 4a.

Figure 4c illustrates three possible embodiments for the first stage (PREAMP) of the two stage amplifier pixel embodiment shown in Figure 4a.

Figure 5a illustrates a four transistor two stage amplifier pixel, multi mode implementation of one embodiment of the present invention.

Figure 5b illustrates a timing diagram for the embodiment of Figure 5a.

Figure 6a illustrates a three transistor two stage amplifier pixel, multi mode implementation of one embodiment of the present invention.

Figure 6b illustrates a timing diagram for the embodiment of Figure 6a.

Figure 7a illustrates a three transistor two stage amplifier pixel, multi mode implementation of one embodiment of the present invention.

Figure 7b illustrates a timing diagram for the embodiment of Figure 7a.

Figure 8a illustrates a three transistor two stage amplifier pixel with current subtraction for higher gain, implementation of one embodiment of the present invention.

Figure 8b illustrates a timing diagram for the embodiment of Figure 8a.

Figure 9a illustrates a four transistor two stage amplifier pixel with current subtraction for higher gain, multi mode implementation of one embodiment of the present invention.

Figure 9b illustrates a timing diagram for the embodiment of Figure 9a.

DETAILED DESCRIPTION OF THE INVENTION

Definitions

The term "detector" is used to define a device that converts photons of electromagnetic radiation to electrical charge. This radiation may be of any wavelength or range of wavelengths from any portion of the electromagnetic spectrum. For example, x-ray photons, ultraviolet photons, infrared photons, or any other photons as would be readily understood may be converted to electrical charge by such a device.

The term "sensor" is used to define the combination of one or more detectors and readout circuitry.

The term "unity gain" is used to define current or voltage gain, such that the output signal obtained as a result of the gain being applied to an input signal has the same magnitude or a different magnitude than the input signal.

Unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs.

The present invention provides digital imaging architectures comprising detectors coupled to readout circuitry, wherein the readout circuitry is capable of providing large amplification via two or more on-pixel amplification stages to small, noise sensitive input signals to improve their noise immunity, as well as providing a fast pixel readout time. An embodiment of the present invention is shown in Figure 4 where each detector generates photo-carriers in response to photons incident upon the detector and produces charge, which results in a voltage change across the detector. To perform amplification of a small, noise

vulnerable, input signal, such as in fluoroscopy, the pixel can be used in three operating cycles; a reset cycle, an integration cycle and a readout cycle. The voltage change at the detector produces the input signal to the first amplification stage (marked PREAMP on Figure 4a). Some alternatives for the first amplification stage are shown in Figure 4c although it will be evident to a worker skilled in the art that others are possible and can easily be substituted. The amplified output of the first stage forms the input to the second stage which converts this input voltage into an output current. The output current of the second stage is integrated on the charge amplifier during the readout cycle as shown in Figure 4b to form a pixel output voltage that is a representative of the photon generated charge on the detector. Thus, the present invention provides a digital imaging system with a very large gain due to two or more on-pixel amplification stages for detection of noise vulnerable signals.

In one embodiment of the present invention as shown in Figure 5, the readout circuitry functions in particular modes, the use of which can depend on characteristics of the input signals transferred to the readout circuitry from the detectors, or can depend on the characteristics of the output signal required from the readout circuitry. For example, when the input signal has a particular magnitude the readout circuitry can function in a first mode in which the input signal can be amplified to a measurable level, and when the input signal has another magnitude, the readout circuitry can function in an alternate mode in which the input signal can be read out with a different or no amplification. Here, the on-pixel PREAMP block, and RESET, AMP and READ2 transistors provide the ability via a reset, integrate and readout cycle to amplify the input signal while the READ1 transistor may be used for unity gain readout.

For implementations of the present invention in applications such as low dose fluoroscopy, high dose fluoroscopy chest radiography and mammography, two modes can provide a sufficient dynamic range for these x-ray detection techniques, or other detection techniques as would be readily understood. However, additional modes can be implemented to provide various levels of amplification to the input signal, for example, three or more modes of operation of the readout circuitry can be implemented. Furthermore, more than one mode can be used to read out the same input signal. In some embodiments, selection of the mode of operation of the readout circuitry may be actuated manually or automatically. For example, an automated switching system can comprise a feedback circuit enabling automatic selection of an appropriate mode of operation of the readout circuitry, or a pre-programmed sequence

to enable automatic selection of an appropriate mode of operation of the readout circuitry, or any other means of enabling automatic selection of an appropriate mode of operation of the readout circuitry as would be readily understood. Thus the digital imaging apparatus and system of the present invention can provide a large dynamic range of detection that can be capable of amplifying sensitive input signals from a detector to improve the noise immunity of the input signals to external noise sources as well as capable of reading larger signals with little or no amplification, both with a fast pixel readout time.

Figure 6 is an embodiment with similar multi-mode readout functionality as Figure 5 where the RESET transistor is removed from the pixel and the READ1 transistor has been multiplexed to provide both a unity gain readout mechanism and to act as a reset switch for the amplification mode readout. Here, the on-pixel PREAMP block, AMP and READ2 transistors provide the ability via reset, integrate and readout cycles to amplify the input signal while the READ1 transistor is used via reset, integrate and readout cycles for unity gain readout.

Figure 7 is another embodiment with similar multi-mode readout functionality as Figure 5 where the on-pixel PREAMP block, RESET, AMP and READ transistors driving the charge amplifier provide the ability via a reset, integrate and readout cycle to amplify the input signal while the PREAMP block, RESET, AMP and READ transistors driving the voltage amplifier provide the ability via a reset, integrate and readout cycle to readout larger input signals.

Figure 8 is another embodiment with similar charge amplification readout functionality as Figure 4 with an additional independently programmable current source in the readout circuitry that plays a role in effectively reducing the total amount of current flowing through parts of the readout circuitry which can saturate, for example, when a large charge gain is used. Here, the on-pixel PREAMP block, RESET, AMP and READ1 transistors driving the charge amplifier provide the ability via a reset, integrate and readout cycle to amplify the input signal.

Figure 9 is another embodiment with similar multi-mode readout functionality as Figure 5 with an additional independently programmable current source in the readout circuitry that plays a role in effectively reducing the total amount of current flowing through parts of the readout circuitry which can

saturate, for example, when a large charge gain is used Here, the on-pixel PREAMP block, RESET, AMP and READ1 transistors driving the charge amplifier provide the ability via a reset, integrate and readout cycle to amplify the input signal while the READ2 transistor is used for unity gain readout.

Each pixel typically comprises one detector, however it is contemplated that more than one detector may be present within each pixel. In addition, the readout circuitry may be partially present within the on-panel pixels and partially present off the imaging panel, or substantially present on the imaging panel. The imaging panel may be rigid, for example comprising a glass substrate, or flexible, for example comprising a flexible plastic or flexible metal substrate. In addition, the present invention may comprise more than one imaging panel. For example, one panel may comprise some parts of the sensor and another panel may comprise other parts of the sensor. Furthermore, the pixel electronics may be fabricated on a single chip or on multiple chips. Furthermore, the readout circuitry present within a pixel may be physically located in the same plane as the detector or this readout circuitry may be embedded under, or fabricated above, the detector to provide a high fill factor.

Portions of the readout circuitry that are common for a column, row, or group of pixels may be multiplexed between these pixels in an array. Thus it would be readily understood by a worker skilled in the art, that in the various embodiments of the present invention, common column, row or group readout circuitry may be multiplexed between pixels, and that this may require additional circuitry, for example switching circuits or multiplexing circuits. In addition, multiplexers may also be used to reduce the readout circuit complexity by decreasing the total number of amplifiers, for example, required for a column, row, or group of pixels. Furthermore, common column or row readout circuitry may also be implemented such that the common readout circuitry is individual to each pixel. It would also be understood that the pixels of various embodiments may be implemented in arrays of any size. Furthermore, where portions of readout circuitry have been identified as being shared by one or more columns of pixels, it should be understood that the circuitry may equivalently be shared by one or more rows of pixels or one or more other groups of pixels.

Embodiments of the present invention can be operated with various switching and timing sequences. For example, where a double sampling technique is used, the transistor switching and timing may vary from a

sequence in which no double sampling technique is used. In various embodiments of the present invention described herein, related transistor switching and timing cycles and sequences are provided as examples, and numerous other cycles and sequences are possible as would be obvious to a worker skilled in the art.

The detector may be any type of detector, for example, solid-state photodetectors such as a-Si:H, amorphous selenium or cadmium zinc telluride based detectors or any other appropriate detector. In addition, other direct detection based detectors such as molybdenum Schottky diodes, as well as indirect detection detectors such as those comprising phosphors for example gadolinium oxysulfide detectors, or caesium iodide detectors, integrated with a-Si:H p-i-n photodiodes may also be used. Any other types of detectors for x-ray detection may further be used as would be readily understood by a worker skilled in the art. The transistors used in various embodiments of the present invention may be amorphous silicon (a-Si:H) thin-film transistors (TFTs), poly-crystalline silicon TFTs, micro-crystalline silicon TFTs, nano-crystalline silicon TFTs, crystalline silicon transistors, or any other similar device as would be readily understood by a worker skilled in the art. In further embodiments, radiation in any region of the electromagnetic spectrum may be detected using the present invention with the selection of detectors, and devices for the readout circuitry being made in order that an appropriate portion of the electromagnetic spectrum can be detected as would be readily understood by a worker skilled in the art.

As would be readily understood by a worker skilled in the art, the present invention may be applied to any digital imaging application. For example, the present invention may be applied to medical imaging, x-ray inspection systems such as in the inspection of aircraft wings, security systems such as screening of luggage at airports, non-destructive material tests, radiography or optical imaging, as well as other forms of digital imaging applications as would be readily understood.

The embodiments of the invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

I CLAIM:

1. A digital imaging apparatus comprising:

   a) a detector for generating a first signal in response to photons incident thereupon; and

   b) readout circuitry coupled to said detector for receiving said first signal and for generating a second signal representative of an amplified first signal, said readout circuitry including two or more amplifying stages;

wherein said second signal is subsequently output from said digital imaging apparatus.

2. A digital imaging apparatus comprising:

   a) a detector for generating a first signal in response to photons incident thereupon; and

   b) multimode readout circuitry coupled to said detector for receiving said first signal and for generating a second or higher signal representative of said first signal, said multimode readout circuitry switchable between two or more modes of operation, a desired mode of operation determined based on characteristics of said first signal, said readout circuitry including two or more amplifying stages;

wherein said second signal is subsequently output from said digital imaging apparatus.

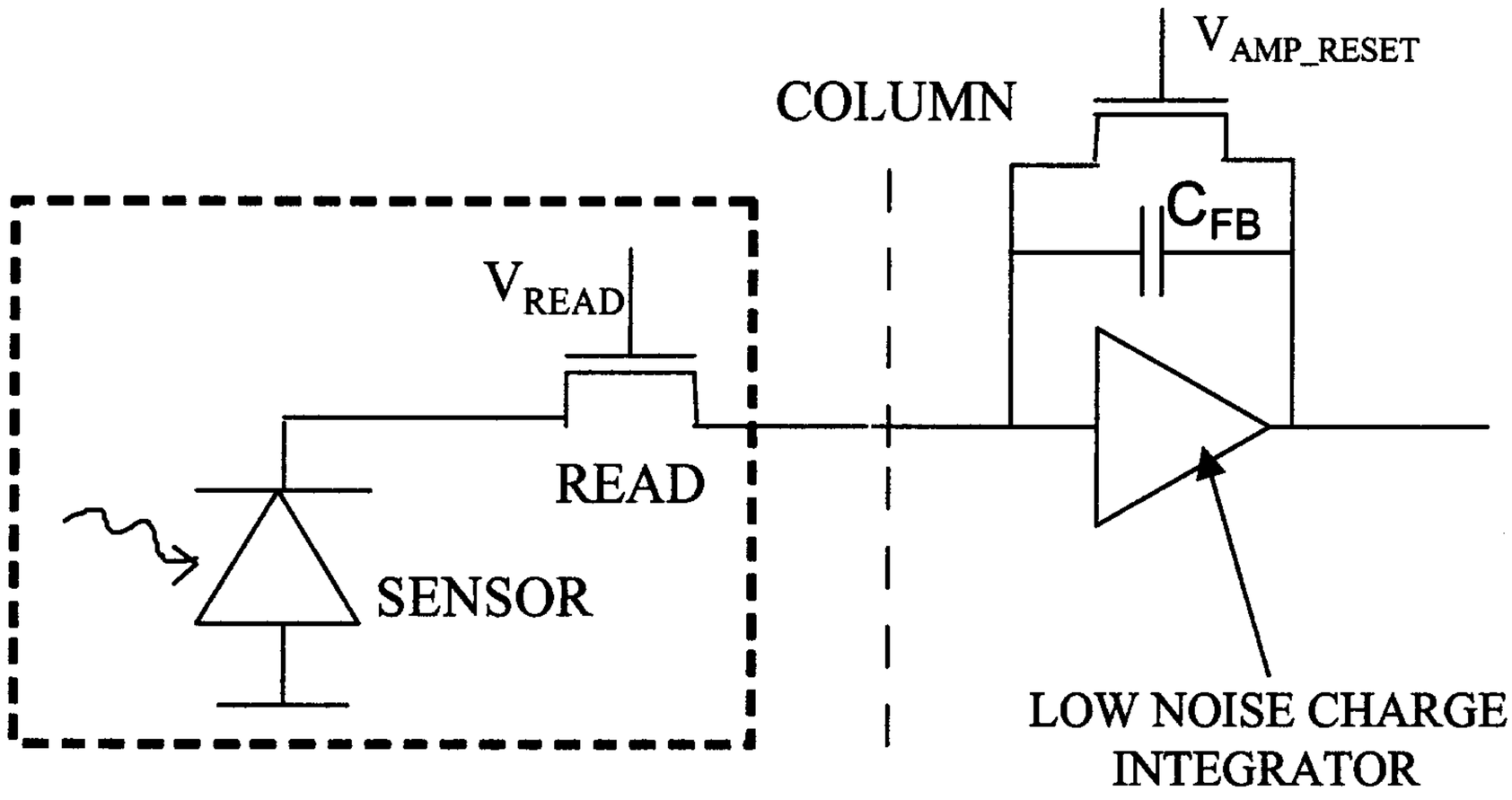


Figure 1a (Prior Art)

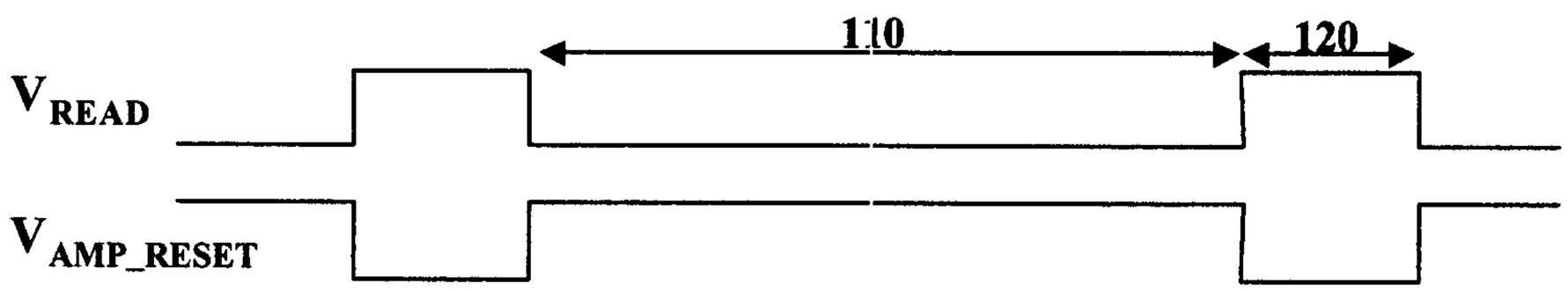


Figure 1b

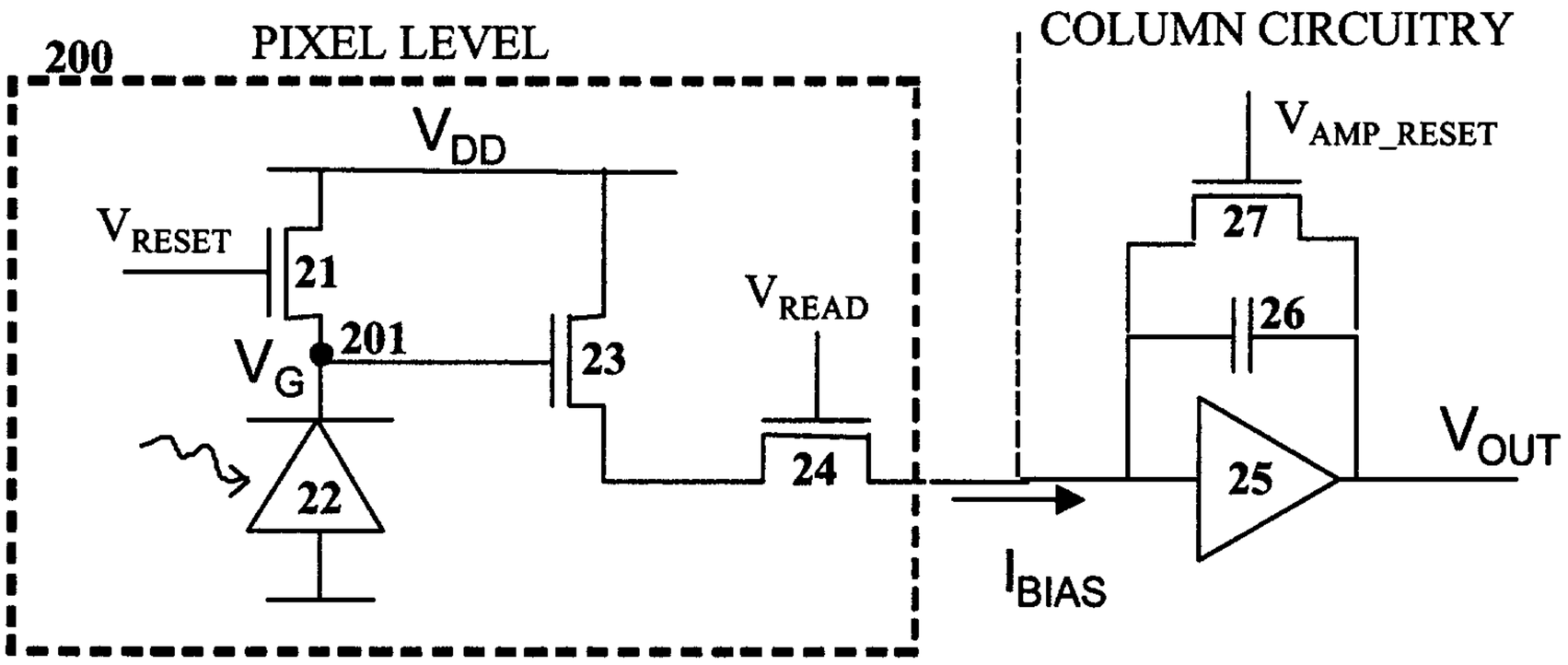


Figure 2a (Prior Art)

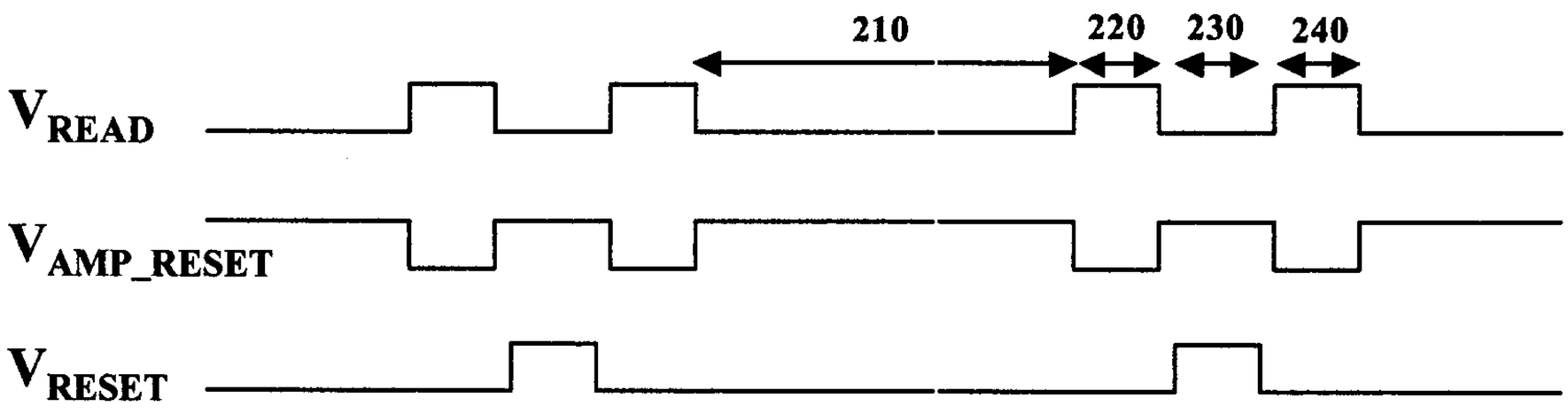


Figure 2b

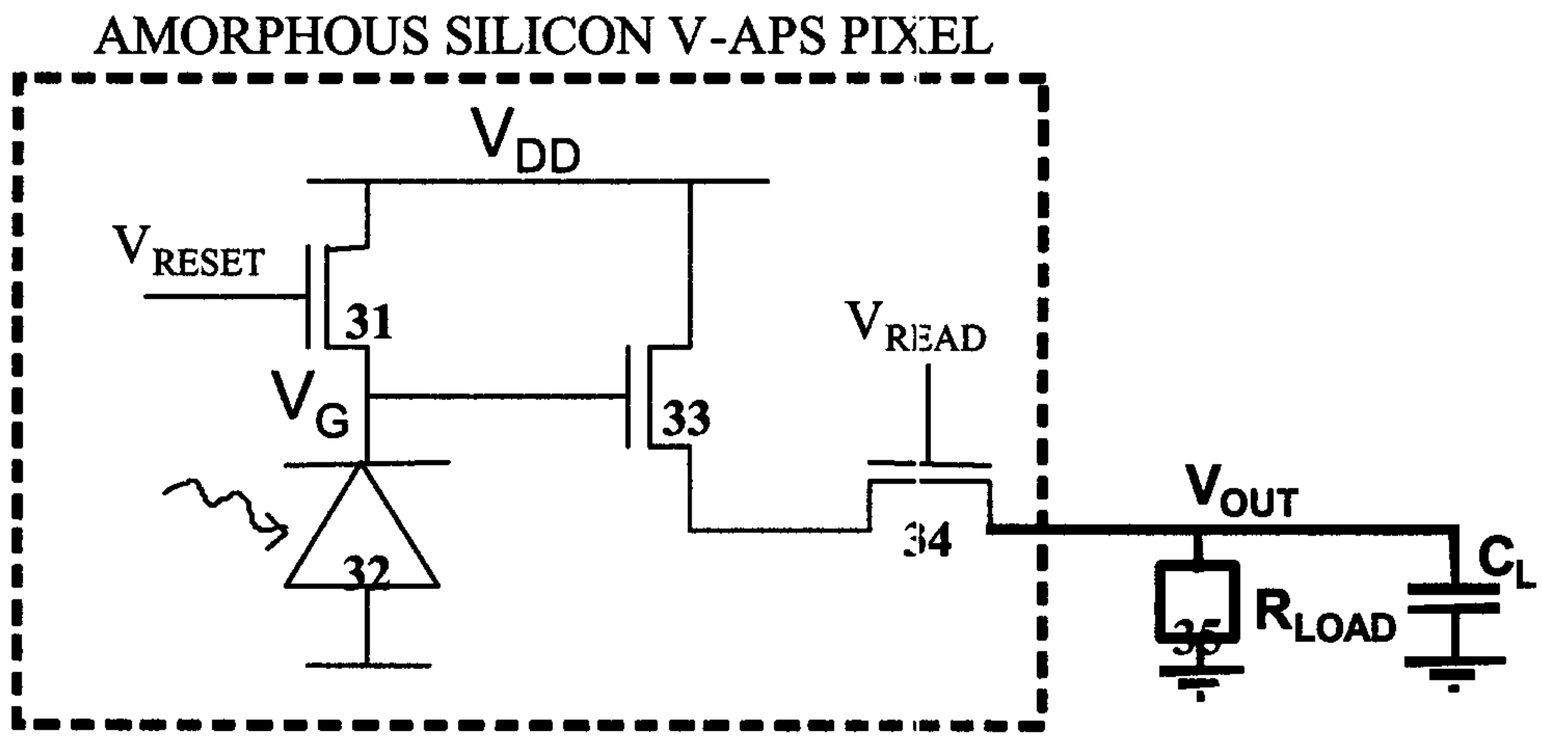


Figure 3 (Prior Art)

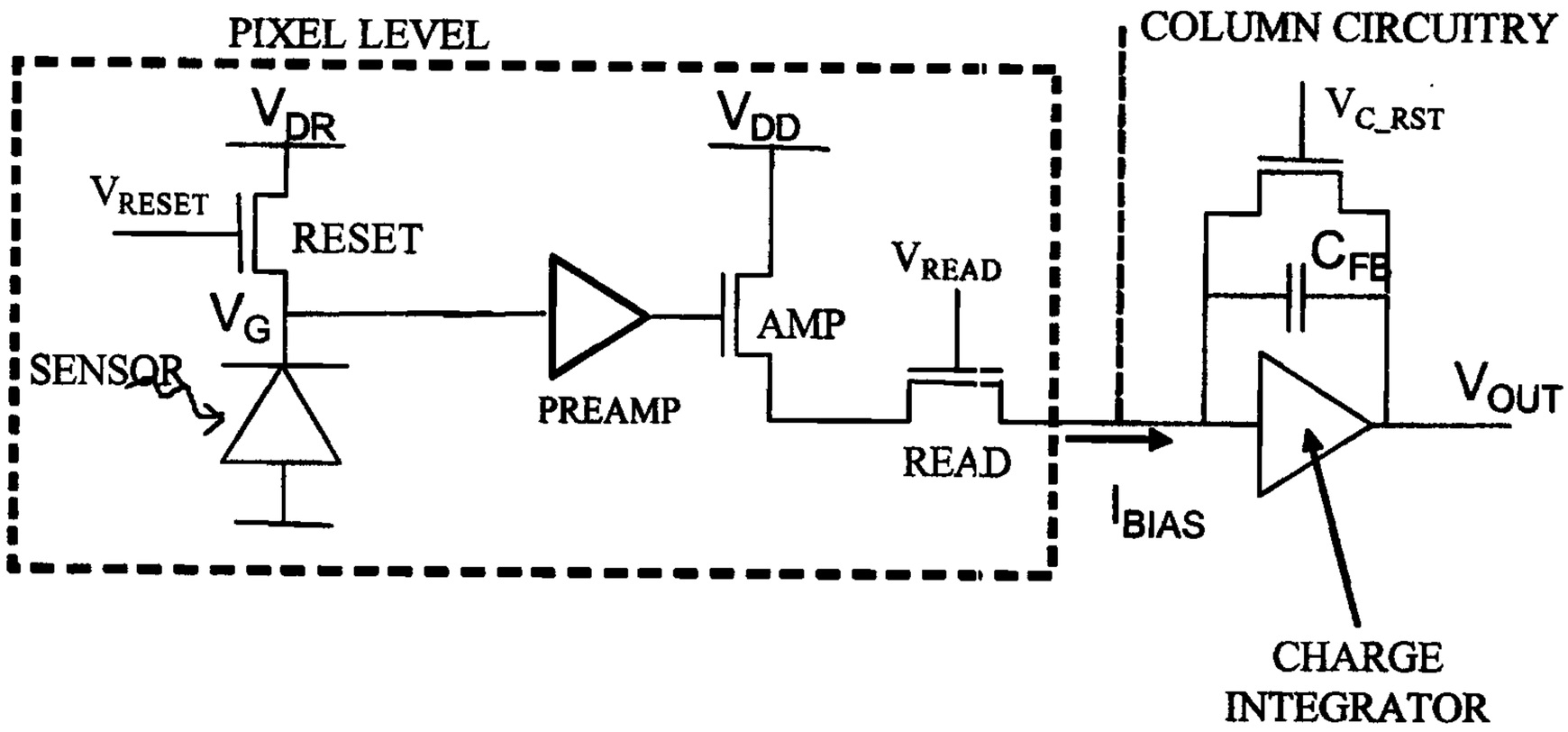


Figure 4a

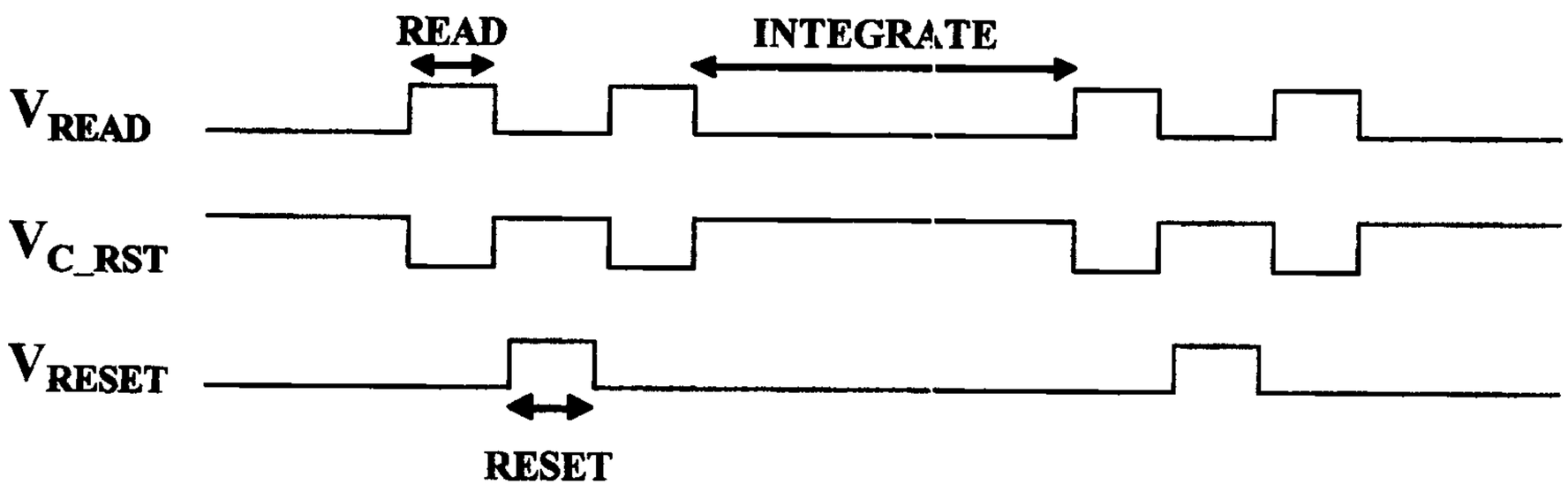


Figure 4b

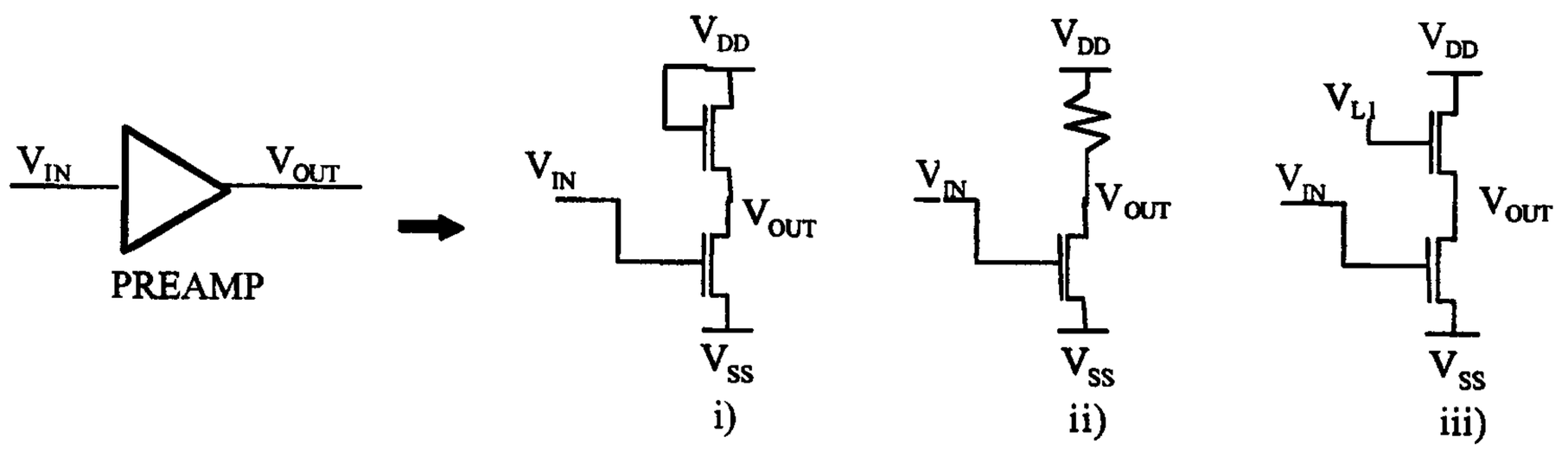


Figure 4c

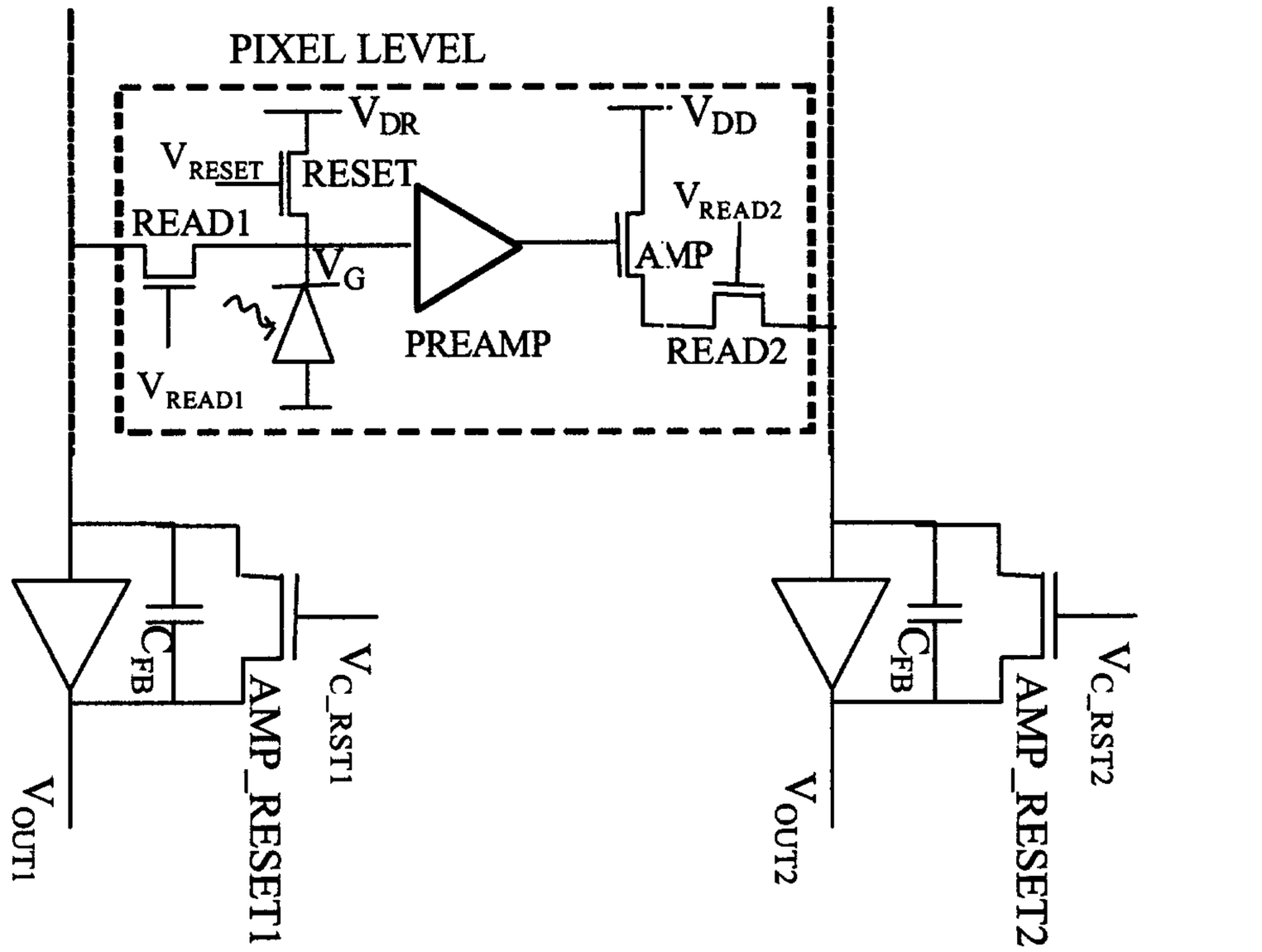


Figure 5a

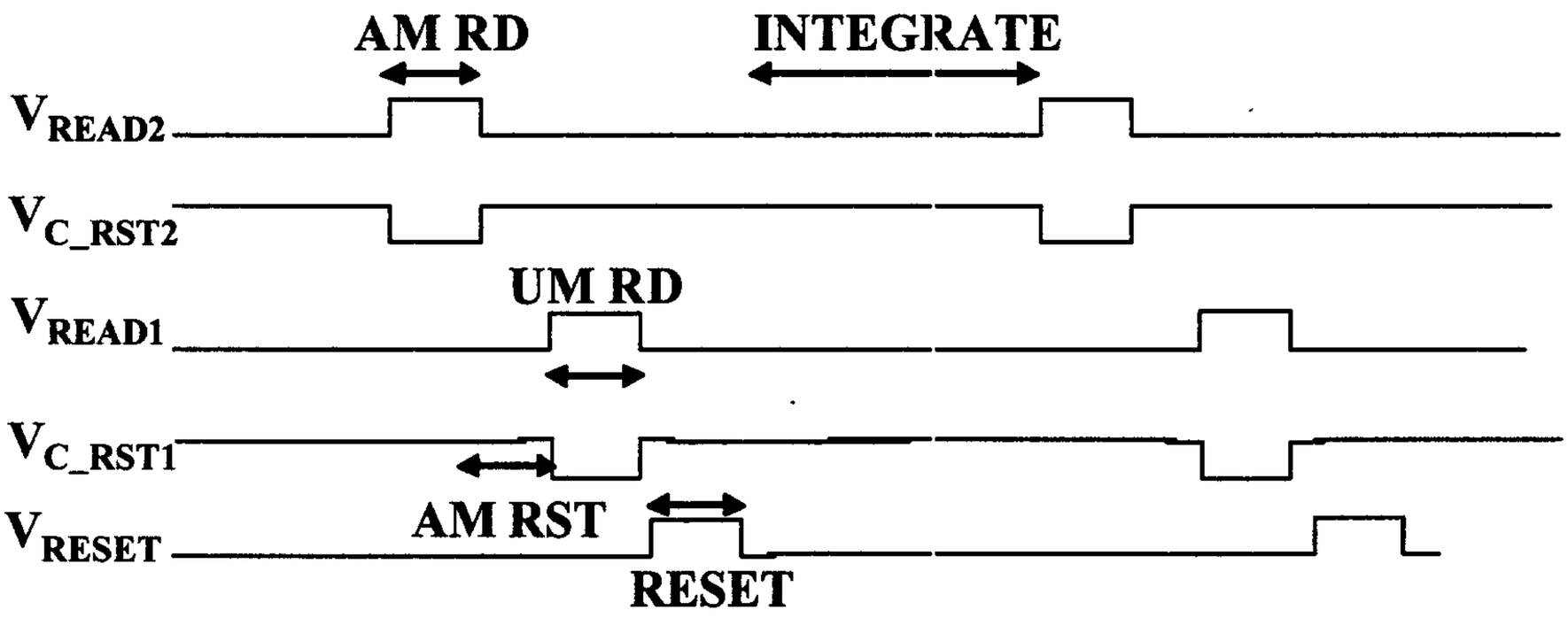


Figure 5b

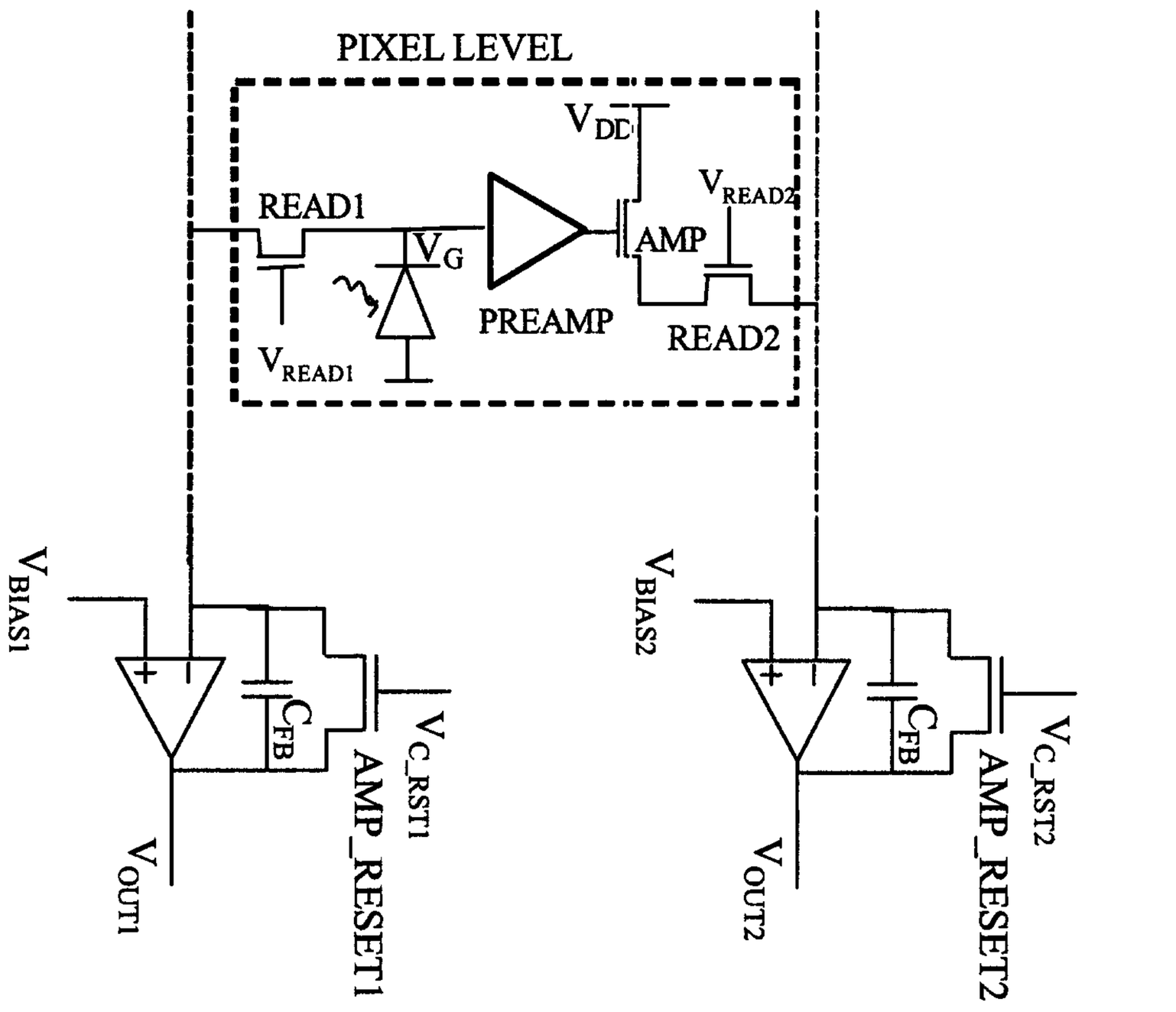


Figure 6a

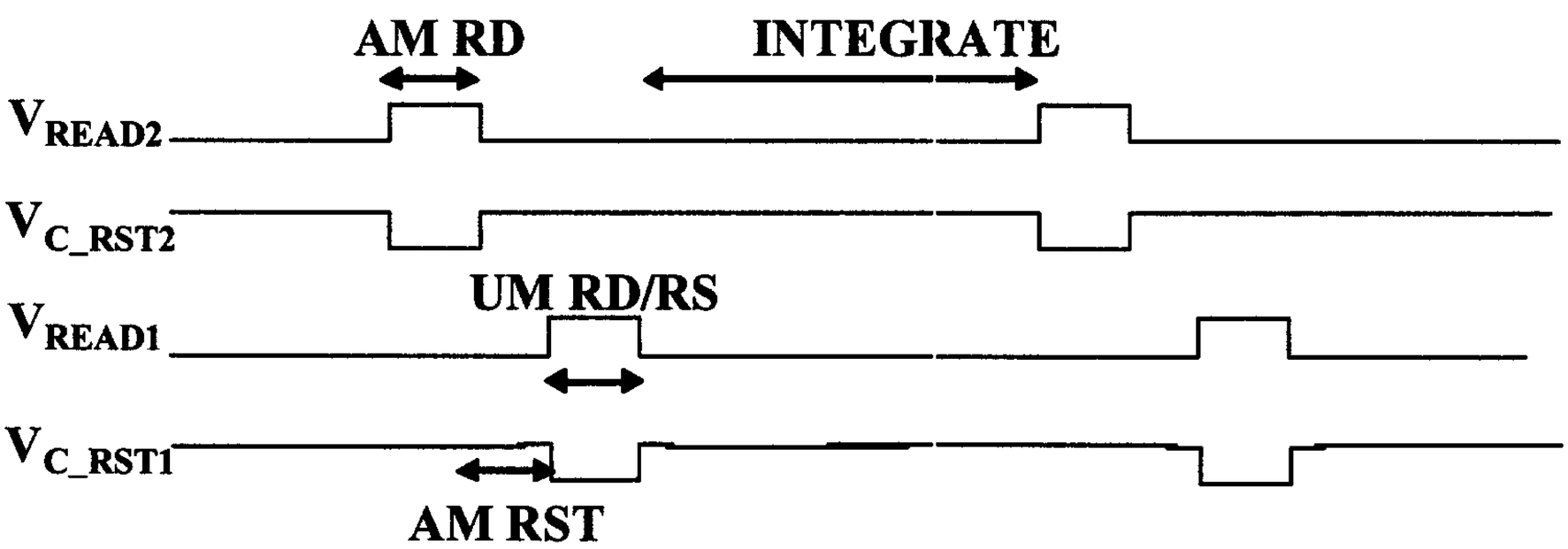


Figure 6b

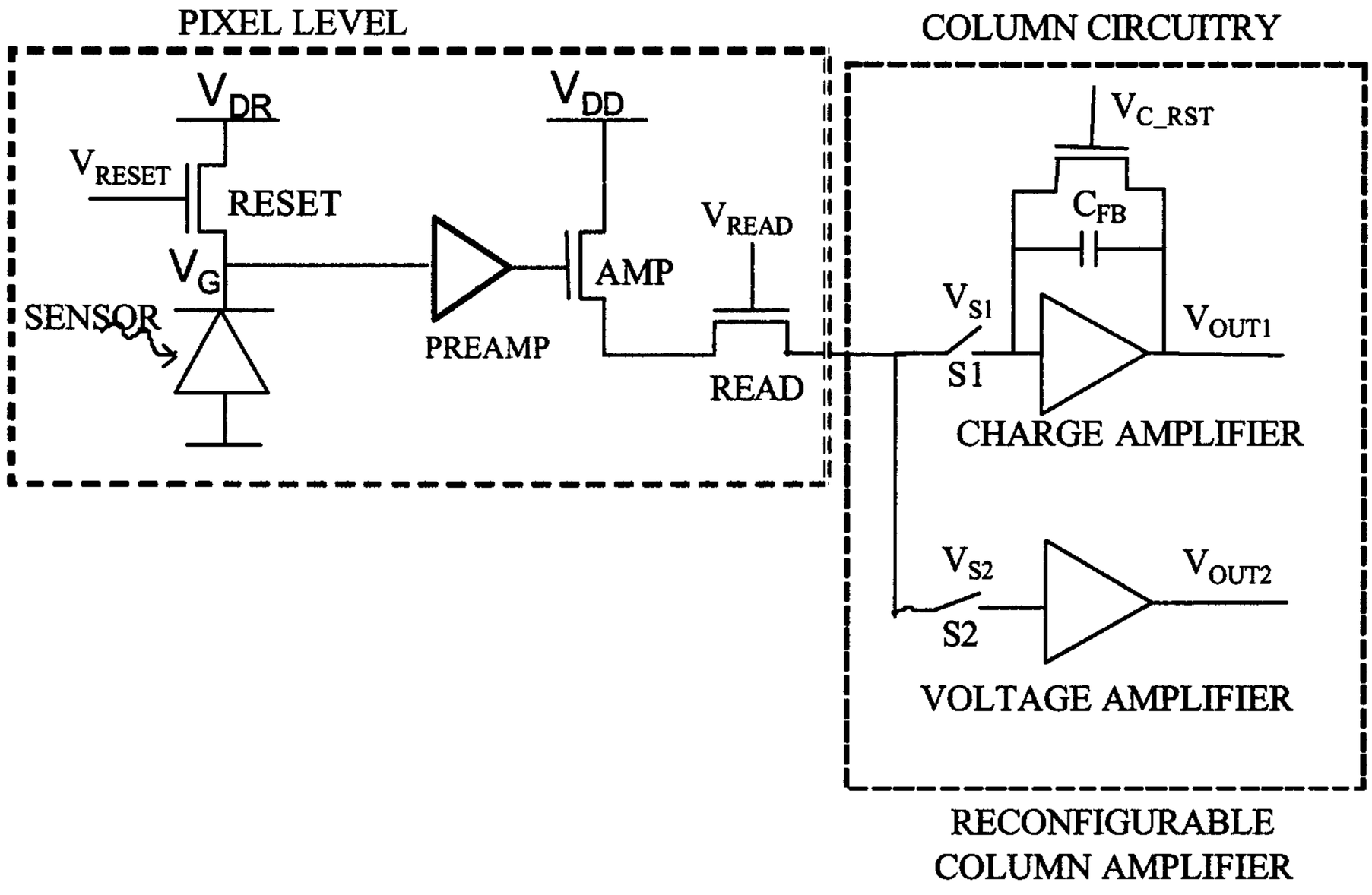


Figure 7a

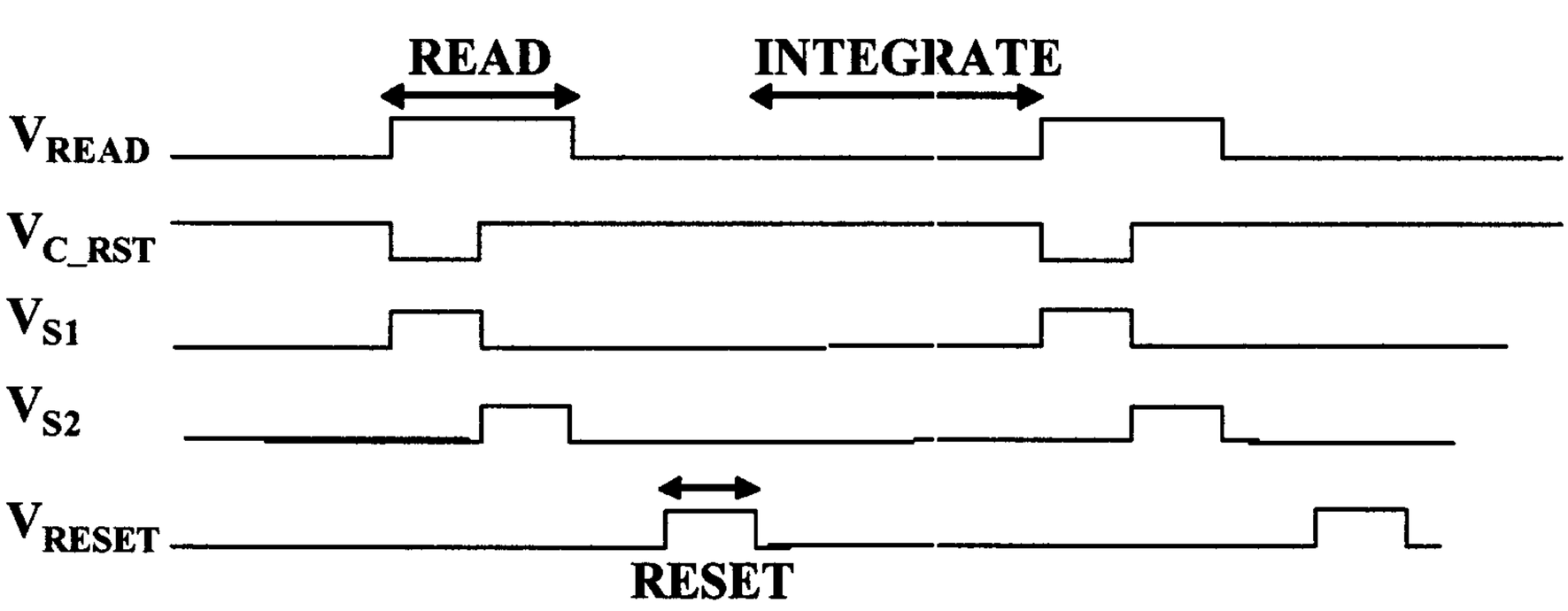


Figure 7b

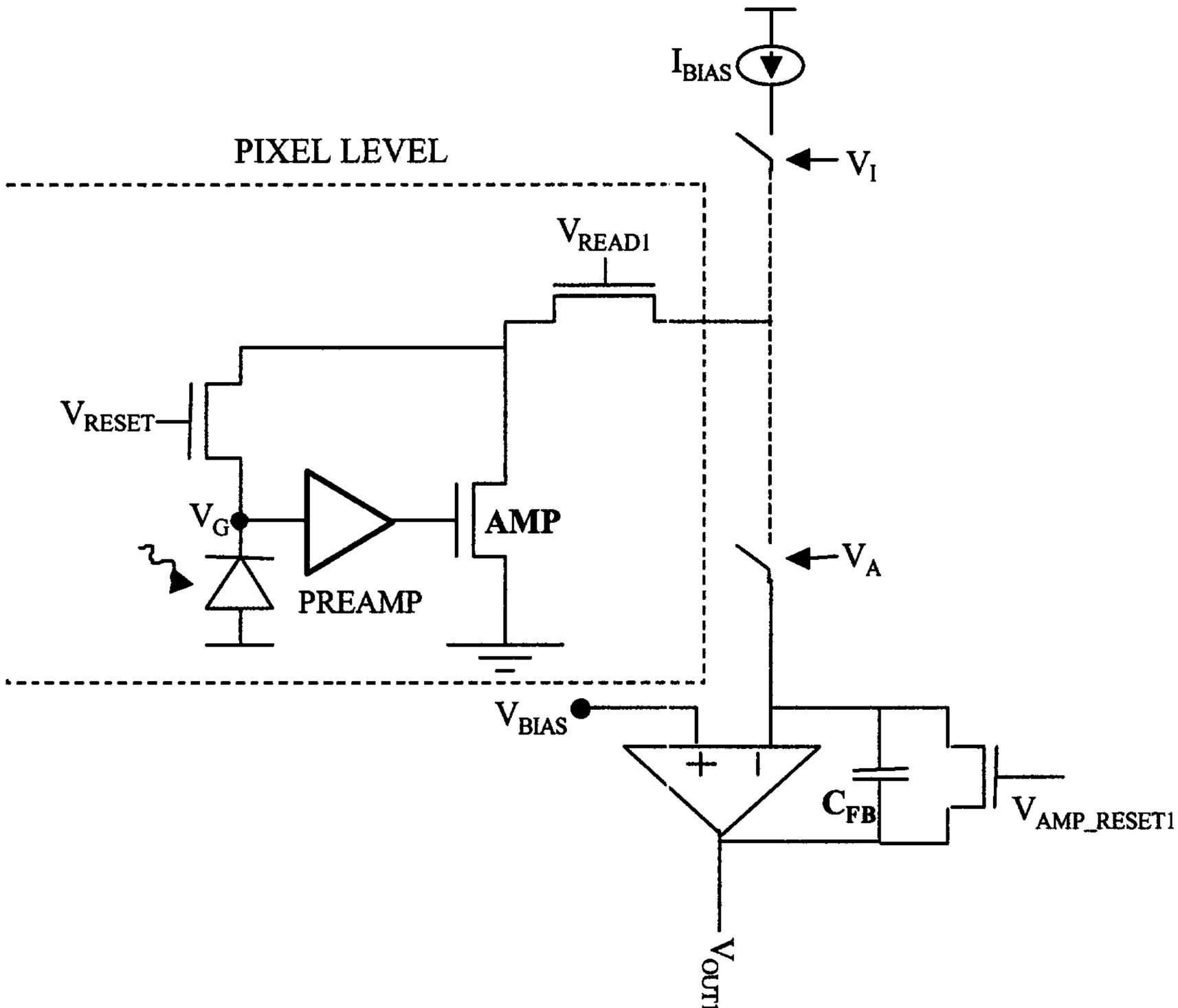


Figure 8a

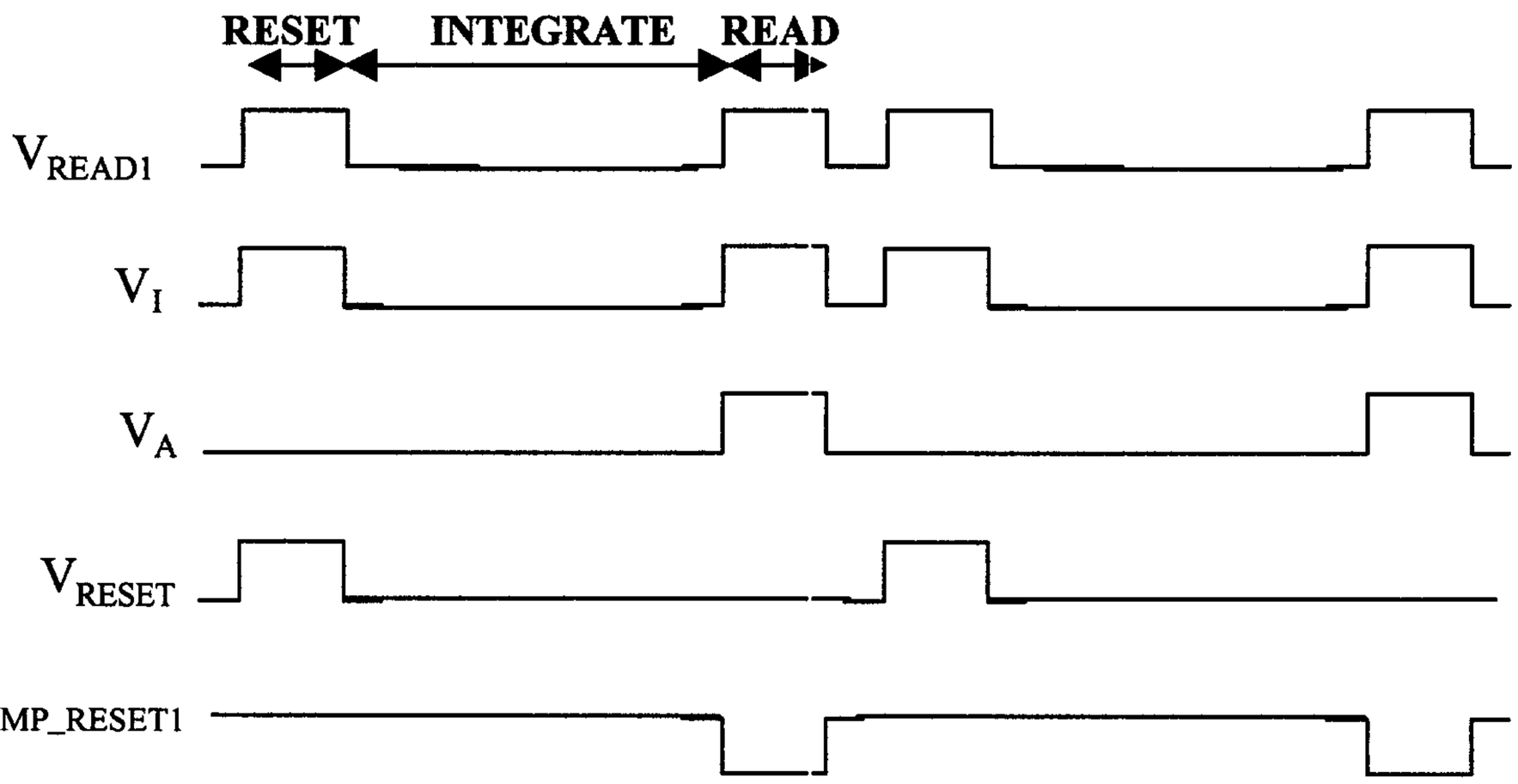


Figure 8b

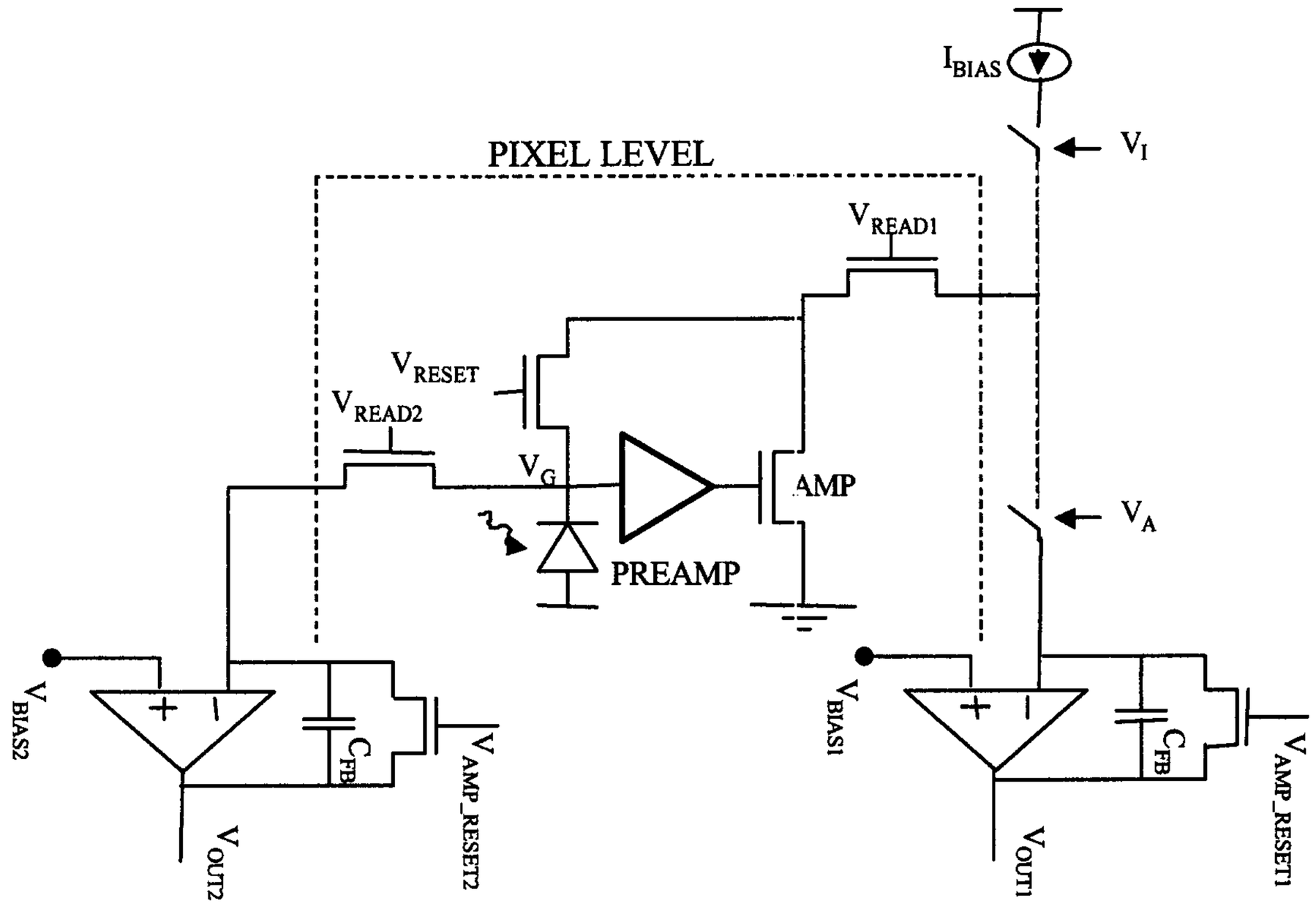


Figure 9a

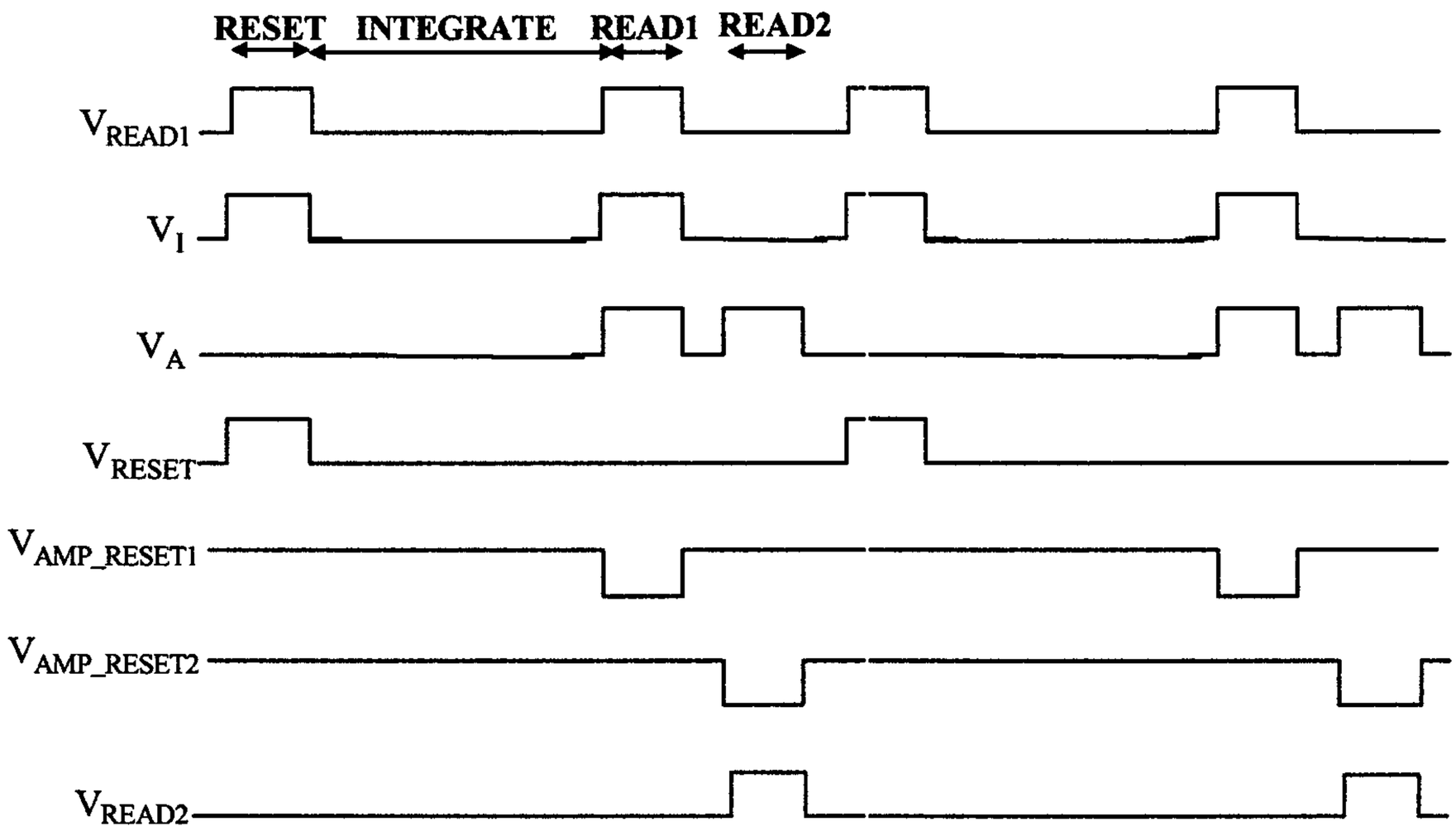
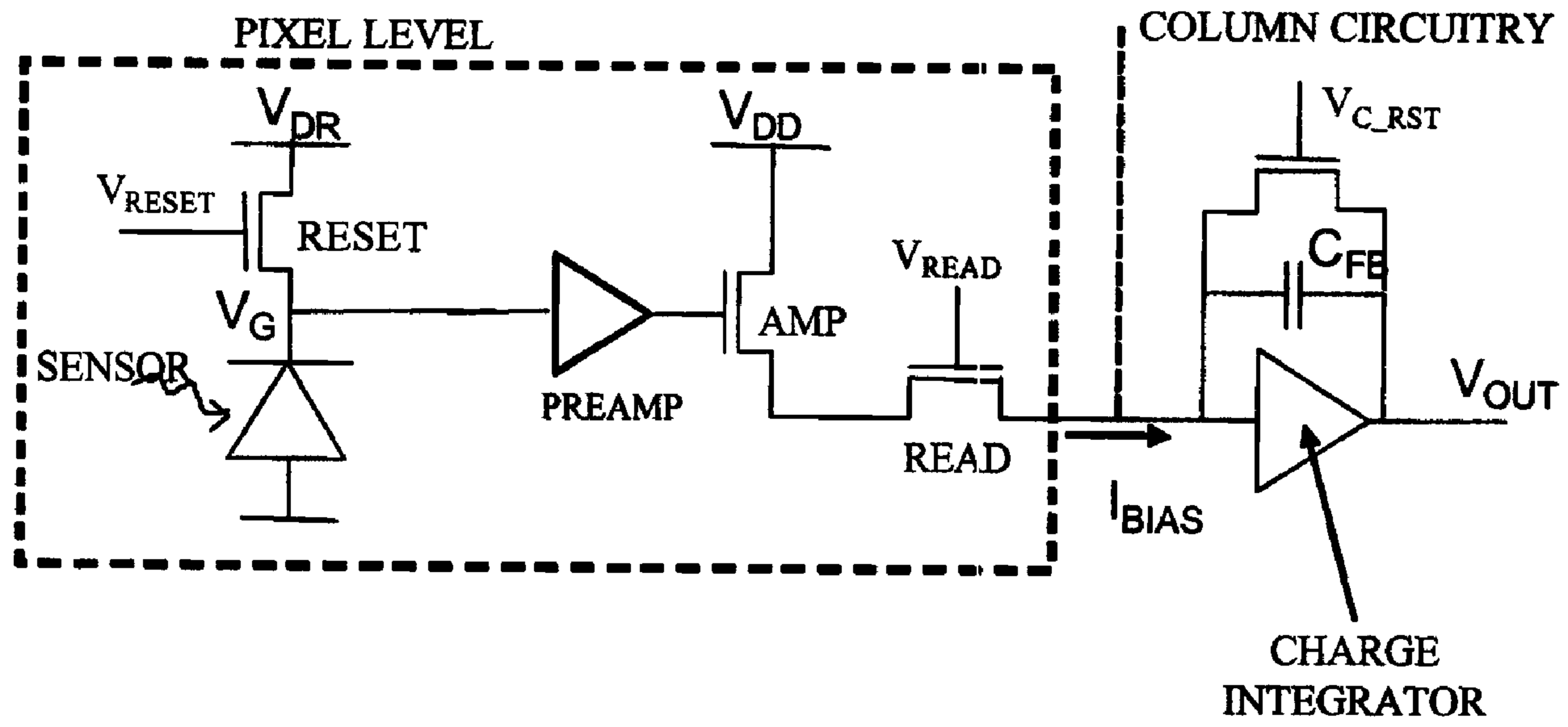


Figure 9b


PIXEL LEVEL
COLUMN CIRCUITRY
V_{DR}
V_{DD}
V_{C_RST}
V_{RESET}
RESET
C_{FB}
V_{READ}
V_G
AMP
SENSOR
PREAMP
V_{OUT}
READ
I_{BIAS}
CHARGE
INTEGRATOR