

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
27 March 2008 (27.03.2008)

PCT

(10) International Publication Number
WO 2008/034850 A3

- (51) International Patent Classification:
H01L 29/06 (2006.01) *H01L 27/088* (2006.01)
- (21) International Application Number:
PCT/EP2007/059914
- (22) International Filing Date:
19 September 2007 (19.09.2007)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
0601998-8 19 September 2006 (19.09.2006) SE
0701884-9 17 August 2007 (17.08.2007) SE
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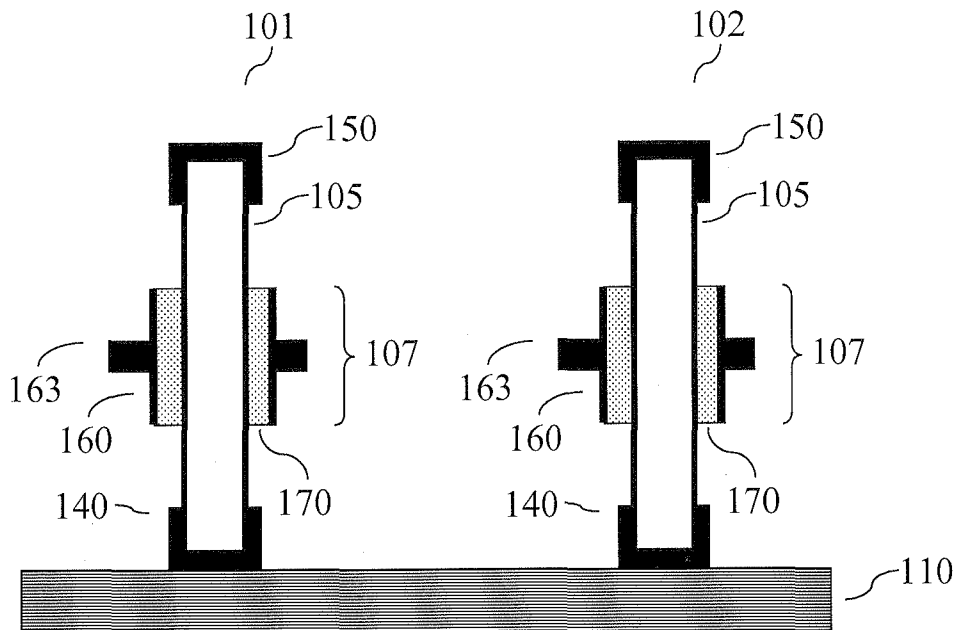
(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

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(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,

[Continued on next page]

(54) Title: ASSEMBLY OF NANOSCALED FIELD EFFECT TRANSISTORS



(57) Abstract: The present invention relates to vertical nanowire transistors with a wrap-gated geometry. The threshold voltage of the vertical nanowire transistors is controlled by the diameter of the nanowire, the doping of the nanowire, the introduction of segments of heterostructures in the nanowire, the doping in shell-structures surrounding the nanowire, tailoring the work function of the gate stack, by strain engineering, by control of the dielectrics or the choice of nanowire material. Transistors with varying threshold voltages are provided on the same substrate, which enables the design of advanced circuits utilizing the shifts in the threshold voltages, similar to the directly coupled field logic.

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FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL,
PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM,
GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

— *before the expiration of the time limit for amending the
claims and to be republished in the event of receipt of
amendments*

Published:

— *with international search report*

(88) Date of publication of the international search report:

22 May 2008

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2007/059914

A. CLASSIFICATION OF SUBJECT MATTER
 INV. H01L29/06 H01L27/088

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2006/011972 A1 (GRAHAM ANDREW [DE] ET AL GRAHAM ANDREW [DE] ET AL) 19 January 2006 (2006-01-19) paragraphs [0042], [0043]; figures 1,4	1, 2, 25
X	US 2005/224888 A1 (GRAHAM ANDREW [DE] ET AL) 13 October 2005 (2005-10-13) paragraphs [0035], [0057], [0060] - [0070]; figures 6-8	1, 2, 25-27

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents :

A document defining the general state of the art which is not considered to be of particular relevance

E earlier document but published on or after the international filing date

L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

O document referring to an oral disclosure, use, exhibition or other means

P document published prior to the international filing date but later than the priority date claimed

T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

Z document member of the same patent family

Date of the actual completion of the international search

31 March 2008

Date of mailing of the international search report

10/04/2008

Name and mailing address of the ISA/

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INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2007/059914

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	<p>NG H T, HAN J, YAMADA T, NGUYEN P, CHEN Y P, MEYYAPPAN M: "Single crystal nanowire vertical surround-gate field-effect transistor"</p> <p>NANO LETTERS AMERICAN CHEM. SOC USA, vol. 4, no. 7, 29 May 2004 (2004-05-29), pages 1247-1252, XP002460579 reference (22), page 1250, right-hand column, line 9 - line 11; figure 4</p>	1, 2, 26, 27
Y	<p>WO 2005/064639 A (KONINKL PHILIPS ELECTRONICS NV [NL]; BAKKERS ERIK P A M [NL]; FEINER L) 14 July 2005 (2005-07-14) page 1, line 28 - page 2, line 2 page 11, line 3 - line 16; claim 21; figures 8-12 page 25, line 8 - line 26</p>	1-5, 25-27
Y	<p>TOMAS BRYLLERT ET AL: "Vertical wrap-gated nanowire transistors"</p> <p>NANOTECHNOLOGY, IOP, BRISTOL, GB, vol. 17, no. 11, 14 June 2006 (2006-06-14), pages S227-S230, XP020103764 ISSN: 0957-4484 Sections 1 and 2, figure 2</p>	1-5, 20, 21, 25
Y	<p>SCHMIDT V ET AL: "Realization of a silicon nanowire vertical surround-gate field-effect transistor"</p> <p>SMALL WILEY-VCH GERMANY, vol. 2, no. 1, January 2006 (2006-01), pages 85-88, XP002460580 figure 3</p>	1-5, 25-27
Y	<p>GOLDBERGER J ET AL: "Silicon vertically integrated nanowire field effect transistors"</p> <p>NANO LETTERS AMERICAN CHEM. SOC USA, vol. 6, no. 5, 30 March 2006 (2006-03-30), pages 973-977, XP002460581 figure 2</p>	1-12, 15-17, 24-27
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INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2007/059914

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Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	<p>WONG H-S P ET AL: "Recent progress in devices and materials for CMOS technology" VLSI TECHNOLOGY, SYSTEMS, AND APPLICATIONS, 2003 INTERNATIONAL SYMPOSIUM ON OCT. 6-8, 2003, PISCATAWAY, NJ, USA, IEEE, 6 October 2003 (2003-10-06), pages 13-16, XP010675906 ISBN: 0-7803-7765-6 Section "Gate Stack", figure 9</p>	9-12
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Y	<p>LIND E ET AL.: "Improved subthreshold slope in an InAs nanowire heterostructure field-effect transistor" NANO LETTERS AMERICAN CHEM. SOC USA, vol. 6, no. 9, 16 August 2006 (2006-08-16), pages 1842-1846, XP002474319 ISSN: 1530-6984 abstract; figures 3,6</p>	13,14
P,Y	<p>KASAI SEIYA ET AL: "Multipath-switching device utilizing a GaAs-based multiterminal nanowire junction with size-controlled dual Schottky wrap gates" APPLIED PHYSICS LETTERS, AIP, AMERICAN INSTITUTE OF PHYSICS, MELVILLE, NY, US, vol. 90, no. 20, 16 May 2007 (2007-05-16), pages 203504-203504, XP012094888 ISSN: 0003-6951 Paragraph after formula (1) on 2nd page. abstract; figure 1</p>	20,21
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INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2007/059914

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>AHMET BINDAL ET AL: "The impact of silicon nano-wire technology on the design of single-work-function CMOS transistors and circuits" NANOTECHNOLOGY, IOP, BRISTOL, GB, vol. 17, no. 17, 14 September 2006 (2006-09-14), pages 4340-4351, XP020104037 ISSN: 0957-4484 figures 1-3</p>	1,26,27
A	<p>MARCHI ET AL: "Investigating the performance limits of silicon-nanowire and carbon-nanotube FETs" SOLID STATE ELECTRONICS, ELSEVIER SCIENCE PUBLISHERS, BARKING, GB, vol. 50, no. 1, January 2006 (2006-01), pages 78-85, XP005239757 ISSN: 0038-1101 figure 10</p>	3
A	<p>US 7 087 920 B1 (KAMINS THEODORE I [US]) 8 August 2006 (2006-08-08) column 8, line 18 - line 56; figure 9 column 15, line 22 - line 47</p>	6-8
A	<p>HO-YOUNG CHA ET AL: "Fabrication and characterization of pre-aligned gallium nitride nanowire field-effect transistors" NANOTECHNOLOGY, IOP, BRISTOL, GB, vol. 17, no. 5, 14 March 2006 (2006-03-14), pages 1264-1271, XP020104533 ISSN: 0957-4484 page 1266, right-hand column; figure 4</p>	6-8
A	<p>YANG-KYU CHOI ET AL: "FinFET process refinements for improved mobility and gate work function engineering" INTERNATIONAL ELECTRON DEVICES MEETING 2002. IEDM. TECHNICAL DIGEST. SAN FRANCISCO, CA, DEC. 8 - 11, 2002, NEW YORK, NY : IEEE, US, 8 December 2002 (2002-12-08), pages 259-262, XP010626036 ISBN: 0-7803-7462-2 Section B "Molybdenum gate technology demonstration", page 260; figures 14,15</p>	9-12
A	<p>GB 2 231 720 A (MIKOSHIBA NOBUO; TSUBOCHI KAZUO; MASU KAZUYA MIKOSHIBA NOBUO; TSUBOCHI) 21 November 1990 (1990-11-21)</p>	9-12
A	<p>page 9, line 21 - page 11, line 4; figure 6</p>	4,7,14,21

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International application No

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	LAUHON L J ET AL: "Epitaxial core-shell and core-multishell nanowire heterostructures" NATURE, NATURE PUBLISHING GROUP, LONDON, GB, vol. 420, 7 November 2002 (2002-11-07), pages 57-61, XP002338449 ISSN: 0028-0836 page 57 - page 58, left-hand column; figures 1,2,5	15-17
A	US 2006/128088 A1 (GRAHAM ANDREW [DE] ET AL) 15 June 2006 (2006-06-15) figure 5	24

INTERNATIONAL SEARCH REPORT

International application No.
PCT/EP2007/059914

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. As all required additional search fees were timely paid by the applicant, this international search report covers allsearchable claims.
2. As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

1-17, 20, 21, 24-27
4. No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-5,25-27

Two vertical nanowire wrap gate FETs with different threshold voltages, wherein the nanowires have different diameters.

2. claims: 6-8,15-17,24

Two vertical nanowire wrap gate FETs with different threshold voltages, wherein the nanowires have different doping levels.

3. claims: 9-12,20,21

Two vertical nanowire wrap gate FETs with different threshold voltages, wherein the gate stacks of the FETs have gates with different work functions or gate dielectrics with different permittivities or thicknesses.

4. claims: 13,14

Two vertical nanowire wrap gate FETs with different threshold voltages, wherein the gate region of at least one FET comprises a heterostructure.

5. claims: 18,19,22,23

Two vertical nanowire wrap gate FETs with different threshold voltages, wherein the nanowires of the FETs have different strains or bandgaps.

6. claims: 28-31

A method of fabricating a semiconductor comprising a plurality of nanowires, the method comprising two separate growth runs in separate areas.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2007/059914

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