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(54) Title: COMBINED 3D ASSEMBLY OF ASIC AND OPTICAL INTERCONNECT FOR COMPACT SWITCHES

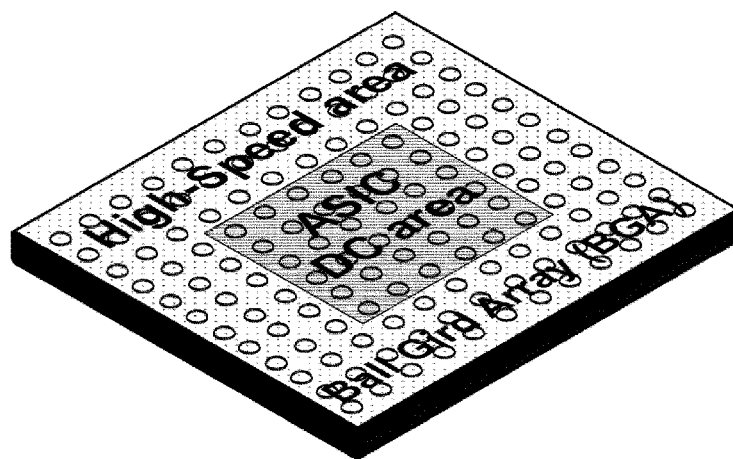


FIG. 1A

(57) Abstract: A compact Ethernet switch is provided whereby the electrical path distance of the Ethernet switch between the ASIC and the optical connections is less than 2cm. At the time of this invention, the Ethernet switch can be considered the most compact transceiver design for Ethernet Switch ASIC, it provides state of art bandwidth density, and avoids retimers and shortens the transmission lines between ASIC high speed pins and optical engine thereby insuring lower cost of ASIC carrying PCB, superior signal quality and reduced power consumption.



COMBINED 3D ASSEMBLY OF ASIC AND OPTICAL INTERCONNECT FOR COMPACT SWITCHES

FIELD OF THE INVENTION

- 5 The invention relates to Ethernet switches.

BACKGROUND OF THE INVENTION

Pluggable front panel optical transceivers have been widely used in data center networks. However, using only the front panel of the switch box implies that
10 eventual total bandwidth is limited. Compared with the pluggable electrical connector, an on-board optical module offers smaller footprint and larger bandwidth density. As a result, on-board optics provide a promising solution to solve the face plate bottleneck problem. Mid board optical modules are far superior to pluggable solutions yet they still require very intricate design of
15 high-speed transmission lines between the pads on the ASIC (Application Specific Integrated Circuit) and those on the mid-board optical modules (MBOM). These result in very expensive PCB (Printed Circuit Board) design and use of specialized PCB materials. As the number (128 to 256 and most recently 512 lanes) and as signaling speeds (from 10 to 25 and eventually to 50
20 Gb/sec) of ASICs continue to rise the complexity of routing these signals requires more and more layers leading to reduced yields and

fabrication/assembly complexity. The present invention addresses these problems, issues and bottlenecks.

SUMMARY OF THE INVENTION

- 5 The present invention provides a compact Ethernet switch whereby the electrical path distance of the Ethernet switch between the ASIC and the optical connections is less than 2cm.

In one embodiment, the Ethernet switch distinguishes a circuit board (e.g. a
10 PCB) which has high-speed through-vias. The circuit board has a first surface and an opposite second surface. The Ethernet switch further distinguishes an ASIC for bi-directional high-speed signals. The ASIC is mounted to the first surface of the circuit board.

- 15 Ethernet switch further distinguishes an optical engine which itself distinguishes an electrical interface with high-speed connections and an interposer for bidirectional conversion of high-speed digital to high-speed optical signals. The electrical interface has a central opening, a first surface and an opposite second surface. The first surface of the electrical interface surface
20 faces the second surface of the circuit board. The electrical interface surface has

spring loaded connections with the circuit board, and wherein the high-speed connections of the electrical interface are aligned with the high-speed through-vias of the circuit board to therewith carry high-speed signals from the ASIC via the high-speed through-vias to the electrical interface.

5

The interposer has a central opening, which overlays the central opening of the electrical interface, a first surface and an opposite second surface. The first surface of the interposer faces the second surface of the electrical interface. The electrical interface and the interposer are mounted together with screws and
10 therewith becoming interchangeable or replaceable from the Ethernet switch.

Ethernet switch further distinguishes optical connections mounted to the second surface of the interposer.

15 In alternate embodiments, the following distinctions can be made and considered:

1. The electrical interface does not necessarily need to have springs on one side. It can also be an arrangement of pins with an appropriate socket soldered to the BGAs on the optical engine side.

2. The optical engine and all the related parts making it do not necessarily need to have a hole in the center (central opening). Any other solution with appropriate heat management and fiber routing solution could work. The area in the middle of the ASIC on the opposite side of the board does need
5 to be free of any socket since it is the place DC capacitors will be placed. But if one can make the electrical interface high enough so that it can be connected above the decoupling capacitors it would also work, assuming it is properly thermally managed.
3. In principal the conversion of the high speed digital electrical signal to
10 optical signals and back can take place on both sides of the interposer for optical engine (**FIG. 4**). This will influence the way light is coupled in/out of the optical engine but should be both included.

The Ethernet switch of the present invention has the following advantages
15 compared to other switches:

1. At the time of this invention, the Ethernet switch will be the most compact transceiver design for Ethernet Switch ASIC.
2. The Ethernet switch provides state of art bandwidth density.
3. The Ethernet switch avoids retimers and shortens the transmission line
20 supply for a better signal quality and reduced power consumption.

4. The combined 3D ASIC and optical engine offers a route for the deployment of mid-board optics, which can be part of a complete pluggable Ethernet switch solution.
5. With the embodiments of this invention, the cost of motherboard on which
5 the ASIC is to be mounted is drastically reduced as no high speed lines are needed and the number of layers can be dramatically reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A shows according to an exemplary embodiment of the invention
10 high-speed differential signals placed in the outside rows (to ease routing and reduce electronic crosstalk) and the DC signals are concentrated in the central area. Schematics not to scale and area should be specifically divided by the chip layout.

FIG. 1B shows according to an exemplary embodiment of the invention
15 high-speed connector, which can be ultra-low profile, high density, highly customizable for board-to-board, IC-to-board, and cable-to-board applications, is specially designed to be compatible with the high-speed differential pairs of ASIC. Schematic not to
20 scale and connector detail information such as geometry, contacted type, compress solution etc. should be specifically designed.

FIGs. 2-6 show according to an exemplary embodiment of the invention schematic designs with various views for the on-board transceiver modules for a full ASIC. Schematic not to scale, the 3D assembly design main concept is shown and specific design might depend
5 on components, locations, routing and optical accesses etc.

DETAILED DESCRIPTION

The present invention provides a new type of mid-board optical engine, which includes all the required optical interconnects needed for connecting the ASIC
10 to the outside world in a single module. This module can be a pluggable (interchangeable) module and can be assembled on the same PCB on which the ASIC is assembled, but on the other side of the PCB board. In this way the PCB design can be drastically simplified since the high-speed signals only need to go through a via to the back side of the board and the signal degradation due to
15 propagation in the PCB will be almost completely removed as the length of the resulting transmission lines between ASIC and MBOM will drop to several millimeters. At these distances, it is possible that CDR (Clock and Data Recovery) functionality which consumes more than 70% of the power budget of the link can be discarded. The resulting 3D switch system will have the most
20 compact size possible while still retaining all the switching capabilities of the standard size switching system. Such a switch module can be, on its own,

considered as a pluggable switch solution which will relieve some of the inhibitions from using MBOM in switches.

The BGA (Ball Grid Array) layout of a standard switching ASIC was selected
5 as a starting point for an initial demonstration. The high-speed differential signals are placed in the outside rows (to ease routing and reduce electronic crosstalk) and the DC signals are concentrated in the central area (**FIG. 1A**). A high-speed connector, which can be ultra-low profile, high density, highly customizable for board-to-board, IC-to-board, and cable-to-board applications,
10 is specially designed to be compatible with the high-speed differential pairs of ASIC (**FIG. 1B**). The High-Speed connector can be based on commercially available high-speed connectors which are used to mate BGA type packaged ICs with PCB. In order to accommodate the required additional signals and power supplies of the ASIC, and seeing that the optical engines will be placed
15 on the perimeter of the optical interposer part, the central area of such a standard BGA type connector is preferably removed to allow for appropriate assembly.

An interposer (PCB, FPC (Flexible Printed Circuit board), ceramic, silicon, glass etc.) is designed with the same pad layout of the connector, which can be
20 used to connect the interposer and high-speed signal of ASIC. The transceiver modules are also integrated on the interposer. This means that all the required CMOS (Complementary Metal-Oxide Silicon) driving ICs, trans impedance amplifier ICs as well as the electro-optic VCSEL (vertical cavity surface

emitting laser) and PD (photo detector) arrays are integrated into this interposer. This insures that the electrical connection between ASIC SerDes (Serializer/Deserializer) and optical interconnect module are as short as possibly can, since they are only as long as the thickness of the PCB board on which the ASIC is mounted. For connecting to the outside-world the back-side optical interconnect module can use optical connectors such as multiple MPO (Multi-fiber Push-On) type connectors combined with either a light turning solution or a 3D glass interposer etc. to take the light to and from the opto-electronic dies and connect them to fibers.

10

As a result, the on-board transceiver modules are fully designed on the back side of the ASIC and connected with the ASIC through a high-speed connector and an interposer. Screws can be used to fix the interposer and connector between ASIC and transceiver modules. Optical connectors or waveguides can be used to give the light access for this on-board transceiver module to the front panel. This approach successfully not only reduces the size of the switch in the data center network and gives more flexibility but also solves the front panel bandwidth problem and provides more bandwidth density. The schematic 3D assembly views and cross-section views of this on-board transceiver modules for full ASIC are shown in **FIGs. 2- 6**.

20

Conventional on-board transceivers are commercially available and in some niche applications have replaced pluggable transceivers (mostly for HPC (High

Performance Computing)). However, none of these mid-board solutions has been designed to include more than 12 channels and none of them has been suggested for mounting at the opposite side of the PCB to shorten the distance between ASIC BGA and mid-board module BGA to the minimum without
5 placing the optical module inside the ASIC package. Attempts to include the optics inside the ASIC package have not been commercially successful so far (COMPASSEOS who pioneered his work has gone bankrupt after 150M\$ investment and 7 years of R&D work). It is clear that any solution has to be separable from the ASIC itself as the market is not ready for a full blown
10 integrated optical front-end inside the ASIC package.

CLAIMS

What is claimed is:

1. An Ethernet switch, comprising:

- 5 (a) a circuit board comprising high-speed through-vias, wherein the circuit board has a first surface and an opposite second surface;
- (b) an ASIC for bi-directional high-speed signals, wherein the ASIC is mounted to the first surface of the circuit board;
- 10 (c) an optical engine comprising an electrical interface with high-speed connections and an interposer for bidirectional conversion of high-speed digital to high-speed optical signals,
- wherein the electrical interface has a central opening, a first surface and an opposite second surface, wherein the first surface of the electrical interface surface faces the second surface of the circuit board, wherein the electrical interface surface has spring loaded connections with the circuit board, and wherein the high-speed connections of the electrical interface are aligned with the high-speed through-vias of the circuit board to therewith carry high-speed signals from the ASIC via the high-speed through-vias to the electrical interface,
- 15

wherein the interposer has a central opening, which overlays the central opening of the electrical interface, a first surface and an opposite second surface, and wherein the first surface of the interposer faces the second surface of the electrical interface,

5 wherein the electrical interface and the interposer are mounted together with screws and therewith interchangeable or replaceable from the Ethernet switch;

(d) optical connections mounted to the second surface of the interposer,

wherein the electrical path distance of the Ethernet switch between the
10 ASIC and the optical connections is less than 2cm.

2. An Ethernet switch, comprising:

- (a) a circuit board comprising high-speed through-vias, wherein the circuit board has a first surface and an opposite second surface;
- 15 (b) an ASIC for bi-directional high-speed signals, wherein the ASIC is mounted to the first surface of the circuit board;
- (c) an optical engine comprising an electrical interface with high-speed connections and an interposer for bidirectional conversion of high-speed digital to high-speed optical signals,

wherein the electrical interface has a first surface and an opposite second surface, wherein the first surface of the electrical interface surface faces the second surface of the circuit board, and wherein the high-speed connections of the electrical interface are aligned with the high-speed through-vias of the circuit board to therewith carry high-speed signals from the ASIC via the high-speed through-vias to the electrical interface,

wherein the interposer has a first surface and an opposite second surface, and wherein the first surface of the interposer faces the second surface of the electrical interface,

wherein the electrical interface and the interposer are removeably mounted together and therewith interchangeable or replaceable from the Ethernet switch;

(d) optical connections mounted to the second surface of the interposer, wherein the electrical path distance of the Ethernet switch between the ASIC and the optical connections is less than 2cm.

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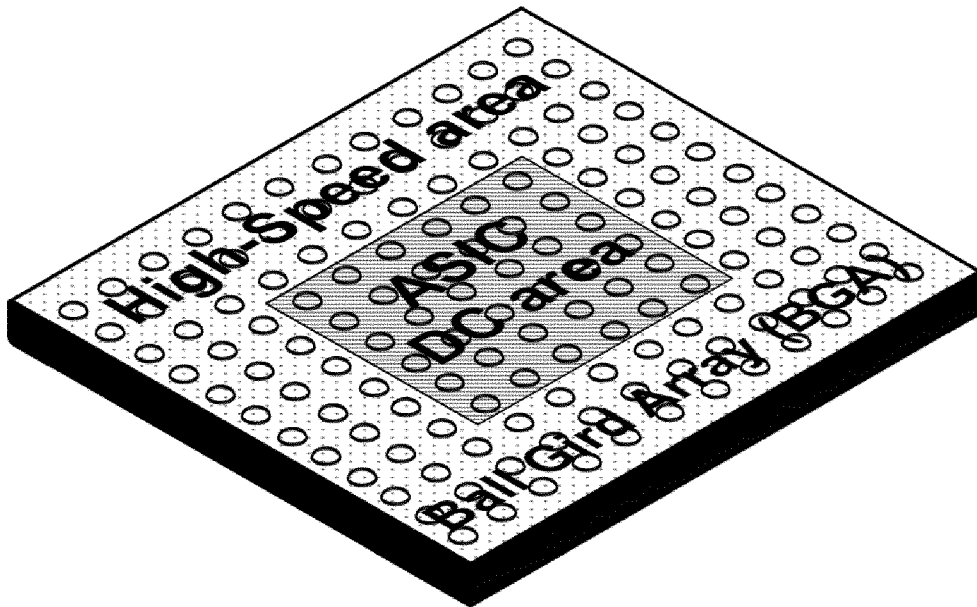


FIG. 1A

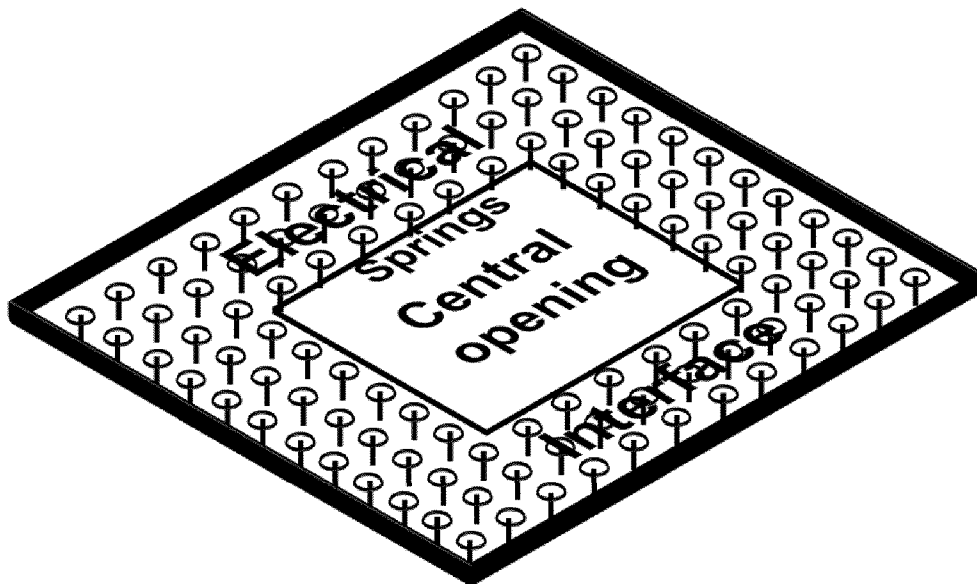
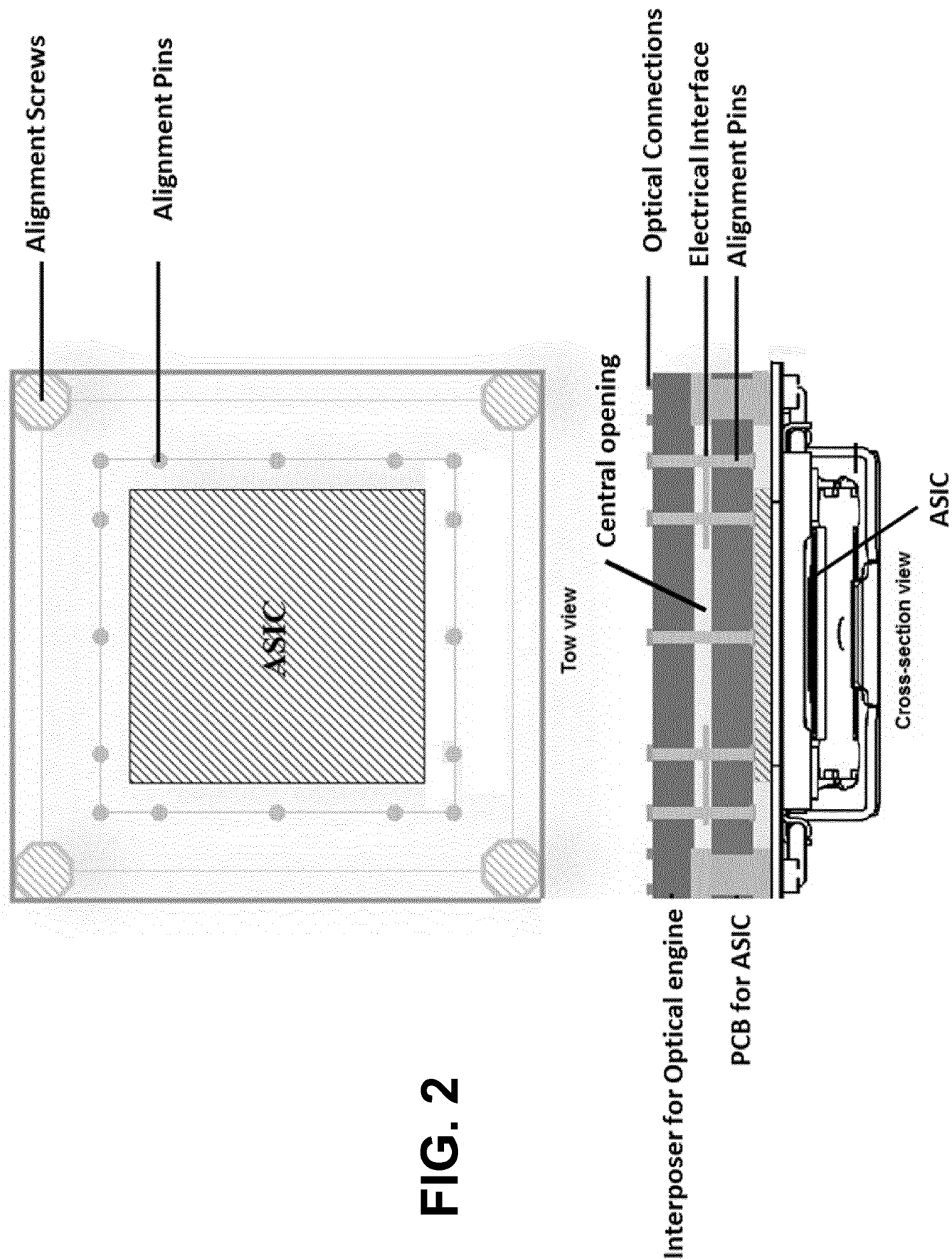


FIG. 1B

FIG. 2



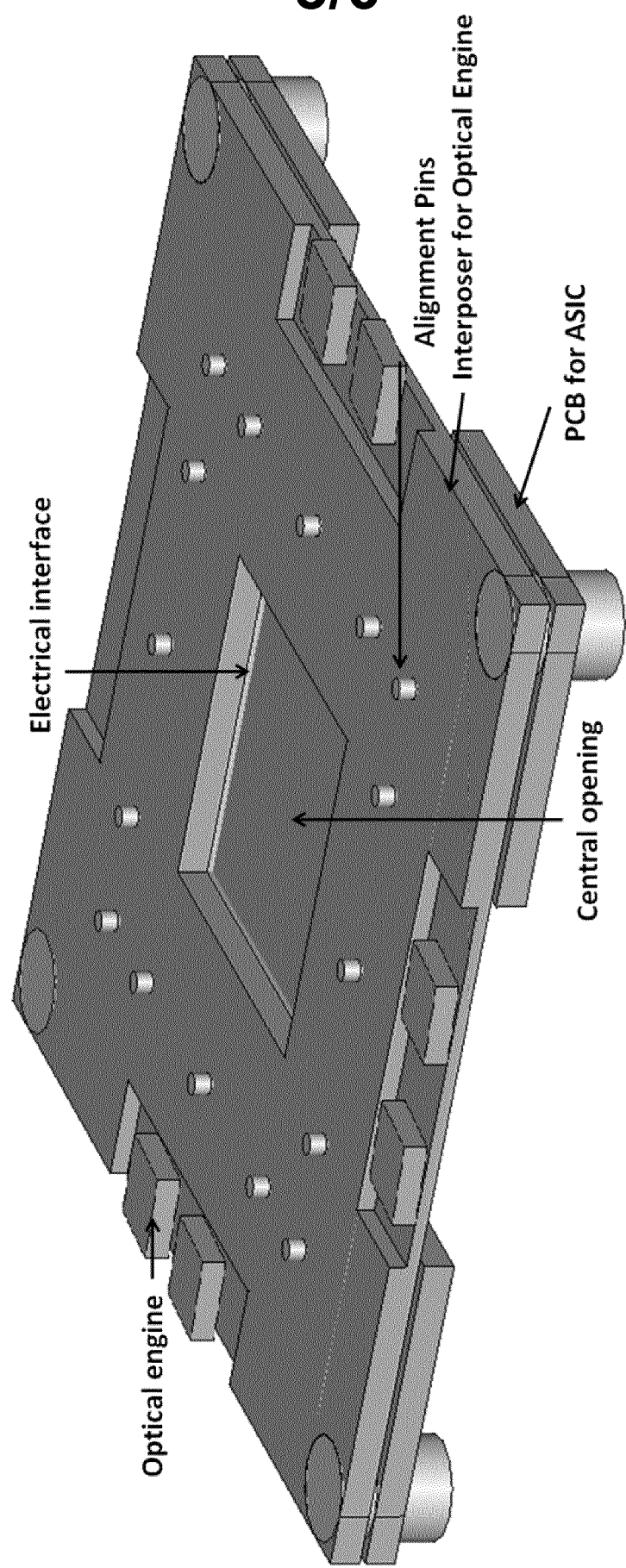
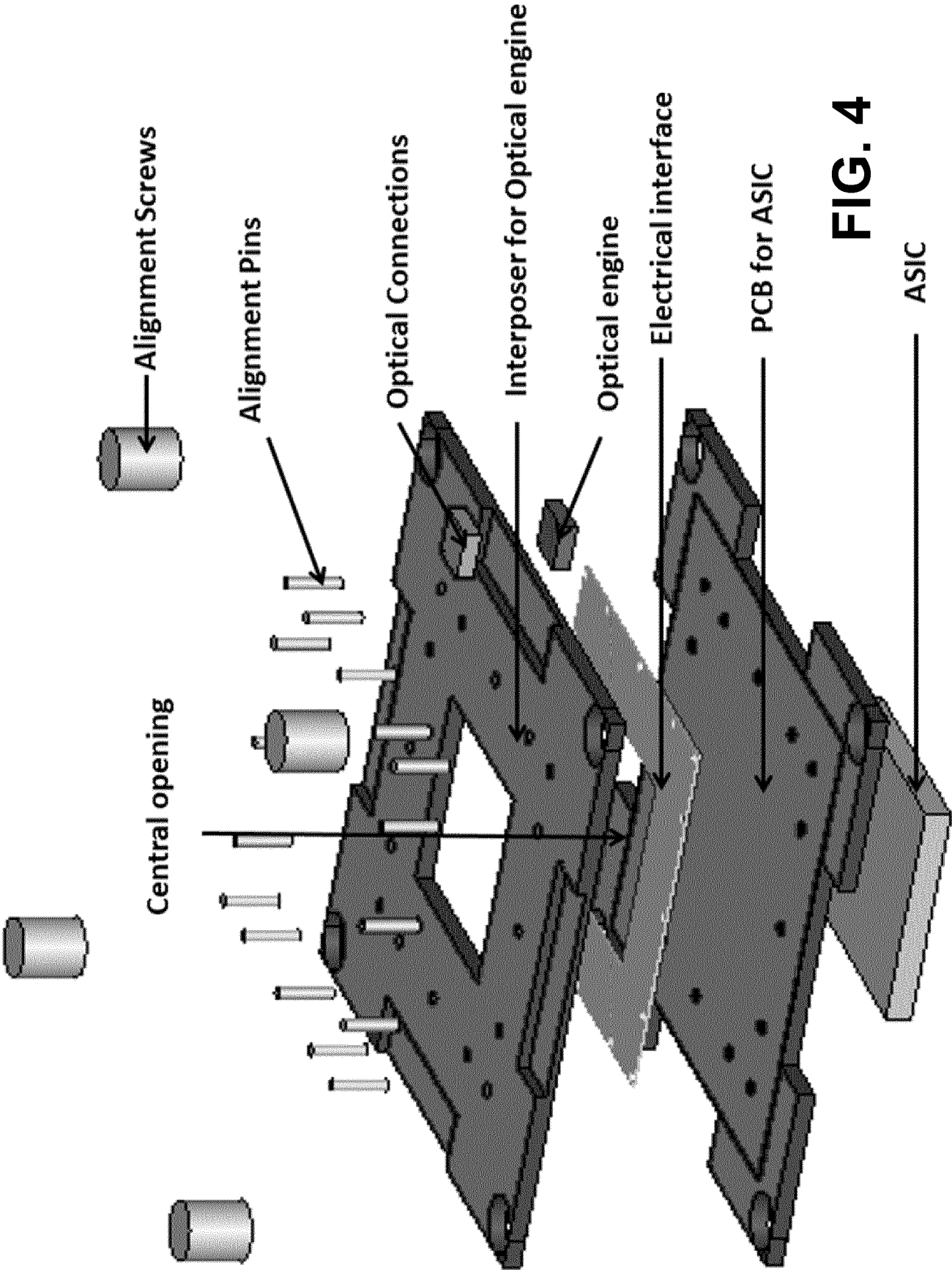
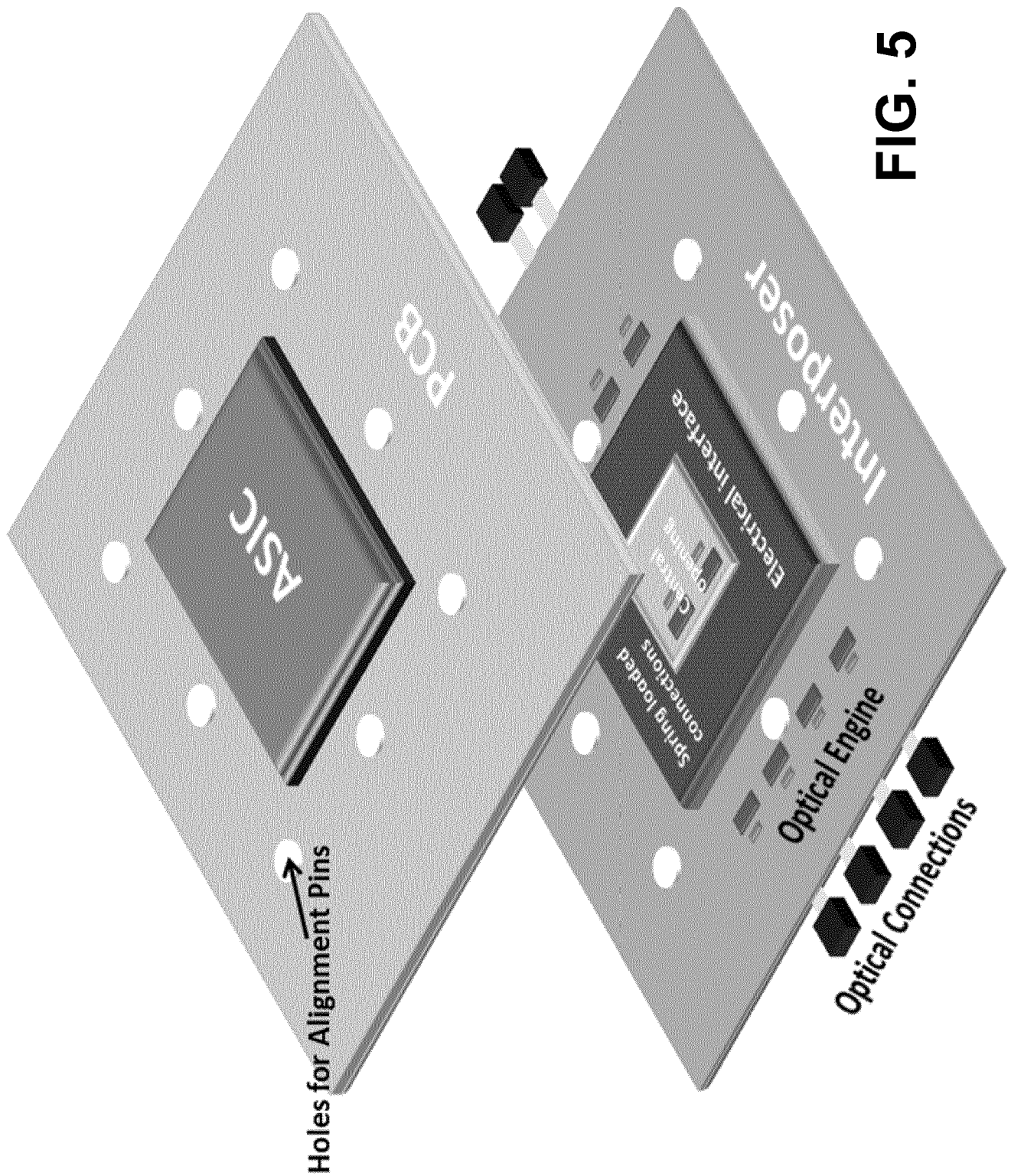


FIG. 3





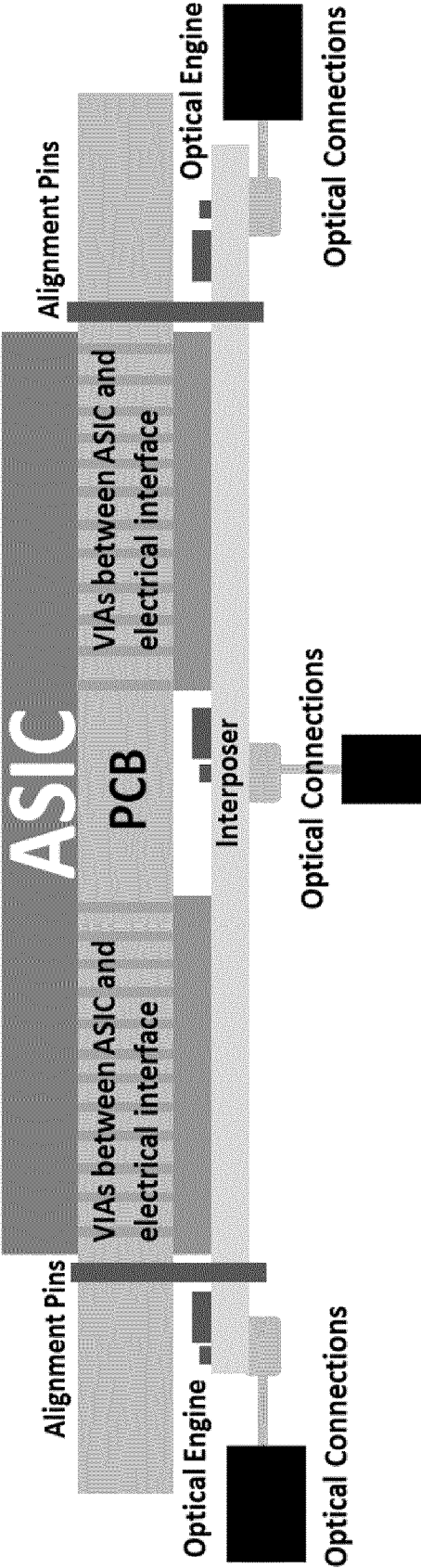


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2018/060891

A. CLASSIFICATION OF SUBJECT MATTER
INV. G02B6/42 H04B10/40
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G02B H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Reflex Photonics: "Optical IC Package Product Family Summary Updated", 10 August 2016 (2016-08-10), XP055489447, Retrieved from the Internet: URL: http://reflexphotonics.com/wp-content/uploads/Light-on-Board-Product-Family_White_Paper_-2016.pdf [retrieved on 2018-07-02] the whole document ----- -/--	1,2



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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Date of the actual completion of the international search

2 July 2018

Date of mailing of the international search report

09/07/2018

Name and mailing address of the ISA/

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Authorized officer

Lefebvre, Laurent

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2018/060891

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	BENJAMIN YEHOASHUA ET AL: "Assembly development of 1.3 Tb/s full duplex optical module", 34<TH> ELECTRONIC COMPONENTS CONFERENCE, IEEE, 28 May 2013 (2013-05-28), pages 292-296, XP032474090, ISSN: 0569-5503, DOI: 10.1109/ECTC.2013.6575586 ISBN: 978-1-4799-0233-0 [retrieved on 2013-08-06] page 293, paragraph optical.modules.component; figure 2 -----	1,2
A	US 2013/315586 A1 (KIPP SCOTT G [US]) 28 November 2013 (2013-11-28) paragraphs [0029], [0034] - [0036]; figures 3a,3c -----	1,2

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2018/060891

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2013315586	A1	28-11-2013	NONE
