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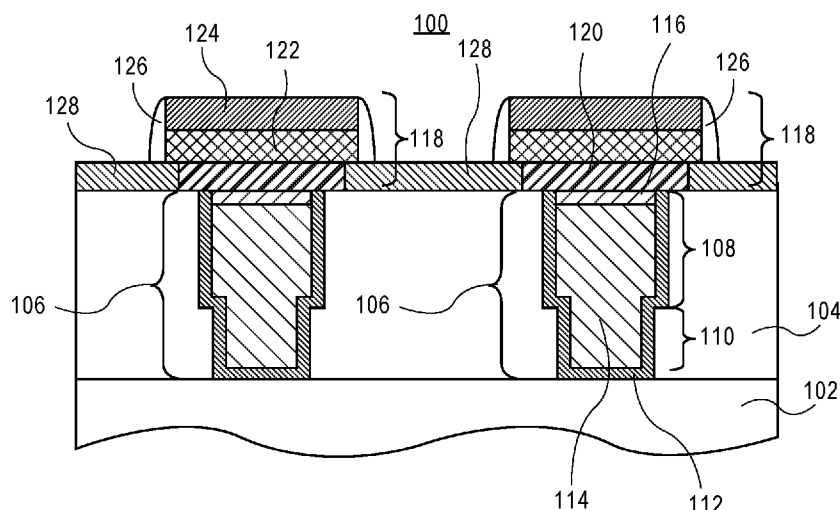


FIG. 1

(57) Abstract: Approaches for fabricating back end of line (BEOL)-compatible resistive random access memory (RRAM) elements and devices, and the resulting structures, are described. In an example, a resistive random access memory (RRAM) device includes a conductive interconnect disposed in an inter-layer dielectric (ILD) layer disposed above a substrate. The ILD layer has an uppermost surface substantially co-planar with an uppermost surface of the conductive interconnect. An RRAM element is disposed on the conductive interconnect. The RRAM element includes a first electrode layer disposed on the uppermost surface of the conductive interconnect, a resistance switching layer disposed on the first electrode layer, and a second electrode layer disposed on the resistance switching layer. An insulating metal oxide layer is disposed on the uppermost surface of the ILD layer and laterally adjacent to and in contact with the first electrode layer.

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APPROACHES FOR FABRICATING BACK END OF LINE (BEOL)-COMPATIBLE RRAM DEVICES AND THE RESULTING STRUCTURES

TECHNICAL FIELD

5 Embodiments of the invention are in the field of integrated circuit fabrication and, in particular, approaches for fabricating back end of line (BEOL)-compatible resistive random access memory (RRAM) elements and devices, and the resulting structures.

BACKGROUND

10 For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips. For example, shrinking transistor size allows for the incorporation of an increased number of memory devices on a chip, lending to the fabrication of products with
15 increased capacity. The drive for ever-more capacity, however, is not without issue. The necessity to optimize the performance of each device becomes increasingly significant.

 Embedded SRAM and DRAM have problems with non-volatility and soft error rates, while embedded FLASH memories require additional masking layers or processing steps during manufacture, require high-voltage for programming, and have issues with endurance and
20 reliability. Nonvolatile memory based on resistance change is known as RRAM or ReRAM. Although commonly anticipated as a replacement technology for flash memory, the cost benefit and performance benefit of RRAM have not been obvious enough to most companies to proceed with the replacement. Also, for low voltage non-volatile embedded applications, operating voltages less than 1V and compatible with CMOS logic processes may be desirable but
25 challenging to achieve.

 Thus, significant improvements are still needed in the area of nonvolatile memory device manufacture and operation. In particular, significant improvements are still needed in the area of non-volatile memory arrays and their integration with logic processors.

30 BRIEF DESCRIPTION OF THE DRAWINGS

 Figure 1 illustrates a cross-sectional view of two RRAM devices separated by an insulating metal oxide layer, in accordance with an embodiment of the present invention.

 Figure 2A illustrates a plan view of a pair of RRAM elements integrated with a common line electrode, in accordance with an embodiment of the present invention.

Figure 2B illustrates a plan view of a pair of RRAM elements integrated with discrete via electrodes, in accordance with an embodiment of the present invention.

Figure 3 illustrates cross-sectional views of various operations in a method of fabricating RRAM devices separated by an insulating metal oxide layer, in accordance with an embodiment
5 of the present invention.

Figure 4 illustrates cross-sectional views of various operations in another method of fabricating RRAM devices separated by an insulating metal oxide layer, in accordance with another embodiment of the present invention.

Figure 5 illustrates a cross-sectional view of an RRAM element coupled to a drain side of a transistor selector, in accordance with an embodiment of the present invention.
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Figure 6A illustrates schematic views of several options for positioning an RRAM element in an integrated circuit, in accordance with an embodiment of the present invention.

Figure 6B illustrates a cross-sectional view of a logic region together with an RRAM memory array integrated on a common substrate, in accordance with an embodiment of the
15 present invention.

Figures 7A and 7B illustrate a schematic and corresponding I-V plot, respectively, demonstrating concepts involved with filament formation in an RRAM element, in accordance with an embodiment of the present invention.

Figure 8 illustrates an operational schematic representing a changing of states for an anionic-based metal-conductive oxide-metal RRAM memory element, in accordance with an
20 embodiment of the present invention.

Figure 9 illustrates a schematic representation of resistance change in a conductive oxide layer induced by changing the concentration of oxygen vacancies in the conductive oxide layer, in accordance with an embodiment of the present invention.

Figure 10 illustrates an operational schematic representing a changing of states for a cationic-based metal-conductive oxide-metal RRAM memory element, in accordance with an
25 embodiment of the present invention.

Figure 11 illustrates a schematic representation of resistance change in a cationic-based conductive oxide layer induced by changing the concentration of cation vacancies in the
30 conductive oxide layer, in accordance with an embodiment of the present invention.

Figure 12 illustrates a schematic of a memory bit cell which includes a metal-conductive oxide-metal RRAM memory element, in accordance with an embodiment of the present invention.

Figure 13 illustrates a block diagram of an electronic system, in accordance with an
35 embodiment of the present invention.

Figure 14 illustrates a computing device in accordance with one embodiment of the invention.

Figure 15 illustrates an interposer that includes one or more embodiments of the invention.

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DESCRIPTION OF THE EMBODIMENTS

Approaches for fabricating back end of line (BEOL)-compatible resistive random access memory (RRAM) elements and devices, and the resulting structures, are described. In the following description, numerous specific details are set forth, such as specific RRAM material regimes and structure architectures, in order to provide a thorough understanding of
10 embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known features, such as operations associated with embedded memory, are not described in detail in order to not unnecessarily obscure embodiments of the present invention.
15 Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

Certain terminology may also be used in the following description for the purpose of reference only, and thus are not intended to be limiting. For example, terms such as “upper”, “lower”, “above”, and “below” refer to directions in the drawings to which reference is made.
20 Terms such as “front”, “back”, “rear”, and “side” describe the orientation and/or location of portions of the component within a consistent but arbitrary frame of reference which is made clear by reference to the text and the associated drawings describing the component under discussion. Such terminology may include the words specifically mentioned above, derivatives thereof, and words of similar import.

25 One or more embodiments are directed to backend compatible RRAM stacks for dense arrays, such as copper interconnect or via compatible RRAM material stacks. One or more embodiments of the present invention are directed to methods for integrating RRAM memory arrays into a logic processor. Specific embodiments are directed to insulating metal oxide layers for electrically isolating adjacent RRAM elements and devices fabricated therefrom. Particular
30 embodiments may be suitable for fabricating embedded non-volatile memory (e-NVM). Approaches described herein may provide a fabrication pathway for high performance RRAM cells and increase the potential of using scaled RRAM cells for future e-NVM needs, such as for integration in system on chip (SoC) products.

In accordance with one or more embodiments of the present invention, an RRAM
35 memory thin film stack is designed to improve the switching properties while rendering the stack

compatible with standard backend processing. In particular embodiments, RRAM stack integration is enabled using nitride electrodes that are both an electrode to the RRAM stack as well as a barrier to copper (Cu) metal lines. In one such embodiment, the portions of the nitride electrode outside of the footprint of the RRAM cell is sacrificial in that it is converted to an oxide insulator.

To provide context, many high performance RRAM memory stacks have been demonstrated using nitride electrodes compatible with RRAM switching layer oxides. However, integrating such nitride electrodes with Cu metallization has been challenging due to limited etch selectivity between the nitride electrode (for RRAM) and the nitride barrier for Cu metal. In an embodiment, an RRAM stack is compatible with standard Cu metallization. Embodiments described herein may be implemented to improve performance and reliability of RRAM memory, increasing its potential for use as e-NVM.

As an exemplary implementation, Figure 1 illustrates a cross-sectional view of two RRAM devices separated by an insulating metal oxide layer, in accordance with an embodiment of the present invention.

Referring to Figure 1, a resistive random access memory (RRAM) device 100 includes a conductive interconnect 106 disposed in an inter-layer dielectric (ILD) layer 104 disposed above a substrate 102. The ILD layer 106 has an uppermost surface substantially co-planar with an uppermost surface of the conductive interconnect 106. An RRAM element 118 is disposed on the conductive interconnect 106. The RRAM element 118 includes a first electrode layer 120 disposed on the uppermost surface of the conductive interconnect 106. A resistance switching layer 122 is disposed on the first electrode layer 120. A second electrode layer 124 is disposed on the resistance switching layer 122. An insulating metal oxide layer 128 is disposed on the uppermost surface of the ILD layer and laterally adjacent to and in contact with the first electrode layer 120.

In an embodiment, the insulating metal oxide layer 128 electrically isolates the first electrode layer 120 from a first electrode layer 120 of a second RRAM element 118 laterally adjacent to the RRAM element 118 on the uppermost surface of the ILD layer, as is depicted in Figure 1. In an embodiment, the first electrode layer 120 extends onto a portion of the uppermost surface of the ILD layer 106, as is also depicted in Figure 1. In an embodiment, the resistance switching layer 122 has a width greater than a width of the first electrode layer 120, and the resistance switching layer 122 extends onto a portion of an uppermost surface of the insulating metal oxide layer 128, as is depicted in Figure 1. In one such embodiment, the second electrode layer 124 has a width approximately the same as the width of the resistance switching layer 122.

In an embodiment, each RRAM device 118 further includes a dielectric sidewall spacer 126, such as a silicon nitride spacer, laterally adjacent to and in contact with sidewalls of the second electrode layer 124 and the resistance switching layer 122. In one such embodiment, the dielectric sidewall spacer 126 is disposed on a portion of the uppermost surface of the insulating metal oxide layer 128, as is depicted in Figure 1.

In an embodiment, the insulating metal oxide layer 128 and the first electrode layer 120 include a same metal species. In one such embodiment, the metal species is titanium (Ti). In a specific such embodiment, the insulating metal oxide layer 128 includes titanium oxide, and the first electrode layer 120 includes titanium nitride.

In an embodiment, the conductive interconnect 106 includes a conductive line portion 108 and an underlying via portion 110, as is depicted in Figure 1. In another embodiment, the conductive interconnect is a conductive via. In one embodiment, the conductive interconnect includes a conductive fill material 114 surrounded by a barrier layer 112, which may include an upper barrier layer 116, as is depicted in Figure 1. In a specific such embodiment, the conductive fill material 114 but not the barrier layer 112 is recessed to form an opening in which the upper barrier layer 116 is then formed. In an embodiment, although depicted using different shading, the upper barrier layer 116 is composed of substantially the same material as barrier layer. In one such embodiment, the material include tantalum nitride. In an embodiment, the conductive interconnect 106 is coupled to a drain region of an underlying select transistor disposed on the substrate 102, as is described below in association with Figure 5.

Referring again to Figure 1, and as used throughout the present disclosure, exemplary material combinations for the first electrode layer 120, the resistance switching layer 122, and the second electrode layer 124 are described below in association with Figures 7A and 8-11. In one embodiment, the resistance switching layer 122 is an oxide-based material layer including a dielectric oxide material (e.g., such as a layer of HfO_2 , as is described in association with Figures 7A and 7B) or a conductive oxide material (e.g., as described below in association with Figures 8 and 9).

Referring again to Figure 1, and as used throughout the present disclosure, in an embodiment, one or more interlayer dielectrics (ILDs), such as ILD layer 104, are included in an RRAM device structure. Such ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as low-k dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide (SiO_2), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce

their dielectric constant. In cases where a stack of ILD layers is implemented, etch stop materials may be included as intervening dielectric layers between the ILD layers. Such etch stop layers may be composed of dielectric materials different from the interlayer dielectric material. In some embodiments, an etch stop layer includes a layer of a nitride of silicon (e.g., silicon nitride) or a layer of an oxide of silicon, or both, or a combination thereof. Other suitable materials may include carbon-based materials, such as silicon carbide. Alternatively, other etch stop layers known in the art may be used depending upon the particular implementation. The etch stop layers may be formed by CVD, PVD, or by other deposition methods.

Referring again to Figure 1, and as used throughout the present disclosure, in an embodiment, the metal lines (such as 108) and vias (such as 110) are composed of one or more metal or other conductive structures. A common example is the use of copper lines and structures that may or may not include barrier layers (such as Ta or TaN layers) between the copper and surrounding ILD material. As used herein, the term metal includes alloys, stacks, and other combinations of multiple metals. For example, the metal interconnect lines may include barrier layers, stacks of different metals or alloys, etc. The interconnect lines are also sometimes referred to in the arts as traces, wires, lines, metal, or simply interconnect.

Referring again to Figure 1, and as used throughout the present disclosure, in an embodiment, substrate 102 is a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present invention.

It is to be appreciated that the layers and materials described in association with to Figure 1, and as used throughout the present disclosure, are typically formed on or above an underlying semiconductor substrate or structure, such as underlying device layer(s) of an integrated circuit. In an embodiment, an underlying semiconductor substrate 102 represents a general workpiece object used to manufacture integrated circuits. The semiconductor substrate often includes a wafer or other piece of silicon or another semiconductor material. Suitable semiconductor substrates include, but are not limited to, single crystal silicon, polycrystalline silicon and silicon on insulator (SOI), as well as similar substrates formed of other semiconductor materials. The semiconductor substrate, depending on the stage of manufacture, often includes transistors,

integrated circuitry, and the like. The substrate may also include semiconductor materials, metals, dielectrics, dopants, and other materials commonly found in semiconductor substrates. In one embodiment, the illustrated structure depicted in Figure 1 is fabricated on underlying transistor or other semiconductor device layer(s) formed in or above the substrate 102. In
5 another embodiment, the illustrated structures depicted in Figure 1 are fabricated on underlying lower level interconnect layers formed above the substrate 102.

An insulating conductive oxide may be used to laterally electrically isolate electrodes of adjacent RRAM elements formed on a common conductive line. As an example, Figure 2A illustrates a plan view of a pair of RRAM elements integrated with a common line electrode, in
10 accordance with an embodiment of the present invention.

Referring to Figure 2A, a conductive interconnect housed in an ILD layer includes two RRAM stacks 300 thereon (e.g., stacks including layers 120/122/124 as described in association with Figure 1). Each RRAM stack 300 is disposed on a portion of an upper barrier layer 116 or a conductive fill material 114 of the conductive interconnect. The conductive interconnect in this
15 example is a conductive line coupled to a first and second RRAM stacks 300. An insulating metal oxide layer 128 laterally electrically isolates first electrode layers of the RRAM stacks 300.

An insulating conductive oxide may be used to laterally electrically isolate electrodes of adjacent RRAM elements formed on respective conductive vias. As an example, Figure 2B illustrates a plan view of a pair of RRAM elements integrated with discrete via electrodes, in
20 accordance with an embodiment of the present invention.

Referring to Figure 2B, a pair of conductive vias housed in an ILD layer each has a respective RRAM stack 310 thereon (e.g., stacks including layers 120/122/124 as described in association with Figure 1). Each via is discrete and includes an exposed upper barrier layer 116 or conductive fill material 114, on which a corresponding RRAM stack 310 is disposed. An
25 insulating metal oxide layer 128 laterally electrically isolates first electrode layers of the RRAM stacks 310.

A process flow may include fabrication of an insulating metal oxide layer by oxidation of a metal-containing layer for isolating, at least laterally, adjacent RRAM devices. As an example, Figure 3 illustrates cross-sectional views of various operations in a method of fabricating RRAM
30 devices separated by an insulating metal oxide layer, in accordance with an embodiment of the present invention.

Referring to part (a) of Figure 3, a method of fabricating a resistive random access memory (RRAM) device includes forming a conductive interconnect 106 in an inter-layer dielectric (ILD) layer 104 formed above a substrate 102. In an embodiment, the conductive
35 interconnect 106 includes an upper metal line 108 on a conductive via 110, as is depicted in part

(a) of Figure 3. In other embodiments, the conductive interconnect 106 is a uniform conductive via. In an embodiment, the conductive interconnect 106 is fabricated using a damascene or dual damascene integration process.

Referring to part (b) of Figure 3, a first electrode material layer 120' is formed over the
5 ILD layer 104 and over the conductive interconnect 106. A resistance switching material layer 122' is formed on the first electrode material layer 120'. A second electrode material layer 124' is formed on the resistance switching material layer 122'.

Referring to part (c) of Figure 3, the second electrode material layer 124' and the
10 resistance switching material layer 122' are etched to form a second electrode layer 124 and a resistance switching layer 122, respectively. In one such embodiment, the etching process involves first patterning of a resist layer and/or hardmask layer formed above the second electrode material layer 124'. As depicted, the etch stops on or with insubstantial impact to the first electrode material layer 120'.

In an embodiment, upper barrier layer 116 is a tantalum nitride layer. The first electrode
15 material layer 120' is a titanium nitride layer. In cases where an etch process further etches the titanium nitride electrode layer, the etch typically readily extends through the tantalum nitride barrier layer and undesirably exposes and erodes copper in the underlying interconnect. As such, in an embodiment, the etching of the second electrode material layer 124' and the resistance switching material layer 122' is performed in a manner that does not remove or etch a substantial
20 portion of the titanium nitride electrode layer, protecting underlying layers from the etch process.

Referring to part (d) of Figure 3, a dielectric sidewall spacer 126 is laterally adjacent to
and in contact with sidewalls of the second electrode layer 124 and the resistance switching layer 122. In one such embodiment, dielectric sidewall spacer 126 formation includes conformal deposition of a dielectric material and subsequent anisotropic etching to form the dielectric
25 sidewall spacer 126.

Referring to part (e) of Figure 3, portions of the first electrode material layer 120' not
covered by the second electrode layer 124 and the resistance switching layer 122 are oxidized to form insulating metal oxide regions 128 adjacent to a first electrode region 120. The first
30 electrode region 120 is beneath the second electrode layer 124 and the resistance switching layer 122. In an embodiment, the oxidizing is performed using an oxygen-based plasma process to form insulating metal oxide regions 128. In another embodiment, oxygen atoms are implanted into the first electrode material layer 120' and then an anneal process is performed to form insulating metal oxide regions 128.

In an embodiment, exposed regions of the first electrode material layer 120' immediately
35 adjacent the dielectric sidewall spacer 126 are not converted to insulating metal oxide regions

128, as is depicted in part (e) of Figure 3. In another embodiment, oxidizing portions of the first electrode material layer 120' further includes oxidizing outermost portions but not innermost portions of the first electrode material layer 120' covered by the second electrode layer 124 and the resistance switching layer 122, as is depicted in Figure 1. In either case, however, dielectric sidewall spacer 126 is used to dictate the extent and location of the formation of insulating metal oxide regions 128.

In an embodiment, oxidizing portions of the first electrode material layer 120' includes isolating the first electrode region 120 from an electrode layer of another RRAM element 118 laterally adjacent the first electrode region 120. In an embodiment, oxidizing portions of the first electrode material layer 120' includes modifying a titanium nitride material to form a titanium oxide material. In one such embodiment, the titanium nitride material is made highly resistive by oxidizing in an oxygen plasma.

A process flow may include fabrication of an insulating metal oxide layer by forming an opening in a metal-containing layer for isolating, at least laterally, adjacent RRAM devices. Figure 4 illustrates cross-sectional views of various operations in another method of fabricating RRAM devices separated by an insulating metal oxide layer, in accordance with another embodiment of the present invention.

Referring to part (a) of Figure 4, a method of fabricating a resistive random access memory (RRAM) device includes forming a conductive interconnect 106 in an inter-layer dielectric (ILD) layer 104 formed above a substrate 102. In an embodiment, the conductive interconnect 106 includes an upper metal line 108 on a conductive via 110, as is depicted in part (a) of Figure 4. In other embodiments, the conductive interconnect 106 is a uniform conductive via. In an embodiment, the conductive interconnect 106 is fabricated using a damascene or dual damascene integration process.

Referring again to part (a) of Figure 4, an insulating metal oxide layer 400 is formed over the conductive interconnect 106 and the ILD layer 104. In an embodiment, the insulating metal oxide layer 400 is formed by a chemical vapor deposition (CVD) or atomic layer deposition (ALD) process. In an embodiment, the insulating metal oxide layer 400 is a transition metal oxide layer such as, but not limited to, a titanium oxide layer, a zirconium oxide layer, or a tantalum oxide layer.

Referring to part (b) of Figure 4, an opening 404 is formed in the insulating metal oxide layer 404 to form patterned insulating metal oxide layer 402 and to expose at least a portion of an uppermost surface of the conductive interconnect 106.

Referring to part (c) of Figure 4, a first electrode layer 120 is formed in the opening 400, in contact with the uppermost surface of the conductive interconnect 106. A resistance switching

layer 122 is formed on the first electrode layer 120. A second electrode layer 124 is formed on the resistance switching layer 122. In an embodiment, the resistance switching layer 122 and the second electrode layer 124 are formed by first forming a second electrode material layer and a resistance switching material layer, and then etching the second electrode material layer and the resistance switching material layer to form the second electrode layer 124 and the resistance switching layer 122.

In an embodiment, the insulating metal oxide layer 400 (and, thus, the patterned insulating metal oxide layer 402) includes a metal species included in the first electrode layer 120. In another embodiment, the insulating metal oxide layer 400 includes a metal species not included in the first electrode layer. In one embodiment, the first electrode layer 120 is formed in the opening 404 by first forming a blanket first electrode material layer and then planarizing the blanket first electrode material layer to form the first electrode layer 120 confined to the opening 404.

Referring to part (d) of Figure 4, a dielectric sidewall spacer 126 is laterally adjacent to and in contact with sidewalls of the second electrode layer 124 and the resistance switching layer 122. In one such embodiment, dielectric sidewall spacer 126 formation includes conformal deposition of a dielectric material and subsequent anisotropic etching to form the dielectric sidewall spacer 126.

Referring to part (e) of Figure 4, an ILD layer 406 is formed over the structure of part (d) of Figure 4. Electrodes 408 are formed in the ILD layer 406 and contact the second electrode 124 of the RRAM stack 118. In one embodiment, the patterned insulating metal oxide layer 402 electrically isolates the first electrode layer 120 in a lateral direction, e.g., between two RRAM devices 118.

In an aspect, a conductive interconnect of an associated RRAM element stack may be coupled to a drain region of an underlying select transistor disposed on a substrate. As an example, Figure 5 illustrates a cross-sectional view of an RRAM element coupled to a drain side of a transistor selector, in accordance with an embodiment of the present invention.

Referring to Figure 5, a memory structure 500 includes a transistor 502 disposed in or above an active region 504 of a semiconductor substrate 506. The transistor 502 includes a gate electrode 508 with source/drain regions 510 on either side of the gate electrode 508, and in active region 504 of substrate 506. In an embodiment, the source/drain region 510 on the left-hand side of Figure 5 is a source region, and the source/drain region 510 on the right-hand side of Figure 5 is a drain region. An RRAM element 118 is coupled to the drain region of the transistor 502, but not to the source region of the transistor 502. The arrangement enables driving of the RRAM

element 118 by the drain side only. The RRAM element 118 and portions of the transistor 502 may be included in an inter-layer dielectric (ILD) layer 550, as is depicted in Figure 5.

The RRAM element 118 includes a top (second) electrode layer 124, a resistance switching layer 122, and a bottom (first) electrode layer 120. In an embodiment, the first
5 electrode layer 120 is electrically isolated in a lateral direction by an insulating metal oxide layer 128. The RRAM element 118 is, in an embodiment, included as an interrupting feature along a conductive drain contact 530. In one such embodiment, corresponding gate contact 534 and source contact 532 are not coupled to, or interrupted by the RRAM element 118, as is depicted in Figure 5. It is to be appreciated that although the RRAM element 118 is shown generically along
10 the drain contact 530 without a lateral reference, the actual layer in which the RRAM element 118 is included may be viewed as an interconnect layer (e.g., M1, M2, M3, M4, etc.) corresponding to a logic region in another area of the substrate 506. It is also to be appreciated that additional interconnect layer(s) may be formed on top of the structure 500 shown in Figure 5, e.g., using standard dual damascene process techniques that are well-known in the art.

15 In an embodiment, transistor 502 is a metal-oxide-semiconductor field-effect transistor (MOSFET or simply MOS transistor), fabricated on a substrate. In various implementations of the invention, the MOS transistors described herein may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors
20 such as nanoribbon and nanowire transistors.

In an embodiment, each MOS transistor includes a gate stack formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide (SiO₂) and/or a high-k dielectric material. The high-k dielectric material may include elements
25 such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide,
30 strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

The gate electrode layer of each MOS transistor is formed on the gate dielectric layer and may consist of at least one P-type workfunction metal or N-type workfunction metal, depending
35 on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the

gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a fill metal layer.

For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g.,
5 ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide.
10 An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV.

In some implementations, the gate electrode may consist of a “U”-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another
15 implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the invention, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of
20 one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

In some implementations of the invention, a pair of sidewall spacers 552 may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in
25 the art and generally include deposition and etching process steps. In an alternate implementation, a plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

As is well known in the art, source and drain regions are formed within the substrate adjacent to the gate stack of each MOS transistor. The source and drain regions are generally
30 formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to form recesses
35 at the locations of the source and drain regions. An epitaxial deposition process may then be

carried out to fill the recesses with material that is used to fabricate the source and drain regions. In some implementations, the source and drain regions may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some implementations the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In

5 further embodiments, the source and drain regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. And in further embodiments, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

To provide further context, integrating memory directly onto a microprocessor chip
10 would be advantageous since it enables higher operation speeds compared to having physically separate logic and memory chips. Unfortunately, traditional charge-based memory technologies such as DRAM and NAND Flash are now facing severe scalability issues related to increasingly precise charge placement and sensing requirements. As such, embedding charge-based memory directly onto a high performance logic chip is not very attractive for future technology nodes.

15 However, a memory technology that does have the potential to scale to much smaller geometries compared to traditional charge-based memories is resistive random access memory (RRAM), since it relies on resistivity rather than charge as the information carrier. However, in order to exploit the potential benefits of a high performance logic chip with embedded RRAM memory, an appropriate integrated logic plus RRAM structure and fabrication method is needed.

20 Embodiments of the present invention include such structures and fabrication processes.

Relating to one or more embodiments described herein, it is to be appreciated that traditional DRAM memory is facing severe scaling issues and, so, other types of memory devices are being actively explored in the electronics industry. One future contender is RRAM devices. Embodiments described herein include a fabrication method for embedding RRAM bit cell
25 arrays into a logic process technology. Embodiments described may be advantageous for processing schemes involving the fabrication of logic processors with embedded memory arrays.

In an aspect, an RRAM element may be included in an integrated circuit in regions typically referred to as back end or back end of line (BEOL) layers of the integrated circuit. As examples, Figure 6A illustrates schematic views of several options for positioning an RRAM
30 element in an integrated circuit, in accordance with an embodiment of the present invention.

Referring to Figure 6A, five examples (A)-(E) of an RRAM cell situated above a second metal logic layer (M2) or higher are provided. In each case, a memory region 600 and a logic region 602 of an integrated circuit are depicted schematically. Each memory region 600 and logic region 602 is associated with a corresponding transistor (or group of transistors) 604 or
35 606, respectively. Stacks of metallization layers (as housed in encompassing dielectric layer or

layers 697) include metal lines 608 and vias 610 that are generally alternating. Thus, all arrangements depicted include an RRAM element disposed above a second metal line (M2) in the stack. The RRAM element typically includes a resistance switching layer, such as a conductive oxide memory layer, sandwiched between a bottom electrode and a top electrode, and may be formed in an opening of an insulating layer. The described arrangements can enable integration of both logic and memory on a same die versus stand-alone memory. Although depicted at a very high level conceptual view for the sake of illustrating general placement options, it is to be appreciated that, in accordance with an embodiment of the present invention, elements labeled RRAM in Figure 6A may associated with an electrically insulating metal oxide material layer, examples of which are described above in association with Figure 1, 3 and 4.

Referring again to Figure 6A, in a first example (A), an RRAM element is fabricated on top of a unique via 650 intended for memory devices. In a second example (B), an RRAM element is fabricated first and an upper unique via 660 contacts the RRAM from above. In a third example (C), an RRAM element has a top electrode with an increased thickness such that the RRAM element occupies a full via depth, between metal lines. In a fourth example (D), an RRAM element has a top electrode with an increased thickness such that the RRAM element occupies a full metal line height. In a fifth example (E), an RRAM element has a top electrode with an increased thickness such that the RRAM element occupies a full interconnect level (via plus metal line). Accordingly, in an embodiment, an RRAM element or an array of RRAM elements can be embedded in a logic chip.

An RRAM array may be embedded in a logic chip. As an example, Figure 6B illustrates a cross-sectional view of a logic region together with an RRAM memory array integrated on a common substrate, in accordance with an embodiment of the present invention. Referring to Figure 6B, a structure 4000 includes a logic region 4020 and an RRAM array region 4040.

Referring to the RRAM array region 4040 of Figure 6B, in a first layer, metal 2 (M2) 4080 and via 1 (V1) 4100 structures are formed above a substrate 4060. The M2 4080 and V1 4100 structures are formed in an inter-layer dielectric layer 4120 disposed over an etch stop layer 4140.

Referring again to the RRAM array region 4040 of Figure 6B, in a second layer, a plurality of RRAM stacks 118 is formed in the inter-layer dielectric layer 4200 disposed over the etch stop layer 4220. The plurality of RRAM stacks 118 may be coupled to corresponding ones of the M2 4080 structures by a conductive layer 4240, as is depicted in Figure 6B. A dielectric spacer layer 126 may be formed on sidewalls of portions of the RRAM stacks, as is also depicted in Figure 6B. Each of the RRAM stacks 118 includes a first electrode layer 120, a switching layer 122, and a second electrode layer 124. A top electrode 4340 may also be included, as is

depicted in Figure 6B. In an embodiment, an insulating metal oxide layer electrically isolates first electrode layers 120 of the RRAM stacks 118 at least in a lateral direction.

Referring again to the RRAM array region 4040 of Figure 6B, in a third layer, an etch stop layer 4360 is disposed on the inter-layer dielectric layer 4200. Metal 4 (M4) 4380 and via to memory 4400 structures are formed in the inter-layer dielectric layer 4420 disposed over the etch stop layer 4360. It is to be appreciated that additional interconnect layer(s) may be formed on top of the M4/via to memory layers of the RRAM array region 4040 of Figure 6B, e.g., using standard dual damascene process techniques that are well-known in the art.

It is to be appreciated that although the RRAM stacks may actually include multiple layers of very thin films, for the sake of simplicity the RRAM stacks 118 are depicted as described above. It is also to be appreciated that although in the illustrations the RRAM stacks are shown embedded into a corresponding logic metal 3 (M3) layer, they may instead be embedded into some other interconnect layer (e.g., M1, M2, M4, etc.)

Referring again to Figure 6B, in an embodiment, the conductive metal layer 4240 is a tantalum nitride (TaN) layer. In one embodiment, the conductive metal layer 4240 is referred to as a “thin via” layer. In an embodiment, the top electrode 4340 is composed of a material or stack of materials suitable for electrically contacting the RRAM stack 118. In an embodiment, the top electrode 4340 is a topographically smooth electrode. In one such embodiment, the top electrode 4340 has a thickness suitable for good conductivity but has little to no columnar structure formation that would otherwise lead to a rough top surface. Such a topographically smooth electrode may be referred to as amorphous in structure. In an embodiment, the top electrode 4340 begins as a hardmask layer, such as a titanium nitride hardmask layer, used for patterning the RRAM stack and is ultimately retained as a conductive contact.

Referring now to the logic region 4020 of Figure 6B, in the first layer, metal 2 (M2) 4500 and via 1 (V1) 4520 structures are formed in the inter-layer dielectric layer 4120 disposed over the etch stop layer 4140. In the second layer, the etch stop layer 4220 is disposed on the inter-layer dielectric layer 4120. Metal 3 (M3) 4540 and via 2 (V2) 4560 structures are formed in the inter-layer dielectric layer 4200 disposed over the etch stop layer 4220. In the third layer, the etch stop layer 4360 is disposed on the inter-layer dielectric layer 4200. Metal 4 (M4) 4580 and via 3 (V3) 4600 structures are formed in the inter-layer dielectric layer 4420 disposed over the etch stop layer 4360. It is to be appreciated that additional interconnect layer(s) may be formed on top of the M4/V3 layers of the logic region 4020 of Figure 6B, e.g., using standard dual damascene process techniques that are well-known in the art.

In another aspect, upon fabrication of an RRAM element associated with an insulating metal oxide material layer, the RRAM may be subjected to an intentional one-time “break-down”

process for filament formation in the resulting RRAM device fabricated from the RRRAM memory element. To illustrate the above aspect, Figures 7A and 7B illustrate a schematic and corresponding I-V plot, respectively, demonstrating concepts involved with filament formation in an RRAM element, in accordance with an embodiment of the present invention.

5 Referring to Figure 7A, a material stack 700 includes a bottom electrode (BE) 702, an oxide layer 704 such a hafnium oxide layer (HfO_2 , which may be considered a dielectric oxide layer), and a top electrode (TE) 706. Oxide vacancies 708 may be depicted as circles in Figure 7A. Oxide RRAM cell filament formation begins with a stoichiometric oxide layer 704 which is subjected to a forming (soft breakdown) operation (1) to provide a low resistance state (LRS). A
10 first reset operation (2) is then performed to provide switching to a high resistance state (HRS). A set operation (3) is then performed to return to the LRS. Performing operations (1)-(3) involves motion of oxygen vacancies and redox phenomena. Plot 710 of Figure 7B illustrates the I-V characteristics association with operations (1), (2) and (3) of Figure 7A.

In another aspect, an RRAM element or device may be an anionic-based conductive
15 oxide memory element. Figure 8 illustrates an operational schematic representing a changing of states for an anionic-based metal-conductive oxide-metal RRAM memory element, in accordance with an embodiment of the present invention. Referring to Figure 8, a memory element 800 includes an electrode/conductive oxide/electrode material stack. The memory element 800 may begin in a less conductive state (1), with the conductive oxide layer being in a less conductive
20 state 804A. An electrical pulse, such as a duration of a positive bias (2) may be applied to provide memory element 800 in a more conductive state (3), with the conductive oxide layer being in a more conductive state 804B. An electrical pulse, such as a duration of a negative bias (4) may be applied to again provide memory element 600 having the less conductive state (1). Thus, electrical pulsing may be used to change resistance of the memory element 800.

25 As such, in an embodiment, a memory element includes an anionic-based conductive oxide layer sandwiched between two electrodes. Resistivity of the conductive oxide layer in low field (when device is read) is, in some embodiments, in the range found typical of conductive films of metal compounds, e.g. TiAlN . For example, in a specific embodiment, the resistivity for such a layer is approximately in the range of $0.1 \text{ Ohm cm} - 10 \text{ kOhm cm}$ when measured at low
30 field. Resistivity of the film is tuned depending in the memory element size to achieve final resistance value in the range compatible with fast read. Composition of the conductive oxide layer may be tuned in such a way that a small change in its composition results in a large change in resistance. Resistance change occurs, in some embodiments, due to a Mott transition, e.g., when injected/extracted charge causes phase transition in the conductive oxide layer between

more and less resistive phase configurations. In other embodiments, the resistance change can be induced by changing the concentration of oxygen vacancies in the conductive oxide layer.

As an example of one approach, Figure 9 illustrates a schematic representation of resistance change in an anionic-based conductive oxide layer induced by changing the concentration of oxygen vacancies in the conductive oxide layer, in accordance with an embodiment of the present invention. Referring to Figure 9, a memory element 900 is shown as deposited (A). The memory element includes a conductive oxide layer 904 between a palladium (Pd) electrode 902 and a tungsten (W) electrode 906. Oxygen atoms and oxygen vacancies may be distributed as shown in (A). Referring to (B) of Figure 9, upon application of a positive bias, the memory element 900 can be made more conductive. In that state, oxygen atoms migrate to the electrode 906, while vacancies remain throughout the layer 904. Referring to (C) of Figure 9, upon application of a negative bias, the memory element can be made less conductive. That that state, oxygen atoms are distributed more evenly throughout layer 904. Accordingly, in an embodiment, effective composition (e.g., the location of oxygen atoms versus vacancies) of a conductive oxide layer is modified to change resistance of a memory element. In a specific embodiment, an applied electrical field, which drives such compositional change, is tuned to values approximately in the range of $1e6$ - $1e7$ V/cm. Referring again to Figure 9, although surface stage are demonstrated, it is to be appreciated that if filament formation is used, such as described in association with Figures 7A and 7B, vacancies will penetrate the film to a greater extent.

As mentioned briefly above, in an embodiment, one electrode in a memory element including an anionic-based conductive oxide layer is a noble metal based electrode, while the other electrode in is a transition metal for which some of the lower valence oxides are conductive (e.g., to act as an oxygen reservoir). That is, when oxygen atoms migrate to the transition metal oxide, the resulting interfacial transition metal oxide formed remains conductive. Examples of suitable transition metals which form conductive oxides include but are not limited to, W, V, Cr, or Ir. In other embodiments, one or both of the electrodes is fabricated from an electro-chromic material. In other embodiments, one or both of the electrodes is fabricated from a second, different conductive oxide material. In an embodiment, examples of suitable conductive oxides include, but are not limited to: ITO ($In_2O_{3-x}SnO_{2-x}$), In_2O_{3-x} , sub-stoichiometric yttria doped zirconia ($Y_2O_{3-x}ZrO_{2-x}$), or $La_{1-x}Sr_xGa_{1-y}Mg_yO_{3-x-0.5(x+y)}$. In another embodiment, the conductive oxide layer is composed of a material with two or more metal elements (e.g., as contrasted to common RRAM memories using one metal such as found in binary oxides, such as HfO_x or TaO_x). In such ternary, quaternary, etc. alloys, the metals used are from adjacent columns of the periodic table. Specific examples of suitable such conductive oxides include, but are not limited

to: Y and Zr in $Y_2O_{3-x}ZrO_{2-x}$, In and Sn in $In_2O_{3-x}SnO_{2-x}$, or Sr and La in $La_{1-x}Sr_xGa_{1-y}Mg_yO_3$. Such materials may be viewed as compositions selected to have aliovalent substitution to significantly increase the number of oxygen vacancies. It is to be appreciated that in some embodiments the change of resistance of such electrode during programming can contribute to the total resistance change.

In an embodiment, examples of suitable noble metals include, but are not limited to Pd or Pt. In a specific embodiment, a more complex, yet still all-conductive, stack includes an approximately 10nm Pd first electrode layer, an approximately 3nm In_2O_{3-x} and/or SnO_{2-x} conductive oxide layer, and a second electrode stack composed of approximately 20nm tungsten/10nm Pd/100nm TiN/55nm W.

In another aspect, an RRAM element or device may be a cationic-based conductive oxide memory element. As an example, Figure 10 illustrates an operational schematic representing a changing of states for a cationic-based metal-conductive oxide-metal RRAM memory element, in accordance with an embodiment of the present invention. Referring to Figure 10, memory element 1000 may begin in a more conductive state (1), with a cationic-based conductive oxide layer being in a more conductive state 1004A. An electrical pulse, such as a duration of a positive bias (2) may be applied to provide memory element 1000 in a less conductive state (3), with the cationic-based conductive oxide layer being in a less conductive state 1004B. An electrical pulse, such as a duration of a negative bias (4) may be applied to again provide memory element 1000 having the more conductive state (1). Thus, electrical pulsing may be used to change resistance of the memory element 1000. Polarity applied is such as to attract active cations of in the memory layer to the intercalation electrode under negative bias.

As such, in an embodiment, a memory element includes a cationic-based conductive oxide layer sandwiched between two electrodes. Resistivity of the cationic-based conductive oxide layer in low field (when device is read) is, in some embodiments, can be as low as found typical of conductive films of metal compounds, e.g. TiAlN. For example, in a specific embodiment, the resistivity for such a layer is approximately in the range of 0.1 Ohm cm – 10 kOhm cm when measured at low field (measured for the specific thickness used in the stack). Resistivity of the film is tuned depending in the memory element size to achieve final resistance value in the range compatible with fast read.

As an example of one approach, Figure 11 illustrates a schematic representation of resistance change in a cationic-based conductive oxide layer induced by changing the concentration of cation vacancies (such as lithium cation vacancies) in the conductive oxide layer, in accordance with an embodiment of the present invention.

Referring to Figure 11, a memory element 1100 is shown as deposited (A). The memory element includes a cationic-based conductive oxide layer 1104 between a bottom electrode 1102 and a top electrode 1106. In a specific example, the layer 1104 is a lithium cobalt oxide layer, described in greater details below, and lithium atoms and lithium vacancies are distributed as shown in (A). Referring to (B) of Figure 11, upon application of a negative bias, the memory element 1100 can be made more conductive. In that state, lithium atoms migrate to the top electrode 1106, while vacancies remain throughout the layer 1104. Referring to (C) of Figure 11, upon application of a positive bias to one of the electrodes, the memory element can be made less conductive. In that state, lithium atoms are distributed more evenly throughout layer 1104.

Accordingly, in an embodiment, effective composition (e.g., the location of lithium atoms (or cations) versus vacancies) of a cationic-based conductive oxide layer is modified to change resistance of a memory element, in some embodiments due to stoichiometry-induced Mott transition. In a specific embodiment, an applied electrical field, which drives such compositional change during write operation, is tuned to values approximately in the range of $1\text{e}6\text{-}1\text{e}7$ V/cm.

In an embodiment, referring again to Figure 11, the cationic-based conductive oxide layer 1104 is composed of a material suitable for cation-based mobility within the layer itself. In a specific exemplary embodiment, layer 1104 of Figure 11 part (A) is composed of lithium cobalt oxide (LiCoO_2). Then, in part (B), the corresponding layer becomes lithium deficient (e.g., $\text{Li}_{<0.75}\text{CoO}_2$) when a negative bias is applied and lithium atoms (e.g., as cations) migrate toward electrode 1106. By contrast, in part (C), the corresponding layer becomes lithium rich (e.g., $\text{Li}_{>0.95}\text{CoO}_2$) when a positive bias is applied and lithium atoms (e.g., as cations) migrate away from electrode 1106. In other embodiments, other suitable compositions with cationic conductivity include, but are not limited to, LiMnO_2 , $\text{Li}_4\text{TiO}_{12}$, LiNiO_2 , LiNbO_3 , $\text{Li}_3\text{N:H}$, LiTiS_2 (all of which are lithium atom or Li^+ mobility based), Na β -alumina (which is sodium atom or Na^+ mobility based), or AgI , RbAg_4I_5 , AgGeAsS_3 (all of which are silver atom or Ag^+ mobility based). In general, these examples provide materials based on cation mobility or migration, which is typically much faster than anionic-based mobility or migration (e.g., for oxygen atoms or O^{2-} anions).

In an embodiment, referring again to Figure 11, one electrode (e.g., bottom electrode 1102) in a memory element including a cationic conductive oxide layer is a noble metal based electrode. In one embodiment, examples of suitable noble metals include, but are not limited to palladium (Pd) or platinum (Pt). In a specific embodiment, a memory stack includes a bottom electrode composed of an approximately 10 nanometer thick Pd layer. It is to be understood that use of the terms “bottom” and “top” for electrodes 1102 and 1106 need only be relative and are not necessarily absolute with respect to, e.g., an underlying substrate.

In an embodiment, referring again to Figure 11, the other electrode (e.g., top electrode 1106) in a memory element including a cationic conductive oxide layer is an “intercalation host” for migrating cations. The material of the top electrode is a host in a sense that the material is conductive with or without the presence of the migrating cations and is not substantially altered in the absence or presence of the migrating cations. In an exemplary embodiment, the top electrode is composed of a material such as, but not limited to, graphite, or metal chalcogenides such as disulfides (e.g., TaS₂). Such materials are conductive as well as absorbing of cations such as Li⁺. This is in contrast to an electrode for an anionic based conductive oxide which may include a metal with a corresponding conductive oxide to accommodate migrating oxygen atoms or anions.

Referring again to the description associated with Figures 8-11 above, a stack of conductive layers including a conductive metal oxide layer may be used to fabricate as memory bit cell. For example, Figure 12 illustrates a schematic of a memory bit cell 1200 which includes a metal-conductive oxide-metal RRAM memory element 1210, in accordance with an embodiment of the present invention. Such an RRAM memory element may be suitable for manufacture on a substrate in common with logic regions of the substrate.

Referring to Figure 12, the RRAM memory element 1210 may include a first conductive electrode 1212 with a conductive metal oxide layer 1214 adjacent the first conductive electrode 1212. A second conductive electrode 1216 is adjacent the conductive metal oxide layer 1214. The second conductive electrode 1216 may be electrically connected to a bit line 1232. The first conductive electrode 1212 may be coupled with a transistor 1234. The transistor 1234 may be coupled with a wordline 1236 and a source line 1238 in a manner that will be understood to those skilled in the art. The memory bit cell 1200 may further include additional read and write circuitry (not shown), a sense amplifier (not shown), a bit line reference (not shown), and the like, as will be understood by those skilled in the art, for the operation of the memory bit cell 1200. It is to be appreciated that a plurality of the memory bit cells 1200 may be operably connected to one another to form a memory array, wherein the memory array can be incorporated into a non-volatile memory region of a substrate in common with a logic region. It is to be appreciated that the transistor 1234 may be connected to the second conductive electrode 1216 or the first conductive electrode 1212, although only the latter is shown. In accordance with an embodiment of the present invention, one of the second conductive electrode 1216 or the first conductive electrode 1212 is laterally adjacent an insulating metal oxide layer.

Figure 13 illustrates a block diagram of an electronic system 1300, in accordance with an embodiment of the present invention. The electronic system 1300 can correspond to, for example, a portable system, a computer system, a process control system, or any other system

that utilizes a processor and an associated memory. The electronic system 1300 may include a microprocessor 1302 (having a processor 1304 and control unit 1306), a memory device 1308, and an input/output device 1310 (it is to be appreciated that the electronic system 1300 may have a plurality of processors, control units, memory device units and/or input/output devices in various embodiments). In one embodiment, the electronic system 1300 has a set of instructions that define operations which are to be performed on data by the processor 1304, as well as, other transactions between the processor 1304, the memory device 1308, and the input/output device 1310. The control unit 1306 coordinates the operations of the processor 1304, the memory device 1308 and the input/output device 1310 by cycling through a set of operations that cause instructions to be retrieved from the memory device 1308 and executed. The memory device 1308 can include a memory element having a conductive oxide and electrode stack as described in the present description. In an embodiment, the memory device 1308 is embedded in the microprocessor 1302, as depicted in Figure 13. In an embodiment, the processor 1304, or another component of electronic system 1300, includes an array of BEOL-compatible RRAM devices.

Figure 14 illustrates a computing device 1400 in accordance with one embodiment of the invention. The computing device 1400 houses a board 1402. The board 1402 may include a number of components, including but not limited to a processor 1404 and at least one communication chip 1406. The processor 1404 is physically and electrically coupled to the board 1402. In some implementations the at least one communication chip 1406 is also physically and electrically coupled to the board 1402. In further implementations, the communication chip 1406 is part of the processor 1404.

Depending on its applications, computing device 1400 may include other components that may or may not be physically and electrically coupled to the board 1402. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communication chip 1406 enables wireless communications for the transfer of data to and from the computing device 1400. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires,

although in some embodiments they might not. The communication chip 1406 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 1400 may include a plurality of communication chips 1406. For instance, a first communication chip 1406 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1206 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 1404 of the computing device 1400 includes an integrated circuit die packaged within the processor 1404. In some implementations of embodiments of the invention, the integrated circuit die of the processor includes one or more arrays, such as RRAM memory arrays integrated into a logic processor, built in accordance with embodiments of the present invention. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 1406 also includes an integrated circuit die packaged within the communication chip 1406. In accordance with another implementation of an embodiment of the invention, the integrated circuit die of the communication chip includes RRAM memory arrays integrated into a logic processor, built in accordance with embodiments of the present invention.

In further implementations, another component housed within the computing device 1400 may contain a stand-alone integrated circuit memory die that includes one or more arrays, such as RRAM memory arrays integrated into a logic processor, built in accordance with embodiments of the present invention.

In various implementations, the computing device 1400 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 1400 may be any other electronic device that processes data.

Accordingly, one or more embodiments of the present invention relate generally to the fabrication of embedded microelectronic memory. The microelectronic memory may be non-volatile, wherein the memory can retain stored information even when not powered. One or more embodiments of the present invention relate to the fabrication of RRAM memory arrays

integrated into a logic processor. Such arrays may be used in an embedded non-volatile memory, either for its non-volatility, or as a replacement for embedded dynamic random access memory (eDRAM). For example, such an array may be used for 1T-1R memory or 2T-1R memory (R = resistor) at competitive cell sizes within a given technology node.

5 Figure 15 illustrates an interposer 1500 that includes one or more embodiments of the invention. The interposer 1500 is an intervening substrate used to bridge a first substrate 1502 to a second substrate 1504. The first substrate 1502 may be, for instance, an integrated circuit die. The second substrate 1504 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 1500 is to spread a
10 connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 1500 may couple an integrated circuit die to a ball grid array (BGA) 1506 that can subsequently be coupled to the second substrate 1504. In some embodiments, the first and second substrates 1502/1504 are attached to opposing sides of the interposer 1500. In other embodiments, the first and second substrates 1502/1504 are attached to the same side of the
15 interposer 1500. And in further embodiments, three or more substrates are interconnected by way of the interposer 1500.

 The interposer 1500 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same
20 materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

 The interposer may include metal interconnects 1508 and vias 1510, including but not limited to through-silicon vias (TSVs) 1512. The interposer 1500 may further include embedded devices 1514, including both passive and active devices. Such devices include, but are not
25 limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 1500. In accordance with
 embodiments of the invention, apparatuses or processes disclosed herein may be used in the
30 fabrication of interposer 1500.

 Thus, embodiments of the present invention include approaches for fabricating back end of line (BEOL)-compatible resistive random access memory (RRAM) elements and devices, and the resulting structures.

 In an embodiment, a resistive random access memory (RRAM) device includes a
35 conductive interconnect disposed in an inter-layer dielectric (ILD) layer disposed above a

substrate. The ILD layer has an uppermost surface substantially co-planar with an uppermost surface of the conductive interconnect. An RRAM element is disposed on the conductive interconnect. The RRAM element includes a first electrode layer disposed on the uppermost surface of the conductive interconnect, a resistance switching layer disposed on the first electrode layer, and a second electrode layer disposed on the resistance switching layer. An insulating metal oxide layer is disposed on the uppermost surface of the ILD layer and laterally adjacent to and in contact with the first electrode layer.

In one embodiment, the insulating metal oxide layer electrically isolates the first electrode layer from a first electrode layer of a second RRAM element laterally adjacent to the RRAM element on the uppermost surface of the ILD layer.

In one embodiment, the first electrode layer extends onto a portion of the uppermost surface of the ILD layer.

In one embodiment, the resistance switching layer has a width greater than a width of the first electrode layer, and the resistance switching layer extends onto a portion of an uppermost surface of the insulating metal oxide layer.

In one embodiment, the second electrode layer has a width approximately the same as the width of the resistance switching layer.

In one embodiment, the RRAM device further includes a dielectric sidewall spacer laterally adjacent to and in contact with sidewalls of the second electrode layer and the resistance switching layer, the dielectric sidewall spacer disposed on a portion of the uppermost surface of the insulating metal oxide layer.

In one embodiment, the insulating metal oxide layer and the first electrode layer include a same metal species.

In one embodiment, the metal species is titanium (Ti).

In one embodiment, the insulating metal oxide layer includes titanium oxide, and the first electrode layer includes titanium nitride.

In one embodiment, the conductive interconnect is a conductive line further coupled to a second RRAM element.

In one embodiment, the conductive interconnect is a conductive via.

In one embodiment, the conductive interconnect includes a conductive fill material surrounded by a barrier layer.

In one embodiment, the conductive interconnect is coupled to a drain region of an underlying select transistor disposed on the substrate.

In an embodiment, a method of fabricating a resistive random access memory (RRAM) device includes forming a conductive interconnect in an inter-layer dielectric (ILD) layer formed

above a substrate. A first electrode material layer is formed over the ILD layer and over the conductive interconnect. A resistance switching material layer is formed on the first electrode material layer. A second electrode material layer is formed on the resistance switching material layer. The second electrode material layer and the resistance switching material layer are etched to form a second electrode layer and a resistance switching layer, respectively. Portions of the first electrode material layer not covered by the second electrode layer and the resistance switching layer are oxidized to form insulating metal oxide regions adjacent to a first electrode region, the first electrode region beneath the second electrode layer and the resistance switching layer.

In one embodiment, the method further includes, subsequent to etching the second electrode material layer and the resistance switching material layer and prior to oxidizing portions of the first electrode material layer, forming a dielectric sidewall spacer laterally adjacent to and in contact with sidewalls of the second electrode layer and the resistance switching layer.

In one embodiment, oxidizing portions of the first electrode material layer further includes oxidizing outermost portions but not innermost portions of the first electrode material layer covered by the second electrode layer and the resistance switching layer.

In one embodiment, oxidizing portions of the first electrode material layer includes modifying a titanium nitride material to form a titanium oxide material.

In one embodiment, oxidizing portions of the first electrode material layer includes isolating the first electrode region from an electrode layer of an RRAM element laterally adjacent to the first electrode region.

In an embodiment, a method of fabricating a resistive random access memory (RRAM) device includes forming a conductive interconnect in an inter-layer dielectric (ILD) layer formed above a substrate. An insulating metal oxide layer is formed over the conductive interconnect and the ILD layer. An opening is formed in the insulating metal oxide layer to expose at least a portion of an uppermost surface of the conductive interconnect. A first electrode layer is formed in the opening, in contact with the uppermost surface of the conductive interconnect. A resistance switching layer is formed on the first electrode layer. A second electrode layer is formed on the resistance switching layer.

In one embodiment, forming the resistance switching layer and the second electrode layer includes forming a second electrode material layer and a resistance switching material layer, and then etching the second electrode material layer and the resistance switching material layer to form the second electrode layer and the resistance switching layer.

In one embodiment, the method further includes, subsequent to etching the second electrode material layer and the resistance switching material layer, forming a dielectric sidewall spacer laterally adjacent to and in contact with sidewalls of the second electrode layer and the resistance switching layer.

5 In one embodiment, the insulating metal oxide layer includes a metal species included in the first electrode layer.

In one embodiment, the insulating metal oxide layer includes a metal species not included in the first electrode layer.

10 In one embodiment, forming the first electrode layer in the opening includes forming a blanket first electrode material layer and then planarizing the blanket first electrode material layer to form the first electrode layer confined to the opening.

In one embodiment, the insulating metal oxide layer electrically isolates the first electrode layer in a lateral direction.

CLAIMS

What is claimed is:

1. A resistive random access memory (RRAM) device, comprising:
 - 5 a conductive interconnect disposed in an inter-layer dielectric (ILD) layer disposed above a substrate, the ILD layer having an uppermost surface substantially co-planar with an uppermost surface of the conductive interconnect;
 - an RRAM element disposed on the conductive interconnect, the RRAM element comprising:
 - 10 a first electrode layer disposed on the uppermost surface of the conductive interconnect;
 - a resistance switching layer disposed on the first electrode layer; and
 - a second electrode layer disposed on the resistance switching layer; and
 - an insulating metal oxide layer disposed on the uppermost surface of the ILD layer and laterally adjacent to and in contact with the first electrode layer.
- 15 2. The RRAM device of claim 1, wherein the insulating metal oxide layer electrically isolates the first electrode layer from a first electrode layer of a second RRAM element laterally adjacent to the RRAM element on the uppermost surface of the ILD layer.
- 20 3. The RRAM device of claim 1, wherein the first electrode layer extends onto a portion of the uppermost surface of the ILD layer.
4. The RRAM device of claim 3, wherein the resistance switching layer has a width greater than a width of the first electrode layer, and wherein the resistance switching layer extends onto a
25 portion of an uppermost surface of the insulating metal oxide layer.
5. The RRAM device of claim 4, wherein the second electrode layer has a width approximately the same as the width of the resistance switching layer.
- 30 6. The RRAM device of claim 5, further comprising:
 - a dielectric sidewall spacer laterally adjacent to and in contact with sidewalls of the second electrode layer and the resistance switching layer, the dielectric sidewall spacer disposed on a portion of the uppermost surface of the insulating metal oxide layer.

7. The RRAM device of claim 1, wherein the insulating metal oxide layer and the first electrode layer comprise a same metal species.
8. The RRAM device of claim 7, wherein the metal species is titanium (Ti).
- 5 9. The RRAM device of claim 8, wherein the insulating metal oxide layer comprises titanium oxide, and wherein the first electrode layer comprises titanium nitride.
- 10 10. The RRAM device of claim 1, wherein the conductive interconnect is a conductive line further coupled to a second RRAM element.
11. The RRAM device of claim 1, wherein the conductive interconnect is a conductive via.
12. The RRAM device of claim 1, wherein the conductive interconnect comprises a conductive
15 fill material surrounded by a barrier layer.
13. The RRAM device of claim 1, wherein the conductive interconnect is coupled to a drain region of an underlying select transistor disposed on the substrate.
- 20 14. A method of fabricating a resistive random access memory (RRAM) device, the method comprising:
forming a conductive interconnect in an inter-layer dielectric (ILD) layer formed above a substrate;
forming a first electrode material layer over the ILD layer and over the conductive
25 interconnect;
forming a resistance switching material layer on the first electrode material layer;
forming a second electrode material layer on the resistance switching material layer;
etching the second electrode material layer and the resistance switching material layer to form
a second electrode layer and a resistance switching layer, respectively; and
30 oxidizing portions of the first electrode material layer not covered by the second electrode layer and the resistance switching layer to form insulating metal oxide regions adjacent to a first electrode region, the first electrode region beneath the second electrode layer and the resistance switching layer.
- 35 15. The method of claim 14, further comprising:

subsequent to etching the second electrode material layer and the resistance switching material layer and prior to oxidizing portions of the first electrode material layer, forming a dielectric sidewall spacer laterally adjacent to and in contact with sidewalls of the second electrode layer and the resistance switching layer.

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16. The method of claim 14, wherein oxidizing portions of the first electrode material layer further comprises oxidizing outermost portions but not innermost portions of the first electrode material layer covered by the second electrode layer and the resistance switching layer.

10 17. The method of claim 14, wherein oxidizing portions of the first electrode material layer comprises modifying a titanium nitride material to form a titanium oxide material.

18. The method of claim 14, wherein oxidizing portions of the first electrode material layer comprises isolating the first electrode region from an electrode layer of an RRAM element
15 laterally adjacent the first electrode region.

19. A method of fabricating a resistive random access memory (RRAM) device, the method comprising:

forming a conductive interconnect in an inter-layer dielectric (ILD) layer formed above a
20 substrate;
forming an insulating metal oxide layer over the conductive interconnect and the ILD layer;
forming an opening in the insulating metal oxide layer to expose at least a portion of an uppermost surface of the conductive interconnect;
forming a first electrode layer in the opening, in contact with the uppermost surface of the
25 conductive interconnect;
forming a resistance switching layer on the first electrode layer; and
forming a second electrode layer on the resistance switching layer.

20. The method of claim 19, wherein forming the resistance switching layer and the second
30 electrode layer comprises forming a second electrode material layer and a resistance switching material layer, and then etching the second electrode material layer and the resistance switching material layer to form the second electrode layer and the resistance switching layer.

21. The method of claim 19, further comprising:

subsequent to etching the second electrode material layer and the resistance switching material layer, forming a dielectric sidewall spacer laterally adjacent to and in contact with sidewalls of the second electrode layer and the resistance switching layer.

5 22. The method of claim 19, wherein the insulating metal oxide layer comprises a metal species included in the first electrode layer.

23. The method of claim 19, wherein the insulating metal oxide layer comprises a metal species not included in the first electrode layer.

10 24. The method of claim 19, wherein forming the first electrode layer in the opening comprises forming a blanket first electrode material layer and then planarizing the blanket first electrode material layer to form the first electrode layer confined to the opening.

15 25. The method of claim 19, wherein the insulating metal oxide layer electrically isolates the first electrode layer in a lateral direction.

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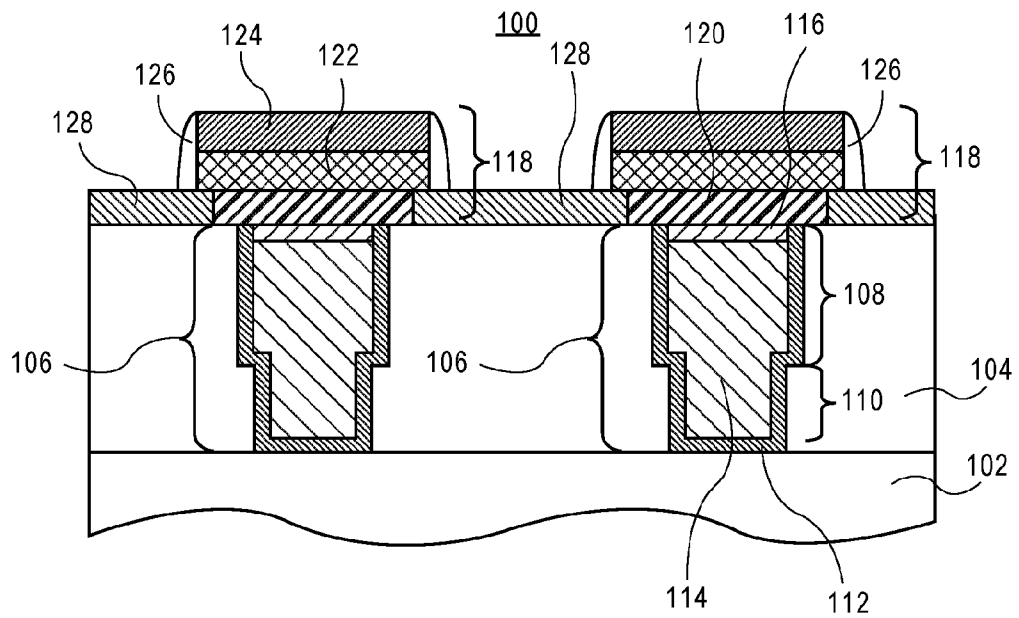


FIG. 1

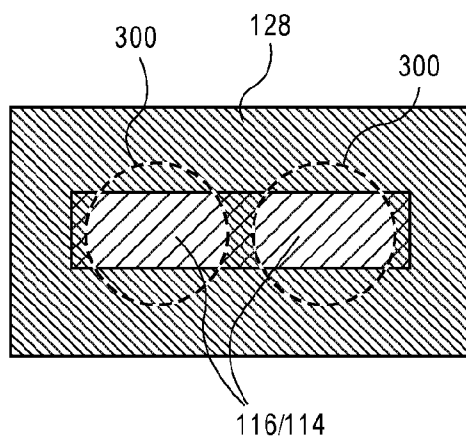


FIG. 2A

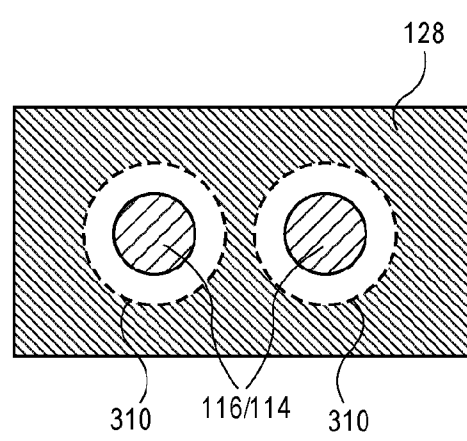


FIG. 2B

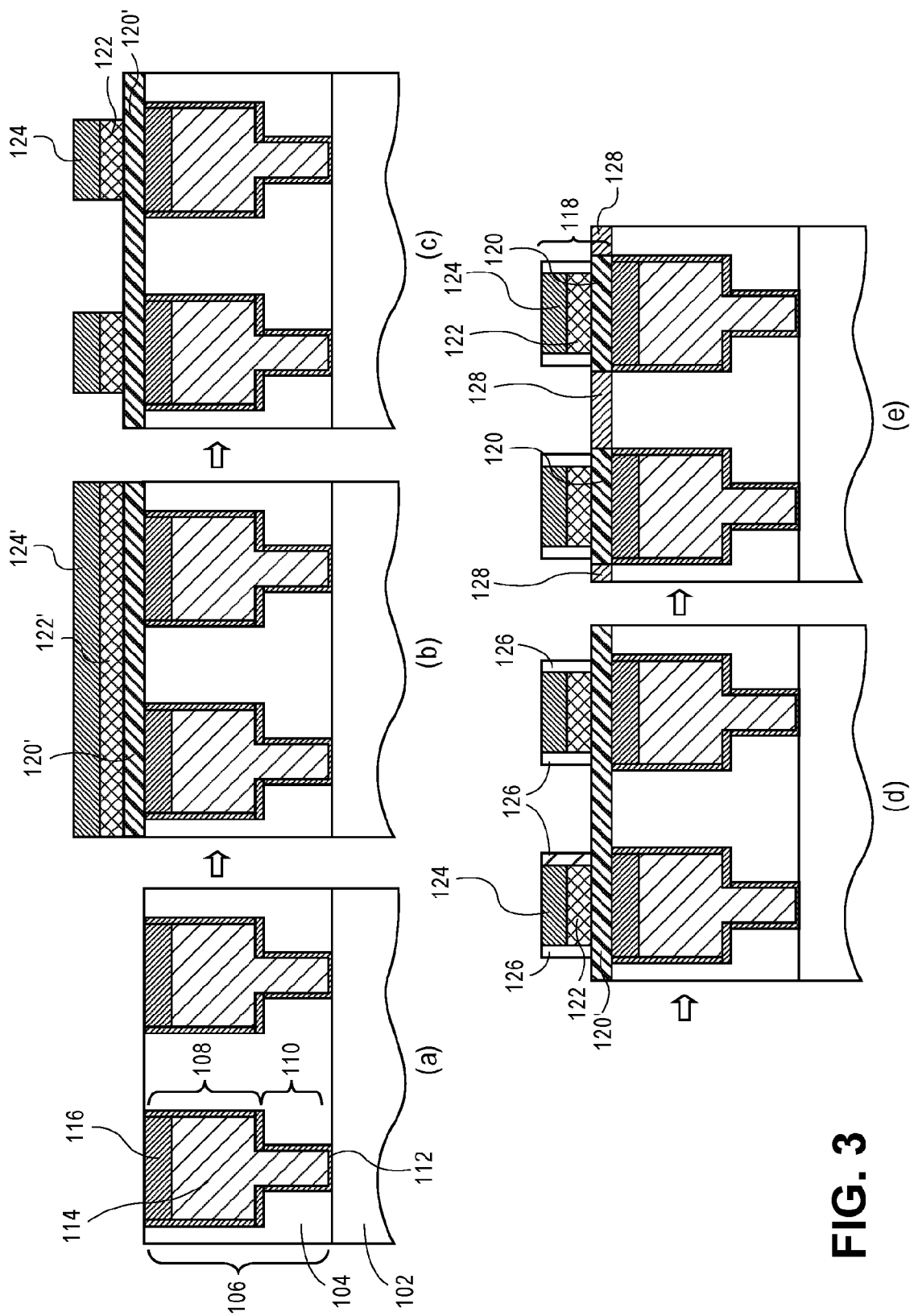


FIG. 3

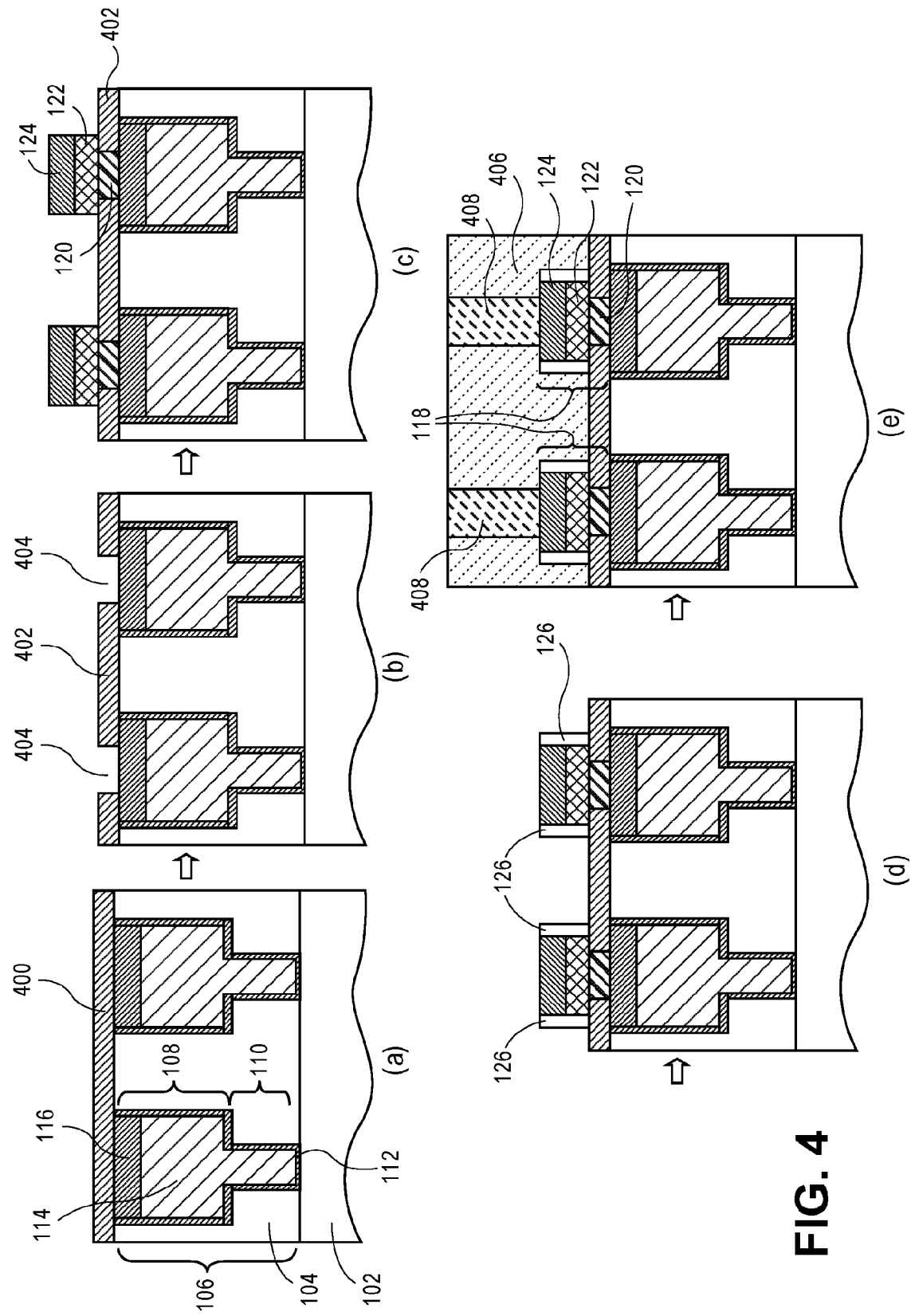


FIG. 4

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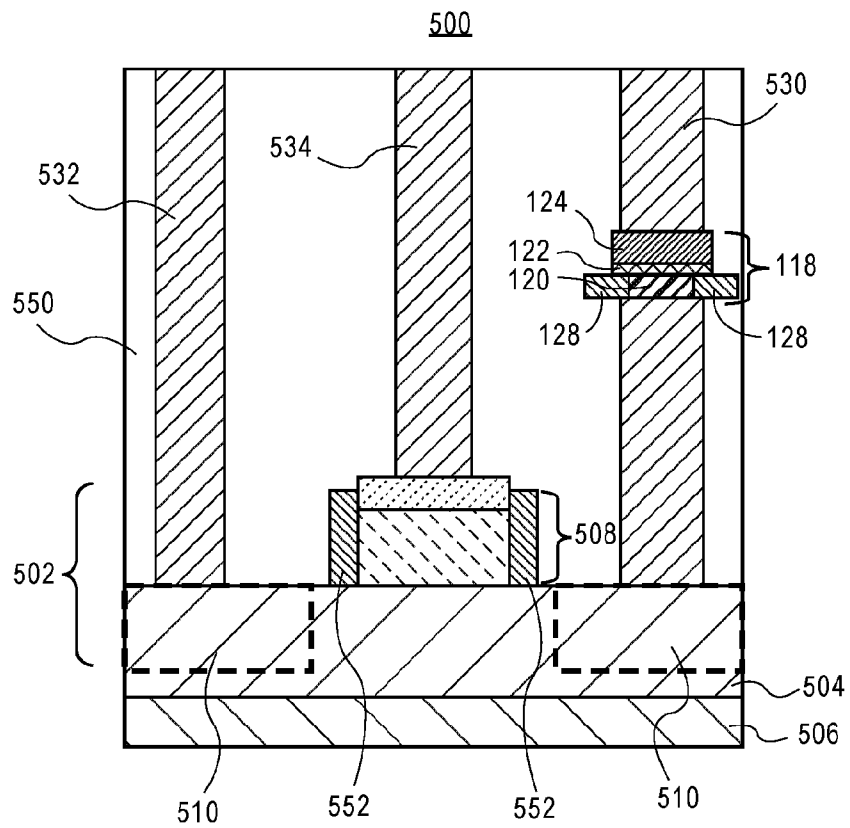


FIG. 5

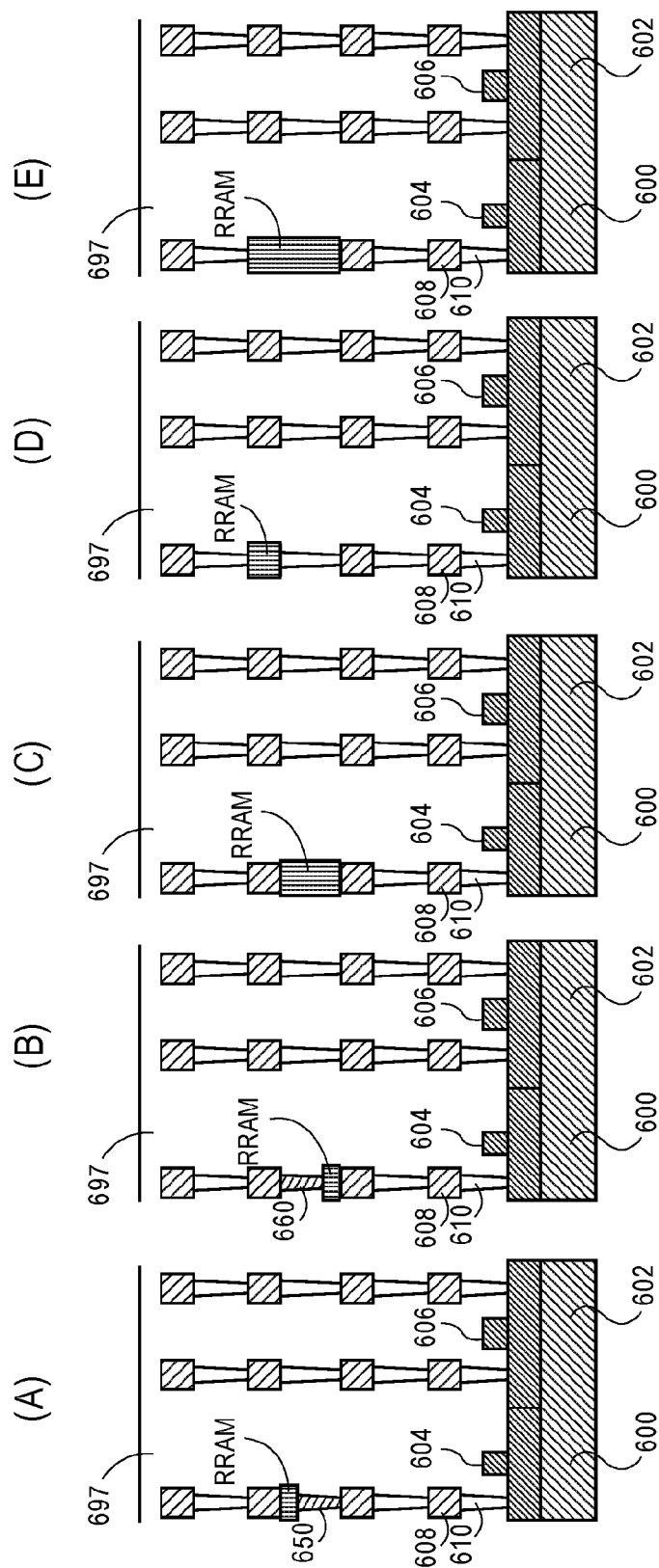


FIG. 6A

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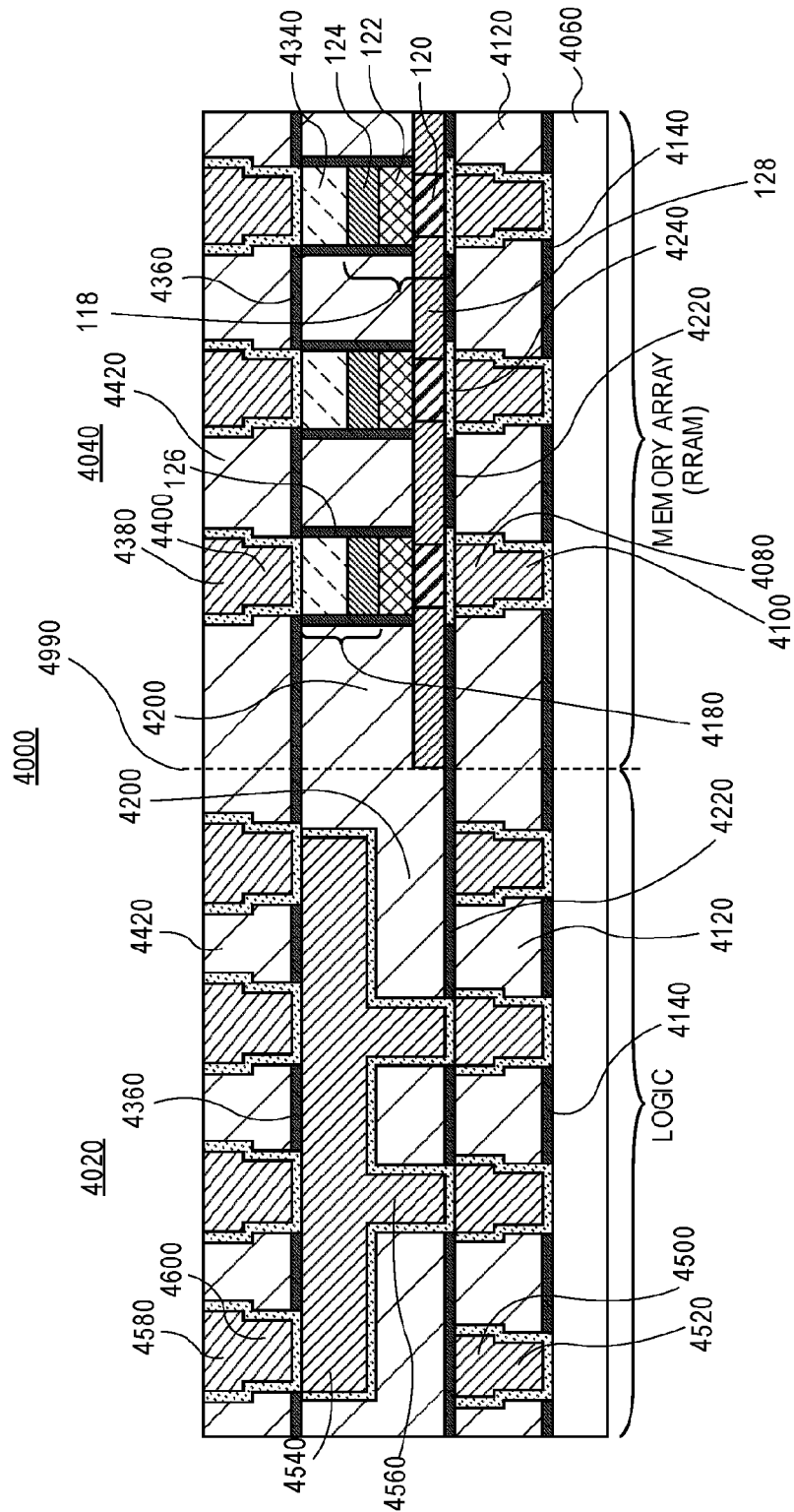


FIG. 6B

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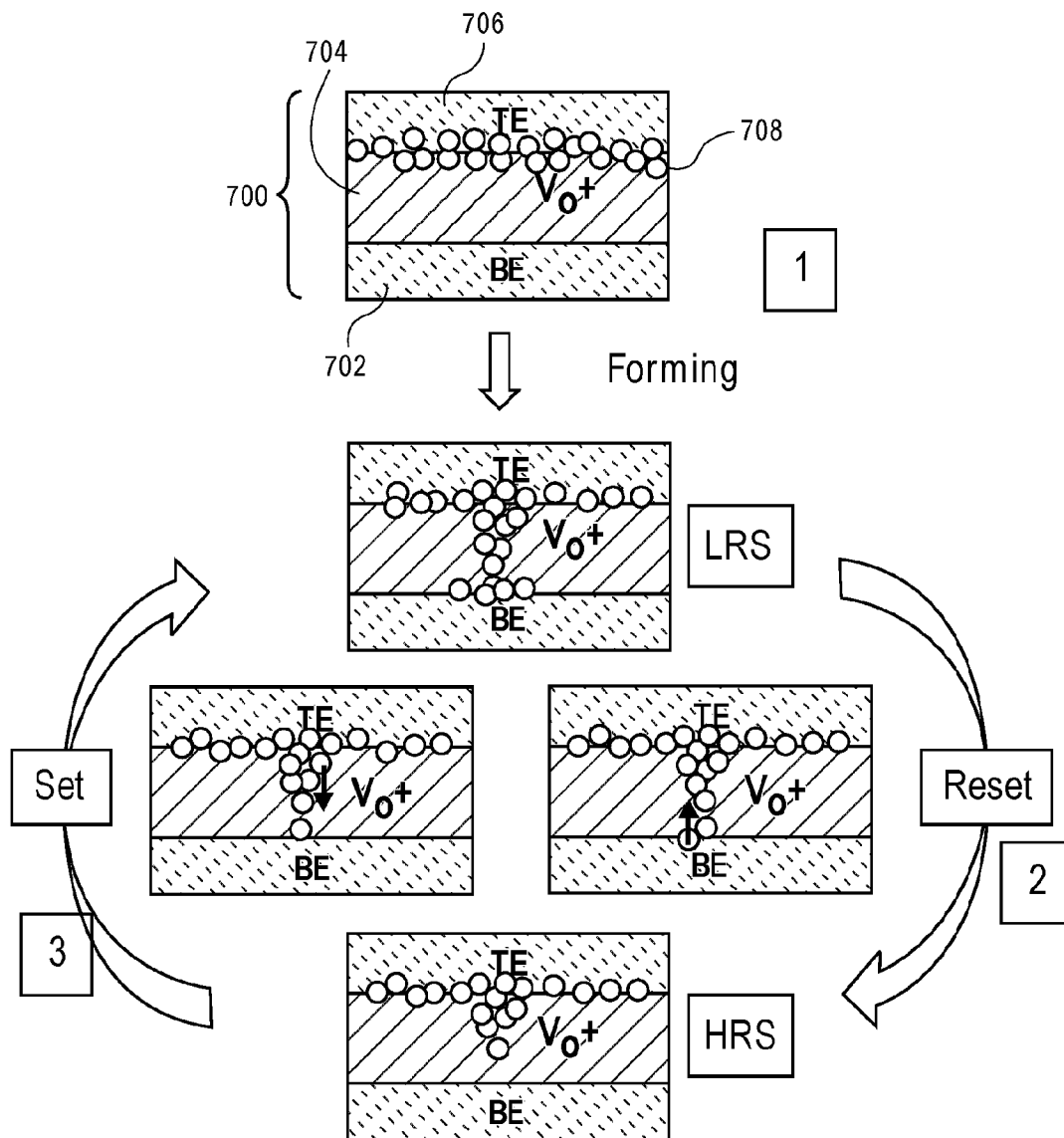
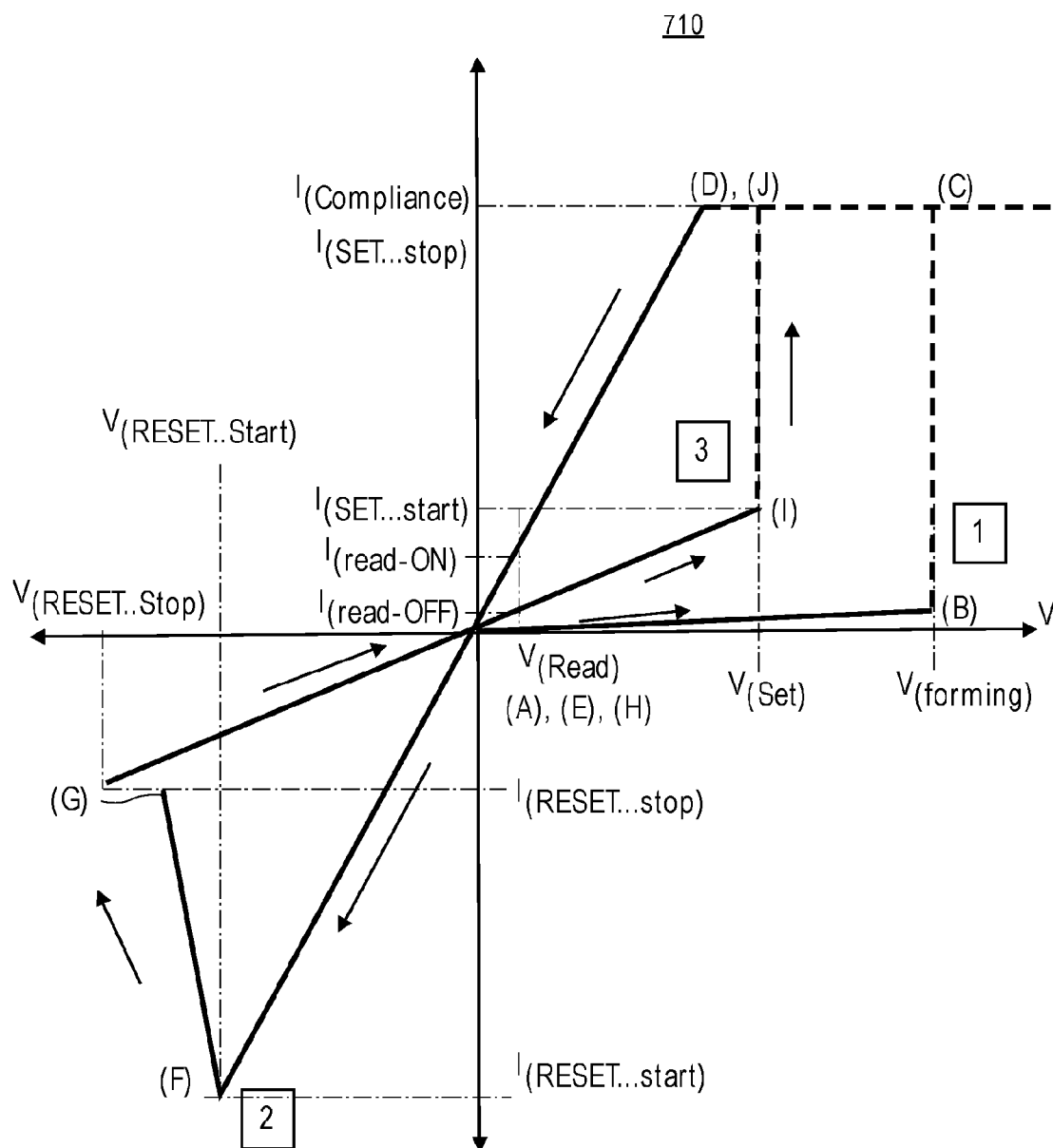


FIG. 7A

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**FIG. 7B**

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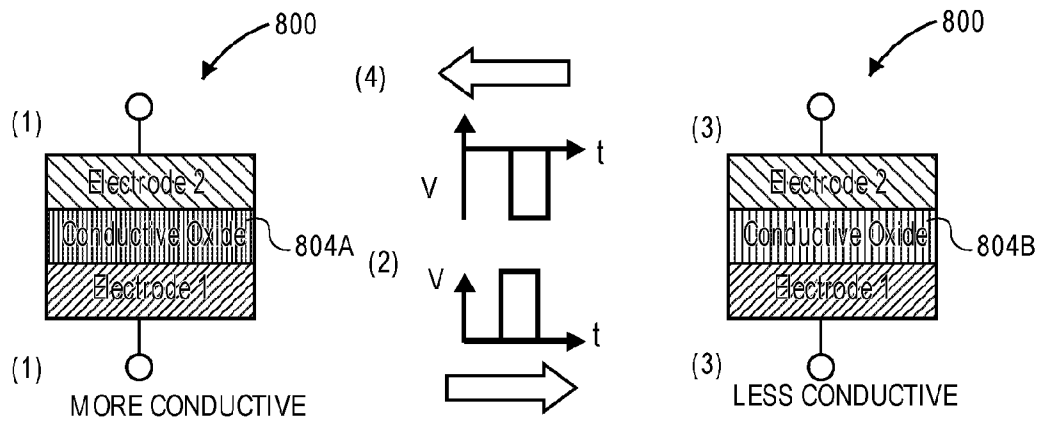


FIG. 8

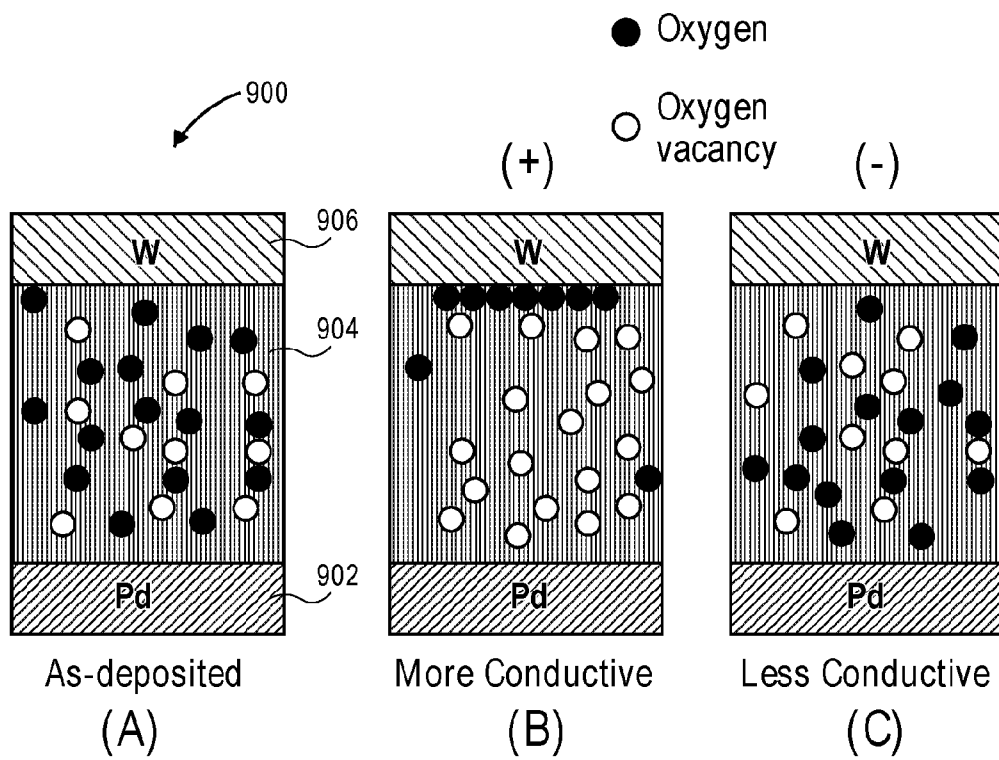
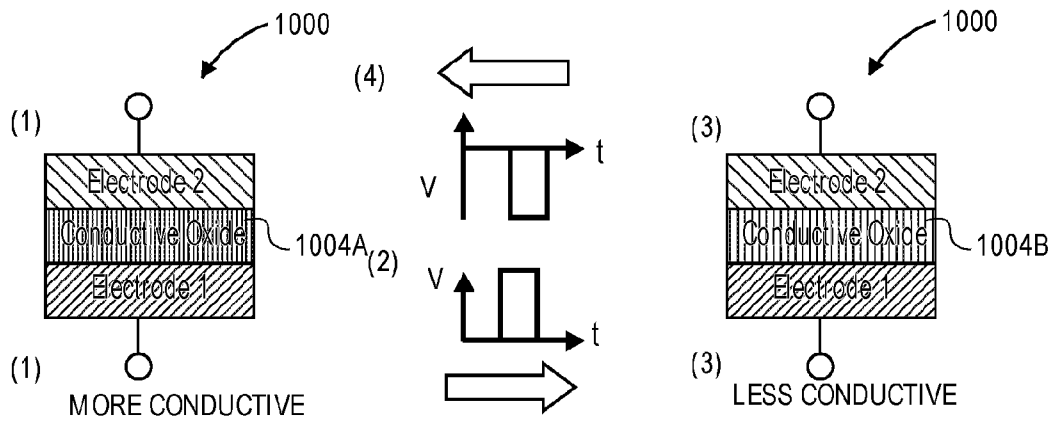
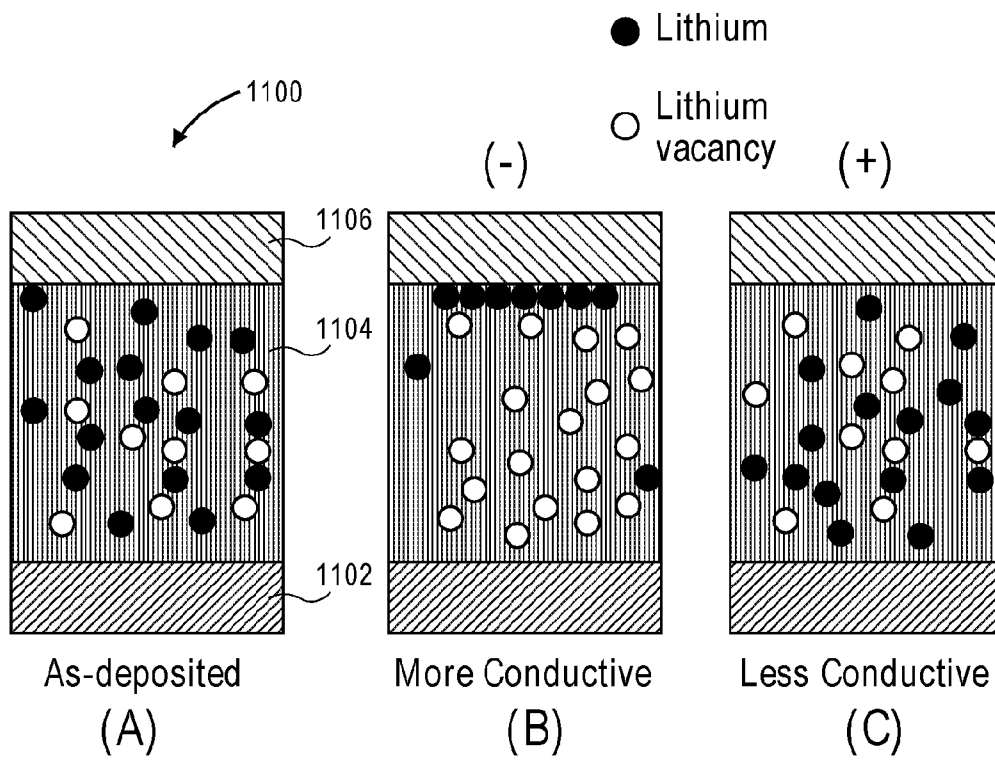


FIG. 9

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**FIG. 10****FIG. 11**

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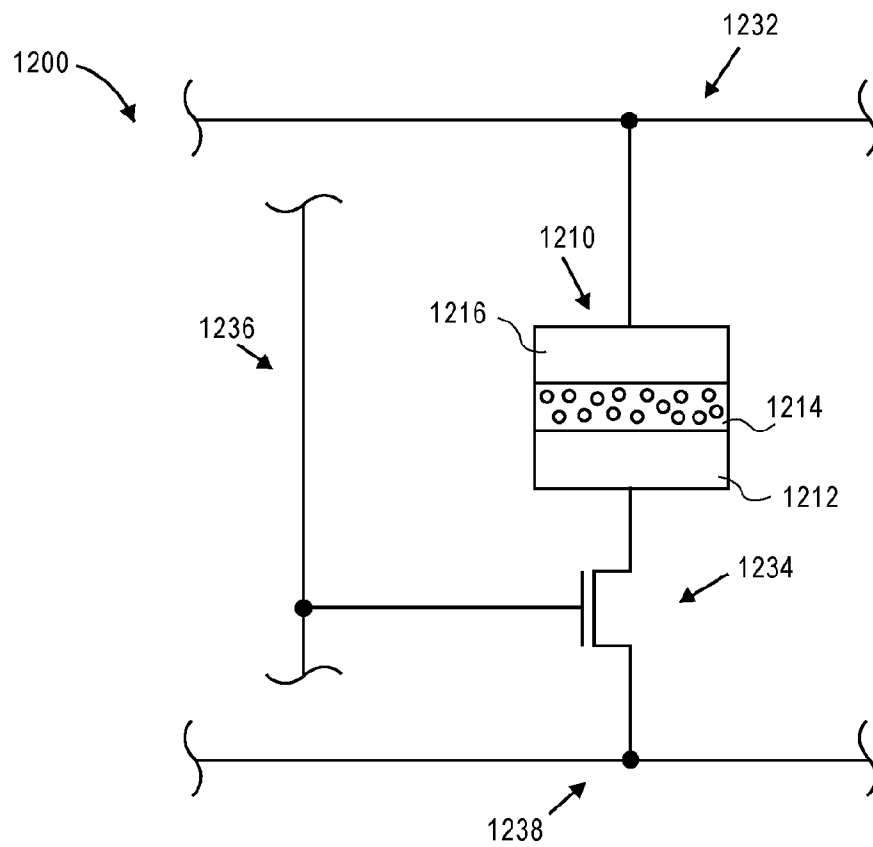


FIG. 12

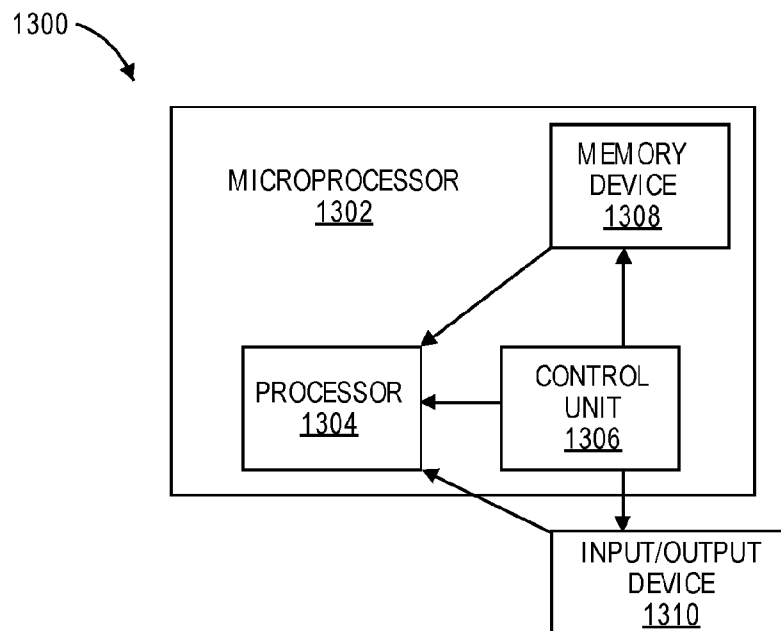


FIG. 13

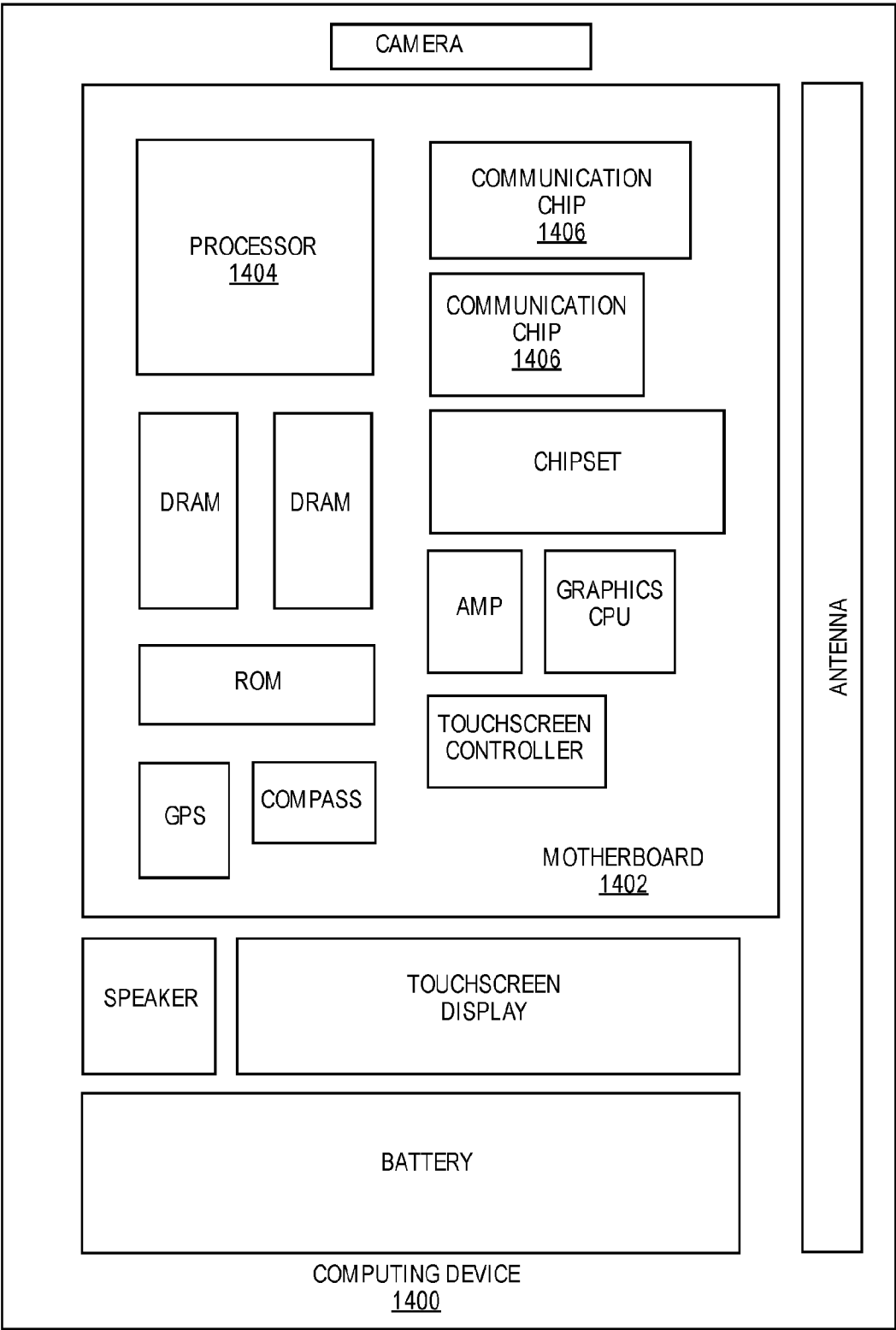


FIG. 14

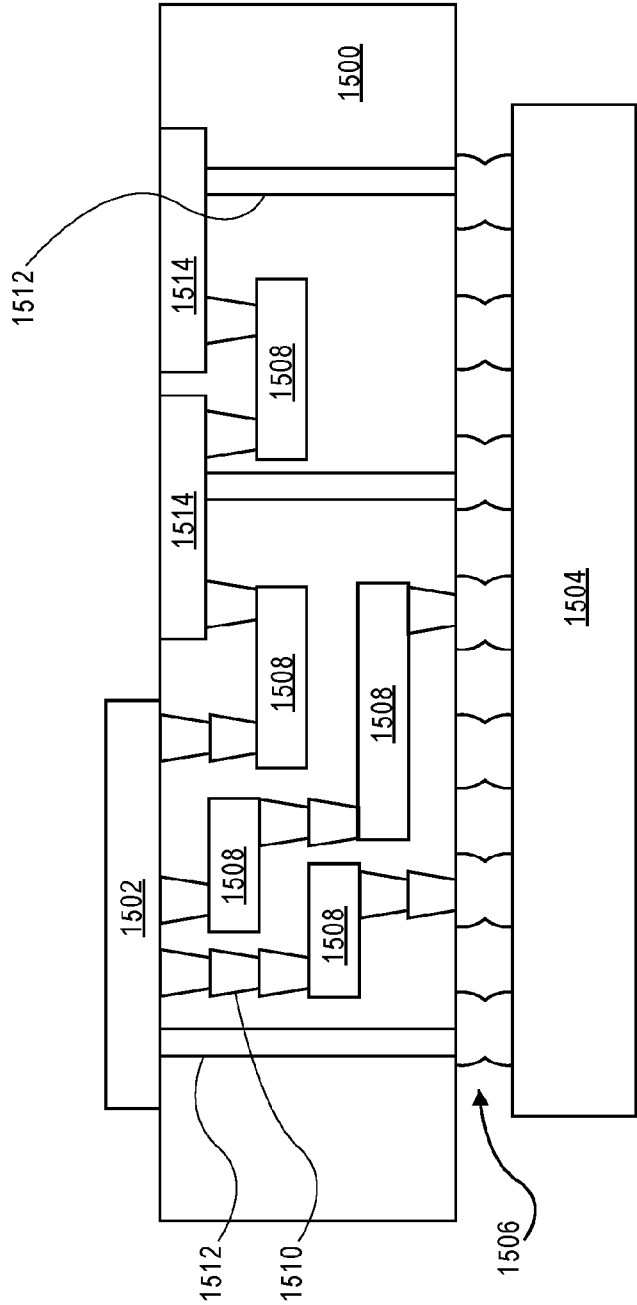


FIG. 15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/040302**A. CLASSIFICATION OF SUBJECT MATTER****H01L 45/00(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHEDMinimum documentation searched (classification system followed by classification symbols)
H01L 45/00; H01L 21/02; H01L 27/24Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: resistive random access memory (RRAM), conductive interconnect, inter-layer dielectric (ILD), electrode layer, insulating metal oxide layer**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015-0194602 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.) 09 July 2015 See paragraphs [0010]–[0040]; and figures 6, 8B, 9.	1–25
A	US 2011-0140067 A1 (FREDERICK T. CHEN et al.) 16 June 2011 See paragraphs [0022]–[0044]; and figures 1A–9B.	1–25
A	US 2011-0193051 A1 (KYUNGTAЕ NAM et al.) 11 August 2011 See paragraphs [0023]–[0057]; and figures 1A–6B.	1–25
A	US 2015-0325786 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.) 12 November 2015 See paragraphs [0018]–[0047]; and figures 1A–8.	1–25
A	US 2014-0322862 A1 (ASM IP HOLDING B.V.) 30 October 2014 See paragraphs [0028]–[0098]; and figures 1–10.	1–25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

24 March 2017 (24.03.2017)

Date of mailing of the international search report

28 March 2017 (28.03.2017)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/040302

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US 2015-0325786 A1	12/11/2015	CN 104518085 A KR 10-1573146 B1 KR 10-2015-0037517 A US 2015-0090949 A1 US 9112148 B2	15/04/2015 01/12/2015 08/04/2015 02/04/2015 18/08/2015
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