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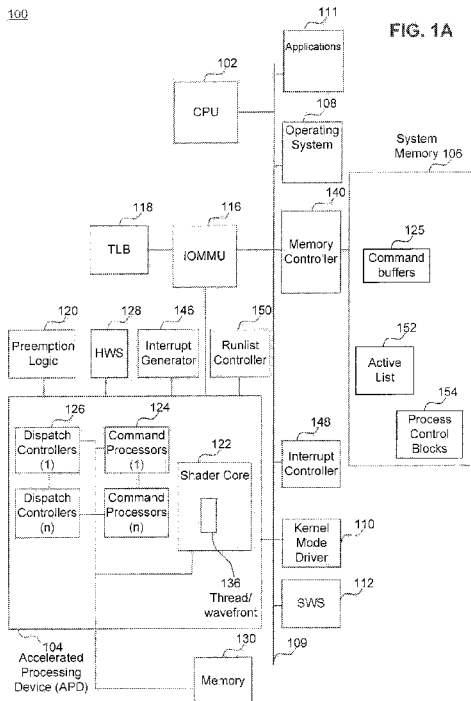
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[Continued on next page]

(54) Title: DYNAMIC WORK PARTITIONING ON HETEROGENEOUS PROCESSING DEVICES

(57) Abstract: A method, system and article of manufacture for balancing a workload on heterogeneous processing devices. The method comprising accessing a memory storage of a processor of one type by a dequeuing entity associated with a processor of a different type, identifying a task from a plurality of tasks within the memory that can be processed by the processor of the different type, synchiOnizing a plurality of dequeuing entities capable of accessing the memory storage, and dequeuing the task form the memory storage.



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INTERNATIONAL SEARCH REPORT

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<p>A. CLASSIFICATION OF SUBJECT MATTER IPC(8) - G06F 9/46 (2012.01) USPC - 718/105 According to International Classification (IPC) or to both national classification and IPC</p>														
<p>B. FIELDS SEARCHED</p> <p>Minimum documentation searched (classification system followed by classification symbols) 718/105</p> <p>Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched 718/100   712/32   712/220</p> <p>Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) PubWEST(PGPB,USPT,EPAB,JPAB); Google Scholar; dequeue, task, CPU, load, workload, GPU, balance, accelerated processing device, APD, heterogeneous, processor, central processing unit, graphic processing unit, software</p>														
<p>C. DOCUMENTS CONSIDERED TO BE RELEVANT</p> <table border="1"> <thead> <tr> <th>Category*</th> <th>Citation of document, with indication, where appropriate, of the relevant passages</th> <th>Relevant to claim No.</th> </tr> </thead> <tbody> <tr> <td>X</td> <td>Chen et al. "Dynamic Load Balancing on Single- and Multi-GPU Systems." [online] in Proc. of the IEEE International Parallel &amp; Distributed Processing Symposium (IPDPS 2010), Atlanta, Georgia, April 19 - 23, 2010. [retrieved on 25 March 2012]. Retrieved from the Internet&lt;URL: <a href="http://www.capsl.udel.edu/pub/doc/papers/LongChen-IPDPS2010.pdf">http://www.capsl.udel.edu/pub/doc/papers/LongChen-IPDPS2010.pdf</a>&gt; (entire document especially pg. 1, col. 2; pg. 2, col. 2; pg. 3, col. 2; pg. 4, col. 1; pg. 6, col. 2)</td> <td>1-23</td> </tr> <tr> <td>X</td> <td>Zhao et al. "An architecture design of GPU-accelerated VoD streaming servers with network coding." [online] Collaborative Computing: Networking, Applications and Worksharing (CollaborateCom), 2010 6th International Conference, October 9-10, 2010 [retrieved on 25 March 2012]. Retrieved from the Internet&lt;URL: <a href="http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5767035">http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5767035</a>&gt; pg. 5, col. 1 to col. 2</td> <td>1-23</td> </tr> <tr> <td>A</td> <td>US 7,159,221 B1 (Willen et al.) 02 January 2007 (02.01.2007) entire document</td> <td>1-23</td> </tr> </tbody> </table>			Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.	X	Chen et al. "Dynamic Load Balancing on Single- and Multi-GPU Systems." [online] in Proc. of the IEEE International Parallel & Distributed Processing Symposium (IPDPS 2010), Atlanta, Georgia, April 19 - 23, 2010. [retrieved on 25 March 2012]. Retrieved from the Internet<URL: <a href="http://www.capsl.udel.edu/pub/doc/papers/LongChen-IPDPS2010.pdf">http://www.capsl.udel.edu/pub/doc/papers/LongChen-IPDPS2010.pdf</a> > (entire document especially pg. 1, col. 2; pg. 2, col. 2; pg. 3, col. 2; pg. 4, col. 1; pg. 6, col. 2)	1-23	X	Zhao et al. "An architecture design of GPU-accelerated VoD streaming servers with network coding." [online] Collaborative Computing: Networking, Applications and Worksharing (CollaborateCom), 2010 6th International Conference, October 9-10, 2010 [retrieved on 25 March 2012]. Retrieved from the Internet<URL: <a href="http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5767035">http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5767035</a> > pg. 5, col. 1 to col. 2	1-23	A	US 7,159,221 B1 (Willen et al.) 02 January 2007 (02.01.2007) entire document	1-23
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"P" document published prior to the international filing date but later than the priority date claimed														
<p>Date of the actual completion of the international search 25 March 2012 (25.03.2012)</p>		<p>Date of mailing of the international search report <b>26 APR 2012</b></p>												
<p>Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201</p>		<p>Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774</p>												