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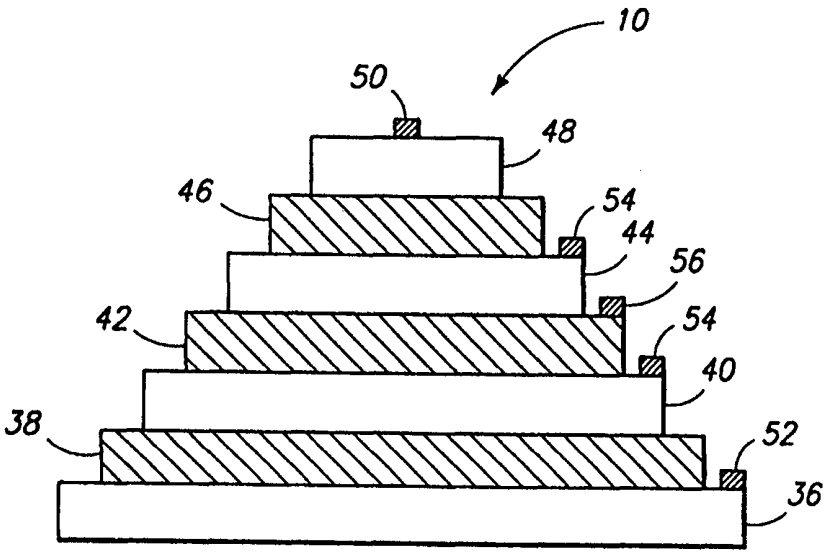
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(57) Abstract

A heterostructure thermionic cooler and a method for making thermionic coolers, employing a barrier layer of varying conduction bandedge for n-type material, or varying valence bandedge for p-type material, that is placed between two layers of material. The barrier layer bandedge is at least k_BT higher than the Fermi level of the semiconductor layer, which allows only selected, "hot" electrons, or electrons of high enough energy, across the barrier. The barrier layer is constructed to have an internal electric field such that the electrons that make it over the initial barrier are assisted in travel to the anode. Once electrons drop to the energy level at the anode, they lose energy to the lattice, thus heating the lattice of the anode. The barrier height of the barrier layer is high enough to prevent the electrons from traveling in the reverse direction.

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HIGH-EFFICENCY HETEROSTRUCTURE THERMIONIC COOLERS

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This invention was made with Government support under Contract No. 442530-25845, awarded by the Office of Naval Research. The Government has certain rights in this invention.

CROSS REFERENCE TO RELATED APPLICATIONS

This application is related to United States Patent Application Serial No. 08/767,955, filed on December 17, 1996, entitled "HETEROSTRUCTURE THERMIONIC COOLERS," by Ali Shakouri, et al., now United States Patent No. 5,955,772; and United States Patent Application Serial No. 09/280,284, filed on March 29, 1999, entitled "METHOD FOR MAKING HETEROSTRUCTURE THERMIONIC COOLERS," by Ali Shakouri et al., both of which applications are incorporated by reference herein. This application also claims priority under 35 U. S. C. § 119(e) of United States Provisional Patent Application No. 60/109,342, filed November 20, 1999, entitled "HIGH-EFFICENCY HETEROSTRUCTURE THERMIONIC COOLERS," by Ali Shakouri et al., which application is incorporated by reference herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention.

This invention relates in general to electronic devices, and more specifically to the use of semiconductor materials to fabricate thermionic coolers and generators.

2. Description of Related Art.

The use of electronics to transport heat to and away from certain areas has expanded in recent years due to increased packing densities and hostile environments. For cooling applications, thermoelectric (TE) coolers have been used to cool areas both in electronic and nonelectronic applications. TE coolers typically include a p-type doped region alternatively connected to an n-type doped region, which creates cooling effects at one metal-doped region junction and heating effects at the other metal-doped region junction, depending on the direction of the current through the device.

However, TE coolers are limited in their overall efficiency by the bulk properties of the materials used in the TE cooler. Further, the reliability of assemblies of many elements, such as in TE coolers, is often not sufficient for many applications. The cost of TE coolers has not dropped at the same rate as other electronic devices such as transistor circuits, lasers and detectors, because TE cooler elements are not fabricated using high volume planar integrated circuit technology. Further, TE coolers that can generate a large cooling effect tend to be large devices, typically 1 cm x 1 cm or larger, and are slow cooling devices, and thus, are not acceptable in small electronic devices.

From the foregoing, it can be seen then that there is a need for improved electronic coolers. It can also be seen then that there is a need for better electronic cooler fabrication techniques. It can also be seen that there is a need for low cost electronic coolers. It can also be seen that there is a need for more space efficient electronic coolers. It can also be seen that there is a need for more energy efficient electronic coolers. It can also be seen that there is a need for coolers with faster response times. It can also be seen that there is a need for more reliable electronic coolers. It can also be seen that there is a need for electronic coolers that reach lower temperatures.

SUMMARY OF THE INVENTION

The present invention minimizes the above-described problems by using bandgap engineering and modulation doping to fabricate small thermionic coolers that operate at room temperature. By using proper materials and geometries, efficient and space conserving thermionic cooler elements which can reach lower temperatures are fabricated in a cost-effective manner. Further, these coolers can have a much faster response.

The present invention comprises a method and apparatus for thermionic cooling. The method of the present invention comprises growing two semiconductor layers. The second layer has a variable conduction bandedge as a function of distance (for the case of electron transport) which has a Fermi level on the order of $k_B T$ from the bandedge of the semiconductor layer. This structure allows for selective thermionic emission of high energy carriers from cathode to anode that suppresses the reverse current, and creates a cold junction at the cathode and a hot junction at the anode. Using the same device in contact with a hot and a cold bath will create a thermionic generator.

One object of the present invention is to provide better electronic cooler fabrication techniques. It is a further object of the invention to reduce electronic cooler fabrication costs. It is a further object of the invention to make more efficient electronic coolers which reach lower temperatures. It is a further object of the invention to make electronic coolers that have a faster response time.

These and various other advantages and features of novelty which characterize the invention are pointed out with particularity in the claims annexed hereto and form a part hereof. However, for a better understanding of the invention, its advantages, and the objects obtained by its use, reference should be made to the drawings which form a further part hereof, and to accompanying descriptive matter, in which there are illustrated and described specific examples of an apparatus in accordance with the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Referring now to the drawings in which like reference numbers represent corresponding parts throughout:

FIGS. 1A-1E are diagrams of a first embodiment of the present invention;

FIGS. 2A-2E are graphs of the conduction bandedge of devices made using the present invention;

FIG. 3 shows an alternative structure for the device;

FIG. 4 shows a cascaded device using stages with different bandedge discontinuities;

FIG. 5 shows a combination of n-doped and p-doped devices of the present invention;

FIG. 6 illustrates indicates the potential of Heterostructure Integrated Thermionic (HIT) devices to achieve high cooling power densities;

FIG. 7 displays the surface temperature on top and on the bottom of the device as well as the substrate temperature far away from the device as a function of current;

FIG. 8 illustrates the measured cooling on top of the device at various substrate temperatures;

FIG. 9A illustrates the Fermi levels of a large barrier height device in accordance with the present invention;

FIG. 9B illustrates the predicted thermoelectric figure-of-merit for bulk InGaAs and for large barrier InGaAs/InP and InGaAs/InAlAs superlattices as a function of doping as used in the present invention; and

FIG. 9C illustrates the predicted net cooling as a function of current for the high barrier heterostructure thermionic coolers of the present invention.

DETAILED DESCRTPTION OF THE INVENTION

In the description of the preferred embodiment, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration the specific embodiment in which the invention may be practiced. It is to be understood that other embodiments may be utilized as structural changes may be made without departing from the scope of the present invention.

Overview

The present invention uses thermionic emission in semiconductor heterostructures for heat pumping and cooling of high power electronic and optoelectronic devices. These integrated micro-coolers can improve the efficiency and lifetime of electrical and optoelectronic components. The thermionic coolers could also be used as an additional means for tuning temperature sensitive devices.

The coolers that are commercially available are typically thermoelectric (TE) coolers, based on the Peltier effect at the junction of two dissimilar materials. TE coolers use materials bulk properties, such as the Seebeck coefficient, electrical, and thermal conductivity, and are mostly based on Bismuth Telluride (Bi_2Te_3) for room temperature applications. The basis of the heterostructure integrated thermionic (HIT) cooler described herein is to use bandstructure engineering to increase the cooling power and efficiency.

Recent proposals to use quantum wells, quantum wires, and superlattice structures to increase the TE cooler figure of merit can be divided into two categories. The first category changes the density of electronic states of the cooler materials to make it more "peaked" and also more asymmetric with respect to the Fermi energy. This increases the electrical power factor, $S^2\sigma$, and thus the TE cooler figure of merit $Z = S^2\sigma/\beta$, where S is the Seebeck coefficient or thermopower, σ is the electrical conductivity, and β is the thermal conductivity.

The second category uses perpendicular transport of electrons in small barrier superlattices, e.g., where the barrier height is on the order of k_BT, in a way that modifies the mobility of low energy electrons with respect to high energy electrons. This asymmetry also increases the electrical power factor.

Both methods are expected to only give moderate improvements when various non-ideal effects, such as the role of barriers and finite level widths, are

included in the final models and devices, as shown in papers written by Mahan (Appl. Phys. Lett. 65(21) p. 2690, 1994) and Rowe (13th International Conference on Thermoelectrics, Kansas City, Missouri, 1994, p. 339), which are herein incorporated by reference.

U.S. Patent No. 5,955,772 proposed the use of thermionic emission in heterostructures. Thermionic emission from metallic plates into a vacuum or gas filled diode is a key technology for the conversion of heat into electricity at high temperatures (>1000°K). If metals with very low work functions were available and could be placed at small distances apart, the same principle would make a thermionic refrigerator at room temperatures. U.S. Patent No. 5,955,772 also used semiconductor heterostructures to tailor the thermionic emission by using bandedge discontinuity between various compounds. The accurate epitaxial growth of thin and uniform layers in conjunction with modulation doping helped to minimize the problem of space charge which limits the operation of vacuum thermionic diodes at low temperatures.

The present invention uses thermionic emission in highly degenerate tall barrier superlattices. This combines the advantages of large density of states with selective emission of hot electrons.

Thermoelectric Cooler Background

Electron conduction in a solid is affected by the temperature and the temperature gradient. This interaction between the "electrical" current, e.g., the amount of charge transported by electrons I, and the "thermal" current, e.g., the amount of heat transported by electrons Q, has been used for various applications such as thermoelectric cooling (I to Q) thermoelectric generation (Q to I) and thermal (bolometric) detectors (ΔT to V).

The periodicity of crystalline solids allows a description of electron movement in a complicated voltage potential of many atoms, using some parameters such as bandgap, effective mass, etc. In a point-particle picture, localized scattering events can be assumed with acoustic and optical phonons, along with various impurities, and coherent scattering events can be neglected. The electron motion can be adequately described and modeled using the electronic distribution function and the Boltzmann Transport Equation (BTE).

Thermoelectric Cooler Modeling

A single element TE cooler is composed of two branches, one branch of n-doped and one branch of p-doped material. The two branches are connected electrically in series and thermally in parallel. When the current is flowing from n to p, e.g., electrons are moving from the p-branch to a metallic contact between the branches and then to the n-branch, the heat is absorbed at the junctions p-metal and metal-n. Electrons in the p-branch have an average transport energy smaller than the Fermi energy, and the ones in the n-branch have an average transport energy larger than the Fermi energy. Metals are considered to have their average transport energy equal to their Fermi energy.

In a perfect ohmic conduction from the p-branch to metal to the n-branch, electrons should absorb energy in the form of heat to increase their average energy. The same argument can be applied to the contacts at the outside ends of the branches where the heat is generated. The heat absorption or generation occurs at distances very close to the contacts, on the order of electron average velocity times its thermalization time constant. This heat absorption or generation, called the Peltier effect, is a reversible thermodynamic phenomena, depending on the direction of the current flow.

Thermionic Coolers

To create a heterostructure integrated thermionic (HIT) cooler, one uses precise control of layer thickness and composition, achieved by molecular beam epitaxy (MBE), metal-organic chemical vapor deposition (MOCVD), or other growth techniques, in conjunction with bandgap engineering to allow for the design of specific conduction or valence band profiles within a device. The use of a typically higher bandgap material between two lower bandgap materials, the two lower bandgap materials comprising the cathode and the anode, will produce a barrier for electrons or holes as they travel from cathode to anode. Thermionic emission of carriers over this barrier selectively removes high energy carriers. The strong electron-electron interaction at the cathode will tend to restore quasi-Fermi distribution by absorbing heat from the lattice. Electrons that reach the anode will lose their energy by generating heat. By choosing the appropriate bandedge discontinuities at the cathode and anode, which are typically 0 to 1 eV, the reverse current is suppressed and cooling is achieved at room temperatures.

Depending on the growth constraints and lattice mismatch between materials, the barrier composition can be graded or modulated to produce internal fields and to

enhance electron transport properties. In the case of a vacuum diode, the problem of space charge, which is the presence of charged electrons in the space between the cathode and the anode, will create an extra potential barrier for the current going from the cathode to the anode, further limits the low temperature cooling or power generation applications. Using heterostructure thermionic coolers, close and uniform spacing of cathode and anode is less of a problem, and is controlled by accurate crystal growth technologies. Furthermore, doping the barrier material (modulation doping) can be used to create internal fields, modify the electron flow, and control space charge effects.

By using the thermionic effect, instead of the thermoelectric effect, two immediate advantages are evident. The TE cooler materials are restricted to those materials that have high electrical conductivity and thermopower, and low thermal conductivity. These materials then only produce cooling or heating at the junction between two materials, with different Seebeck coefficients.

Heterostructure integrated thermionic cooling, on the other hand, does not have a requirement for high thermopower materials. Bandedge discontinuities, also known as Schottky barriers, between the anode and cathode will perform the cooling or heating as needed. One has to find the barrier material that has high electrical conductivity and low thermal conductivity. The cooling and/or heating effect produced by thermionic devices, depending on the direction of the current through the device, will be called a non-isothermal effect, as it is a change in the temperature distribution in the device compared to the case that has no current flow.

The second advantage is that thermionic structures can be made from conventional semiconductor materials and can be monolithically integrated with other electronic or optoelectronic devices.

Detailed Drawings

FIGS. 1A-1E are diagrams of a first embodiment of the present invention.

FIG. 1A shows device 10 consisting initially of layer 12. Layer 12 is typically gallium arsenide (GaAs), but can be other materials, such as silicon (Si), indium phosphide (InP), lead telluride (PbTe), gallium nitride (GaN), Gallium phosphide (GaP), indium. arsenide (InAs), germanium (Ge), mercury cadmium selenide ($Hg_xCd_{1-x}Se$), indium gallium arsenide ($In_xGa_{1-x}As$), indium arsenide (InAs), indium antimonide (InSb), indium gallium arsenide antimonide ($In_xGa_{1-x}As_ySb_{1-y}$), mercury cadmium telluride ($Hg_xCd_{1-x}Te$) , aluminum gallium nitride ($Al_xGa_{1-x}N$), indium gallium nitride

($In_xGa_{1-x}N$), indium arsenide phosphide ($InAs_yP_{1-y}$), indium gallium arsenide phosphide ($In_xGa_{1-x}As_yP_{1-y}$), indium gallium aluminum arsenide ($In_xGa_yAl_{1-x-y}As$), gallium aluminum arsenide antimonide ($Ga_{1-x}Al_xAs_ySb_{1-y}$), lead tin telluride ($Pb_xSn_{1-x}Te$), aluminum arsenide (AlAs), aluminum antimonide (AlSb), zinc selenide (ZnSe), zinc telluride (ZnTe), boron nitride (BN), gallium phosphide (GaP), gallium antimonide (GaSb), gallium aluminum arsenide ($Ga_xAl_{1-x}As$), gallium arsenide phosphide ($GaAs_yP_{1-y}$), gallium indium phosphide ($Ga_xIn_{1-x}P$), gallium indium antimonide ($Ga_xIn_{1-x}Sb$), bismuth telluride (Bi_2Te_3), and bismuth selenide (Bi_2Se_3) or other ternary or quaternary materials, where the subscripts x, y, 1-x, and 1-y denote the relative amounts of the atomic species in each ternary or quartenary material and range from zero to one, inclusive. Further, layer 12 may be doped n-type or p-type, or can be a metal layer.

FIG. 1D shows device 10 being constructed by adding layer 14 on top of layer 12. Layer 14 is a barrier layer for device 10, and for layer 12 consisting of GaAs, layer 14 is typically a graded $Al_xGa_{1-x}As$ layer. Layer 14 creates a slight internal electric field throughout the thickness of layer 14 to eliminate the space charge problem around the cathode, which, in this case, is layer 12. Layer 14 is typically grown by MBE or MOCVD techniques, but can be grown in other ways. If layer 14 is n-type, layer 14 has a conduction bandedge that increases as a function of the distance from the layer 12, e.g., the value of the conduction bandedge at a first distance from the layer 12 is more than the value of the conduction bandedge at a second, greater distance from the layer 12. The layer 14 conduction bandedge increases for layers 14 that are doped n-type; corresponding p-type doped layers 14 will have a valence bandedge that is decreasing. The conduction bandedge of the layer 14 can be monotonically increasing, stepped, or piecewise linear, or any other shape, so long as at some point in the layer 14 the conduction bandedge has a level higher than the conduction bandedge of the layer 12. Layer 14 can also be a strained layer, to increase the bandedge offset between layer 12 and layer 14. For layers 12 that are Si_xGe_{1-x}, layer 14 can be a silicon-germanium (Si_yGe_{1-y}) , layer where $y > x$, or $x > y$ depending on the strain in the SiGe layer. For layers 12 that are $In_{x1}Ga_{1-x1}As_{y1}P_{1-y1}$, layer 14 is typically $In_{x2}Ga_{1-x2}As_{y2}P_{1-y2}$, where $x2 < x1$, or $y2 < y1$. For layers 12 that are PbTe, layer 14 is typically $Pb_{1-x}Eu_xTe$. For layer 12 that is $Hg_{x1}Cd_{1-x1}Te$, layer 14 is typically $Hg_{x2}Cd_{1-x2}Te$, where $x2 < x1$. For layer 12 that is $Hg_{x1}Cd_{1-x1}Se$, layer 14 is $Hg_{x2}Cd_{1-x2}Se$, where $x2 < x1$. Layer 14 can also be made of other materials, such as silicon oxide, aluminum oxide, vacuum, air, indium gallium arsenide antimonide, indium gallium aluminum nitride, bismuth telluride, bismuth selenide, boron nitride, zinc telluride, zinc selenide,

lead tin telluride, aluminum antimonide, lead telluride, other insulators, other gases, a selectively oxidized layer, or other gradations or modulations of materials for a given layer 12. The HIT device 10 of FIG. 1B can be used as a thermal imaging system, wherein the device 10 is a single pixel or multiple pixels of a thermal imaging system.

FIG. 1C shows device 10 in another format, where anode layer 16 is added to device 10 on top of layer 14. Anode layer 16 is typically made of the same material as layer 12, but can be made of other materials. Because of the gradation or modulation of layer 14, the difference in conduction bandedge between layer 16 and layer 14 is larger than the difference in conduction bandedge between layer 12 and layer 14. This difference in conduction bandedge between the three layers 12-16 creates, under an applied voltage, a large forward current from layer 12 to layer 16 and a small reverse current from layer 16 to layer 12. Within layer 14, the gradation or modulation creates a small electric field that assists electron movement away from layer 12 and through layer 14.

FIG. 1D shows a series of layers 14-20 on layer 12 to form device 10. This series connection creates two devices 10 back to back, and thus, multiple forward and reverse barriers are created in series. This series connection places the layers 14-20 in thermal series, which allows a larger temperature difference between the layer 12 and the final layer 20 of the device 10. Layers 14-20 can be successive barrier layers, alternating barrier layers and semiconductor layers, or any combination of barrier layers and semiconductor layers.

FIG. 1E is a diagram showing the selective removal of layer 14 in the device 10. After growing layer 16 on layer 14, certain portions 14A of layer 14 can be removed by photolithography and dry or wet selective etching techniques. This creates a vacuum space in layer 14, and provides even lower thermal conductivity between layer 12 and layer 16. This structure allows for a precise cathode-anode separation in an extremely small space, namely the thickness of layer 14. Device 10 is a monolithic version of the original metal vacuum diodes. Layer 12 could be a negative electron affinity material such as Aluminum Nitride (AlN), or coated with an electronegative material such as Cesium.

FIGS. 2A-2E are graphs of the conduction bandedge of an n-type device 10, or the valence bandedge of a p-type device 10 made using the present invention. For a p-type device 10, the increasing energy is in the downward direction.

FIG. 2A is a graph of the conduction bandedge of the device 10. Level 22 is the conduction bandedge of layer 12. Transition 24 is the change in conduction bandedge at the boundary between layer 12 and layer 14. This amount, labeled ϕ_C, is

the difference in conduction bandedge at the cold side of the device 10. Level 26 is the conduction bandedge across layer 14. This layer is increasing as the distance from boundary 24 increases. Distance 28 (Fig. 2B) is the thickness of layer 14. Distance 28 is typically 0.001 to 1 micron.

Transition 30 is the change in conduction bandedge at the boundary between layer 14 and layer 16. This difference, labeled ϕ_H, is the difference in conduction bandedge at the hot side of device 10. If level 26 increases across the distance of layer 14, the transition 30 will have a larger ϕ_H difference than transition 24. Level 32 is the conduction bandedge across layer 16. ϕ_H can be small, or even zero, if the maximum bandedge is at the beginning of layer 14, as shown in FIG. 2D.

FIG. 2B shows the conduction bandedge graph of FIG. 2A when device 10 is being biased. A bias voltage V 34 is applied across device 10, with the positive voltage applied at layer 16 and the negative voltage applied at layer 12. The level 22 of the conduction bandedge of layer 12 will thus be increased by bias voltage 34. Certain electrons in layer 12 will have enough energy to be able to get over transition 24 and continue on through layer 14. These electrons are called "hot electrons" because they are of sufficient energy to carry heat away from the cold junction at transition 24.

There will also be electrons in layer 12 that do not have enough energy to get over the barrier at transition 24. These electrons are called "cold electrons" because they are not of sufficient energy to carry heat away from the cold junction.

As the hot electrons get over transition 24, the hot electrons encounter the conduction bandedge of layer 14. Under bias voltage V 34, the level 26 of the conduction bandedge of layer 14 becomes tilted in the other direction, e.g., it is slightly "downhill," and thus aids the hot electrons in their travel away from the layer 12 and through the layer 14.

Once the hot electrons get to transition 30, the hot electrons see a large energy drop because of the large difference in conduction bandedge between layer 14 and layer 16. The electrons lose their energy to the lattice, heating the lattice up, and heat up the junction between layer 14 and layer 16, the hot junction of the device 10.

In the device 10, reversing the direction of the current will make a heterostructure thermionic heater. Note that the same device 10, in contact with two heat baths (a hot bath in contact with layer 16 and a cold bath in contact with layer 12) will produce electricity. This thermionic generator should operate at temperatures much lower than required in vacuum thermionic diode generators.

FIG. 2C is a graph of three devices 10 placed in series under bias conditions. The device 10 has a structure as shown in FIG. 1D, which illustrates two devices in series.

The barrier layer can be graded so ϕ_H is small or zero, as shown in FIG. 2D. These barrier layers can also be stacked as shown in FIG. 2E. The barrier layer does not have to be linear; FIG. 2E shows that the barrier layers can have a curved bandedge. The bandedge of the barrier layer can take any shape.

By operating the devices 10 in a cascade arrangement, which is a series thermal arrangement, higher temperature differences can be achieved. The first stage of the cascade in FIG. 2C (layers 36, 38, and 40) provides a low temperature heat sink for the second stage (layers 40, 42, and 44) which in turn provides a temperature sink at an even lower temperature for the third stage (layers 44, 46, and 48). By adding more stages, more temperature heat sinks can be added, and larger temperature differences can be achieved. It is necessary that the cooling capacity of the higher temperature stages (layers 36, 38, and 40) be greater than those which operate at lower temperatures (layers 40, 42, and 44 and layers 44, 46, and 48).

For example, the first stage (layer 36, 38, and 40) should have a cooling power equal to the sum of the cooling capacities of all of the other stages in the device, in this case, the second stage (layers 40, 42, and 44), and the third stage (layers 44, 46, and 48). This can be achieved by constructing the layers in a pyramid structure, shown in FIG. 3.

The structure of FIG. 3 can be fabricated by using selective wet etching, or reactive ion etching, or other techniques. Current flows through device 10 by having electrons injected at contact 50 and emerging from contact 52.

The current can be adjusted within each stage by injecting current into or withdrawing current from contacts 54 and 56 on the side of the pyramid.

The series connection places the devices 10 in the stack in thermal series, which is easily done during the construction of the device 10.

The same device 10 can be p-doped, resulting in a device 10 that utilizes hole thermionic emission to perform the cooling task. The p-doped device 10 uses the bandedge discontinuity in the valence band to modify non-isothermal current transport in the device 10, similar to the conduction band discontinuity in the n-doped electron thermionic device 10 previously described.

Devices 10 that are optimized for electron current cooling are not necessarily optimized for hole current cooling. Thus, materials that have larger valence bandedge

discontinuities and different effective masses may provide better cooling performance under hole thermionic cooling than electron thermionic cooling.

FIG. 2D shows the bandedge of a device 10 with a barrier layer as the final layer of the device 10. The layer 58 is the initial layer, and under bias voltage 60, the barrier layer bandedge 62 will extend all the way down to level 64, which is at one end of the voltage potential for the device 10. The bandedge 62 can take any shape.

FIG. 2E shows the bandedge of a device 10 that has several devices 10 cascaded together. Layer 66 is coupled to barrier layer 68. Barrier layer 68 is shown to have a curved bandedge, but barrier layer 68 can have a bandedge of any shape. Barrier layer 68 is directly coupled to another barrier layer 70, again shown with a curved bandedge. This cascade connection continues, with barrier layer 70 coupled directly to barrier layer 72, which is further coupled to barrier layer 74, ending at layer 76. layer 76 is coupled to the bias voltage 78.

FIG. 4 shows a cascaded device using stages with different bandedge discontinuities. The difference in bandedge from level 80 to level 82 is not the same as the difference in bandedge between level 84 and level 86. The difference in bandedge from level 84 to level 86 is not the same as the difference in bandedge between level 88 and level 90. The difference in bandedge from level 88 to level 90 is not the same as the difference in bandedge between level 92 and level 94. Thus, the cascade structure can accommodate different cooling capacities.

FIG. 5 shows a combination of n-doped and p-doped devices as described in the present invention. The combination of n-doped and p-doped devices 10 can be used in electrical series, similar to conventional thermoelectric coolers. The cascade structure of FIG. 5 will increase the cooling area of the device 10 without increasing the input current through the device 10. Electrons are injected at contact 50 and emitted from contact 52. Electrons travel through each layer and contacts 56 in a serpentine fashion, as in thermoelectric coolers.

Small Barrier Devices

FIG. 6 illustrates indicates the potential of Heterostructure Integrated Thermionic (HIT) devices to achieve high cooling power densities. These devices have however a low efficiency, e.g., have only a small percent of the Carnot value. The main problem is that the high cooling power at the cathode should fight the large heat flux that is coming from the hot junction only 1 or 2 microns away. As can be seen in FIG. 6, the device can not achieve net cooling when the barrier is thick. For

the case of thick barriers, electron transport is no longer determined by the supply of electrons at the cathode.

Graph 800 illustrates the cooling power of a device that has a difference in conduction bandedge, ϕ_C, of 0.03 electron volts. Graph 802 illustrates the cooling power of a device that has a difference in conduction bandedge, ϕ_C, of 0.04 electron volts. Graph 804 illustrates the cooling power of a device that has a difference in conduction bandedge, ϕ_C, of 0.05 electron volts.

When the barrier layers are thick, i.e., as the x-coordinate in the graph of FIG. 6 increases, the advantages of thermionic emission cooling are lost. Recent proposals, such as Mahan in Appl. Phys. Lett. 65(21), p. 2690, 1994, which is herein incorporated by reference, use multi-barrier thermionic coolers to achieve figure-of-merit (ZT) values that are a factor of two better than the bulk values. This proposed design is based on small barrier heights, e.g., on the order of k_BT, and uses the ballistic transport of electrons in very thin superlattice barriers. However, this analysis is a simple generalization of the expression of single barrier thermionic refrigeration to a small barrier multi-barrier case. The present invention provides a more detailed analysis of electron transport in superlattices. The present invention shows that tall barriers, e.g., $>>k_BT$, in conjunction with highly doped semiconductors provide large cooling power densities and higher efficiencies.

Experimental Results: Small Barrier Devices

A small barrier height device used a single InGaAsP (λ_{gap} =1.3 microns) barrier surrounded by n+ doped InGaAs cathode and anode layers. The InGaAs layers were grown using metal organic vapor phase epitaxy (MOCVD). The cathode layer thickness was 0.3 microns, and the anode layer thickness was 0.5 microns, and both layers were doped to 3×10^{18} cm^{-3}. The barrier layer had a n-doping of 2×10^{17} cm^{-3} and was one micron thick. Mesas with an area of 90 x 180 $microns^2$ were etched down using dry etching techniques. A Ni/AuGe/Ni/Au layer was used for top and bottom contact metallization.

FIG. 7 displays the temperature on top, shown by graph 900, and on the bottom, shown by graph 906, of the device as well as the substrate temperature far away from the device, shown by graph 904, as a function of current. All temperatures are relative to the value at zero current. The points on graphs 900-906 are experimental results, whereas the solid lines are derived from simulations. The rise in substrate temperature is an indication of the relatively high thermal resistance of ceramic package and the soldering layer used to mount the sample. Graph 900

indicates a net cooling of 0.5 °C on the top of the device at 300 milliamps. Graph 906 illustrates that there is heating of 0.2 degrees on the bottom of the device at 300 milliamps, and graph 904 indicates that there is some cooling or heating of the substrate.

The cooling indicated by graph 900 over a one micron barrier corresponds to cooling capacities on the order of hundreds of watts/cm^2. For the simulation results, joule heating in the layers, substrate, and gold wire bonds were included as well as thermionic emission cooling (heating) at the cathode (anode) junction and the thermoelectric effect at the metal/semiconductor junctions. The Peltier effect at the junction InGaAs(n)/Au was studied by applying current between two bottom contacts. A cooling 2-3 times smaller than the thermionic cooling was measured.

FIG. 8 illustrates the measured cooling at various substrate temperatures for the small barrier height device. Graph 1000 is the measured cooling at 20 °C, graph 1002 is the measured cooling at 30 °C, graph 1004 is the measured cooling at 40 °C, graph 1006 is the measured cooling at 50 °C, graph 1008 is the measured cooling at 60 °C, graph 1010 is the measured cooling at 70 °C, and graph 1012 is the measured cooling at 80 °C. The device provides additional cooling as the temperature of the substrate rises. A net cooling of about 1°C is measured at an 80 °C substrate temperature and a current of 350 milliamps. This improvement as a function of substrate temperature is caused by the decrease of the thermal conductivity of the barrier at higher temperatures, and the increase of thermionic emission cooling due to the larger thermal spread of carriers near the Fermi energy.

High Barrier Heterostructure Thermionic Coolers

The present invention uses tall barriers in highly degenerate semiconductors which combines the advantages of large density of states and selective emission of hot electrons in thermionic emission.

FIG. 9A illustrates the Fermi levels of a large barrier height device in accordance with the present invention. The Fermi energy level 1200 and the barrier height 1202 shown in FIG. 9A illustrate that the barrier height 1202, e.g., the difference in bandedges between the barrier layer 12 and the semiconductor layer 10, is now much larger than k_BT, while the difference between barrier height 1202 and the Fermi energy 1200 of the semiconductor layer 10 is on the order of k_BT.

FIG. 9B illustrates the thermoelectric figure-of-merit for bulk InGaAs and high barrier superlattices as a function of doping as used in the present invention. FIG. 9B shows the ZT 1204 for an InGaAs/InAlAs multibarrier structure (ΔE_C =

0.51 eV), the ZT 1206 for an InGaAs/InP multibarrier structure (ΔE_C = 0.24 eV), and the ZT 1208 for bulk InGaAs. The order of magnitude improvement in ZT is due to a large increase in the Seebeck coefficient at high doping densities in the multibarrier structures. The thermal conductivity of the composite material is taken to be 5 W/m°C, i.e. identical to the bulk InGaAs.

In the above analysis quasi-diffusive transport of elections above the barriers is assumed. In this near ohmic conduction, electrical conductivity and Seebeck coefficients can be defined similar to that of the bulk materials. There are not significant changes in the device performance due to the finite electron energy relaxation length. Instead, corrections due to ballistic transport will tend to further improve the cooling characteristics.

FIG. 9C illustrates the net cooling as a function of current for the high barrier heterostructure thermionic coolers of the present invention.

Graph 1210 illustrates the net cooling for bulk InGaAs, which has a maximum of 4 degrees at a 0.2 amp current. Graph 1212 illustrates the net cooling for the high barrier heterostructure InGaAs/InP material, which has a maximum of 14 degrees at 0.7 amps. Graph 1214 illustrates the net cooling for the high barrier heterostructure InGaAs/InAlAs material, which has cooling above 20 degrees at 0.6 amps.

To take full advantage of the large density of states, conservation of lateral momentum in the thermionic emission process should be relaxed. This can be achieved by using carrier-to-carrier scattering in heavily doped samples and by using non-smooth interfaces. If the high barrier thermionic emission cooling is extended to extremely highly doped materials, (e.g., with doping levels $>10^{20}$-10^{21} cm^{-3}), the materials are in the metallic conduction regime. The thermal conductivity of such a material will no longer be limited by the lattice contribution, but by electronic contributions. Since electrical and thermal conductivities in a metal are related through the Wiedemann-Franz law, the expression for thermoelectric figure-of-merit ZT will reduce only to the Seebeck coefficient and further improvements are possible.

General Considerations

The use of thermionic coolers provides a method for cooling electronics that is currently unavailable. The use of both electron and hole thermionic emission to cool electronics will allow for small thermionic coolers that can be fabricated as part of integrated circuits to allow those circuits to be cooled while in use in various applications.

Conclusion

In summary, the present invention discloses a method and apparatus for high efficiency thermionic cooling. The method comprises the steps of growing a semiconductor layer with a first bandedge, and growing a first barrier layer on the semiconductor layer, wherein a bandedge of the first barrier layer is at least $k_B T$ higher than a Fermi level of the semiconductor layer, where k_B is Boltzman's constant and T is the temperature at a junction between the semiconductor layer and the first barrier layer.

The description of the preferred embodiment is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not with this detailed description, but rather by the claims appended hereto.

WHAT IS CLAIMED IS:

1. A method for making a thermionic non-isothermal device, comprising the steps of:

growing a semiconductor layer with a first bandedge; and

growing a first barrier layer on the semiconductor layer, wherein a bandedge of the first barrier layer is at least $k_B T$ higher than a Fermi level of the semiconductor layer, where k_B is Boltzman's constant and T is the temperature at a junction between the semiconductor layer and the first barrier layer.

2. The method of claim 1, wherein the bandedge of the first barrier layer is substantially greater than $k_B T$ higher than the first bandedge of the semiconductor layer.

3. The method of claim 1, the method further comprising the step of growing a second semiconductor layer on the first barrier layer.

4. The method of claim 3, further comprising the step of growing at least one additional barrier layer on the second semiconductor layer.

5. The method of claim 4, further comprising the step of growing at least one additional semiconductor layer on the additional barrier layer.

6. The method of claim 3, further comprising the step of growing at least one additional pair of alternating barrier layers and semiconductor layers on the second semiconductor layer.

7. The method of claim 1, further comprising the step of growing at least one additional barrier layer on the first barrier layer.

8. The method of claim 1, wherein a thickness of the second semiconductor layer is between 0.001 and 1 micron.

9. The method of claim 1, wherein the first semiconductor layer is selected from a group comprising gallium arsenide, indium phosphide, silicon, silicon germanium, lead telluride, indium gallium arsenide ($In_xGa_{1-x}As$), indium aluminum arsenide ($In_xAl_{1-x}As$), gallium aluminum arsenide antimonide ($Ga_xAl_{1-x}As_ySb_{1-y}$), indium

arsenide (InAs), indium antimonide (InSb), indium gallium arsenide antimonide ($In_xGa_{1-x}As_ySb_{1-y}$), mercury cadmium telluride ($Hg_xCd_{1-x}Te$), mercury cadmium selenide ($Hg_xCd_{1-x}Se$), gallium nitride (GaN), aluminum gallium nitride ($Al_xGa_{1-x}N$), indium gallium nitride ($In_xGa_{1-x}N$), indium arsenide phosphide ($InAs_yP_{1-y}$), indium gallium arsenide phosphide ($In_xGa_{1-x}As_yP_{1-y}$), indium gallium aluminum arsenide ($In_xGa_yAl_{1-x-y}As$), lead tin telluride ($Pb_xSn_{1-x}Te$), aluminum arsenide (AlAs), aluminum antimonide (AlSb), zinc selenide (ZnSe), zinc telluride (ZnTe), boron nitride (BN), germanium (Ge), gallium phosphide (GaP), gallium antimonide (GaSb), gallium aluminum arsenide ($Ga_xAl_{1-x}As$), gallium arsenide phosphide ($GaAs_yP_{1-y}$), gallium indium phosphide ($Ga_xIn_{1-x}P$), gallium indium antimonide ($Ga_xIn_{1-x}Sb$), bismuth telluride (Bi_2Te_3), and bismuth selenide (Bi_2Se_3), where the subscripts x, y, 1-x, and 1-y denote the relative amounts of the atomic species in each ternary or quartenary materials and range from zero to one, inclusive.

10. The method of claim 1, wherein the second semiconductor layer is selected from a group comprising aluminum gallium arsenide, indium gallium arsenide phosphide, indium aluminum arsenide phosphide, gallium aluminum arsenide antimonide, silicon germanium, lead europium telluride, silicon oxide, aluminum oxide, vacuum, mercury cadmium telluride, mercury cadmium selenide, indium gallium arsenide antimonide, indium gallium aluminum nitride, bismuth telluride, bismuth selenide, boron nitride, zinc telluride, zinc selenide, lead tin telluride, aluminum antimonide, lead telluride, and air.

11. The method of claim 1, wherein the third semiconductor layer is the same material as the first semiconductor layer.

12. The method of claim 1, wherein the bandedge of the second semiconductor layer is piecewise linear.

13. The method of claim 1, wherein the bandedge of the second semiconductor layer is monotonically increasing.

14. The method of claim 1, wherein the bandedge of the second semiconductor is a step function.

15. The method of claim 1, wherein the method further comprises selectively removing a portion of the second semiconductor layer.

16. The method of claim 1, wherein the first semiconductor layer is n-type, and the bandedge is a conduction bandedge.

17. The method of claim 1, wherein the first semiconductor layer is p-type, and the bandedge is a valence bandedge.

18. The method of claim 1, wherein the second layer is a strained layer.

19. The method of claim 1, wherein the second layer is selectively oxidized.

20. A thermionic cooling device, comprising:

a first semiconductor layer with a first bandedge;

a first barrier layer attached to the first semiconductor layer, wherein a bandedge of the first barrier layer is at least $k_B T$ higher than a Fermi level of the semiconductor layer, where k_B is Boltzman's constant and T is the temperature at a junction between the first semiconductor layer and the first barrier layer, and selectively allows charge carriers to travel from the first semiconductor layer via thermionic emission to surmount the bandedge of the first barrier layer; and

a heat sink, coupled to the first barrier layer, wherein the charge carriers that travel from the first semiconductor layer to surmount the bandedge of the first barrier layer carry heat away from the first semiconductor layer to the heat sink.

21. The thermionic cooling device of claim 20, wherein the bandedge of the first barrier layer is substantially greater than $k_B T$ higher than the first bandedge of the semiconductor layer.

22. The thermionic cooling device of claim 20, further comprising a second semiconductor layer attached between the first barrier layer and the heat sink.

23. The thermionic cooling device of claim 22, further comprising at least one additional barrier layer attached between the second semiconductor layer and the heat sink.

24. The thermionic cooling device of claim 23, further comprising at least a second semiconductor layer attached between the additional barrier layer and the heat sink.

25. The thermionic cooling device of claim 22, further comprising at least one additional pair of alternating barrier layers and semiconductor layers attached between the second semiconductor layer and the heat sink.

26. The thermionic cooling device of claim 20, further comprising at least one additional barrier layer attached between the first barrier layer and the heat sink.

27. The thermionic cooling device of claim 20, wherein a thickness of the first barrier layer is between 0.001 and 1 micron.

28. The thermionic cooling device of claim 20, wherein the first semiconductor layer is selected from a group comprising gallium arsenide, indium phosphide, silicon, silicon germanium, lead telluride, indium gallium arsenide ($In_xGa_{1-x}As$), indium aluminum arsenide ($In_xAl_{1-x}As$), gallium aluminum arsenide antimonide ($Ga_xAl_{1-x}As_ySb_{1-y}$), indium arsenide (InAs), indium antimonide (InSb), indium gallium arsenide antimonide ($In_xGa_{1-x}As_ySb_{1-y}$), mercury cadmium telluride ($Hg_xCd_{1-x}Te$), mercury cadmium selenide ($Hg_xCd_{1-x}Se$), gallium nitride (GaN), aluminum gallium nitride ($Al_xGa_{1-x}N$), indium gallium nitride ($In_xGa_{1-x}N$), indium arsenide phosphide ($InAs_yP_{1-y}$), indium gallium arsenide phosphide ($In_xGa_{1-x}As_yP_{1-y}$), indium gallium aluminum arsenide ($In_xGa_yAl_{1-x-y}As$), lead tin telluride ($Pb_xSn_{1-x}Te$), aluminum arsenide (AlAs), aluminum antimonide (AlSb), zinc selenide (ZnSe), zinc telluride (ZnTe), boron nitride (BN), germanium (Ge), gallium phosphide (GaP), gallium antimonide (GaSb), gallium aluminum arsenide ($Ga_xAl_{1-x}As$), gallium arsenide phosphide ($GaAs_yP_{1-y}$), gallium indium phosphide ($Ga_xIn_{1-x}P$), gallium indium antimonide ($Ga_xIn_{1-x}Sb$), bismuth telluride (Bi_2Te_3), and bismuth selenide (Bi_2Se_3), where the subscripts x, y, 1-x, and 1-y denote the relative amounts of the atomic species in each ternary or quartenary materials and range from zero to one, inclusive.

29. The thermionic cooling device of claim 20, wherein the first barrier layer is selected from a group comprising aluminum gallium arsenide, indium gallium arsenide phosphide, indium aluminum arsenide phosphide, gallium aluminum arsenide

antimonide, silicon germanium, lead europeum telluride, silicon oxide, aluminum oxide, vacuum, mercury cadmium telluride, mercury cadmium selenide, indium gallium arsenide antimonide, indium gallium aluminum nitride, bismuth telluride, bismuth selenide, boron nitride, zinc telluride, zinc selenide, lead tin telluride, aluminum antimonide, lead telluride, and air.

30. The thermionic cooling device of claim 22, wherein the second semiconductor layer is the same material as the first semiconductor layer.

31. The thermionic cooling device of claim 20, wherein the bandedge of the first barrier layer is piecewise linear.

32. The thermionic cooling device of claim 20, wherein the first barrier layer is selectively removed.

33. The thermionic cooling device of claim 20, wherein the first semiconductor layer is n-type, and the bandedge is a conduction bandedge.

34. The thermionic cooling device of claim 20, wherein the first semiconductor layer is p-type, and the bandedge is a valence bandedge.

35. A thermionic power generation device, comprising:

a heat source;

a heat sink;

a first semiconductor layer with a first bandedge; and

a first barrier layer attached to the first semiconductor layer, wherein the wherein a bandedge of the first barrier layer is at least $k_B T$ higher than a Fermi level of the semiconductor layer, where k_B is Boltzman's constant and T is the temperature at a junction between the first semiconductor layer and the first barrier layer, and selectively allows charge carriers to travel from the first semiconductor layer via thermionic emission to surmount the bandedge of the first barrier layer, wherein the charge carriers that travel from the first semiconductor layer to surmount the bandedge of the first barrier layer are generated when the first semiconductor layer is exposed to the heat source and the first barrier layer is exposed to the heat sink.

36. The thermionic power generation device of claim 35, wherein the bandedge of the first barrier layer is substantially greater than $k_B T$ higher than the first bandedge of the semiconductor layer.

37. The thermionic power generation device of claim 35, further comprising a second semiconductor layer attached between the first barrier layer and the heat sink, wherein the first barrier layer is exposed to the heat sink through the second semiconductor layer.

38. The thermionic power generation device of claim 35, further comprising at least one additional barrier layer attached between the second semiconductor layer and the heat sink.

39. The thermionic power generation device of claim 38, further comprising at least one additional semiconductor layer attached between the additional barrier layer and the heat sink.

40. The thermionic power generation device of claim 37, further comprising at least one additional pair of alternating barrier layers and semiconductor layers attached between the second semiconductor layer and the heat sink.

41. The thermionic power generation device of claim 35, further comprising at least one additional barrier layer attached between the first barrier layer and the heat sink.

42. The thermionic power generation device of claim 35, wherein a thickness of the first barrier layer is between 0.001 and 1 micron.

43. The thermionic power generation device of claim 35, wherein the first semiconductor layer is selected from a group comprising gallium arsenide, indium phosphide, silicon, silicon germanium, lead telluride, indium gallium arsenide ($In_xGa_{1-x}As$), indium aluminum arsenide ($In_xAl_{1-x}As$), gallium aluminum arsenide antimonide ($Ga_xAl_{1-x}As_ySb_{1-y}$) indium arsenide (InAs), indium antimonide (InSb), indium gallium arsenide antimonide ($In_xGa_{1-x}As_ySb_{1-y}$), mercury cadmium telluride ($Hg_xCd_{1-x}Te$), mercury cadmium selenide ($Hg_xCd_{1-x}Se$), gallium nitride (GaN), aluminum gallium nitride ($Al_xGa_{1-x}N$), indium

gallium nitride ($In_xGa_{1-x}N$), indium arsenide phosphide ($InAs_yP_{1-y}$), indium gallium arsenide phosphide ($In_xGa_{1-x}As_yP_{1-y}$), indium gallium aluminum arsenide ($In_xGa_yAl_{1-x-y}As$), lead tin telluride ($Pb_xSn_{1-x}Te$), aluminum arsenide (AlAs), aluminum antimonide (AlSb), zinc selenide (ZnSe), zinc telluride (ZnTe), boron nitride (BN), germanium (Ge), gallium phosphide (GaP), gallium antimonide (GaSb), gallium aluminum arsenide ($Ga_xAl_{1-x}As$), gallium arsenide phosphide ($GaAs_yP_{1-y}$), gallium indium phosphide ($Ga_xIn_{1-x}P$), gallium indium antimonide ($Ga_xIn_{1-x}Sb$), bismuth telluride (Bi_2Te_3), and bismuth selenide (Bi_2Se_3), where the subscripts x, y, 1-x, and 1-y denote the relative amounts of the atomic species in each ternary or quartenary materials and range from zero to one, inclusive.

44. The thermionic power generation device of claim 35, wherein the first barrier layer is selected from a group comprising aluminum gallium arsenide, indium gallium arsenide phosphide, indium aluminum arsenide phosphide, gallium aluminum arsenide antimonide, silicon germanium, lead europeum telluride, silicon oxide, aluminum oxide, vacuum, mercury cadmium telluride, mercury cadmium selenide, indium gallium arsenide antimonide, indium gallium aluminum nitride, bismuth telluride, bismuth selenide, boron nitride, zinc telluride, zinc selenide, lead tin telluride, aluminum antimonide, lead telluride, and air.

45. The thermionic power generation device of claim 35, wherein the second semiconductor layer is the same material as the first semiconductor layer.

46. The thermionic power generation device of claim 35, wherein the bandedge of the first barrier layer is piecewise linear.

47. The thermionic power generation device of claim 35, wherein the first barrier layer is selectively removed.

48. The thermionic power generation device of claim 35, wherein the first semiconductor layer is n-type, and the bandedge is a conduction bandedge.

49. The thermionic power generation device of claim 35, wherein the first semiconductor layer is p-type, and the bandedge is a valence bandedge.

50. The thermionic power generation device of claim 35, wherein the thermionic power generation device is a pixel of an imaging system.

51. The thermionic power generation device of claim 35, wherein the thermionic power generation device forms more than one pixel of an imaging system.

FIG. 1A

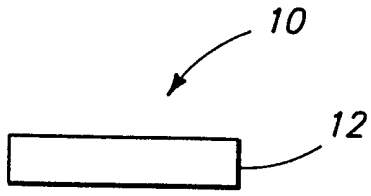


FIG. 1B

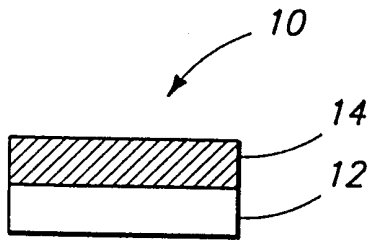


FIG. 1C

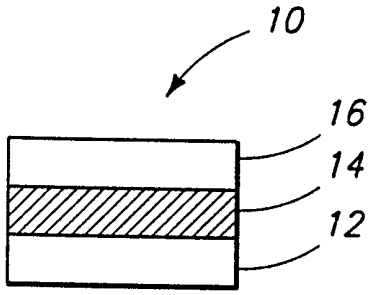


FIG. 1D

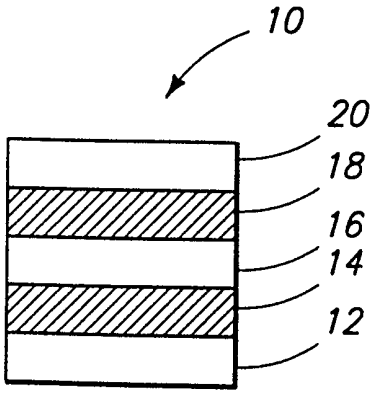


FIG. 1E

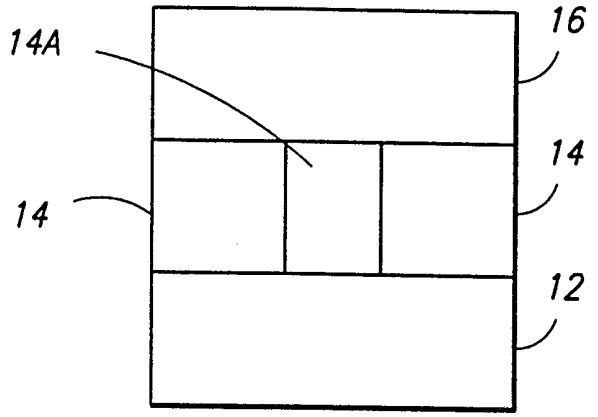


FIG. 2A

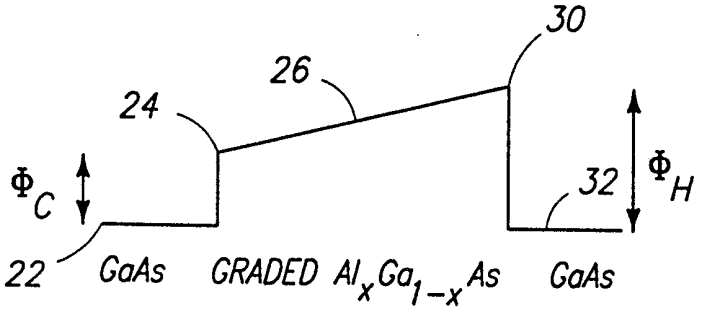


FIG. 2B

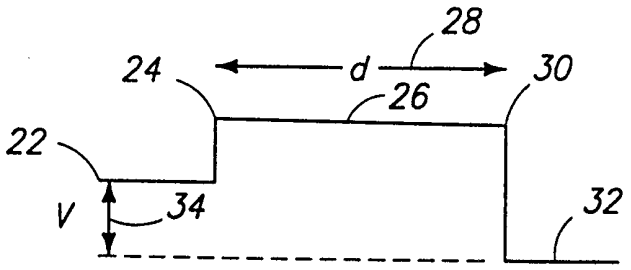


FIG. 2C

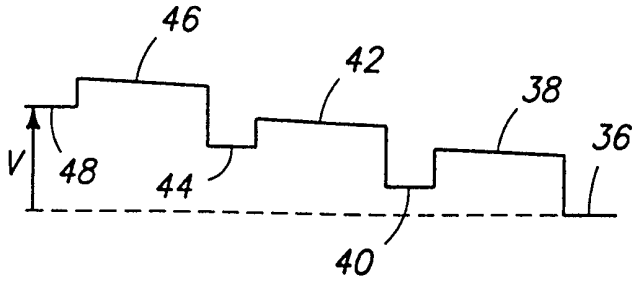
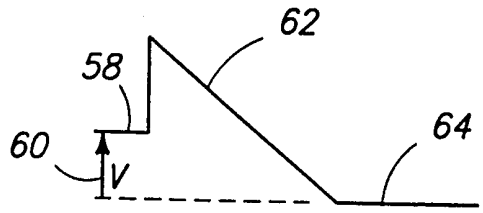


FIG. 2D



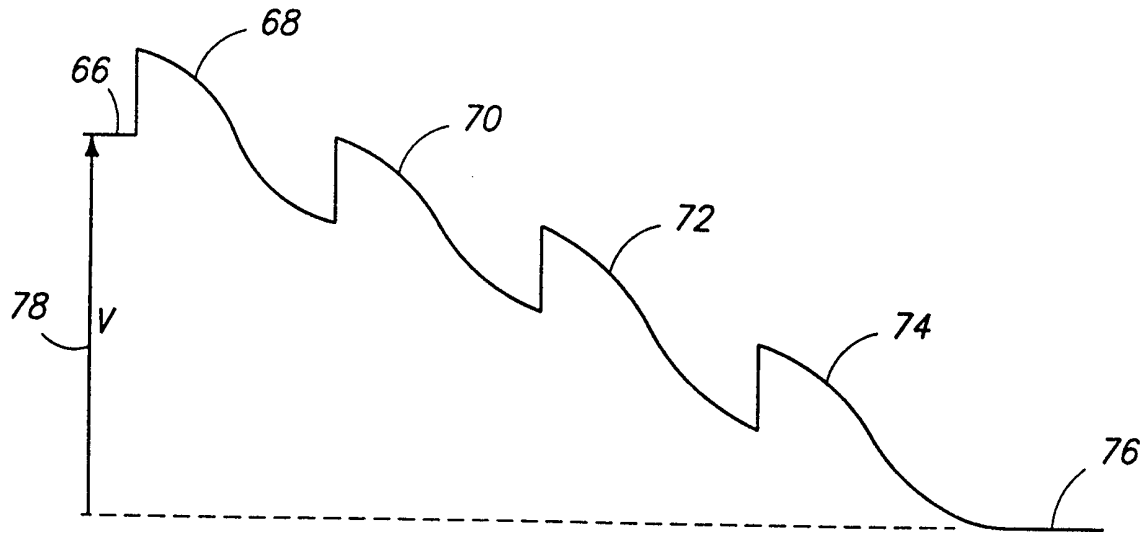


FIG. 2E

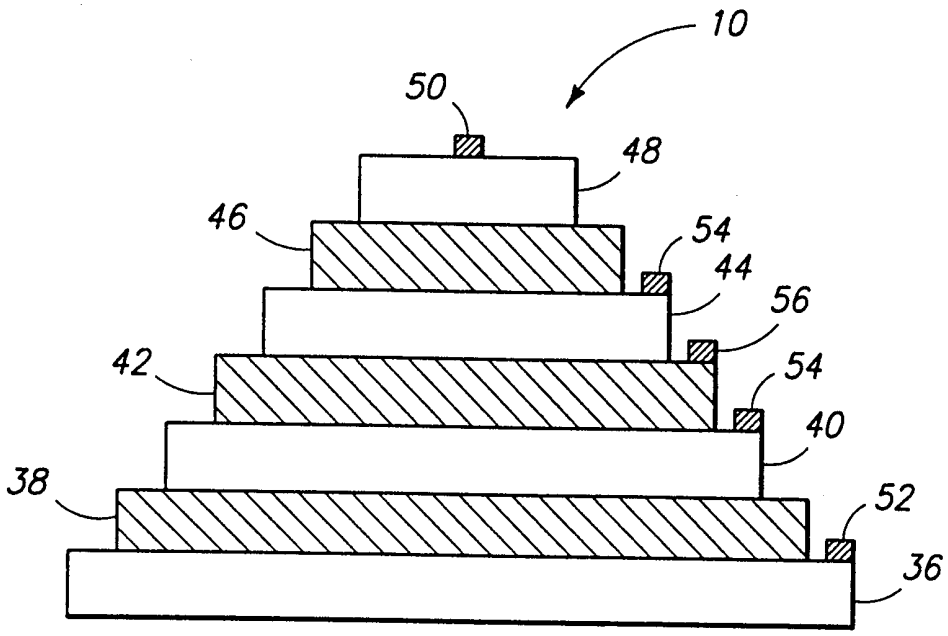


FIG. 3

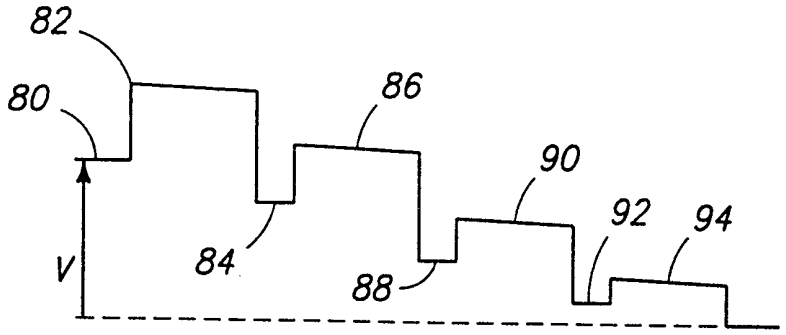


FIG. 4

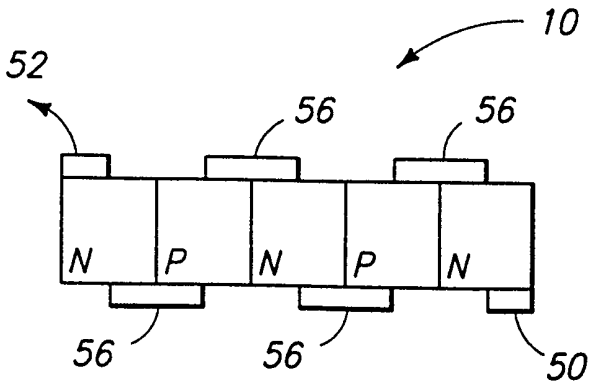


FIG. 5

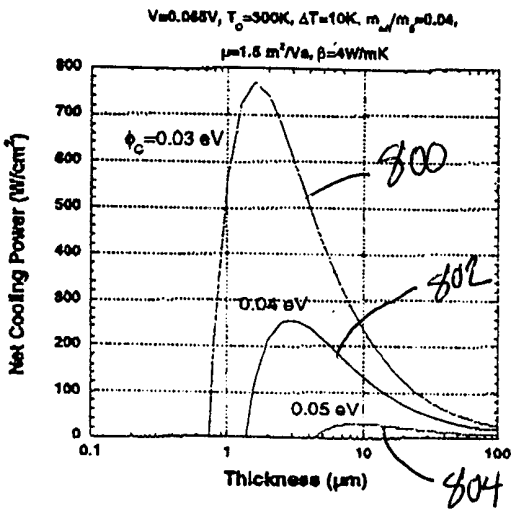

V=0.065V, T_o=300K, ΔT=10K, m_e/m_e=0.04,
μ=1.5 m²/Vs, β=4W/mK
Net Cooling Power (W/cm²)
800
700
600
500
400
300
200
100
0
0.1
1
10
100
Thickness (μm)
φ_c=0.03 eV
0.04 eV
0.05 eV
900
902
904

FIG. 6

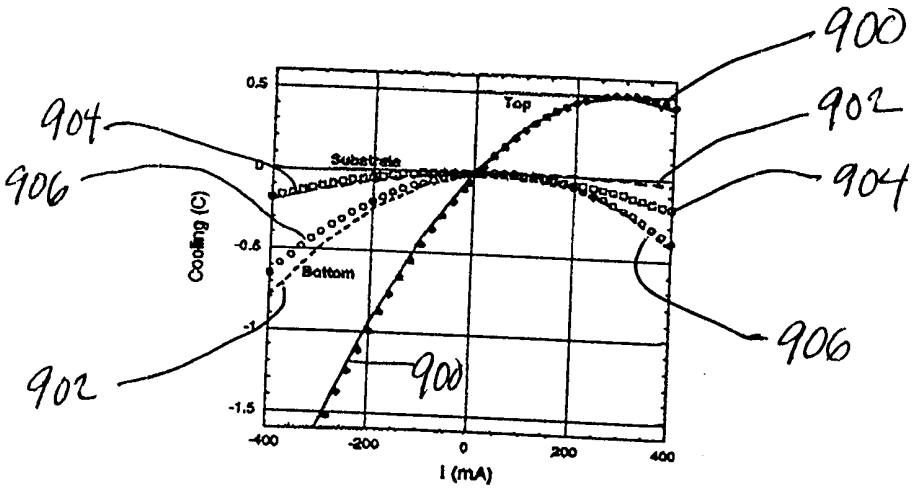

900
902
904
906
Top
Substrate
Bottom
Cooling (C)
0.5
0
-0.5
-1
-1.5
-400
-200
0
200
400
I (mA)

FIG. 7

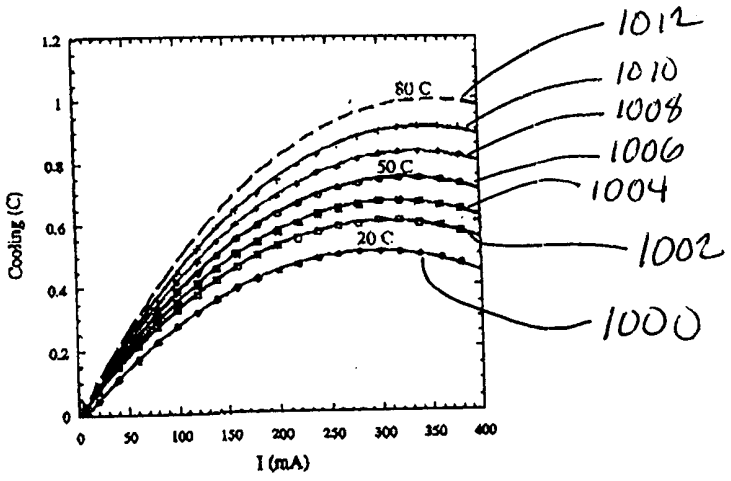

1012
1010
1008
1006
1004
1002
1000
80 C
50 C
20 C
Cooling (C)
I (mA)
0
0.2
0.4
0.6
0.8
1
1.2
0
50
100
150
200
250
300
350
400

FIG. 8

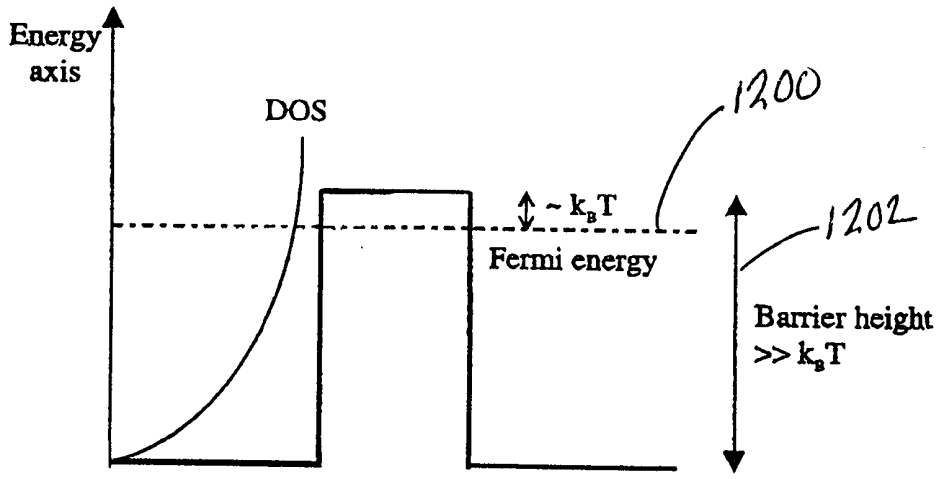

Energy axis
DOS
1200
~ k_BT
Fermi energy
1202
Barrier height
>> k_BT

FIG. 9A

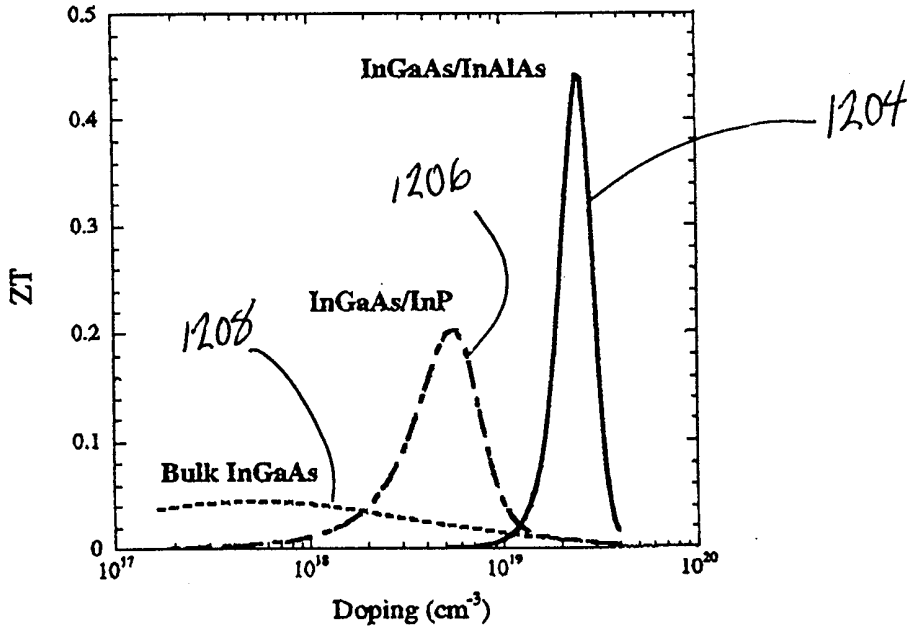

0.5
0.4
0.3
0.2
0.1
0
ZT
InGaAs/InAlAs
1204
1206
InGaAs/InP
1208
Bulk InGaAs
10^{17}
10^{18}
10^{19}
10^{20}
Doping (cm^{-3})

FIG. 9B

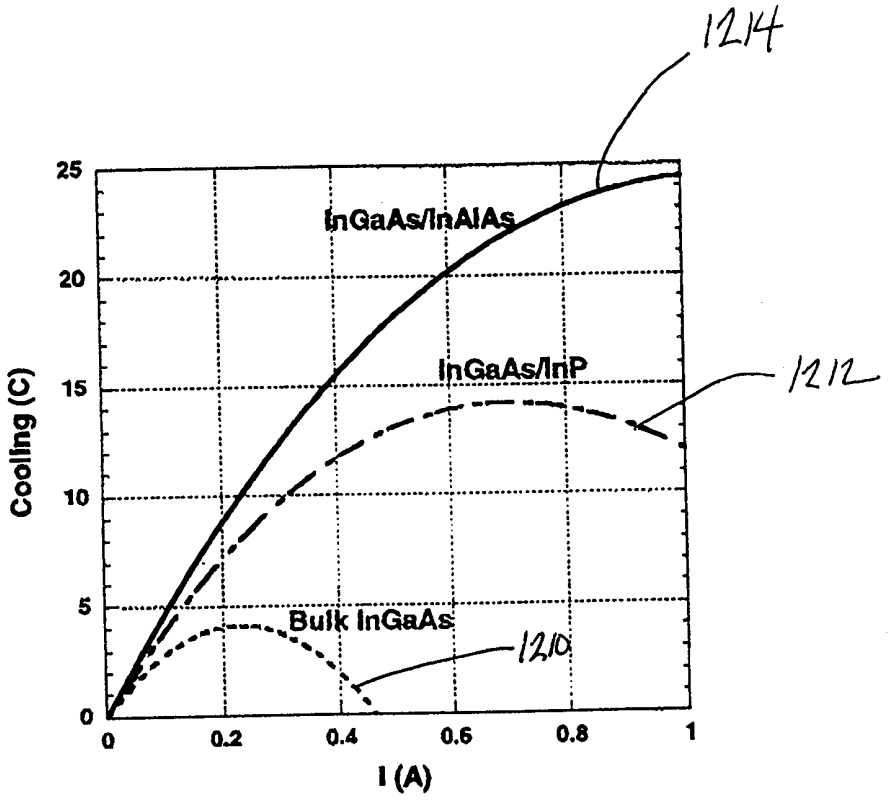

1214
InGaAs/InAlAs
InGaAs/InP
1212
Bulk InGaAs
1210
Cooling (C)
I (A)
0
5
10
15
20
25
0
0.2
0.4
0.6
0.8
1

FIG. 9C