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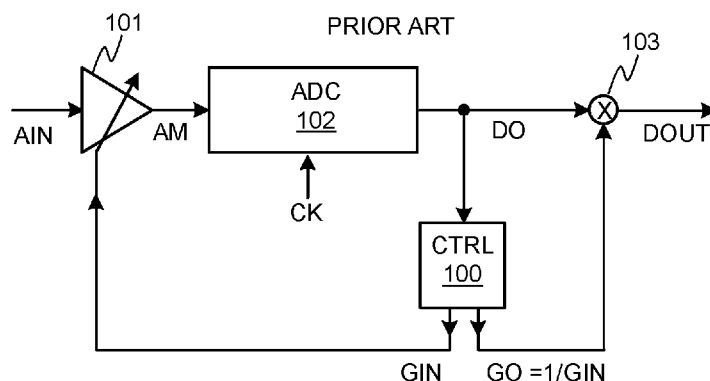


Fig. 1

(57) Abstract: An analogue-to-digital converter (ADC), comprising: an adaptive whitening filter configured to filter an analogue input signal and output a whitened analogue input signal; a first converter configured to receive said whitened analogue input signal and output a whitened digital signal; a controller configured to adapt the whitening filter based on the received analogue input signal.



Analog-to-digital converter and method

Technical Field

[0001] The present disclosure relates to analogue-to-digital converters (ADCs) and in particular ADCs for converting audio signals containing speech.

Background

[0002] Analogue-to-digital converters (ADCs) are known and used in a variety of applications. One particular application is within audio signal paths where it is desired to store and transmit audio in digital format. An ADC may therefore be arranged in an audio signal path to convert an analogue signal such as that detected by a microphone, into an equivalent digital signal, i.e. digital data, which may be stored or passed on for further processing.

[0003] In communications devices, such as mobile telephones, integrated microphones are required to have a relatively large dynamic range to cope with large-amplitude interfering signals such as wind noise. Consequently, there is a need for ADCs used in such devices to also have a large dynamic range to convert analogue signals over their full dynamic range.

Summary

[0004] According to a first aspect of the disclosure, there is provided an analogue-to-digital converter (ADC), comprising: an adaptive whitening filter configured to filter an analogue input signal and output a whitened analogue input signal; a first converter configured to receive said whitened analogue input signal and output a whitened digital signal; a controller configured to adapt the whitening filter based on the received analogue input signal.

[0005] The ADC may further comprise an adaptive de-whitening filter configured to filter the whitened digital output signal and output a de-whitened digital output signal, the de-whitening filter being substantially inverse to the whitening filter. The controller may be configured to adapt the whitening filter based on the received analogue input signal.

[0006] The whitening filter may comprise one or more of a shelving filter, a bandpass filter, a high pass filter, and a differentiator.

[0007] The controller may be configured to adapt the whitening filter based on the whitened digital signal or the de-whitened digital output signal.

[0008] The controller may be further configured to adapt the first converter based on the received analogue input signal.

[0009] Additionally or alternatively, the controller may be configured to adapt the first converter based on the whitened digital signal or the de-whitened digital output signal. In some embodiments, the first converter is a sigma-delta ADC. In some embodiments, adapting of the first converter comprises one or more of: a) changing an order of the ADC; b) changing an over sample ratio of the ADC; c) changing a bias current of one or more circuits in the ADC; d) changing a number of bits in a quantizer of the ADC; and e) switching between a high-performance integrator and a low-performance integrator.

[0010] In some embodiments, adapting the whitening filter comprises selectively bypassing the whitening filter. For example, the whitening filter may be bypassed if it was envisaged that the resultant signal output from the ADC were the input signal to be whitened would be clipped or out of range.

[0011] The ADC may further comprise a second converter configured to receive said analogue input signal and output a secondary digital signal to the controller. In which case, the controller may be configured to selectively bypass the whitening filter based on the secondary digital signal. The second converter may be a faster converter than the first converter. For example, the second converter may have a lower resolution or be of a different type to the first converter. For example, if the first converter is a sigma-delta ADC, the second converter may be a successive approximation ADC.

[0012] The controller may be configured to selectively bypass the whitening filter in response to detecting that the input audio signal exceeds a clipping threshold.

[0013] According to a further aspect of the disclosure, there is provided an integrated circuit comprising an ADC as described above.

[0014] According to a further aspect of the disclosure, there is provided an electronic device comprising an ADC as described above. The electronic device may comprise one or more of: a portable device; a battery powered device; a communications device; a mobile or cellular telephone; a personal media device; a computing device; a laptop, notebook or tablet computer; a gaming device; and a wearable device.

[0015] According to a further aspect of the disclosure, there is provided a method of analogue-to-digital conversion, comprising: whitening an analogue input signal with a whitening filter to generate a whitened analogue input signal; converting the whitened analogue input signal with a first converter to generate a whitened digital signal; and adapting the whitening filter based on the received analogue input signal.

[0016] The method may further comprise de-whitening the whitened digital signal with a de-whitening filter to generate a de-whitened digital signal, the de-whitening filter being substantially inverse to the whitening filter. In which case, the method may further comprise, adapting the de-whitening filter based on the received analogue input signal.

[0017] The whitening filter may comprise one or more of a shelving filter, a bandpass filter, a high pass filter, and a differentiator.

[0018] The de-whitened filter may adapted based on the whitened digital signal or the de-whitened digital output signal.

[0019] The method may further comprise adapting the first converter based on the received analogue input signal.

[0020] The first converter may be adapted based on the whitened digital signal or the de-whitened digital output signal.

[0021] In some embodiments, the first converter is a sigma-delta ADC. Adapting of the first converter may comprise one or more of a) changing an order of the ADC; b) changing an over sample ratio of the ADC; c) changing a bias current of one or more circuits in the ADC; and d) changing a number of bits in a quantizer of the ADC.

[0022] Adapting the whitening filter may comprise selectively bypassing the whitening filter.

[0023] The method may further comprise converting with a second converter the analogue input signal to generate a secondary digital signal. The whitening filter may be selectively bypassed based on the secondary digital signal. The whitening filter may be otherwise adapted based on the secondary digital signal. The second converter may be a faster converter than the first converter. For example, the second converter may have a lower resolution or be of a different type to the first converter. For example, if the first converter is a sigma-delta ADC, the second converter may be a successive approximation ADC.

[0024] The whitening filter may be selectively bypassed in response to detecting that the input audio signal exceeds a clipping threshold.

[0025] Throughout this specification the word "comprise", or variations such as "comprises" or "comprising", will be understood to imply the inclusion of a stated element, integer or step, or group of elements, integers or steps, but not the exclusion of any other element, integer or step, or group of elements, integers or steps.

Brief Description of Drawings

[0026] Embodiments of the present disclosure will now be described by way of non-limiting examples with reference to the drawings, in which:

[0027] Figure 1 illustrates the general principles of an analogue-to-digital convertor (ADC) implementing dynamic range extension (DRE);

[0028] Figure 2 graphically illustrates the effect of conversion of an audio signal comprising human speech derived from a microphone using the ADC shown in Figure 1;

[0029] Figure 3 is a block diagram of an ADC according to embodiments of the present disclosure;

[0030] Figure 4 is a block diagram of a process performed by the ADC shown in Figure 3;

[0031] Figure 5 graphically illustrates the effect of conversion of an audio signal comprising human speech derived from a microphone using the ADC shown in Figure 3;

[0032] Figure 6 is a circuit diagram of a whitening filter of the ADC shown in Figure 3;

[0033] Figure 7 is a graph showing a frequency response of the whitening filter of Figure 6 according to embodiments of the present disclosure;

[0034] Figure 8 is a graph showing frequency response of an audio signal input into the ADC of Figure 3 and a digital output signal output from the ADC of Figure 3; and

[0035] Figure 9 is a graph showing frequency response of an audio signal input into the ADC of Figure 3 and a digital output signal output from the ADC of Figure 3 with and without whitening and de-whitening implemented.

Description of Embodiments

[0036] To maximise the effective resolution of an ADC, it is known to apply a signal-dependent analogue gain (G_{IN}) to the input analogue signal prior to digital conversion and to apply a corresponding inverse digital gain ($G_O = 1/G_{IN}$) adjustment to the converted digital signal in order to compensate for the applied analogue gain change G_{IN} . This is known as dynamic range extension (DRE). Typically, a small amplitude analogue input signal may be amplified by a large value of G_{IN} so as to make use of more of the ADC input range, thus effectively improving the resolution of the ADC for small amplitude signals. A correspondingly large digital attenuation is applied to the digital signal to compensate for the large analogue amplification. This means that, for small signals, the quantisation noise and thermal noise of the ADC may be attenuated by the low digital gain ($G_O = 1/G_{IN}$).

[0037] **Figure 1** illustrates the general principles of an analogue-to-digital convertor (ADC) implementing dynamic range extension (DRE). A control block 100 adjusts the

gain GIN applied to an analogue input signal AIN by an analogue gain element such as an analogue amplifier 101 so that, regardless of the peak value of the magnitude of the incoming signal AIN, the ADC 102 receives an amplified analogue signal AM (where $AM = AIN \cdot GIN$) with peak values near the ADC full scale input range. The control block 100 also compensates for this analogue gain adjustment GIN by arranging for the output signal DO to be scaled by a digital gain GO, which is the inverse of the analogue gain GIN, via digital multiplier 103. The control block 100 adjusts the allocation of the gains between the analogue and digital gain elements 101 and 103 based on the amplitude or envelope of the input signal AIN.

[0038] Conventional dynamic range extension is effective for input audio signals with a flat frequency response. However, in instances where the frequency response of the input signal is not flat, such as for speech, gain is limited by the maximum signal level at any one frequency across the signal's spectrum.

[0039] The typical power spectrum for an audio signal derived from human speech is particularly non uniform. The human speech spectrum is inversely proportional to frequency, having a relatively high signal level at low frequencies, the signal level tailing off at high frequencies.

[0040] **Figure 2** graphically illustrates the effect of conversion of an audio signal comprising human speech derived from a microphone using the ADC 102. In this case the ADC 102 is a sigma delta ADC of the type typically used in audio applications. The input speech signal, shown in graph (a), is amplified by the amplified 101 and the amplified signal shown in graph (b) provided to the ADC 102 which converts the received amplified signal to a digital representation. The sigma delta ADC 102 applies noise, shown in graph (c), which increases at high frequencies due to inherent noise shaping in the ADC 102. This noise is added by the ADC 102 to the digital representation of the input audio signal and the ADC 102 outputs a digital audio signal as shown in graph (d). It can thus be seen that as frequency increases the SNR of the digital output signal decreases to a point at which the level of the speech drops below the ADC 102's noise floor.

[0041] Embodiments of the present disclosure aim to address or at least ameliorate one or more of the above issues by implementing a non-uniform, adaptive filtering technique in which an input audio signal is filtered to substantially whiten or flatten its frequency response. This filtered or whitened audio signal is then provided to an ADC and subsequently apply an inverse whitening filter to the digital representation output from the ADC.

[0042] **Figure 3** is a block diagram of an analogue-to-digital convertor (ADC) 200 according to embodiments of the present disclosure. The ADC 200 comprises a first ADC 202, a whitening filter 204, a de-whitening filter 206 and a control module 208. Optionally, the ADC 200 comprises a second ADC 210.

[0043] The whitening filter 204 is configured to receives an audio signal AIN and output a whitened audio signal AW to the first ADC 202. The whitening filter 204 may be configured to implement any filter configured to whiten or flatten the audio signal AIN. Non-limiting examples include a shelving filter, a low pass filter, a high pass filter, a bandpass filter, a pre-emphasis filter and a differentiator or any reasonable combination thereof. Further implementation examples of the whitening filter 204 will be explained in more detail below.

[0044] The first ADC 202 receives a clock signal CK, which may or may not be provided by the control module 208 and converts the whitened audio signal AW to a digital whitened audio signal DW. The first ADC 202 is preferably a sigma delta ADC of the type typically used in audio applications. The digital whitened audio signal DW is provided to a de-whitening filter 206 which equalises the digital whitened audio signal to remove the whitening introduced by the whitening filter 204. Thus, the de-whitening filter 206 may apply a digital filter which is an approximate inverse of the analogue filter applied to the audio signal AIN by the whitening filter 204. The de-whitening filter 206 then outputs this digital output signal DOUT.

[0045] In a variation, the de-whitening filter 206 may be omitted and the digital whitened signal DW output from the ADC 200. In such cases, the characteristics of the whitening filter 204 may also be output, for example by the control module 208 or from the whitening filter 204 itself. This variation may be applicable where the output digital

whitened signal DW is being provided to a machine learning block (not shown). For example, the digital whitened signal DW and one or more control outputs from the control module 208 may be provided to one or more neural networks.

[0046] The whitening filter 204 and the de-whitening filter 206 are preferably adaptive. The adaptive nature of the whitening filter 204 may avoid or at least reduce clipping of the audio signal AIN by the first ADC 202. The control module 208 is thus configured to control at least the whitening filter 204 based on, directly or indirectly, the audio signal AIN received by the ADC 200. In the embodiment shown, the control module 208 adapts the whitening filter 204 based on the digital whitened signal DW output from the first ADC 202 (i.e. indirectly on the audio signal AIN). In alternative embodiments, the control module may, additionally or alternatively, adapt the whitening filter 204 based on the whitened audio signal AW output from the whitening filter 204, or directly based on the audio signal AIN. Equally, the digital output signal DOUT could be used as an input to the control module 208 upon which to base the adaptation of the whitening filter 204.

[0047] The de-whitening filter 206 may also be controlled by the control module 208, as is shown in Figure 3. In which case, the de-whitening filter 206 may be adapted in a similar manner to that described in respect of the whitening filter 204. Alternatively, the de-whitening filter 206 may be adapted based on the characteristics of the whitening filter 204.

[0048] The control module 208 may also be configured to bypass the whitening filter 204, the de-whitening filter 206 or both. Such bypassing may be performed, for example, if it is determined that clipping may occur due to one or more events in the audio input signal AIN.

[0049] Optionally, the ADC 200 may comprise a second ADC 210 configured to convert the analogue audio input signal AIN to a digital audio input signal DIN which may then be provided to the control module 208. The second ADC 210 may have a lower resolution than the first ADC 202 and may be substantially faster than the first ADC 202 in converting an analogue input signal into a corresponding digital signal. In some embodiments, the second ADC 210 is a successive-approximation ADC or a low-resolution sigma-delta ADC. By providing the second ADC 210, any events in the audio

input signal AIN that might lead to clipping in the first ADC 202 can be detected by the control module 208. In response to detecting such events, the control module 208 may adjust one or more characteristics of the whitening filter 204 and/or the de-whitening filter 206 to prevent or reduce clipping. In some embodiments control module 208 may bypass the whitening filter 204, the de-whitening filter 206 or both based on the digital input signal DIN received from the second ADC 210.

[0050] Optionally, the control module 208 may be configured to adapt the first ADC 202 based on one or more of the above described inputs to the control module 208. For instance, the control module 208 may adjust the performance of the first ADC 202 based on the audio signal AIN, the whitened signal AW, the digital whitened signal DW or the output signal DOUT. Performance of the first ADC 202 may be adapted by changing one or more characteristics of configurations of the first ADC 202. For example, the order of the first ADC 202 may be changed. For example, an over-sampling ratio of the first ADC 202 may be changed. For example, a bias current of one or more circuits of the ADC 202 may be changed. For example, a number of bits in a quantizer of the first ADC 202 (where the first ADC 202 is a sigma delta ADC) may be changed. In a further example, one or more analogue amplifier-based integrators used in the first ADC 202 may be switched out or substituted for a corresponding inverter-based amplifier, such as a switch capacitor integrator circuit comprising an inverter. Such inverter-based amplifiers are well known and will not be described in detail here. An example of such architecture is described in “A Two Stage Switched-Capacitor Integrator for High Gain Inverter-Like Architectures”, P Bruschi et al, IEEE Transactions on Circuits and Systems, Vol. 67, No. 2, the contents of which is incorporated by reference in its entirety.

[0051] **Figures 4** illustrates steps for conversion of an audio signal AIN comprising human speech derived from a microphone by the ADC 200 and **Figure 5** illustrates the effect of the conversion in accordance with embodiments of the present disclosure. For simplicity, the control module 208 and the second ADC 210 have been omitted from Figure 5.

[0052] Referring to both Figure 4 and Figure 5, at **step 402**, an audio signal AIN is received by the ADC 200.

[0053] The audio signal AIN, which comprises human speech and is shown in graph (a), is whitened at **step 404** by the whitening filter 204 which applies an equalisation shown in graph (b) to substantially whiten or flatten the input speech signal AIN. The characteristics of the whitening filter 204 may be controlled by the control module 208.

[0054] At **step 406**, the whitened audio signal AW, shown in graph (c), is provided to the ADC 202 which converts the whitened input signal AW to a digital representation. Noise inherent to the sigma delta ADC 202, shown in graph (d) is added during the conversion. Again, this noise increases at high frequencies due to inherent noise shaping in the ADC 202. This noise is added by the ADC 202 to the digital representation of the input audio signal and the ADC 202 outputs a whitened digital signal DW as shown in graph (e).

[0055] Because the signal input to the ADC 202 is substantially whitened, it can be seen from graph (e) that SNR of the digital representation output from the ADC 202 is maintained across a larger frequency range. It can also be seen that the noise crossover occurs at a much higher frequency when compared to the prior art arrangement shown in Figure 2.

[0056] To restore the information from the original input speech signal shown in (a), at **step 408**, a de-whitening filter 204 digitally filters the whitened digital signal DW with a filter which is substantially inverse to that which was applied by the whitening filter 202, as shown by graph (f). The result shown in graph (g) is a digital output signal DOUT which is a digital representation of the input speech signal AIN. The dashed line represents the filtered noise whose level is below the level of the speech signal substantially across the frequency range of speech.

[0057] The digital output signal DOUT is then output at **step 410**.

[0058] Referring again to Figure 3 and as mentioned above, the whitening filter 204 may implement any conceivable filter configured to whiten the audio signal AIN.

[0059] **Figure 6** illustrates an example configuration for the whitening filter 204 as a shelving filter. In the example shown in Figure 6, the whitening filter 204 comprises a

non-inverting amplifier 212 comprising an operational amplifier (op-amp) 214, a capacitor C1, a first resistor R1 and a second resistor R2. It will however be appreciated that a corresponding inverting topology may be equally used to achieve a similar effect as that of the non-inverting topology shown in Figure 6.

[0060] The input audio signal AIN is provided to the non-inverting input of the op-amp 214. The inverting input of the op-amp 214 is coupled to ground GND via the first resistor R1 followed by the capacitor C1. The inverting input of the op-amp 214 is coupled to the output of the op-amp 214 via the second resistor R2. The output of the op-amp 214 is then provided to the first ADC 202.

[0061] The frequency response of the whitening filter 204, in this instance a shelving filter, is shown in **Figure 7**, where:

$$g_{LOW} = 1$$

$$g_{HIGH} = \frac{R2}{R1} = \frac{f_{LOW}}{f_{HIGH}}$$

$$f_{LOW} = \frac{1}{2\pi C1(R1 + R2)}$$

$$f_{HIGH} = \frac{1}{2\pi C1R1}$$

[0062] Thus, by adjusting the values of the first resistor R1, the second resistor R2 and the capacitor C1, the frequency response of the whitening filter 204 can be adapted. As such, one or more of the first and second resistors R1, R2 and the capacitor C1 may be variable, the values controlled by the control module 208.

[0063] In some embodiments, the frequency f_{LOW} may be fixed. The maximum gain g_{HIGH} that can be applied without clipping of the input audio signal AIN may then be determined by the control module. In doing so, the value f_{HIGH} can be calculated:

$$f_{HIGH} = \frac{f_{LOW}}{g_{HIGH}}$$

[0064] In some embodiments, the value R1 may be fixed for input noise requirements. C1 and R2 may then be adjusted by the control module 208. From the above equations for f_{HIGH} , C1 and R1 are given by:

$$C1 = \frac{1}{2\pi * f_{HIGH} * R1}$$

$$R2 = \frac{1 - 2\pi C1 * f_{LOW} * R1}{2\pi C1 * f_{LOW}}$$

[0065] As mentioned above, the control module 208 may determine a transfer function for the de-whitening filter 206. In some embodiments, this transfer function W^{-1} may be approximated by discretising and subsequently inverting the analogue transfer function W of the whitening filter 204. The analogue filter or transfer function W may be discretised using a bilinear transform to transform the s-plane to the z-plane as set out by the following equation:

$$s \rightarrow 2f_s \frac{1 - z^{-1}}{1 + z^{-1}}$$

Where f_s is the sampling frequency at the point at which the de-whitening filter 206 is applied.

[0066] It will be appreciated that due to the discretisation of in the digitally implemented de-whitening filter 206, there may be a mismatch between the whitening filter 204 and the de-whitening filter 208. Preferably, to minimise the impact of this over the audio frequency band and maximise the SNR for ultrasonic components of the audio signal, the values of R1, R2 and C1 may be set such that f_{LOW} falls outside of the audio frequency band. For example, f_{LOW} may be set at 6 kHz or above, or 7 kHz or above, or 8 kHz. In doing so, only the power spectrum above f_{LOW} will be whitened by the whitening filter 204.

[0067] **Figures 8 and 9** graphically illustrate the effect of the whitening filter 204 in whitening the audio input signal AIN with the shelving filter depicted in Figure 7.

[0068] **Figure 8** graphically illustrates the audio input signal AIN (line 802) and the digital output signal DOUT (line 804) with the whitening filter 204 and de-whitening filter 206 bypassed such that no whitening is performed. In this example, the first ADC 202 is a 14-bit sigma-delta ADC and at least 14 bits are required for the digital output signal DOUT to substantially match the audio input signal AIN.

[0069] **Figure 9** graphically illustrates the audio input signal AIN (line 902) and the digital output signal DOUT with the whitening filter 204 and de-whitening filter 206 bypassed (line 904) and with the whitening filter 204 and de-whitening filter 206 implemented (line 906) using the shelving filter shown in Figure 7. In this example, the first ADC 202 is a 9-bit sigma delta ADC. It can be seen that with a 9-bit solution, the non-whitened digital output signal depicted by line 904 is substantially mismatched relative to the input signal denoted by line 902. In contrast, at the same 9-bit resolution, the digital output signal which is the product of whitening and de-whitening (line 906) substantially matches the audio input signal AIN (line 902).

[0070] The skilled person will recognise that some aspects of the above-described apparatus and methods may be embodied as processor control code, for example on a non-volatile carrier medium such as a disk, CD- or DVD-ROM, programmed memory such as read only memory (Firmware), or on a data carrier such as an optical or electrical signal carrier. For many applications embodiments of the invention will be implemented on a DSP (Digital Signal Processor), ASIC (Application Specific Integrated Circuit) or FPGA (Field Programmable Gate Array). Thus the code may comprise conventional program code or microcode or, for example code for setting up or controlling an ASIC or FPGA. The code may also comprise code for dynamically configuring re-configurable apparatus such as re-programmable logic gate arrays. Similarly the code may comprise code for a hardware description language such as Verilog™ or VHDL (Very high speed integrated circuit Hardware Description Language). As the skilled person will appreciate, the code may be distributed between a plurality of coupled components in communication with one another. Where appropriate, the embodiments may also be implemented using code running on a field-

(re)programmable analogue array or similar device in order to configure analogue hardware.

[0071] Note that as used herein the term module shall be used to refer to a functional unit or block which may be implemented at least partly by dedicated hardware components such as custom defined circuitry and/or at least partly be implemented by one or more software processors or appropriate code running on a suitable general purpose processor or the like. A module may itself comprise other modules or functional units. A module may be provided by multiple components or sub-modules which need not be co-located and could be provided on different integrated circuits and/or running on different processors.

[0072] Embodiments may be implemented in a host device, especially a portable and/or battery powered host device such as a mobile computing device for example a laptop or tablet computer, a games console, a remote control device, a home automation controller or a domestic appliance including a domestic temperature or lighting control system, a toy, a machine such as a robot, an audio player, a video player, or a mobile telephone for example a smartphone.

[0073] It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. The word “comprising” does not exclude the presence of elements or steps other than those listed in a claim, “a” or “an” does not exclude a plurality, and a single feature or other unit may fulfil the functions of several units recited in the claims. Any reference numerals or labels in the claims shall not be construed so as to limit their scope.

[0074] As used herein, when two or more elements are referred to as “coupled” to one another, such term indicates that such two or more elements are in electronic communication or mechanical communication, as applicable, whether connected indirectly or directly, with or without intervening elements.

[0075] This disclosure encompasses all changes, substitutions, variations, alterations, and modifications to the example embodiments herein that a person having ordinary

skill in the art would comprehend. Similarly, where appropriate, the appended claims encompass all changes, substitutions, variations, alterations, and modifications to the example embodiments herein that a person having ordinary skill in the art would comprehend. Moreover, reference in the appended claims to an apparatus or system or a component of an apparatus or system being adapted to, arranged to, capable of, configured to, enabled to, operable to, or operative to perform a particular function encompasses that apparatus, system, or component, whether or not it or that particular function is activated, turned on, or unlocked, as long as that apparatus, system, or component is so adapted, arranged, capable, configured, enabled, operable, or operative. Accordingly, modifications, additions, or omissions may be made to the systems, apparatuses, and methods described herein without departing from the scope of the disclosure. For example, the components of the systems and apparatuses may be integrated or separated. Moreover, the operations of the systems and apparatuses disclosed herein may be performed by more, fewer, or other components and the methods described may include more, fewer, or other steps. Additionally, steps may be performed in any suitable order. As used in this document, “each” refers to each member of a set or each member of a subset of a set.

[0076] Although exemplary embodiments are illustrated in the figures and described

[0077] below, the principles of the present disclosure may be implemented using any number of techniques, whether currently known or not. The present disclosure should in no way be limited to the exemplary implementations and techniques illustrated in the drawings and described above.

[0078] Unless otherwise specifically noted, articles depicted in the drawings are not necessarily drawn to scale.

[0079] All examples and conditional language recited herein are intended for pedagogical objects to aid the reader in understanding the disclosure and the concepts contributed by the inventor to furthering the art, and are construed as being without limitation to such specifically recited examples and conditions. Although embodiments of the present disclosure have been described in detail, it should be understood that

various changes, substitutions, and alterations could be made hereto without departing from the spirit and scope of the disclosure.

[0080] Although specific advantages have been enumerated above, various embodiments may include some, none, or all of the enumerated advantages. Additionally, other technical advantages may become readily apparent to one of ordinary skill in the art after review of the foregoing figures and description.

CLAIMS:

1. An analogue-to-digital converter (ADC), comprising:

an adaptive whitening filter configured to filter an analogue input signal and output a whitened analogue input signal;

a first converter configured to receive said whitened analogue input signal and output a whitened digital signal;

a controller configured to adapt the whitening filter based on the received analogue input signal.

2. The ADC of claim 1, further comprising:

an adaptive de-whitening filter configured to filter the whitened digital output signal and output a de-whitened digital output signal, the de-whitening filter being substantially inverse to the whitening filter,

wherein the controller is configured to adapt the whitening filter based on the received analogue input signal.

3. The ADC of claims 1 or 2, wherein the whitening filter is one of:

- a) a shelving filter;
- b) a bandpass filter;
- c) a high pass filter; and
- d) a differentiator.

4. The ADC of any one of claims 1 to 3, wherein the controller is configured to adapt the whitening filter based on the whitened digital signal or the de-whitened digital output signal.

5. The ADC of any one of the preceding claims, wherein the controller is further configured to adapt the first converter based on the received analogue input signal.

6. The ADC of claim 5, wherein the controller is configured to adapt the first converter based on the whitened digital signal or the de-whitened digital output signal.

7. The ADC of claims 5 or 6, wherein the first converter is a sigma-delta ADC and wherein adapting of the first converter comprises one or more of:

- a) changing an order of the ADC;
- b) changing an over sample ratio of the ADC;
- c) changing a bias current of one or more circuits in the ADC;
- d) changing a number of bits in a quantizer of the ADC
- e) switching between a high-performance integrator and a low-performance integrator.

8. The ADC of any one of the preceding claims, wherein adapting the whitening filter comprises selectively bypassing the whitening filter.

9. The ADC of claim 8, further comprising a second converter configured to receive said analogue input signal and output a secondary digital signal to the controller, wherein the controller is configured to selectively bypass the whitening filter based on the secondary digital signal.

10. The ADC of claims 8 or 9, wherein the controller is configured to selectively bypass the whitening filter in response to detecting that the input audio signal exceeds a clipping threshold.

11. An integrated circuit comprising an ADC as claimed in any one of the preceding claims.

12. An electronic device comprising an ADC as claimed in any one of claims 1 to 10 or an integrated circuit as claimed in claim 11.

13. An electronic device as claims in claim 12, wherein said device is at least one of: a portable device; a battery powered device; a communications device; a mobile or cellular telephone; a personal media device; a computing device; a laptop, notebook or tablet computer; a gaming device; a wearable device.

14. A method of analogue-to-digital conversion, comprising:

whitening an analogue input signal with a whitening filter to generate a whitened analogue input signal;

converting the whitened analogue input signal with a first converter to generate a whitened digital signal; and

adapting the whitening filter based on the received analogue input signal.

15. The method of claim 14, further comprising:

de-whitening the whitened digital signal with a de-whitening filter to generate a de-whitened digital signal, the de-whitening filter being substantially inverse to the whitening filter,

adapting the de-whitening filter based on the received analogue input signal.

16. The method of claims 14 or 15, wherein the whitening filter is one of:

- a) a shelving filter;
- b) a bandpass filter;
- c) a high pass filter; and
- d) a differentiator.

17. The method of any one of claims 14 to 16, wherein the de-whitened filter is adapted based on the whitened digital signal or the de-whitened digital output signal.

18. The method of any one of claims 14 to 17, further comprising adapting the first converter based on the received analogue input signal.

19. The method of claim 18, wherein the first converter is adapted based on the whitened digital signal or the de-whitened digital output signal.

20. The method of claims 18 or 19, wherein the first converter is a sigma-delta ADC and wherein adapting of the first converter comprises one or more of:

- a) changing an order of the ADC;
- b) changing an over sample ratio of the ADC;
- c) changing a bias current of one or more circuits in the ADC;
- d) changing a number of bits in a quantizer of the ADC.

21. The method of any one of claims 14 to 20, wherein adapting the whitening filter comprises selectively bypassing the whitening filter.

22. The method of claim 21, further comprising converting with a second converter the analogue input signal to generate a secondary digital signal, wherein the whitening filter is selectively bypassed based on the secondary digital signal.

23. The method of claims 21 or 22, wherein the whitening filter is selectively bypassed in response to detecting that the input audio signal exceeds a clipping threshold.

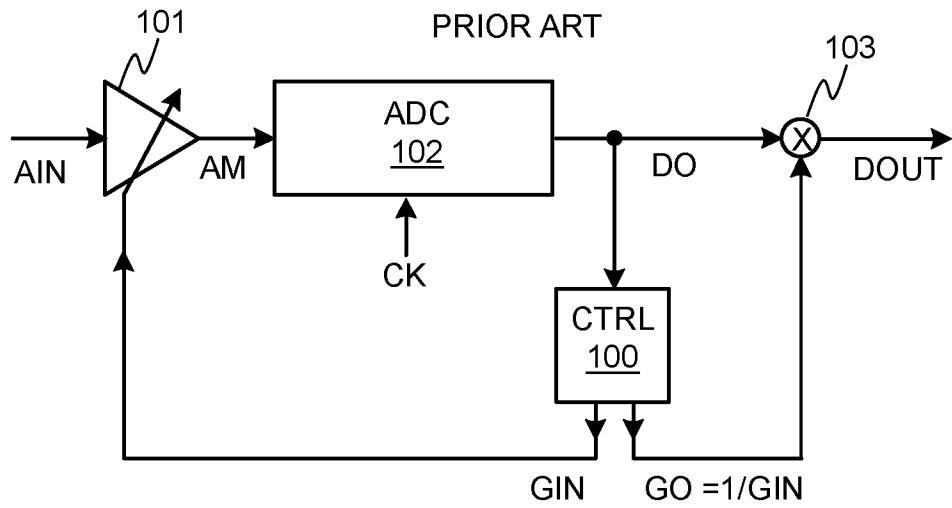


Fig. 1

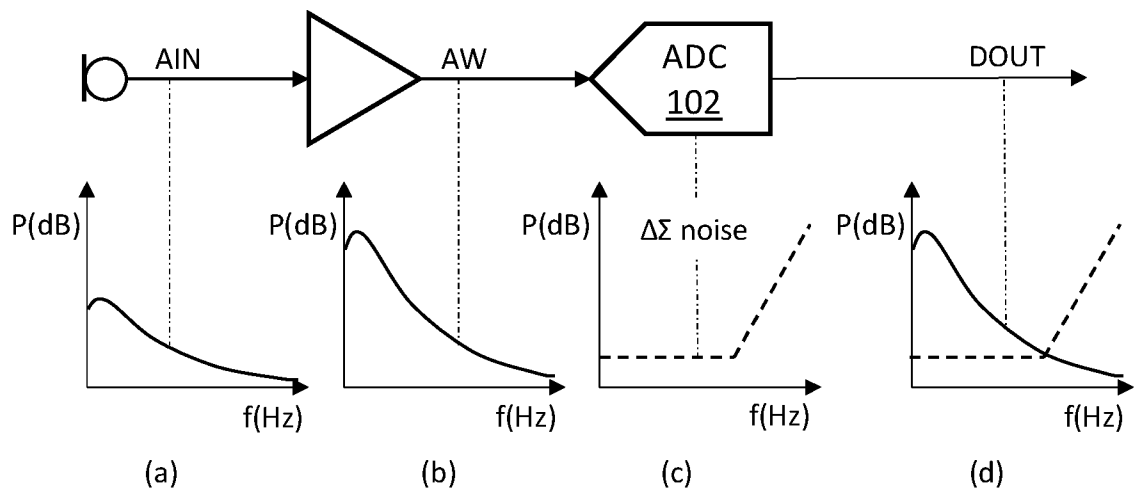


Fig. 2

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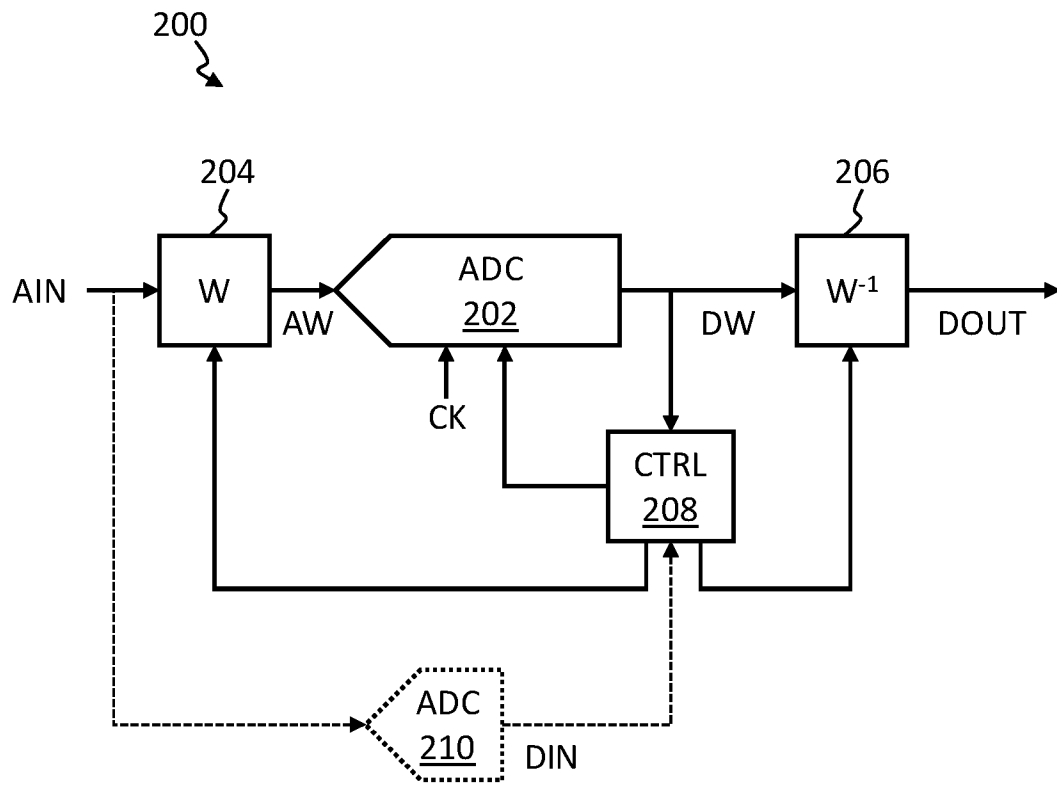


Fig. 3

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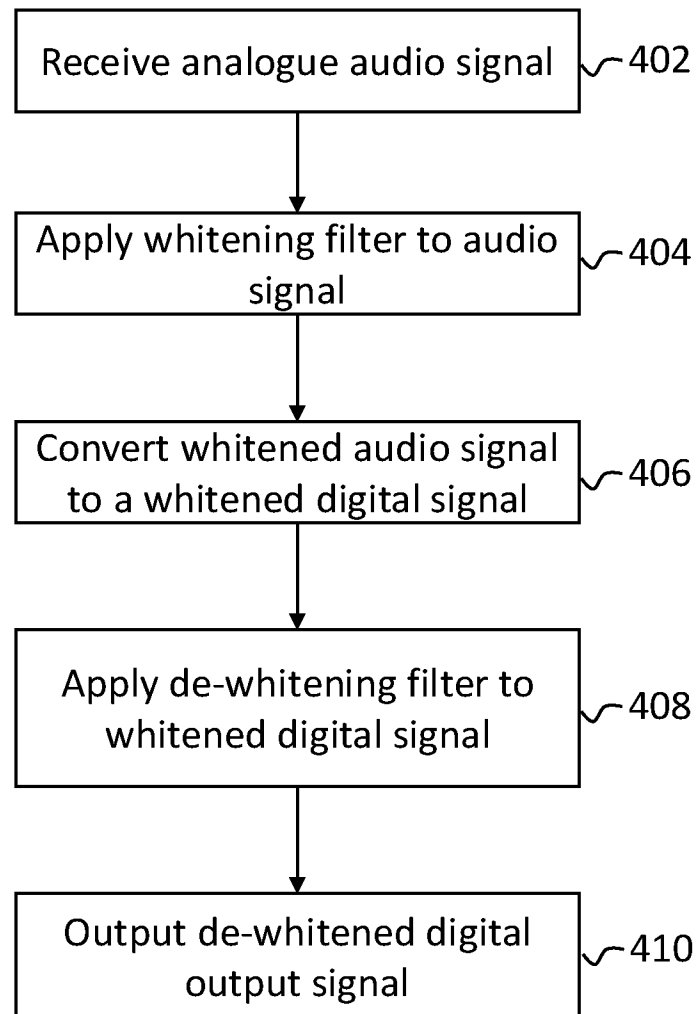


Fig. 4

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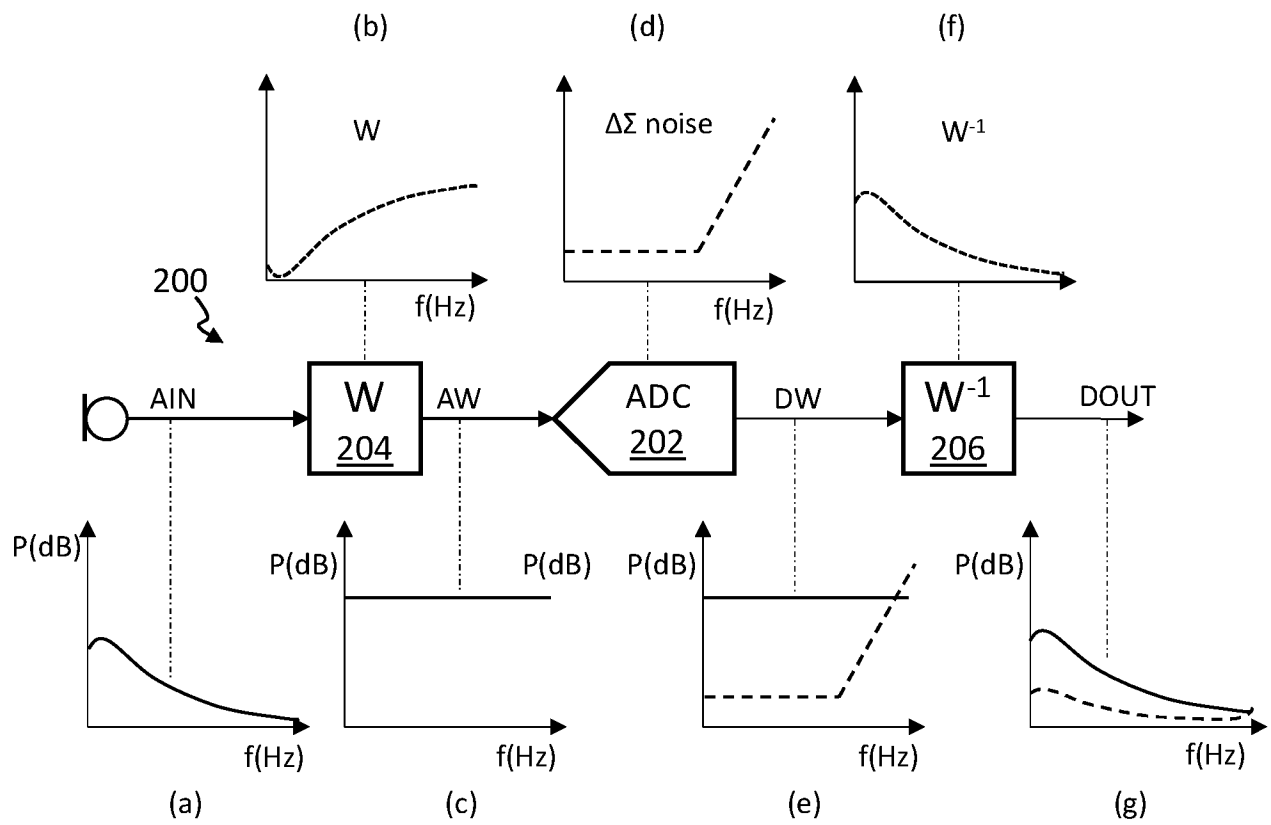


Fig. 5

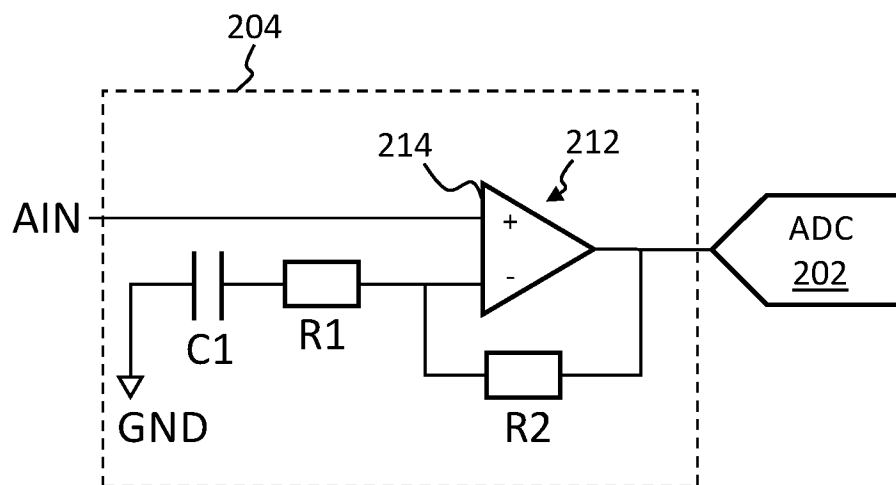


Fig. 6

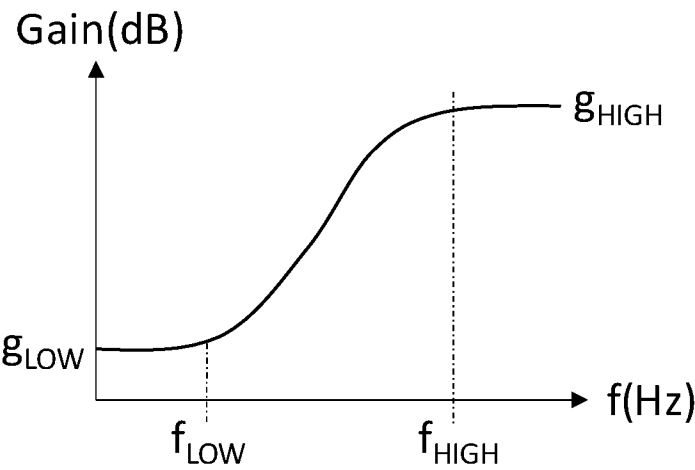


Fig. 7

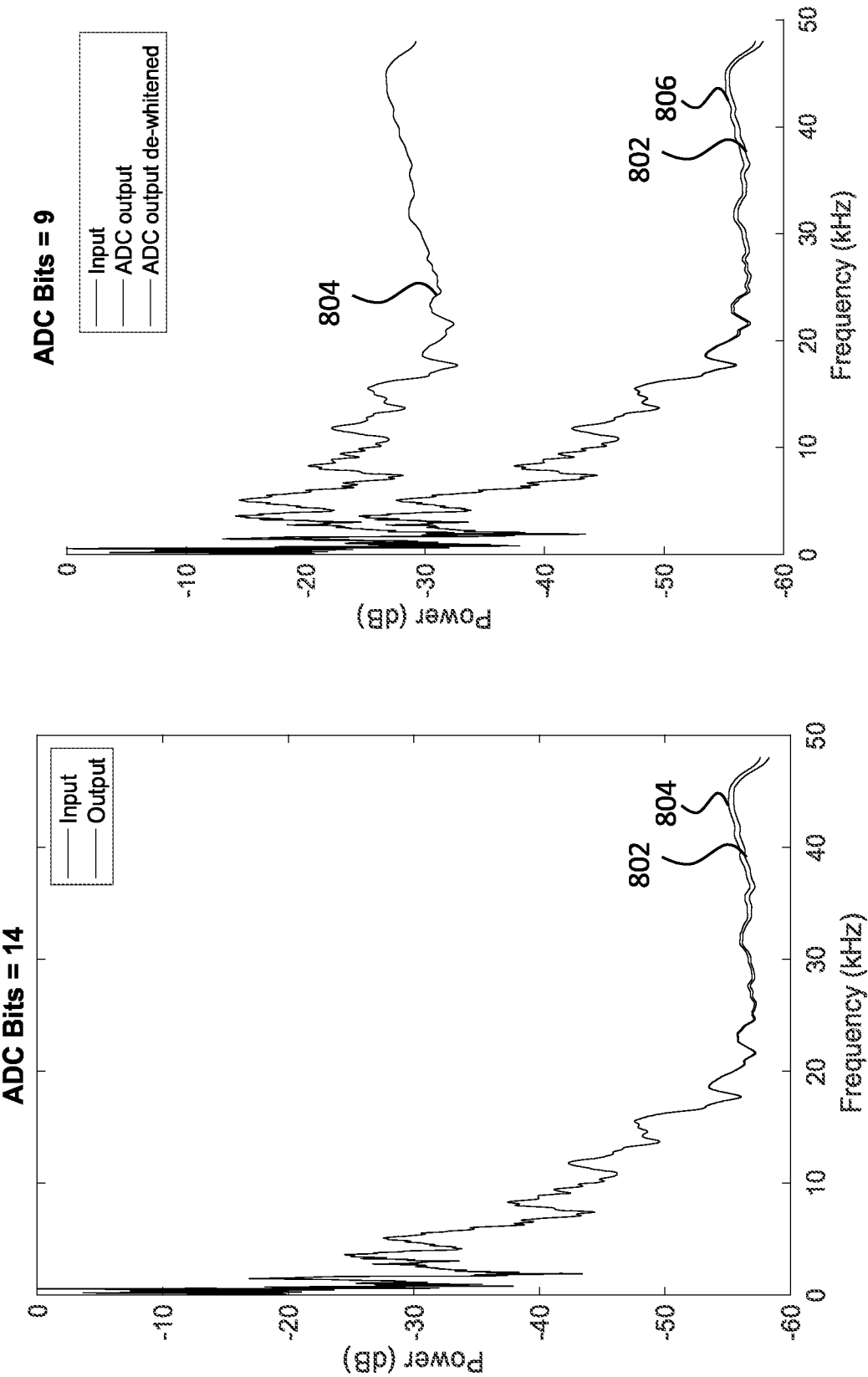


Fig. 8

Fig. 9

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2021/052132

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03M1/08 H03M1/18
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	SMITH WILLIAM A ET AL: "Exploiting Electrocardiographic Spectral Characteristics for Optimized Signal Chain Design: A 1.08 Analog Front End With Reduced ADC Resolution Requirements", IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, IEEE, US, vol. 10, no. 6, 1 December 2016 (2016-12-01), pages 1171-1180, XP011638385, ISSN: 1932-4545, DOI: 10.1109/TBCAS.2016.2518923 [retrieved on 2017-01-02] figures 6-11 page 1174, right-hand column, line 1 - page 1176, right-hand column, line 22 ----- -/--	1-23



Further documents are listed in the continuation of Box C.



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* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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Date of the actual completion of the international search

1 November 2021

Date of mailing of the international search report

10/11/2021

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
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Authorized officer

Jespers, Michaël

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2021/052132

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	VENKATRAMAN S ET AL: "Exploiting the 1/f structure of neural signals for the design of integrated neural amplifiers", PROCEEDINGS OF THE 31ST ANNUAL INTERNATIONAL CONFERENCE OF THE IEEE ENGINEERING IN MEDICINE AND BIOLOGY SOCIETY: ENGINEERING THE FUTURE OF BIOMEDICINE, EMBC 2009, IEEE, 3 September 2009 (2009-09-03), pages 2050-2053, XP031882299, DOI: 10.1109/IEMBS.2009.5334436 ISBN: 978-1-4244-3296-7 figures 1-6 page 2050, left-hand column, line 1 - page 2053, right-hand column, line 15 -----	1-23