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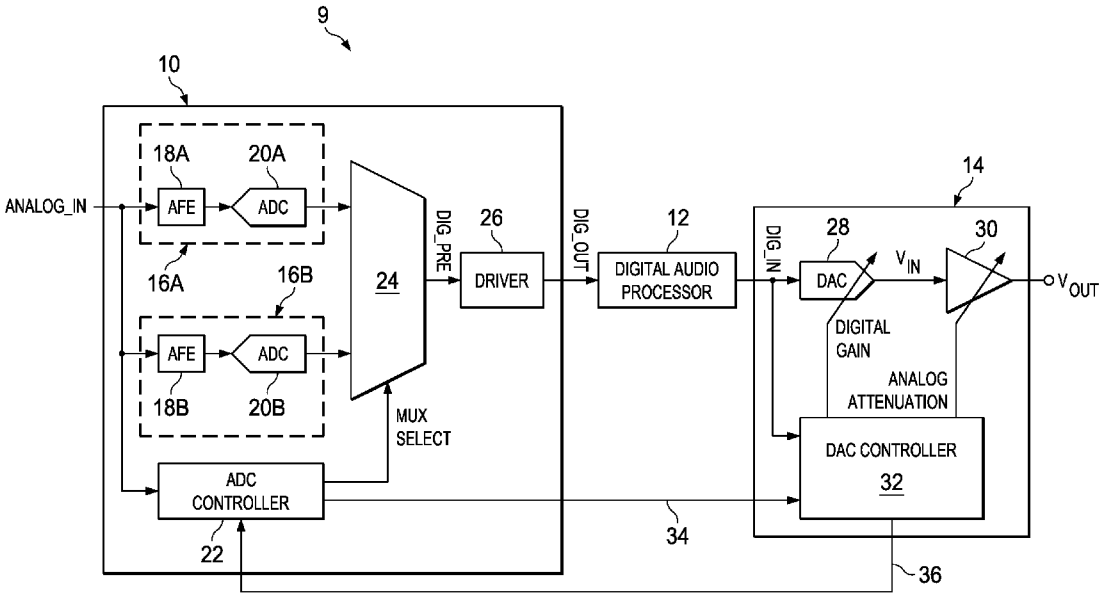

FIG. 2

(57) **Abstract:** In accordance with embodiments of the present disclosure, a method for operating a playback path comprising a first dynamic range enhancement subsystem and a second dynamic range enhancement subsystem, wherein an audio signal generated by the first dynamic range enhancement subsystem is communicated to the second dynamic range enhancement subsystem, is provided. The method may include determining a first operating parameter of one of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem that affects behavior of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem, communicating a control signal between the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem indicative of the first operating parameter, and setting a second operating parameter of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem in

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WO 2018/004569 A1

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response to receipt of the control signal.

OPTIMIZATION OF PERFORMANCE AND POWER IN AUDIO SYSTEM

FIELD OF DISCLOSURE

The present disclosure relates in general to circuits for audio devices, including without limitation personal audio devices such as wireless telephones and media players, and more specifically, to systems and methods for optimizing performance and power in an audio system comprising a multi-path analog-to-digital converter and a dynamic range enhancement based digital-to-analog converter.

BACKGROUND

Personal audio devices, including wireless telephones, such as mobile/cellular telephones, cordless telephones, mp3 players, and other consumer audio devices, are in widespread use. Such personal audio devices may include circuitry for driving a pair of headphones or one or more speakers. Such circuitry often includes a power amplifier for driving an audio output signal to headphones or speakers.

One particular characteristic of a personal audio device which may affect its marketability and desirability is the dynamic range of its audio output signal. Stated simply, the dynamic range is the ratio between the largest and smallest values of the audio output signal. One way to increase dynamic range is through the use of a multipath analog-to-digital subsystem comprising a plurality of parallel analog-to-digital converters (ADCs). Multipath circuits including multiple parallel ADCs may reduce noise as one path may be optimized for processing small amplitude signals (e.g., for processing low noise signals) while another circuit path may be optimized for large amplitude signals (e.g., allowing for higher dynamic range). Examples of such multipath circuits are disclosed in U.S. Patent No. 9,071,267 (the "Schneider Reference"), which is incorporated herein by reference.

Another way to increase dynamic range is through the use of signal magnitude-dependent digital gain and a corresponding analog attenuation applied to a digital-to-analog conversion subsystem comprising a digital-to-analog conversion subsystem having a digital gain and an output amplifier having an analog gain (or attenuation). Such a digital-to-analog conversion subsystem may enhance dynamic range as compared to

approaches in which the digital gain and analog attenuation are static, as it may reduce the noise injected into audio output signal V_{OUT}, which noise may be a generally monotonically increasing function of the gain/attenuation of the output amplifier. Examples of such digital-to-analog conversion subsystems are disclosed in U.S. Patent Appl. Ser. No. 14/083,972 (the "Satoskar Reference"), which is incorporated herein by reference.

SUMMARY

In accordance with the teachings of the present disclosure, one or more disadvantages and problems associated with existing approaches to optimizing power and performance of an audio signal path may be reduced or eliminated.

In accordance with embodiments of the present disclosure, a method for operating a playback path comprising a first dynamic range enhancement subsystem and a second dynamic range enhancement subsystem, wherein an audio signal generated by the first dynamic range enhancement subsystem is communicated to the second dynamic range enhancement subsystem, is provided. The method may include determining a first operating parameter of one of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem that affects behavior of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem, communicating a control signal between the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem indicative of the first operating parameter, and setting a second operating parameter of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem in response to receipt of the control signal.

In accordance with embodiments of the present disclosure, a system may have a playback path comprising a first dynamic range enhancement subsystem and a second dynamic range enhancement subsystem communicatively coupled to the first dynamic range enhancement subsystem such that an audio signal generated by the first dynamic range enhancement subsystem is communicated to the second dynamic range enhancement subsystem. The first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem may be configured to, either alone or in concert with one another, determine a first operating parameter of one of the first

dynamic range enhancement subsystem and the second dynamic range enhancement subsystem that affects behavior of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem, communicate a control signal between the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem indicative of the first operating parameter, and set a second operating parameter of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem in response to receipt of the control signal.

In accordance with these and other embodiments of the present disclosure, an integrated circuit may include circuitry configured to determine a first operating parameter of one of a first dynamic range enhancement subsystem and a second dynamic range enhancement subsystem communicatively coupled to the first dynamic range enhancement subsystem such that an audio signal generated by the first dynamic range enhancement subsystem is communicated to the second dynamic range enhancement subsystem, wherein the firs operating parameter affects behavior of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem, and communicate a control signal between the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem indicative of the first operating parameter such that a second operating parameter of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem is set in response to receipt of the control signal.

Technical advantages of the present disclosure may be readily apparent to one skilled in the art from the figures, description and claims included herein. The objects and advantages of the embodiments will be realized and achieved at least by the elements, features, and combinations particularly pointed out in the claims.

It is to be understood that both the foregoing general description and the following detailed description are examples and explanatory and are not restrictive of the claims set forth in this disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present embodiments and advantages thereof may be acquired by referring to the following description taken in conjunction with the accompanying drawings, in which like reference numbers indicate like features, and wherein:

FIGURE 1 is an illustration of an example personal audio device, in accordance with embodiments of the present disclosure;

FIGURE 2 is a block diagram of selected components of an example audio integrated system of a personal audio device, in accordance with embodiments of the present disclosure;

FIGURE 3 illustrates a flow chart of an example method for optimization of performance and power in an audio system, in accordance with embodiments of the present disclosure; and

FIGURE 4 illustrates a flow chart of another example method for optimization of performance and power in an audio system, in accordance with embodiments of the present disclosure.

DETAILED DESCRIPTION

FIGURE 1 is an illustration of an example personal audio device 1, in accordance with embodiments of the present disclosure. FIGURE 1 depicts personal audio device 1 coupled to a headset 3 in the form of a pair of earbud speakers 8A and 8B. Headset 3 depicted in FIGURE 1 is merely an example, and it is understood that personal audio device 1 may be used in connection with a variety of audio transducers, including without limitation, headphones, earbuds, in-ear earphones, and external speakers. A plug 4 may provide for connection of headset 3 to an electrical terminal of personal audio device 1. Personal audio device 1 may provide a display to a user and receive user input using a touch screen 2, or alternatively, a standard LCD may be combined with various buttons, sliders, and/or dials disposed on the face and/or sides of personal audio device 1. An audio input 5 may provide for receipt of an analog audio signal. For example, in some embodiments, audio input 5 may comprise a microphone. As another example, audio input 5 may comprise a "line in" input jack for receiving a corresponding plug of an analog audio source. As also shown in FIGURE 1, personal audio device 1 may include

an audio system 9 for generating an analog audio signal for transmission to headset 3 and/or another audio transducer.

FIGURE 2 is a block diagram of selected components of an example audio system 9 of a personal audio device, in accordance with embodiments of the present disclosure. As shown in FIGURE 2, audio system 9 may include an analog-to-digital conversion (ADC) subsystem 10, a digital audio processor 12, and a digital-to-analog conversion (DAC) subsystem 14. ADC subsystem 10 may be configured to, as described in greater detail below, receive an analog input signal ANALOG_IN (e.g., via audio input 5) and convert analog input signal ANALOG_IN to an equivalent digital signal DIG_OUT. A digital audio processor 12 may perform audio processing on digital signal DIG_OUT (e.g., volume control based on a volume setting, adaptive noise cancellation, frequency equalization, etc.) to generate a digital signal DIG_IN to be communicated to DAC subsystem 14. DAC subsystem 14 may be configured to, as described in greater detail below, receive digital input signal DIG_IN and convert digital input signal DIG_IN to an equivalent analog output signal V_{OUT} (e.g., which may be driven to a transducer, such as one of earbud speakers 8A and 8B).

As shown in FIGURE 2, ADC subsystem 10 may include two or more processing paths 16A and 16B (which may be referred to herein individually as a processing path 16 and collectively as processing paths 16), each processing path 16 including a respective analog front end (AFE) 18 (e.g., AFE 18A, AFE 18B) and a respective ADC 20 (e.g., ADC 20A, ADC 20B). An AFE 18 may receive analog input signal ANALOG_IN via one or more input lines which may allow for receipt of a single-ended signal, differential signal, or any other suitable analog signal format and may comprise any suitable system, device, or apparatus configured to condition analog input signal ANALOG_IN for processing by ADC 20. Example embodiments of AFEs 18 are described in the Schneider reference. The output of each AFE 18 may be communicated to a respective ADC 20.

An ADC 20 may comprise any suitable system, device, or apparatus configured to convert an analog signal received at its input, to a digital signal representative of such analog signal. An ADC 20 may itself include one or more components (e.g., delta-sigma modulator, decimator, etc.) for carrying out the functionality of ADC 20. Example embodiments of ADCs 20 are described in the Schneider reference.

A multiplexer 24 may receive a respective digital signal from each of processing paths 16 and may select one of the digital signals as digital signal DIG_PRE based on a control signal generated by and communicated from ADC controller 22, as described in greater detail below.

Driver 26 may receive the digital signal DIG_PRE output by multiplexer 24 and may comprise any suitable system, device, or apparatus configured to condition such digital signal (e.g., encoding into Audio Engineering Society/European Broadcasting Union (AES/EBU), Sony/Philips Digital Interface Format (S/PDIF)), in the process generating digital output signal DIG_OUT for transmission over a bus to digital audio processor 12. In FIGURE 2, the bus receiving digital output signal DIG_OUT is shown as single-ended. In some embodiments, driver 26 may generate a differential digital output signal DIG_OUT.

ADC controller 22 may comprise any suitable system, device, or apparatus for selecting one of the digital signals output by the various processing paths 16 as digital output signal DIG_OUT (e.g., selecting between gain modes of ADC subsystem 10). In some embodiments, ADC controller 22 may make such selection based on a magnitude of analog input signal ANALOG_IN or a signal derivative thereof. For example, ADC controller 22 may include an overload detector (not shown) that may determine whether or not analog input signal ANALOG_IN or a derivative thereof (e.g., an output of a modulator of a delta-sigma modulator of ADC 20A) is likely to cause clipping or other distortion of digital output signal DIG_OUT if a particular processing path (e.g., processing path 16A) is selected. If clipping or other distortion of digital output signal DIG_OUT is likely if the particular processing path (e.g., processing path 16A) is selected, ADC controller 22 may generate a control signal so that another processing path (e.g., processing path 16B) is selected. To further illustrate, in some embodiments, processing path 16A may be a path adapted for low amplitudes of analog input signal ANALOG_IN and may thus have a high signal gain, while processing path 16B may be a path adapted for higher amplitudes of analog input signal ANALOG_IN and may thus have a lower signal gain. Thus, if analog input signal ANALOG_IN or a derivative thereof is greater than a threshold value indicative of a condition whereby digital output signal DIG_OUT may experience clipping or other distortion if processing path 16A is selected, ADC controller 22 may detect such condition, and generate a control signal to

select the digital signal generated by processing path 16B as digital output signal DIG_OUT.

As another example, ADC controller 22 may include a level detector (not shown) that may detect an amplitude of analog input signal ANALOG_IN or a signal derivative thereof (e.g., a signal generated within ADC 20B). Responsive to the detected signal, ADC controller 22 may generate the control signal communicated to multiplexer 24. To illustrate, as analog input signal ANALOG_IN decreases from a relatively high amplitude to a lower amplitude, it may cross a threshold amplitude level whereby ADC controller 22 may change the selection of digital output signal DIG_OUT from the digital signal generated by processing path 16B (which may be adapted for higher amplitudes of analog input signal ANALOG_IN) to the digital signal generated by processing path 16A (which may be adapted for lower amplitudes of analog input signal ANALOG_IN). In some embodiments, a threshold amplitude level whereby ADC controller 22 may change the selection of digital output signal DIG_OUT from the digital signal generated by processing path 16B to the digital signal generated by processing path 16B may be lower than another threshold amplitude level whereby ADC controller 22 may change the selection of digital output signal DIG_OUT from the digital signal generated by processing path 16A to the digital signal generated by processing path 16B, in order to provide for hysteresis so that multiplexer 24 does not repeatedly switch between the paths in the event that the magnitude of audio input signal ANALOG_IN persists near the threshold.

As a further example, ADC controller 22 may be configured to determine that a transition between the first processing path and the second processing path needs to occur based on the analog input signal ANALOG_IN crossing a threshold or a prediction that the input signal will cross the threshold. An example of such predictive methodology is described in U.S. Patent Appl. Ser. No. 15/003,371 (the "Second Satoskar Reference"), which is incorporated herein by reference. As also described in the Second Satoskar Reference, such prediction may include a prediction of, a magnitude of the analog input signal ANALOG_IN crossing a predetermined threshold magnitude, the magnitude of the analog input signal ANALOG_IN lacking a persistent pattern of magnitude relative to the predetermined threshold magnitude, and/or the magnitude of the analog input signal

ANALOG_IN refraining from crossing a predetermined threshold magnitude for a period of time.

Also as shown in FIGURE 2, digital audio processor 12 may supply a digital audio input signal DIG_IN to a digital-to-analog converter (DAC) 28 of DAC subsystem 14, which may in turn supply an analog audio signal V_{IN} to a power amplifier stage 30 of DAC subsystem 14 which may amplify or attenuate the audio signal V_{IN} and provide an audio output signal V_{OUT}, which may operate a speaker (e.g., earbuds 8A and/or 8B), headphone transducer, and/or a line level signal output. As shown in FIGURE 2, DAC subsystem 14 may also include a DAC controller 32 configured to, based on digital audio input signal DIG_IN, control a programmable digital gain of DAC 28 and a programmable analog attenuation of amplifier 30.

As an example of the functionality of DAC controller 32, when a magnitude of digital audio input signal DIG_IN is at or near zero decibels (dB) relative to the full-scale magnitude of the digital audio input signal, DAC controller 32 may apply a unity gain (0 dB) to both of the digital gain and the analog attenuation. However, if the magnitude of the digital audio input signal DIG_IN is below a particular predetermined threshold magnitude relative to the full-scale magnitude of digital audio input signal DIG_IN (e.g., -20dB), DAC controller 32 may apply a non-unity digital gain (e.g., 20dB) to the digital gain and a corresponding non-unity attenuation (e.g., -20 dB) to the analog attenuation (although the analog attenuation may be further modified based on a volume control setting). Such approach may increase the dynamic range of DAC subsystem 14 compared to approaches in which the digital gain and analog attenuation are static, as it may reduce the noise injected into audio output signal V_{OUT}, which noise may be a generally monotonically increasing function of the gain/attenuation of amplifier 30. While such noise may be negligible for higher magnitude audio signals (e.g., at or near 0dB), the presence of such noise may become noticeable for lower magnitude audio signals (e.g., at or near -20dB or lower). By applying an analog attenuation at amplifier 30, the amount of noise injected into audio output signal V_{OUT} may be reduced, while the signal level of audio output signal V_{OUT} may be maintained in accordance with the digital audio input signal DIG_IN through application of a digital gain to DAC 28 equal in magnitude to the analog attenuation. A description of example components and functionality of DAC controller 32 is set forth in the Satoskar reference. For example, as set forth in the

Satoskar reference, in some embodiments, DAC controller 32 may be configured to switch between gain modes of DAC subsystem 14 in response to a zero crossing of digital input signal DIG_IN, so as to reduce or eliminate distortion caused by switching gain modes. As another example, as set forth in the Satoskar reference, in some embodiments, DAC controller 32 may be configured to ramp or step in discrete increments the digital gain and analog attenuation when transitioning between gain modes, in order to reduce or eliminate distortion caused by switching gain modes.

As a further example, DAC controller 32 may be configured to predict, based on one or more characteristics of a signal indicative of an output signal (e.g., audio output signal V_{OUT}), an occurrence of a condition for changing the digital gain and the analog attenuation, and responsive to predicting the occurrence of the condition, change, at an approximate zero crossing of the signal indicative of the output signal, the digital gain and the analog attenuation. An example of such predictive methodology is described in U.S. Patent Appl. Ser. No. 14/083,972 (the "Das Reference"), which is incorporated herein by reference. As also described in the Das Reference, such condition for changing the digital gain and the analog attenuation may include, without limitation, a magnitude of a signal indicative of an output signal crossing a predetermined threshold magnitude, the magnitude of the signal indicative of the output signal lacking a persistent pattern of magnitude relative to the predetermined threshold magnitude, and/or the magnitude of the signal indicative of the output signal refraining from crossing a predetermined threshold magnitude for a period of time.

As shown in FIGURE 2, ADC controller 22 may be configured to communicate a control signal 34 to control operation of DAC controller 32, and likewise, DAC controller 32 may be configured to communicate a control signal 36 to control operation of ADC controller 22. During operation of audio system 9, it may occur that respective noise floors of ADC subsystem 10 and DAC subsystem 14 may be substantially different. For example, in an example embodiment, ADC subsystem 10 may have a noise floor of -120 dB relative to full-scale magnitude when the higher-gain processing path 16A is selected, and a noise floor of -100 dB relative to full-scale magnitude when the lower-gain processing path 16B is selected, with a threshold of -30 dB relative to full-scale magnitude for switching between processing paths 16. In such embodiment, DAC subsystem 14 may have a noise floor of -120 dB relative to full-scale magnitude when the

higher-dynamic range gain mode (e.g., increased digital gain, increased analog attenuation) is selected, and may have a noise floor of -90 dB relative to full-scale magnitude when the lower-dynamic range gain mode (e.g., decreased digital gain, decreased analog attenuation), with a threshold of -20 dB relative to full-scale magnitude for switching between gain modes. Thus, in the presence of a -25 dB relative to full-scale magnitude audio signal (and no processing by digital audio processor 12 which alters such magnitude), in existing approaches to path control, ADC subsystem 10 having crossed its -30 dB threshold may switch to the higher-gain, lower noise floor processing path 16A. However, because DAC subsystem 14 is below its -20 dB threshold, the lower-dynamic range gain mode would be selected in existing approaches. Accordingly, using existing approaches in this example instance, the increase in dynamic range of ADC subsystem 10 may be of little use, as dynamic range of overall audio system 9 may be limited by the smaller dynamic range of DAC subsystem 14, and by switching to the higher-gain, lower noise floor processing path 16A, overall audio system 9 may consume more power with no corresponding increase in performance. Other situations may be present in existing approaches in which DAC subsystem 14 may be in a higher dynamic range mode with a low noise floor while ADC subsystem 10 selects the lower-gain, higher noise floor processing path 16B, such that audio system 9 may exhibit a power increase with no corresponding performance increase.

Accordingly, in accordance with systems and methods of the present disclosure, ADC controller 22 and/or DAC controller 32, working in concert, may via communication of control signals 34 and 36, determine whether an output of ADC subsystem 10 (e.g., digital signal DIG_OUT) is communicated to an input of DAC subsystem 14. In response to determining that the output of ADC subsystem 10 is communicated to the input of DAC subsystem 14, ADC controller 22 and/or DAC controller 32, working in concert, may via communication of control signals 34 and 36 determine the relative noise floors of ADC subsystem 10 and DAC subsystem 14. In response to determining that a DAC noise floor of DAC subsystem 14 is higher than an ADC noise floor of ADC subsystem 10, ADC controller 22 may optimize ADC subsystem 10 such that the ADC noise floor is more closely matched to the DAC noise floor (e.g., by selecting the lower-gain, higher noise floor processing path 16B regardless of the magnitude of analog input signal ANALOG_IN). In response to determining that

the DAC noise floor is lower than the ADC noise floor, DAC controller 32 may optimize DAC subsystem 14 such that the DAC noise floor is more closely matched to the ADC noise floor (e.g., by selecting the lower dynamic range, higher noise floor gain mode regardless of the magnitude of digital signal DIG_IN).

In these and other embodiments, in response to a gain mode of the ADC subsystem 10 from a high-gain mode to a low-gain mode (e.g., switching of selection from processing path 16A to processing path 16B), ADC controller 22 may communicate an indication (e.g., via control signal 34) to DAC controller 32 of the switching from the high-gain mode to the low-gain mode. In response, DAC controller 32 may cause DAC subsystem 14 to switch between gain modes (e.g., from the high-gain mode to the low-gain mode) responsive to the indication. Such feedforward indication of the switching between gain modes of ADC subsystem 10 from its high-gain mode to its low-gain mode may be advantageous, as signal clipping due to fast-rising signals in DAC subsystem 14 may be a concern. By using such feed-forward indication, DAC subsystem 14 may begin an early transition between gain modes even though a fast-rising signal has not yet propagated via the signal path to the input of DAC subsystem 14 (e.g., digital input signal DIG_IN). For example, in response to receiving such feed-forward indication, DAC controller 32 may begin looking for zero crossings of digital input signal DIG_IN and switch an occurrence of zero crossing of digital input signal DIG_IN in response to such feed-forward indication even if the fast-rising audio signal has yet to propagate to the input of DAC subsystem 14. As another example, in response to receiving such feed-forward indication, DAC controller 32 may begin ramping or stepping between gain levels of the digital gains of the two gain modes and ramping or stepping between attenuation levels of the two gain modes in response to such feed-forward indication even if the fast-rising audio signal has yet to propagate to the input of DAC subsystem 14.

FIGURE 3 illustrates a flow chart of an example method 40 for optimization of performance and power in an audio system, in accordance with embodiments of the present disclosure. According to one embodiment, method 40 may begin at step 42. As noted above, teachings of the present disclosure may be implemented in a variety of configurations of audio system 9. As such, the preferred initialization point for method 40 and the order of the steps comprising method 40 may depend on the implementation chosen.

At step 42, ADC controller 22 and/or DAC controller 32 may determine whether an output of ADC subsystem 10 is communicated to an input of DAC subsystem 14. If an output of ADC subsystem 10 is communicated to an input of DAC subsystem 14, method 40 may proceed to step 44. Otherwise, method 40 may remain at step 42 until such time as it is determines that an output of ADC subsystem 10 is communicated to an input of DAC subsystem 14.

At step 44, responsive to a determination that an output of ADC subsystem 10 is communicated to an input of DAC subsystem 14, ADC controller 22 and/or DAC controller 32, working in concert, may via communication of control signals 34 and 36 determine the relative noise floors of ADC subsystem 10 and DAC subsystem 14. At step 46, ADC controller 22 and/or DAC controller 32 may determine whether a DAC noise floor of DAC subsystem 14 is higher than an ADC noise floor of ADC subsystem 10. If the DAC noise floor is higher than the ADC noise floor, method 40 may proceed to step 48. Otherwise, method 40 may proceed to step 50.

At step 48, responsive to a determination that the DAC noise floor is higher than the ADC noise floor, ADC controller 22 may optimize ADC subsystem 10 such that the ADC noise floor is more closely matched to the DAC noise floor (e.g., by selecting the lower-gain, higher noise floor processing path 16B regardless of the magnitude of analog input signal ANALOG_IN). After completion of step 48, method 40 may proceed again to step 42.

At step 50, ADC controller 22 and/or DAC controller 32 may determine whether a DAC noise floor of DAC subsystem 14 is lower than an ADC noise floor of ADC subsystem 10. If the DAC noise floor is lower than the ADC noise floor, method 40 may proceed to step 52. Otherwise, method 40 may proceed again to step 42.

At step 52, responsive to a determination that the DAC noise floor is lower than the ADC noise floor, DAC controller 32 may optimize DAC subsystem 14 such that the DAC noise floor is more closely matched to the ADC noise floor (e.g., by selecting the lower dynamic range, higher noise floor gain mode regardless of the magnitude of digital signal DIG_IN). After completion of step 52, method 40 may proceed again to step 42.

Although FIGURE 3 discloses a particular number of steps to be taken with respect to method 40, method 40 may be executed with greater or lesser steps than those depicted in FIGURE 3. In addition, although FIGURE 3 discloses a certain order of steps

to be taken with respect to method 40, the steps comprising method 40 may be completed in any suitable order.

Method 40 may be implemented using audio system 9 or any other system operable to implement method 40. In certain embodiments, method 40 may be implemented partially or fully in software and/or firmware embodied in computer-readable media.

FIGURE 4 illustrates a flow chart of another example method 60 for optimization of performance and power in an audio system, in accordance with embodiments of the present disclosure. According to one embodiment, method 60 may begin at step 62. As noted above, teachings of the present disclosure may be implemented in a variety of configurations of audio system 9. As such, the preferred initialization point for method 60 and the order of the steps comprising method 60 may depend on the implementation chosen.

At step 62, ADC controller 22 and/or DAC controller 32 may determine whether an output of ADC subsystem 10 is communicated to an input of DAC subsystem 14. If an output of ADC subsystem 10 is communicated to an input of DAC subsystem 14, method 60 may proceed to step 64. Otherwise, method 60 may remain at step 62 until such time as it is determines that an output of ADC subsystem 10 is communicated to an input of DAC subsystem 14.

At step 64, responsive to a determination that an output of ADC subsystem 10 is communicated to an input of DAC subsystem 14, ADC controller 22 may determine if a threshold for switching from the high-gain mode to the low-gain mode of ADC subsystem 10 has occurred. If the threshold for switching from the high-gain mode to the low-gain mode of ADC subsystem 10 has occurred, method 60 may proceed to step 66. Otherwise, method 60 may proceed again to step 62.

At step 66, responsive to the threshold for switching from the high-gain mode to the low-gain mode of ADC subsystem 10, ADC controller 22 may forward an indication to DAC controller 32 of the switching from the high-gain mode to the low-gain mode of ADC subsystem 10. At step 68, DAC controller 32 may cause DAC subsystem 14 to switch between gain modes of DAC subsystem 14 responsive to the indication.

Although FIGURE 4 discloses a particular number of steps to be taken with respect to method 60, method 60 may be executed with greater or lesser steps than those

depicted in FIGURE 4. In addition, although FIGURE 4 discloses a certain order of steps to be taken with respect to method 60, the steps comprising method 60 may be completed in any suitable order.

Method 60 may be implemented using audio system 9 or any other system operable to implement method 60. In certain embodiments, method 60 may be implemented partially or fully in software and/or firmware embodied in computer-readable media.

This disclosure encompasses all changes, substitutions, variations, alterations, and modifications to the exemplary embodiments herein that a person having ordinary skill in the art would comprehend. Similarly, where appropriate, the appended claims encompass all changes, substitutions, variations, alterations, and modifications to the exemplary embodiments herein that a person having ordinary skill in the art would comprehend. Moreover, reference in the appended claims to an apparatus or system or a component of an apparatus or system being adapted to, arranged to, capable of, configured to, enabled to, operable to, or operative to perform a particular function encompasses that apparatus, system, or component, whether or not it or that particular function is activated, turned on, or unlocked, as long as that apparatus, system, or component is so adapted, arranged, capable, configured, enabled, operable, or operative.

All examples and conditional language recited herein are intended for pedagogical objects to aid the reader in understanding the invention and the concepts contributed by the inventor to furthering the art, and are construed as being without limitation to such specifically recited examples and conditions. Although embodiments of the present inventions have been described in detail, it should be understood that various changes, substitutions, and alterations could be made hereto without departing from the spirit and scope of the disclosure.

WHAT IS CLAIMED IS:

1. A method for operating a playback path comprising a first dynamic range enhancement subsystem and a second dynamic range enhancement subsystem, wherein an audio signal generated by the first dynamic range enhancement subsystem is communicated to the second dynamic range enhancement subsystem, the method comprising:

determining a first operating parameter of one of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem that affects behavior of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem;

communicating a control signal between the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem indicative of the first operating parameter; and

setting a second operating parameter of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem in response to receipt of the control signal.

2. The method of Claim 1, wherein:

the first dynamic range enhancement subsystem comprises an analog-to-digital converter (ADC) subsystem;

the second dynamic range enhancement subsystem comprises a digital-to-analog converter (DAC) subsystem;

the first operating parameter is an ADC noise floor of the ADC subsystem;

the second operating parameter is a DAC noise floor of the DAC subsystem; and

the method further comprises:

in response to determining that the DAC noise floor of the DAC subsystem is higher than the ADC noise floor of the ADC subsystem, optimizing the ADC subsystem such that the ADC noise floor is more closely matched to the DAC noise floor; and

in response to determining that the DAC noise floor is lower than the ADC noise floor, optimizing the DAC subsystem such that the DAC noise floor is more closely matched to the ADC noise floor.

3. The method of Claim 2, further comprising:

determining whether an output of the ADC subsystem is communicated to an input of the DAC subsystem; and

optimizing the DAC subsystem or optimizing the ADC subsystem in response to determining that the output of the ADC subsystem is communicated to the input of the DAC subsystem.

4. The method of Claim 2, further comprising, in response to a gain mode of the ADC subsystem switching from a high-gain mode to a low-gain mode:

forwarding an indication from the ADC subsystem to the DAC subsystem of the switching from the high-gain mode to the low-gain mode; and

switching the DAC subsystem between gain modes of the DAC subsystem responsive to the indication.

5. The method of Claim 1, wherein:

the first dynamic range enhancement subsystem comprises an analog-to-digital converter (ADC) subsystem;

the second dynamic range enhancement subsystem comprises a digital-to-analog converter (DAC) subsystem;

the first operating parameter is a gain mode of the ADC subsystem;

the second operating parameter is a gain mode of the DAC subsystem; and

the method further comprises, in response to the gain mode of the ADC subsystem switching from a high-gain mode to a low-gain mode:

forwarding an indication from the ADC subsystem to the DAC subsystem of the switching from the high-gain mode to the low-gain mode; and

switching the DAC subsystem between gain modes of the DAC subsystem responsive to the indication.

6. The method of Claim 5, further comprising:

determining whether an output of the ADC subsystem is communicated to an input of the DAC subsystem; and

forwarding the indication and switching the DAC subsystem between the gain modes of the DAC subsystem in response to determining that the output of the ADC subsystem is communicated to the input of the DAC subsystem.

7. A system having a playback path comprising:

a first dynamic range enhancement subsystem; and

a second dynamic range enhancement subsystem communicatively coupled to the first dynamic range enhancement subsystem such that an audio signal generated by the first dynamic range enhancement subsystem is communicated to the second dynamic range enhancement subsystem;

wherein the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem are configured to, in concert with one another:

determine a first operating parameter of one of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem that affects behavior of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem;

communicate a control signal between the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem indicative of the first operating parameter; and

set a second operating parameter of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem in response to receipt of the control signal.

8. The system of Claim 7, wherein:

the first dynamic range enhancement subsystem comprises an analog-to-digital converter (ADC) subsystem;

the second dynamic range enhancement subsystem comprises a digital-to-analog converter (DAC) subsystem;

the first operating parameter is an ADC noise floor of the ADC subsystem;

the second operating parameter is a DAC noise floor of the DAC subsystem; and

the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem are further configured to, in concert with one another:

in response to determining that the DAC noise floor of the DAC subsystem is higher than the ADC noise floor of the ADC subsystem, optimize the ADC subsystem such that the ADC noise floor is more closely matched to the DAC noise floor; and

in response to determining that the DAC noise floor is lower than the ADC noise floor, optimize the DAC subsystem such that the DAC noise floor is more closely matched to the ADC noise floor.

9. The system of Claim 8, wherein the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem are further configured to, in concert with one another:

determine whether an output of the ADC subsystem is communicated to an input of the DAC subsystem; and

optimize the DAC subsystem or optimize the ADC subsystem in response to determining that the output of the ADC subsystem is communicated to the input of the DAC subsystem.

10. The system of Claim 8, wherein the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem are further configured to, in concert with one another:

forward an indication from the ADC subsystem to the DAC subsystem of switching from high-gain mode to low-gain mode; and

switch the DAC subsystem between gain modes of the DAC subsystem responsive to the indication.

11. The system of Claim 7, wherein:

the first dynamic range enhancement subsystem comprises an analog-to-digital converter (ADC) subsystem;

the second dynamic range enhancement subsystem comprises a digital-to-analog converter (DAC) subsystem;

the first operating parameter is a gain mode of the ADC subsystem;

the second operating parameter is a gain mode of the DAC subsystem; and

the first dynamic range enhancement subsystem is further configured to, in response to the gain mode of the ADC subsystem switching from a high-gain mode to a low-gain mode, forward an indication from the ADC subsystem to the DAC subsystem of the switching from the high-gain mode to the low-gain mode; and

the second dynamic range enhancement subsystem is further configured to, in response to the indication, switch the DAC subsystem between gain modes of the DAC subsystem.

12. The system of Claim 11, wherein the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem are further configured to, in concert with one another:

determine whether an output of the ADC subsystem is communicated to an input of the DAC subsystem; and

forward the indication and switch the DAC subsystem between the gain modes of the DAC subsystem in response to determining that the output of the ADC subsystem is communicated to the input of the DAC subsystem.

13. An integrated circuit comprising circuitry configured to:

determine a first operating parameter of one of a first dynamic range enhancement subsystem and a second dynamic range enhancement subsystem communicatively coupled to the first dynamic range enhancement subsystem such that an audio signal generated by the first dynamic range enhancement subsystem is communicated to the

second dynamic range enhancement subsystem, wherein the firs operating parameter affects behavior of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem; and

communicate a control signal between the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem indicative of the first operating parameter such that a second operating parameter of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem is set in response to receipt of the control signal.

14. The integrated circuit of Claim 13, wherein:

the first dynamic range enhancement subsystem comprises an analog-to-digital converter (ADC) subsystem;

the second dynamic range enhancement subsystem comprises a digital-to-analog converter (DAC) subsystem;

the first operating parameter is an ADC noise floor of the ADC subsystem;

the second operating parameter is a DAC noise floor of the DAC subsystem; and

the circuitry is further configured to:

in response to determining that the DAC noise floor of the DAC subsystem is higher than the ADC noise floor of the ADC subsystem, optimize the ADC subsystem such that the ADC noise floor is more closely matched to the DAC noise floor; and

in response to determining that the DAC noise floor is lower than the ADC noise floor, optimize the DAC subsystem such that the DAC noise floor is more closely matched to the ADC noise floor.

15. The integrated circuit of Claim 14, wherein the circuitry is further configured to:

determine whether an output of the ADC subsystem is communicated to an input of the DAC subsystem; and

optimize the DAC subsystem or optimize the ADC subsystem in response to determining that the output of the ADC subsystem is communicated to the input of the DAC subsystem.

16. The integrated circuit of Claim 14, wherein the first dynamic range enhancement subsystem and the circuitry is further configured to:

forward an indication from the ADC subsystem to the DAC subsystem of switching from high-gain mode to low-gain mode; and

switch the DAC subsystem between gain modes of the DAC subsystem responsive to the indication.

17. The integrated circuit of Claim 13, wherein:

the first dynamic range enhancement subsystem comprises an analog-to-digital converter (ADC) subsystem;

the second dynamic range enhancement subsystem comprises a digital-to-analog converter (DAC) subsystem;

the first operating parameter is a gain mode of the ADC subsystem;

the second operating parameter is a gain mode of the DAC subsystem; and

the circuitry is further configured to in response to the gain mode of the ADC subsystem switching from a high-gain mode to a low-gain mode:

forward an indication from the ADC subsystem to the DAC subsystem of the switching from the high-gain mode to the low-gain mode; and

in response to the indication, switch the DAC subsystem between gain modes of the DAC subsystem.

18. The integrated circuit of Claim 17, wherein the circuitry is further configured to:

determine whether an output of the ADC subsystem is communicated to an input of the DAC subsystem; and

forward the indication and switch the DAC subsystem between the gain modes of the DAC subsystem in response to determining that the output of the ADC subsystem is communicated to the input of the DAC subsystem.

AMENDED CLAIMS
received by the International Bureau on 24 May 2017(24.05.2017)

1. A method for operating a playback path comprising a first dynamic range enhancement subsystem and a second dynamic range enhancement subsystem, wherein an audio signal generated by the first dynamic range enhancement subsystem is communicated to the second dynamic range enhancement subsystem, the method comprising:

determining a first operating parameter, other than a signal gain, of one of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem that affects behavior of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem;

communicating a control signal between the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem indicative of the first operating parameter; and

setting a second operating parameter, other than a signal gain, of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem in response to receipt of the control signal.

2. The method of Claim 1, wherein:

the first dynamic range enhancement subsystem comprises an analog-to-digital converter (ADC) subsystem;

the second dynamic range enhancement subsystem comprises a digital-to-analog converter (DAC) subsystem;

the first operating parameter is an ADC noise floor of the ADC subsystem;

the second operating parameter is a DAC noise floor of the DAC subsystem; and

the method further comprises:

in response to determining that the DAC noise floor of the DAC subsystem is higher than the ADC noise floor of the ADC subsystem, optimizing the ADC subsystem such that the ADC noise floor is more closely matched to the DAC noise floor; and

in response to determining that the DAC noise floor is lower than the ADC noise floor, optimizing the DAC subsystem such that the DAC noise floor is more closely matched to the ADC noise floor.

3. The method of Claim 2, further comprising:

determining whether an output of the ADC subsystem is communicated to an input of the DAC subsystem; and

optimizing the DAC subsystem or optimizing the ADC subsystem in response to determining that the output of the ADC subsystem is communicated to the input of the DAC subsystem.

4. The method of Claim 2, further comprising, in response to a gain mode of the ADC subsystem switching from a high-gain mode to a low-gain mode:

forwarding an indication from the ADC subsystem to the DAC subsystem of the switching from the high-gain mode to the low-gain mode; and

switching the DAC subsystem between gain modes of the DAC subsystem responsive to the indication.

5. The method of Claim 1, wherein:

the first dynamic range enhancement subsystem comprises an analog-to-digital converter (ADC) subsystem;

the second dynamic range enhancement subsystem comprises a digital-to-analog converter (DAC) subsystem;

the first operating parameter is a gain mode of the ADC subsystem;

the second operating parameter is a gain mode of the DAC subsystem; and

the method further comprises, in response to the gain mode of the ADC subsystem switching from a high-gain mode to a low-gain mode:

forwarding an indication from the ADC subsystem to the DAC subsystem of the switching from the high-gain mode to the low-gain mode; and

switching the DAC subsystem between gain modes of the DAC subsystem responsive to the indication.

6. The method of Claim 5, further comprising:

determining whether an output of the ADC subsystem is communicated to an input of the DAC subsystem; and

forwarding the indication and switching the DAC subsystem between the gain modes of the DAC subsystem in response to determining that the output of the ADC subsystem is communicated to the input of the DAC subsystem.

7. A system having a playback path comprising:

a first dynamic range enhancement subsystem; and

a second dynamic range enhancement subsystem communicatively coupled to the first dynamic range enhancement subsystem such that an audio signal generated by the first dynamic range enhancement subsystem is communicated to the second dynamic range enhancement subsystem;

wherein the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem are configured to, in concert with one another:

determine a first operating parameter, other than a signal gain, of one of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem that affects behavior of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem;

communicate a control signal between the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem indicative of the first operating parameter; and

set a second operating parameter, other than a signal gain, of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem in response to receipt of the control signal.

8. The system of Claim 7, wherein:

the first dynamic range enhancement subsystem comprises an analog-to-digital converter (ADC) subsystem;

the second dynamic range enhancement subsystem comprises a digital-to-analog converter (DAC) subsystem;

the first operating parameter is an ADC noise floor of the ADC subsystem;

the second operating parameter is a DAC noise floor of the DAC subsystem; and

the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem are further configured to, in concert with one another:

in response to determining that the DAC noise floor of the DAC subsystem is higher than the ADC noise floor of the ADC subsystem, optimize the ADC subsystem such that the ADC noise floor is more closely matched to the DAC noise floor; and

in response to determining that the DAC noise floor is lower than the ADC noise floor, optimize the DAC subsystem such that the DAC noise floor is more closely matched to the ADC noise floor.

9. The system of Claim 8, wherein the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem are further configured to, in concert with one another:

determine whether an output of the ADC subsystem is communicated to an input of the DAC subsystem; and

optimize the DAC subsystem or optimize the ADC subsystem in response to determining that the output of the ADC subsystem is communicated to the input of the DAC subsystem.

10. The system of Claim 8, wherein the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem are further configured to, in concert with one another:

forward an indication from the ADC subsystem to the DAC subsystem of switching from high-gain mode to low-gain mode; and

switch the DAC subsystem between gain modes of the DAC subsystem responsive to the indication.

11. The system of Claim 7, wherein:

the first dynamic range enhancement subsystem comprises an analog-to-digital converter (ADC) subsystem;

the second dynamic range enhancement subsystem comprises a digital-to-analog converter (DAC) subsystem;

the first operating parameter is a gain mode of the ADC subsystem;

the second operating parameter is a gain mode of the DAC subsystem; and

the first dynamic range enhancement subsystem is further configured to, in response to the gain mode of the ADC subsystem switching from a high-gain mode to a low-gain mode, forward an indication from the ADC subsystem to the DAC subsystem of the switching from the high-gain mode to the low-gain mode; and

the second dynamic range enhancement subsystem is further configured to, in response to the indication, switch the DAC subsystem between gain modes of the DAC subsystem.

12. The system of Claim 11, wherein the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem are further configured to, in concert with one another:

determine whether an output of the ADC subsystem is communicated to an input of the DAC subsystem; and

forward the indication and switch the DAC subsystem between the gain modes of the DAC subsystem in response to determining that the output of the ADC subsystem is communicated to the input of the DAC subsystem.

13. An integrated circuit comprising circuitry configured to:

determine a first operating parameter, other than a signal gain, of one of a first dynamic range enhancement subsystem and a second dynamic range enhancement subsystem communicatively coupled to the first dynamic range enhancement subsystem such that an audio signal generated by the first dynamic range enhancement subsystem is communicated to the second dynamic range enhancement subsystem, wherein the first

operating parameter affects behavior of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem; and

communicate a control signal between the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem indicative of the first operating parameter such that a second operating parameter, other than a signal gain, of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem is set in response to receipt of the control signal.

14. The integrated circuit of Claim 13, wherein:

the first dynamic range enhancement subsystem comprises an analog-to-digital converter (ADC) subsystem;

the second dynamic range enhancement subsystem comprises a digital-to-analog converter (DAC) subsystem;

the first operating parameter is an ADC noise floor of the ADC subsystem;

the second operating parameter is a DAC noise floor of the DAC subsystem; and

the circuitry is further configured to:

in response to determining that the DAC noise floor of the DAC subsystem is higher than the ADC noise floor of the ADC subsystem, optimize the ADC subsystem such that the ADC noise floor is more closely matched to the DAC noise floor; and

in response to determining that the DAC noise floor is lower than the ADC noise floor, optimize the DAC subsystem such that the DAC noise floor is more closely matched to the ADC noise floor.

15. The integrated circuit of Claim 14, wherein the circuitry is further configured to:

determine whether an output of the ADC subsystem is communicated to an input of the DAC subsystem; and

optimize the DAC subsystem or optimize the ADC subsystem in response to determining that the output of the ADC subsystem is communicated to the input of the DAC subsystem.

16. The integrated circuit of Claim 14, wherein the first dynamic range enhancement subsystem and the circuitry is further configured to:

forward an indication from the ADC subsystem to the DAC subsystem of switching from high-gain mode to low-gain mode; and

switch the DAC subsystem between gain modes of the DAC subsystem responsive to the indication.

17. The integrated circuit of Claim 13, wherein:

the first dynamic range enhancement subsystem comprises an analog-to-digital converter (ADC) subsystem;

the second dynamic range enhancement subsystem comprises a digital-to-analog converter (DAC) subsystem;

the first operating parameter is a gain mode of the ADC subsystem;

the second operating parameter is a gain mode of the DAC subsystem; and

the circuitry is further configured to in response to the gain mode of the ADC subsystem switching from a high-gain mode to a low-gain mode:

forward an indication from the ADC subsystem to the DAC subsystem of the switching from the high-gain mode to the low-gain mode; and

in response to the indication, switch the DAC subsystem between gain modes of the DAC subsystem.

18. The integrated circuit of Claim 17, wherein the circuitry is further configured to:

determine whether an output of the ADC subsystem is communicated to an input of the DAC subsystem; and

forward the indication and switch the DAC subsystem between the gain modes of the DAC subsystem in response to determining that the output of the ADC subsystem is communicated to the input of the DAC subsystem.

STATEMENT UNDER ARTICLE 19 (1)

No Waiver

All of Applicant's arguments herein are without prejudice or disclaimer. Thus, by not responding specifically to specific allegations or statements of the Authority in the International Search Report/Written Opinion, Applicant does not acquiesce to any such allegations or statements, and reserves the right to refute such allegations or statements in response to correspondence received from any patent office or similar authority of any country in which the Applicant may file a corresponding application. Also, Applicant does not acquiesce to any determination by the Authority of the status of any reference as "prior art" that may be cited against the claims of the present application in one or more particular countries in which the Applicant may file a corresponding application.

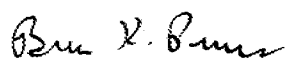
Claims 1-18

In the International Search Report/Written Opinion, at Re Item V, the Authority asserts that the subject matter of Claims 1, 7, and 13 is not new and novel over each of reference D1, U.S. Pat. No. 6,542,612 by Needham (hereinafter "D1"), reference D2, U.S. Pat. No. 4,493,091 by Gundry (hereinafter "D2"), and reference D3, U.S. Pat. Pub. No. 2008/0198048 by Klein et al. (hereinafter "D3"). Applicant respectfully traverses these findings, and submits that Claims 1, 7, and 13 are new and novel over D1, D2, and D3

(collectively, "the references"), at least because the references fail to teach "determining a first operating parameter, other than a signal gain, of one of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem that affects behavior of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem" and "setting a second operating parameter, other than a signal gain, of the other of the first dynamic range enhancement subsystem and the second dynamic range enhancement subsystem in response to receipt of the control signal," as recited in Claim 1 and as similarly recited in Claims 7 and 13.

For at least these reasons, Claims 1, 7, and 13 are new and novel. Given that Claims 2-6 depend from Claim 1, Claims 8-12 depend from Claim 7, and Claims 14-18 depend from Claim 13, Applicant submits that Claims 2-6, 8-12, and 14-18 are also new and novel.

Respectfully Submitted,



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Dated: May 24, 2017

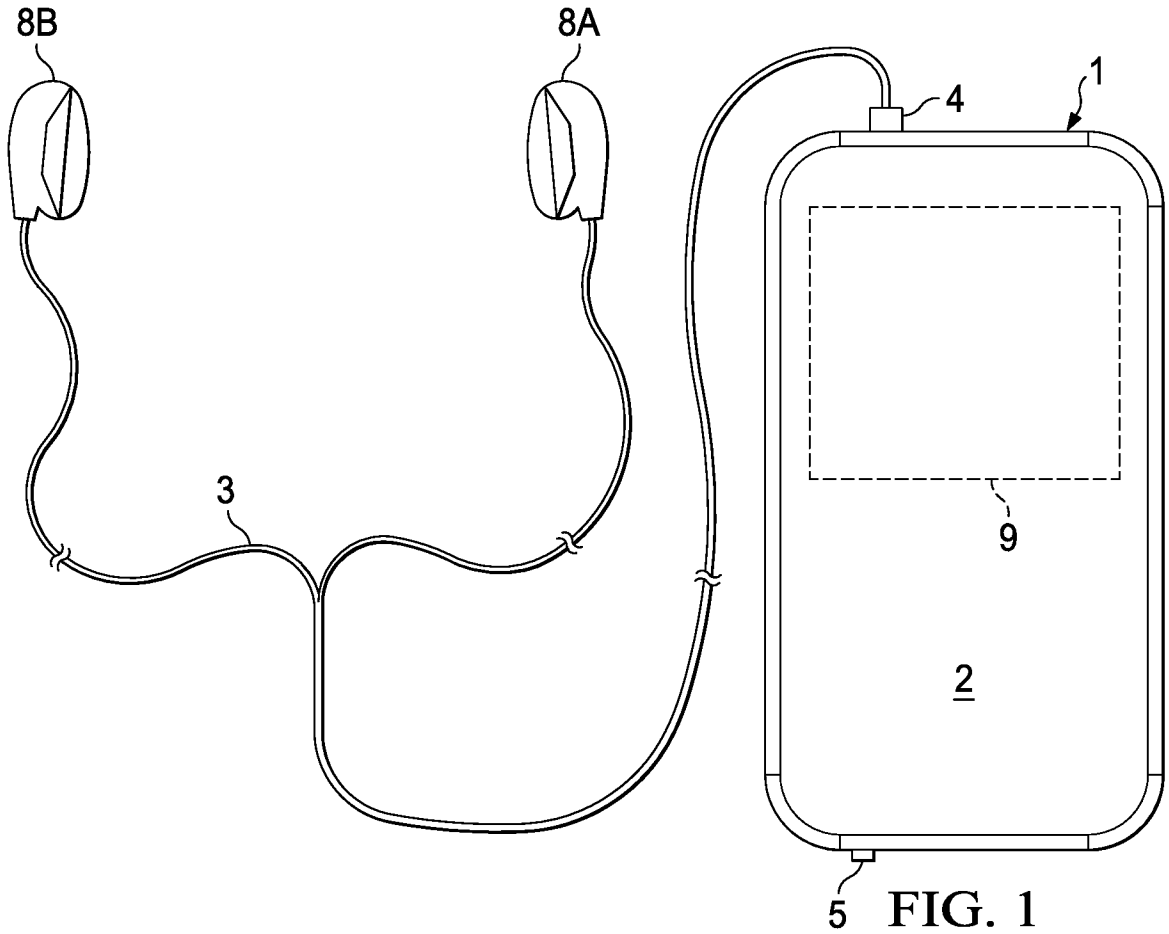

FIG. 1

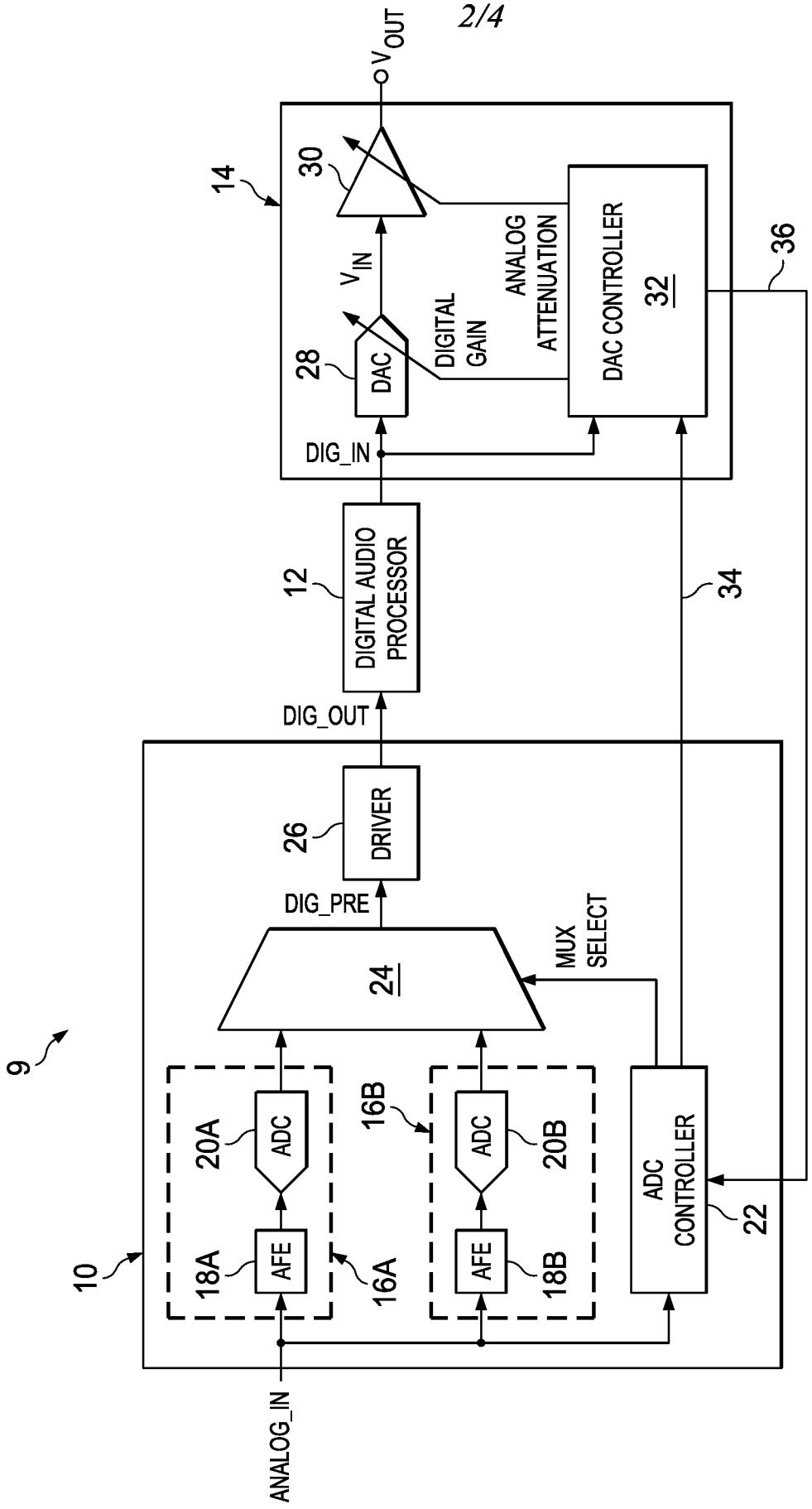
9
10
ANALOG_IN
18A
AFE
20A
ADC
16A
16B
18B
AFE
20B
ADC
ADC CONTROLLER
22
24
MUX SELECT
DIG_PRE
26
DRIVER
DIG_OUT
12
DIGITAL AUDIO PROCESSOR
34
36
14
DIG_IN
28
DAC
DIGITAL GAIN
ANALOG ATTENUATION
DAC CONTROLLER
32
30
V_{IN}
V_{OUT}

FIG. 2

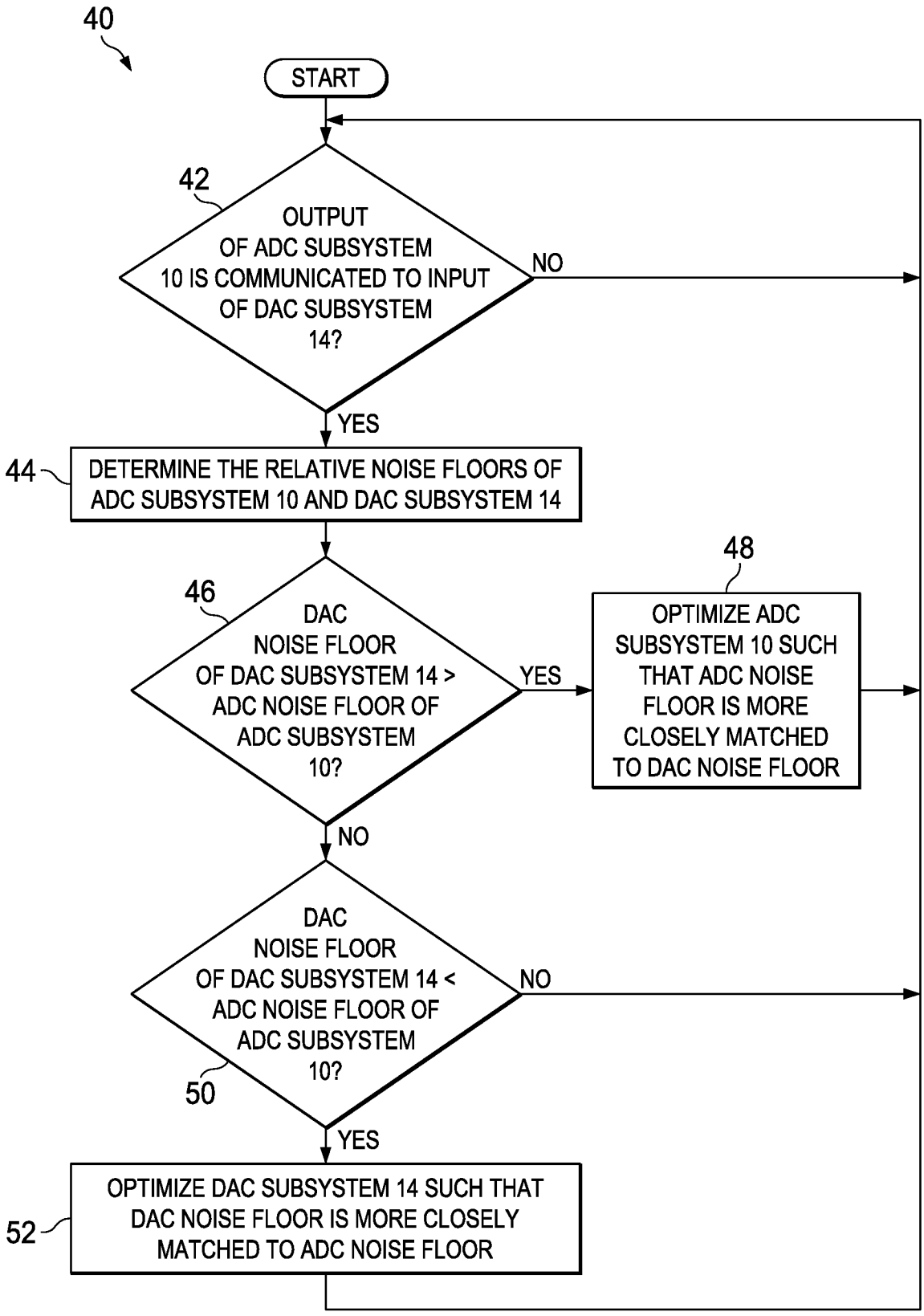
40
START
42
OUTPUT OF ADC SUBSYSTEM 10 IS COMMUNICATED TO INPUT OF DAC SUBSYSTEM 14?
NO
YES
44
DETERMINE THE RELATIVE NOISE FLOORS OF ADC SUBSYSTEM 10 AND DAC SUBSYSTEM 14
46
DAC NOISE FLOOR OF DAC SUBSYSTEM 14 > ADC NOISE FLOOR OF ADC SUBSYSTEM 10?
YES
48
OPTIMIZE ADC SUBSYSTEM 10 SUCH THAT ADC NOISE FLOOR IS MORE CLOSELY MATCHED TO DAC NOISE FLOOR
NO
DAC NOISE FLOOR OF DAC SUBSYSTEM 14 < ADC NOISE FLOOR OF ADC SUBSYSTEM 10?
50
NO
YES
52
OPTIMIZE DAC SUBSYSTEM 14 SUCH THAT DAC NOISE FLOOR IS MORE CLOSELY MATCHED TO ADC NOISE FLOOR

FIG. 3

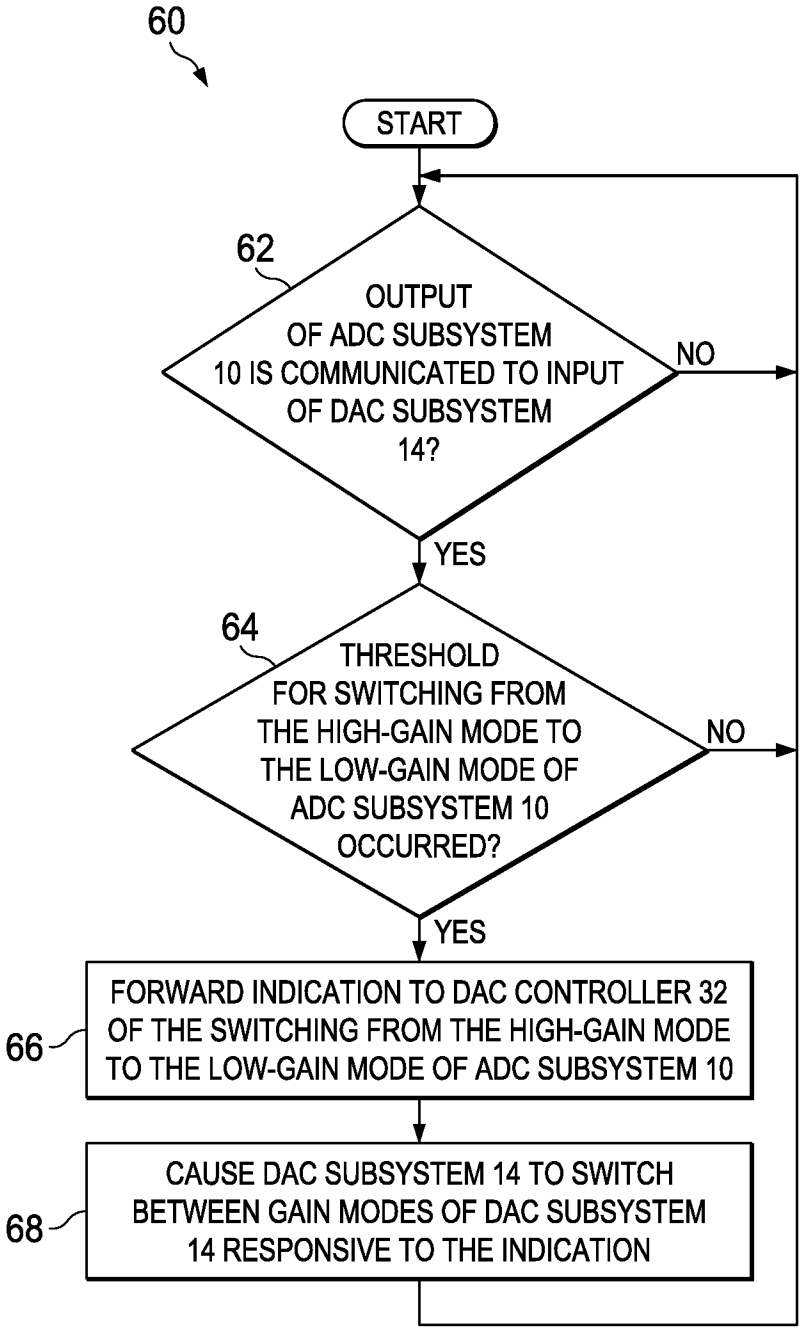
60
START
62
OUTPUT OF ADC SUBSYSTEM 10 IS COMMUNICATED TO INPUT OF DAC SUBSYSTEM 14?
NO
YES
64
THRESHOLD FOR SWITCHING FROM THE HIGH-GAIN MODE TO THE LOW-GAIN MODE OF ADC SUBSYSTEM 10 OCCURRED?
NO
YES
66
FORWARD INDICATION TO DAC CONTROLLER 32 OF THE SWITCHING FROM THE HIGH-GAIN MODE TO THE LOW-GAIN MODE OF ADC SUBSYSTEM 10
68
CAUSE DAC SUBSYSTEM 14 TO SWITCH BETWEEN GAIN MODES OF DAC SUBSYSTEM 14 RESPONSIVE TO THE INDICATION

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2016/040096

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03M1/06
ADD. H03M1/18 H03M1/70

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, COMPENDEX, INSPEC, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 542 612 B1 (NEEDHAM ALAN W [US]) 1 April 2003 (2003-04-01) columns 1-3; figure 1	1-18
X	US 4 493 091 A (GUNDRY KENNETH J [US]) 8 January 1985 (1985-01-08) column 2; claims 1-26; figures 1-8	1-18
X	US 2008/198048 A1 (KLEIN ARI [US] ET AL) 21 August 2008 (2008-08-21) paragraphs [0007] - [0011], [0041] - [0044], [0061] - [0064], [0084]; figures 2,7,8,16	1-18

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 March 2017	24/03/2017

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Jesus, Paulo

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2016/040096

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6542612 B1	01-04-2003	NONE	
US 4493091 A	08-01-1985	BE 896674 A1	01-09-1983
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US 2008198048 A1	21-08-2008	US 2008198048 A1	21-08-2008
		WO 2006102313 A2	28-09-2006