

(51) International Patent Classification:
G11C 7/12 (2006.01)(21) International Application Number:
PCT/US2014/030882(22) International Filing Date:
17 March 2014 (17.03.2014)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/801,486 15 March 2013 (15.03.2013) US(71) Applicant: GSI TECHNOLOGY, INC. [US/US]; 1213
Elko Drive, Sunnyvale, CA 94089 (US).(72) Inventors: SHU, Lee-Lean; 1731 Westbrook Avenue, Los
Altos, CA 94024 (US). CHIANG, Paul, M.; 10932
Wilkinson Avenue, Cupertino, CA 95014 (US). PARK,
Soon-Kyu; 1062 Ondine Court, San Jose, CA 95132 (US).
CHA, Gi-Won; 506 Kinvarra Court, San Ramon, CA
94582 (US).(74) Agent: SCHWAAB, Andrew, B.; DLA Piper LLP (US),
2000 University Avenue, East Palo Alto, CA 94303 (US).(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,
BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM,
DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR,
KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME,
MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ,
OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA,
SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM,
TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM,
ZW.(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ,
UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ,
TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK,
EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,
MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,
TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

[Continued on next page]

(54) Title: DATA BUS INVERSION INCLUDING DATA SIGNALS GROUPED INTO 10 BITS

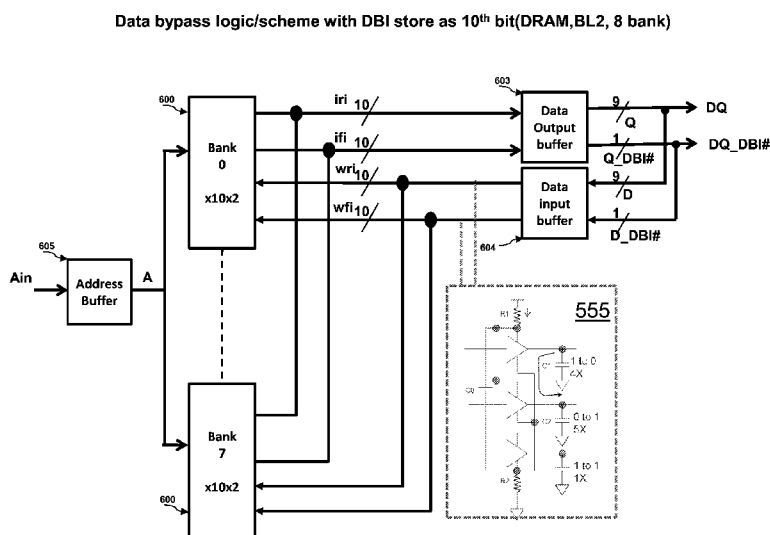


Fig. 6a

(57) Abstract: Systems, methods and fabrica-
tion processes relating to dynamic random
access memory (DRAM) devices involving
data signals grouped into 10 bits are dis-
closed. According to one illustrative imple-
mentation a DRAM device may comprise a
memory core, circuitry that receives a data
signal as input directly, without trans-
mission through DBI logic associated with
an input buffer, circuitry that stores the DBI
bit into the memory core, reads the DBI bit
from the memory core, and provides the DBI
bit as output. In further implementations,
DRAM devices herein may store and pro-
cess the DBI bit on an internal data bus as a
regular data bit.



— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(88) Date of publication of the international search report:
31 December 2014

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US14/30882

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - G11C 7/12 (2014.01)

USPC - 365/189.05

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8) Classification(s): G11C 7/06, 7/10, 7/12 (2014.01)

USPC Classification(s): 365/185.21, 189.05, 189.07; CPC Classification(s): G11C 7/06, 7/1006, 7/1084, 7/1051

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

MicroPatent (US-G, US-A, EP-A, EP-B, WO, JP-bib, DE-C,B, DE-A, DE-T, DE-U, GB-A, FR-A); ProQuest; IEEE; Google/Google Scholar, Espacenet; Keywords: dbi, inversion, conversion, address, compare, write, read, buffer, register, latch, bus, power, ground, circuit, logic, double data rate, clock

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ----- Y	US 2012/0066570 A1, (BROWN, J. et al.), 15 March 2012; paragraphs [0037], [0049], [0074].	14, 77, 80 ----- 39
X ----- Y	US 2009/0313521 A1, (HOLLIS, T), 17 December 2009; paragraphs [0018], [0034], [0048].	1-3, 23, 25, 27, 67, 88 ----- 19, 24, 26, 39, 54, 85-87, 89-91
Y	US 2008/0019451 A1, (JANG, S. et al.), 24 January 2008; figure 1; paragraphs [0052], [0055].	19, 26, 54, 85-87, 90-91
Y	EP 0 241 129 A2, (JOSHI, S. et al.), 14 October, 1987; paragraphs [0025], [0051], [0055], [0107].	24, 86, 89
Y	US 6,356,485 B1, (PROEBSTING, R.), 12 March 2002; column 15, lines 37-61.	86

☐ Further documents are listed in the continuation of Box C.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

19 August 2014 (19.08.2014)

Date of mailing of the international search report

07 NOV 2014

Name and mailing address of the ISA/US

Mail Stop PCT, Attn: ISA/US, Commissioner for Patents
P.O. Box 1450, Alexandria, Virginia 22313-1450
Facsimile No. 571-273-3201

Authorized officer:

Shane Thomas

PCT Helpdesk: 571-272-4300
PCT OSP: 571-272-7774

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US14/30882

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☒ Claims Nos.: 4-10, 12-13, 15-18, 20-22, 28-38, 40-53, 55-66, 68-73, 75-76, 78-79, 81-84
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Group I: Claims 1-3, 14, 19, 23-27, 39, 54, 67, 77, 80, 85-91; Group II: Claims 11 and 74

-Please see Supplemental Page-

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
4-10, 12-13, 15-18, 20-22, 28-38, 40-53, 55-66, 68-73, 75-76, 78-79, 81-84

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US14/30882

****-Continued from Box No. III - Observations where unity of invention is lacking-****

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fee must be paid.

Group I: Claims 1-3, 14, 19, 23-27, 39, 54, 67, 77, 80, 85-91 are directed toward a DRAM device comprising section circuitry and stores and processes a DBI bit on an internal data bus as a regular data bit.

Group II: Claims 11 and 74 are directed toward a DRAM device including a decoupling capacitor.

The inventions listed as Groups I-II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

The special technical features of Group I include storing a DBI bit into a memory core; a plurality of sense lines connecting sense circuitry to output circuitry; data input registers/latches; and bypass logic storing and processing the DBI bit as a 10th bit on an internal data bus as a regular data bit, which are not present in Group II.

The special technical features of Group II include circuitry indicating whether a data bus is to be inverted; a power supply bus shared by the data bus and a DBI data bit; and a decoupling capacitor provided between the power supply bus and a ground bus, which are not present in Group I.

The common technical feature shared by Groups I-II is a DRAM device including a DBI bus involving data signals grouped into 10 bits, the DBI bus comprising: a data bus configured such that no more than half the data bits are set to low; and circuitry including a DBI data bit. However, this common feature is previously disclosed by US 8,018,358 B2 (HOLLIS). Hollis discloses a DRAM device (SDRAM; column 1, lines 15-19) including a DBI bus involving data signals grouped into 8 bits (output data bits D0-D7 (8 bits) on the output bus and a DBI bit on a DBI line (bus) column 4, lines 8-33), the DBI bus comprising: a data bus configured such that no more than half the data bits are set to low (invert bits to guarantee that no more than four transmitted bits (half of 8 bits) are logic '0' (low); column 4, lines 20-33); and circuitry including a DBI data bit (DBI bit; column 4, lines 14-15). However, Hollis does not disclose that DBI bus involves data signal specifically grouped into 10 bits. US 2012/0066570 A1 to BROWN et al. (hereinafter 'Brown') disclose a DRAM device (DRAM; paragraph [0024]) including a bus involving data signals grouped into 10 bits (five groups of 10 bits; paragraph [0060]). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the system of Hollis to include a DBI bus involving data signals grouped into 10 bits, as taught by Brown, in order to provide a larger bandwidth capability for wider I/O configurations.

Since the common technical feature is previously disclosed by the Hollis reference, this common feature is not special and so Groups I-II lack unity.