

(51) International Patent Classification:
H01L 21/28 (2006.01)(21) International Application Number:
PCT/US2013/075133(22) International Filing Date:
13 December 2013 (13.12.2013)

(25) Filing Language: English

(26) Publication Language: English

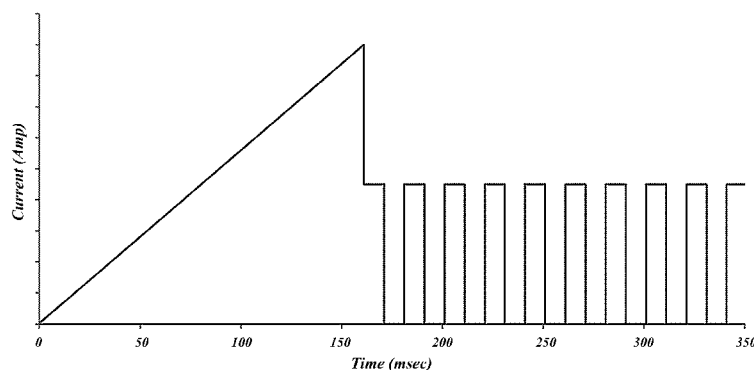
(30) Priority Data:
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Seattle, WA 98101 (US).(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,
BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM,DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR,
KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME,
MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ,
OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA,
SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM,
TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM,
ZW.(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ,
UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ,
TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK,
EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,
MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,
TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
KM, ML, MR, NE, SN, TD, TG).**Declarations under Rule 4.17:**

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

Published:

- with international search report (Art. 21(3))

(54) Title: METHODS FOR ACHIEVING METAL FILL IN SMALL FEATURES

**FIG. 1**

(57) **Abstract:** A method of electroplating on a workpiece having a sub-30 nm feature generally includes applying a chemistry to the workpiece, the chemistry including a halide ion concentration in the range of about 55 ppm to about 250 ppm and a metal cation solute species, and applying an electric waveform for less than about 5 seconds, wherein the electric waveform includes a period of ramping of current and a period of pulse plating.

METHODS FOR ACHIEVING METAL FILL IN SMALL FEATURES

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the benefit of U.S. Provisional Application
5 No. 61/737044, filed December 13, 2012, the disclosure of which is hereby expressly
incorporated by reference in its entirety.

BACKGROUND

An integrated circuit is an interconnected ensemble of devices formed within a
semiconductor material and within a dielectric material that overlies a surface of the
10 semiconductor material. Devices that may be formed within the semiconductor include
MOS transistors, bipolar transistors, diodes, and diffused resistors. Devices that may be
formed within the dielectric include thin film resistors and capacitors. The devices are
interconnected by conductor paths formed within the dielectric. Typically, two or more
levels of conductor paths, with successive levels separated by a dielectric layer, are
15 employed as interconnections. In current practice, copper and silicon oxide are typically
used for, respectively, the conductor and the dielectric.

The deposits in a copper interconnect typically include a dielectric layer, a barrier
layer, a seed layer, copper fill, and a copper cap. Conventional electrochemical
deposition (ECD) for copper fill and cap is performed in the feature using an acid plating
20 chemistry. Electrochemical deposition of copper has been found to be the most cost
effective manner by which to deposit a copper metallization layer. In addition to being
economically viable, such deposition techniques provide a substantially bottom up (e.g.,
non-conformal) copper fill that is mechanically and electrically suitable for interconnect
structures.

25 Conventional ECD copper acid plating chemistry may include, for example,
copper sulfate, sulfuric acid, hydrochloric acid, and organic additives (such as
accelerators, suppressors, and levelers). The additives drive void-free, bottom-up fill in a
feature through their adsorptive and desorptive properties and through competitive
reactions, for example, by suppressing plating at the top and on the sidewalls of the
30 feature, while enhancing plating at the bottom of the feature.

The steady downscaling of interconnect features presents new challenges, because
the characteristic dimensions (such as feature width and aspect ratio) hinder and alter the
reactivity characteristics of additives typically used. In that regard, sub-30 nm features

used for copper interconnects have small enough volume and require such few copper atoms that, in a conventional ECD copper acid plating chemistry, the features become filled within the first few seconds of plating. This is a shorter time period than that required for the adsorption and desorption kinetics of the bath additives that drive
5 traditional bottom-up filling.

Therefore, in small features (e.g., sub-30 nm features), a conventional ECD fill may result in a lower quality interconnect due to the presence of voids. As one example of a type of void formed using conventional ECD deposition, the opening of the feature may pinch off. Many other types of voids can also result from using the conventional
10 ECD copper fill process in a small feature. Such voids and other intrinsic properties of a deposit formed using conventional ECD copper fill can increase the resistance of the interconnect, thereby slowing the device and deteriorating the reliability of the copper interconnect.

Therefore, there exists a need for methods of electrochemical deposition for filling
15 sub-30 nm features from the bottom up, leaving a reduced number of void regions. Embodiments of the present disclosure are directed to filling this and other needs.

SUMMARY

This summary is provided to introduce a selection of concepts in a simplified form that are further described below in the Detailed Description. This summary is not
20 intended to identify key features of the claimed subject matter, nor is it intended to be used as an aid in determining the scope of the claimed subject matter.

In accordance with one embodiment of the present disclosure, a method of electroplating on a workpiece having a sub-30 nm feature is provided. The method generally includes applying a chemistry to the workpiece, the chemistry including a
25 halide ion concentration in the range of about 55 ppm to about 250 ppm and a metal cation solute species, and applying an electric waveform for less than about 5 seconds, wherein the electric waveform includes a period of ramping of current and a period of pulse plating.

In accordance with another embodiment of the present disclosure, a method of
30 electroplating on a workpiece having a sub-30 nm feature is provided. The method generally includes applying a chemistry to the workpiece, the chemistry including a halide ion concentration in the range of about 55 ppm to about 250 ppm and a metal cation solute species, and applying an electric waveform, wherein the electric waveform

includes a period of ramping of current for a period of less than 0.2 secs and a period of pulse plating for less than about 2 secs.

In accordance with another embodiment of the present disclosure, a method of electroplating on a workpiece having a sub-30 nm feature is provided. The method generally includes applying a chemistry to the workpiece, the chemistry including a halide ion concentration in the range of about 120 ppm to about 150 ppm and a metal cation solute species, and applying an electric waveform, wherein the electric waveform includes a period of ramping of current for a period of less than 0.2 secs and a period of pulse plating for less than about 2 secs.

In accordance with another embodiment of the present disclosure, in any of the methods described herein, the metal cation may be copper.

In accordance with another embodiment of the present disclosure, in any of the methods described herein, the halide ion concentration may be in the range of about 120 ppm to about 150 ppm.

In accordance with another embodiment of the present disclosure, in any of the methods described herein, the halide ion may be selected from the group consisting of chloride, bromide, and iodide ions, and combinations thereof.

In accordance with another embodiment of the present disclosure, in any of the methods described herein, the ramping of current may be selected from the group consisting of linear continuous ramping, non-linear continuous ramping, or pulsed ramping.

In accordance with another embodiment of the present disclosure, in any of the methods described herein, the ramping period may be for a period selected from the group consisting of less than about 0.1 seconds (100 msec), less than about 0.2 seconds (200 msec), and less than about 0.4 seconds (400 msec).

In accordance with another embodiment of the present disclosure, in any of the methods described herein, the ramping period may begin after a delay period.

In accordance with another embodiment of the present disclosure, in any of the methods described herein, the ramping may achieve a current level selected from the group consisting of in the range of about 1 amps to about 15 amps, in the range of about 7 amps to about 15 amps, in the range of about 18 amps to about 25 amps, and in the range of about 7 amps to about 25 amps.

In accordance with another embodiment of the present disclosure, in any of the methods described herein, the pulsing period may be for a period of less than about 2 seconds (2000 msec).

5 In accordance with another embodiment of the present disclosure, in any of the methods described herein, the pulsing period may have a duty cycle in the range of about 20% to about 75%.

In accordance with another embodiment of the present disclosure, in any of the methods described herein, the pulsing period may have a duty cycle of about 50%.

10 In accordance with another embodiment of the present disclosure, in any of the methods described herein, the individual pulses extend for a pulse length selected from the group consisting of about 1 msec to about 100 msec, about 5 msec to about 100 msec, and about 5 msec to about 50 msec.

15 In accordance with another embodiment of the present disclosure, in any of the methods described herein, the on current pulses may be at a current level selected from the group consisting of in a range of about 1 to about 30 amps and in a range of about 4.5 to about 30 amps.

20 In accordance with another embodiment of the present disclosure, in any of the methods described herein, the off current pulses may be at a current level in a range selected from the group consisting of about 0 amps to about 20 amps, about 0 amps to about 10 amps, and about 0 amps to about 5 amps.

In accordance with another embodiment of the present disclosure, in any of the methods described herein, the waveform may further include a triggered hot entry.

DESCRIPTION OF THE DRAWINGS

25 The foregoing aspects and many of the attendant advantages of this disclosure will become more readily appreciated by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIGURE 1 is an exemplary current waveform for use in a copper electrochemical deposition plating process in accordance with one embodiment of the present disclosure;

30 FIGURE 2 is an exemplary current waveform for use in a copper electrochemical deposition plating process in accordance with one embodiment of the present disclosure;

FIGURE 3 is a cross-sectional SEM image of a workpiece after using copper electrochemical deposition plating process in accordance with one embodiment of the present disclosure; and

FIGURE 4 is a void count comparison for various test substrates subject to various test conditions prepared in accordance with embodiments of the present disclosure.

DETAILED DESCRIPTION

5 Embodiments of the present disclosure are directed to workpieces, such as semiconductor wafers, devices, or processing assemblies for processing workpieces, and methods of processing the same. The term workpiece, wafer, or semiconductor wafer means any flat media or article, including semiconductor wafers and other substrates or wafers, glass, mask, and optical or memory media, MEMS substrates, or any other
10 workpiece having micro-electric, micro-mechanical, or microelectro-mechanical devices.

Processes described herein are to be used for metal or metal alloy deposition in features of workpieces, which include trenches and vias. In one embodiment of the present disclosure, the process may be used in small features, for example, features having a feature diameter of less than 30nm. However, it should be appreciated that the
15 processes described herein are applicable to any feature size. The dimension sizes discussed in the present application are post-etch feature dimensions at the top opening of the feature. The processes described herein may be applied to various forms of metal and metal alloy deposition, for example, in Damascene applications.

It should be appreciated that the descriptive terms "micro-feature workpiece" and
20 "workpiece" as used herein include all structures and layers that have been previously deposited and formed at a given point in the processing. Embodiments of the present disclosure are directed to methods for void-free, bottom-up fill in small features. In accordance with one embodiment of the present disclosure, a method includes providing a chemical-physical driving force to encourage void-free, bottom-up fill in small features.
25 A suitable chemical-physical driving force may include increasing the halide ion concentration in the bath and applying a unique entry and early plating electric waveform at the beginning of the plating process.

In embodiments of the present disclosure, small features described herein may be sub-30 nm features, sub-20 nm features, features in the range of 10-30 nm, or features in
30 the range of 5-30 nm.

The term "void-free fill" is defined in the art as a feature having a reduced void fill so as not to significantly increase the resistance of the interconnect or significantly affect yield or performance of the interconnect. Although features may include a

population of voids, whether generated during plating or during later processing conditions, these voids are generally undetectable in a "void-free fill." In that regard, the voids are undetectable when examined visually, for example, using an SEM image as seen in FIGURE 3. Moreover, the voids are undetectable if the smaller feature achieves
5 comparable performance values, for example, yield, resistance, and reliability values, when compared to a larger feature that has been determined to be acceptable in the industry for its performance achievements, for example, a 45 nm feature.

The plating bath may be an acid metal damascene plating bath, including, for example, metal ions (such as copper ions in the form of copper sulfate), an acid
10 concentration (such as sulfuric acid) a halide concentration (such as a chloride ion concentration in the form of hydrochloric acid), and organic additives (such as accelerators, suppressors, and levelers). It should be appreciated, however, that the methods described herein may apply to other metals besides copper and other types of chemistries besides those having an acid concentration, such as sulfuric acid.

15 In accordance with embodiments of the present disclosure, the halide ion concentration in the plating bath is increased by the use of, for example, increased chloride ion, bromide ion, or iodide ion concentration, as well as other suitable halide ions, or combinations thereof.

As a non-limiting example of a suitable halide, increased chloride ion
20 concentration may be used in the plating bath. Chloride concentration in a traditional plating bath is typically at a concentration of about 50 ppm. In accordance with embodiments of the present disclosure, the chloride concentration may be in the range of about 1.1 to about 5 times this typical concentration. In one embodiment of the present disclosure, the chloride concentration may be about 3 times the typical chloride
25 concentration in a traditional plating bath. In one embodiment of the present disclosure, the chloride concentration may be in the range of about 120 to 150 ppm. In one embodiment of the present disclosure, the chloride concentration may be in the range of about 55 ppm to about 250 ppm.

Plating baths in accordance with embodiments of the present disclosure may
30 further include optional organic additives, which may be present in various concentrations depending on the operational conditions of the plating baths. In that regard, because organic additives in conventional ECD copper acid plating chemistry (such as accelerators, suppressors, and levelers) are largely ineffective in plating

chemistry for small features in accordance with embodiments of the present disclosure, some or all of these additives may not be needed, and therefore, may be removed from the plating bath. However, if larger features are being plated using the same chemistry bath as the smaller features, then these additives must be included in the plating bath to
5 facilitate void-free plating in the larger features, as will be described in greater detail below.

The plating bath may also include complexing agents that are designed to facilitate copper deposition without requiring some or all of the organic additives. As a non-limiting example, a suitable copper complexing agent may include a chelator, such as
10 ethylenediaminetetraacetic acid (EDTA). Other complexing agents known by those skilled in the art may also be employed.

In combination with the chemical effects of increased halide concentration in the plating bath, the use of an electric waveform adds a physical component to the chemistry plating bath. In that regard, the waveform adds kinetic energy in locations inside the
15 feature that chemistry alone will not affect. Because the feature size is very small and approximately of the same scale or on the same order as the plating additive molecules, the plating chemistry does not behave as expected in larger features. Therefore, the use of a waveform physically manipulates the behavior of the molecules during plating. The waveform may be an electric current waveform or an electric potential waveform.

Although not wishing to be bound by theory, the waveform is believed by the inventors to decrease the time delays of the effectiveness of additives in a small feature. Because the additives are generally included for use in larger features and not particularly
20 useful in smaller features, an increased halide concentration is believed to mitigate any negative effects of the additives in a small feature. For example, the increased halide concentration may mitigate the negative effects of a suppressor in the small feature, for
25 which its activation time has been accelerated by the use of an electric waveform.

In accordance with one embodiment of the present disclosure, a suitable current waveform includes a triggered hot entry and a ramped current, followed by a short time period (less than 5 seconds) of pulse plating. In the triggered hot entry, the current is an
30 open circuit until the wafer touches the chemistry, thereby closing the circuit to initiate the start of the pre-set waveform.

Because the entire workpiece is not all wet at once, a ramping of current is used to maintain a constant current density in the workpiece during the wetting stage. The

ramping of the current may be performed in one or more ways. Referring to the non-limiting example in FIGURE 1, the ramping is a steady ramping. In this example, it takes about 150 msec (from about 0 to about 150 msec) for the entire workpiece to be immersed in the chemistry. Referring to the non-limiting example in FIGURE 2, steady
5 ramping occurs after a short delay and then is held constant. The length of the delay may be dependent on when the power supply is triggered. In this example, steady ramping occurs from about 0.15 to about 0.40 seconds, and then is held constant from about 0.40 seconds to about 0.85 seconds.

It should be appreciated that the ramping stage may be a linear continuous
10 ramping, a non-linear continuous ramping, or a pulsed ramping. In accordance with one embodiment of the present disclosure, the ramping may achieve a current level in the range of about 1 amp to about 15 amps. In accordance with one embodiment of the present disclosure, the ramping may achieve a current level in the range of about 7 amps to about 15 amps. In accordance with another embodiment of the present disclosure, the
15 ramping may achieve a current level in the range of about 18 amps to about 25 amps. In accordance with another embodiment of the present disclosure, the ramping may achieve a current level in the range of about 7 amps to about 25 amps.

In accordance with embodiments of the present disclosure, the ramping period may be less than 0.1 seconds, less than 0.2 seconds, less than 0.4 seconds or less than 1.0
20 second.

Although not wishing to be bound by theory, it is believed by the inventors that after the ramping stage, a pulsed waveform can be used to account for the transient effects of current when the pulsing is off. In that regard, it is believed that a pulsed waveform helps to control voltage overshoots that affect the chemistry near the wafer.

25 The pulsing stage is calculated based on the fill time, topography, and architecture of the features. The inventors found that pulsing is advantageous in reducing voids in very small features (e.g., sub-30 nm features). However, pulsing has a negative effect on larger features in that it tends to create a counter plating effect (for example, by driving additives away from the plating surface), which results in conformal deposition, as
30 opposed to desired bottom-up (or non-conformal) fill (see, e.g., experimental results described in EXAMPLE 4 below). Conformal deposition is not desirable in larger features because of the tendency to create pinch-off. Therefore, the pulsing stage is

limited to a time period in which the sub-30 nm features fill, ending before negative consequences are experienced in the larger features.

In accordance with one embodiment of the present disclosure, the pulsing stage may extend for up to 2 seconds (2000 msec). In accordance with one embodiment of the present disclosure, the pulsing stage may extend for up to 0.5 seconds (500 msec). In accordance with embodiments of the present disclosure, pulses may be in the range from about greater than 1 msec to about 100 msec in length. In one embodiment, pulses may be in the range from about 5 msec to about 100 msec in length. In one embodiment, pulses may be in the range from about 5 msec to about 50 msec in length. In the illustrated embodiments of FIGURES 1 and 2, the pulses are about 10 msec in length. (Of note, the pulsing scheme appears as a block from 0.85 to 3.1 seconds in FIGURE 2 because of the limited resolution for the timescale shown.) A non-limiting example of a "long" pulsing scheme may include, for example, a pulsing period of 15 seconds, with pulses occurring about every 10 msec. Pulses length can be as long as 4 seconds per pulse.

In one embodiment of the present disclosure, current "on" or "high" pulses may be in the range of about 1 to about 30 amps. In another embodiment of the present disclosure, current "on" or "high" pulses may be in the range of about 4.5 to about 30 amps. Current "off" or "low" pulses may be in the range of about 0 to about 20 amps, about 0 to about 10 amps, and about 0 to about 5 amps.

The duty cycle of the pulsing stage may be in the range of about 20% to about 70%, using a maximum duty cycle of 75%. In one embodiment of the present disclosure, the duty cycle is about 50%.

The combination of increased halide ion concentration and a specific pattern of electric waveform is generally believed by those skilled in the art to be counterproductive in an electrochemical deposition process. In that regard, increased halide ion concentration is generally believed by those skilled in the art to accelerate electrochemical deposition in a small features, whereas an electric waveform is generally believed by those skilled in the art to suppress electrochemical deposition.

Although not wishing to be bound by theory, the inventors of the present application believe that the combination of the increased halide ion concentration and a specific pattern of electric waveform provides advantageous electrochemical deposition results because of the specific timing of activities in a small feature. In a non-limiting

example, within about the first 100 msec of plating in a small feature, the presence of halide ions causes deposition to be accelerated. During this time period, a suppressing additive present in the plating chemistry has likely not reached the inside the small feature, and therefore is not yet effective there. However, the suppressing additive may help suppress deposition outside the feature on the field.

As the small feature begins to fill during this time period, a waveform may be applied to slow down or suppress deposition. The waveform may have a period of ramping so as not to completely suppress the acceleration caused by the increased halide concentration, thereby allowing some deposition in the small feature.

Within about the second 100 msec of plating in a small feature, a suppressing additive present in the plating chemistry may begin to take effect in the small feature. The waveform adds to the suppression effects to slow down deposition and reduce the likelihood of voids in the feature.

After about 1 second, an accelerating additive present in the plating chemistry begins to take effect. Therefore, pulse plating can be used to control the acceleration effects.

As described in the EXAMPLES that follow, void-free fill has been achieved on a test substrate in the Applied Materials CFD3LM plating chamber, and verified by SEM imaging. Sub-30 nm features on both internal and external wafers have been successfully filled and verified using post-CMP defect inspection.

EXAMPLE 1: EXEMPLARY WAVEFORM

An exemplary waveform is provided in FIGURE 1 for the first 350 msec of plating, showing current ramping at entry for 150 msec, followed by 10 msec, 50% duty cycle pulses. In FIGURE 1, about 0.2 seconds (200 msec) of pulsing is shown; however, the pulsing scheme can continue for a longer duration. In one non-limiting example, the pulsing scheme may continue for 0.5 seconds (500 msec).

EXAMPLE 2: EXEMPLARY WAVEFORM

Another exemplary waveform is provided in FIGURE 2 for the first 4 secs of plating, showing current ramping beginning at 0.15 secs, when the wafer is fully submerged in the plating solution. The 10 msec pulses appear as a "block" from 0.85 to 3.1 secs in FIGURE 2 because of the limiting resolution for the timescale shown. In FIGURE 2, a little over 2 seconds (2000 msec) of pulsing is shown.

EXAMPLE 3: SEM IMAGE

Referring to FIGURE 3, a cross-sectional SEM image showing void-free gap fill with 120 ppm chloride in the plating solution and the plating waveform of EXAMPLE 2 and FIGURE 2.

5 EXAMPLE 4: COMPARATIVE VOID COUNT RESULTS

Referring to FIGURE 4, comparative void count results are provided for three different substrates: Substrate A, a sub-20 nm feature; Substrate B, a sub-20 nm feature; and Substrate C, a 65 nm feature. Substrate A generally has smaller arrays for denser feature population. Substrate B also has small features, but much larger arrays with less
10 dense spacing of feature population.

Each substrate is exposed to five different conditions: (1) control conditions of 50 ppm chloride ion concentration and no pulse plating; (2) increased chloride conditions of 120 ppm chloride ion concentration; (3) increased chloride conditions of 120 ppm chloride ion concentration and pulse plating, for example, in accordance with the scheme
15 of FIGURE 1; (4) increased chloride conditions of 120 ppm chloride ion concentration, changed additive conditions of increasing overall bath suppression, and pulse plating with a "long" pulse step, for example, in accordance with a scheme that continues for 15 seconds with pulses occurring every 10 msecs; and (5) increased chloride conditions of 120 ppm chloride ion concentration, changed additive conditions of increasing overall
20 bath suppression, same as condition (4) above, and pulse plating, for example, in accordance with the scheme of FIGURE 1. The void counts of these five conditions are graphically shown in FIGURE 4.

The results show that the void counts for Substrate A and Substrate B decrease as chloride ion concentration is increased in the plating bath, as seen by comparing the data
25 for condition (2) and the data for condition (1) control. In addition, the void counts for Substrate A and Substrate B decrease as chloride ion concentration is increased in the plating bath in conjunction with a pulse plating scheme, as seen by comparing the data for condition (3) with the data for condition (2). The void counts for Substrate A and Substrate B still decrease with Bath B (increased chloride concentration, but changed
30 additive conditions), as seen by comparing the data for condition (4) with the data for conditions (1) and (2), but increase slightly over the void counts achieved under condition (3).

The data for condition (5) as compared to the data for condition (4), the void count for Substrate A decreases and void count for Substrate B increases. This change in data may be dependent on the differences in array size between Substrate A and Substrate B, as discussed above, and the effects of the length of the pulsing period on
5 substrates having different array size.

For each specific substrate, a desirable waveform can be optimized; therefore, in some instances, a long pulse step may be more desirable over a shorter pulse step, and vice versa. In addition, for each specific substrate a desirable bath additive concentration may be determined. Therefore, bath chemistry and waveforms can be optimized for each
10 individual substrate.

As seen in comparing the data for conditions (3), (4), and (5), voiding increases in Substrate C (65 nm feature) as pulsing is added (particularly a "long" pulse step, as used in condition (4)), which indicates that pulsing does not improve bottom-up fill in larger features.

15 While illustrative embodiments have been illustrated and described, it will be appreciated that various changes can be made therein without departing from the spirit and scope of the disclosure.

20

CLAIMS

The embodiments of the disclosure in which an exclusive property or privilege is claimed are defined as follows:

1. A method of electroplating on a workpiece having a sub-30 nm feature, the method comprising:

(a) applying a chemistry to the workpiece, the chemistry including a halide ion concentration in the range of about 55 ppm to about 250 ppm and a metal cation solute species; and

(b) applying an electric waveform for less than about 5 seconds, wherein the electric waveform includes a period of ramping of current and a period of pulse plating.

2. The method of Claim 1, wherein the metal cation is copper.

3. The method of Claim 1, wherein the halide ion concentration is in the range of about 120 ppm to about 150 ppm.

4. The method of Claim 1, wherein the halide ion is selected from the group consisting of chloride, bromide, and iodide ions, and combinations thereof.

5. The method of Claim 1, wherein the ramping of current is selected from the group consisting of linear continuous ramping, non-linear continuous ramping, or pulsed ramping.

6. The method of Claim 1, wherein the ramping period is for a period selected from the group consisting of less than about 0.1 seconds (100 msec), less than about 0.2 seconds (200 msec), and less than about 0.4 seconds (400 msec).

7. The method of Claim 1, wherein the ramping period begins after a delay period.

8. The method of Claim 1, wherein the ramping achieves a current level selected from the group consisting of in the range of about 1 amps to about 15 amps, in the range of about 7 amps to about 15 amps, in the range of about 18 amps to about 25 amps, and in the range of about 7 amps to about 25 amps.

9. The method of Claim 1, wherein the pulsing period is for a period of less than about 2 seconds (2000 msec).

10. The method of Claim 1, wherein the pulsing period has a duty cycle in the range of about 20% to about 75%.

11. The method of Claim 1, wherein the pulsing period has a duty cycle of about 50%.

12. The method of Claim 1, wherein the individual pulses extend for a pulse length selected from the group consisting of about 1 msec to about 100 msec, about 5 msec to about 100 msec, and about 5 msec to about 50 msec.

13. The method of Claim 1, wherein the on current pulses are at a current level selected from the group consisting of in a range of about 1 to about 30 amps and in a range of about 4.5 to about 30 amps.

14. The method of Claim 1, wherein the off current pulses are at a current level in a range selected from the group consisting of about 0 amps to about 20 amps, about 0 amps to about 10 amps, and about 0 amps to about 5 amps.

15. The method of Claim 1, wherein the waveform further includes a triggered hot entry.

16. A method of electroplating on a workpiece having a sub-30 nm feature, the method comprising:

(a) applying a chemistry to the workpiece, the chemistry including a halide ion concentration in the range of about 55 ppm to about 250 ppm and a metal cation solute species; and

(b) applying an electric waveform, wherein the electric waveform includes a period of ramping of current for a period of less than 0.2 secs and a period of pulse plating for less than about 2 secs.

17. A method of electroplating on a workpiece having a sub-30 nm feature, the method comprising:

(a) applying a chemistry to the workpiece, the chemistry including a halide ion concentration in the range of about 120 ppm to about 150 ppm and a metal cation solute species; and

(b) applying an electric waveform, wherein the electric waveform includes a period of ramping of current for a period of less than 0.2 secs and a period of pulse plating for less than about 2 secs.

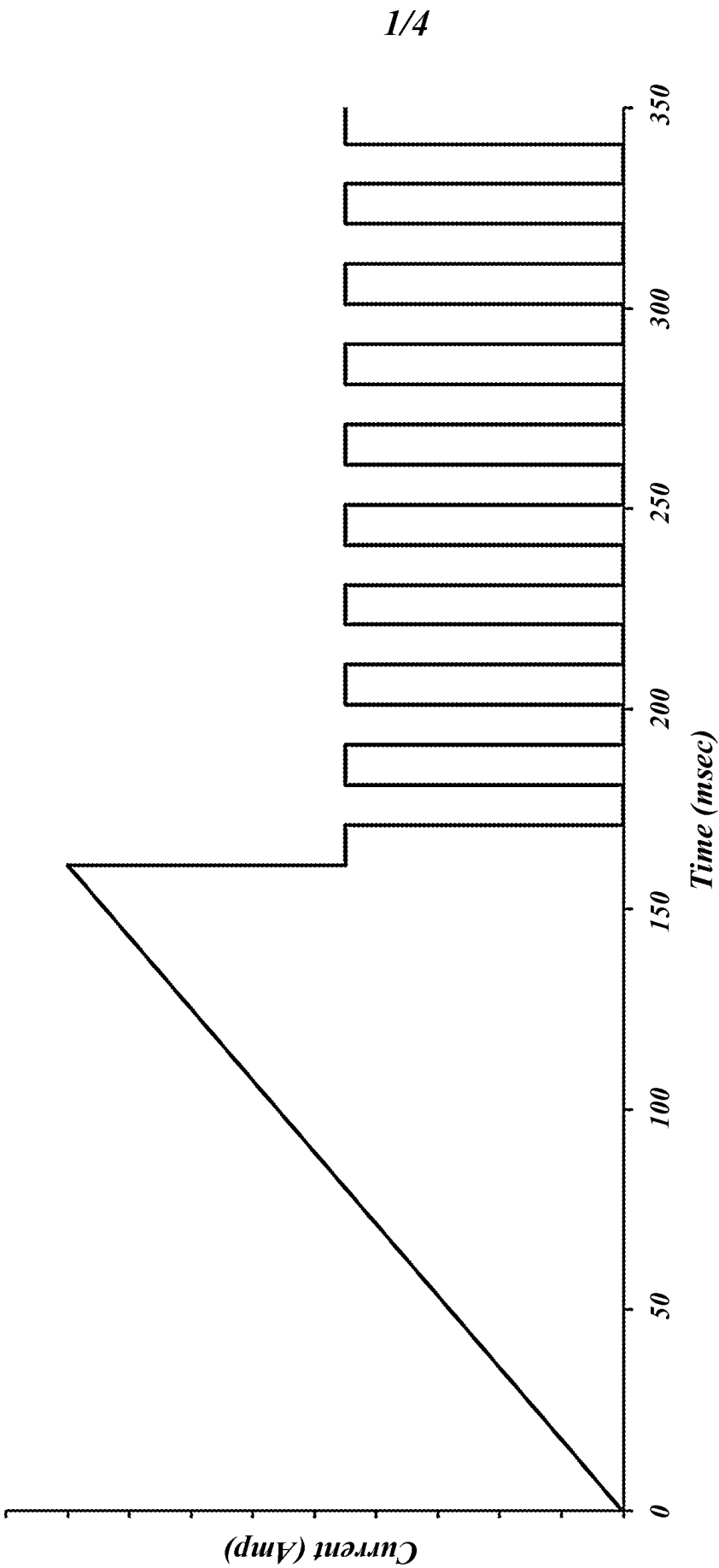


FIG. 1

2/4

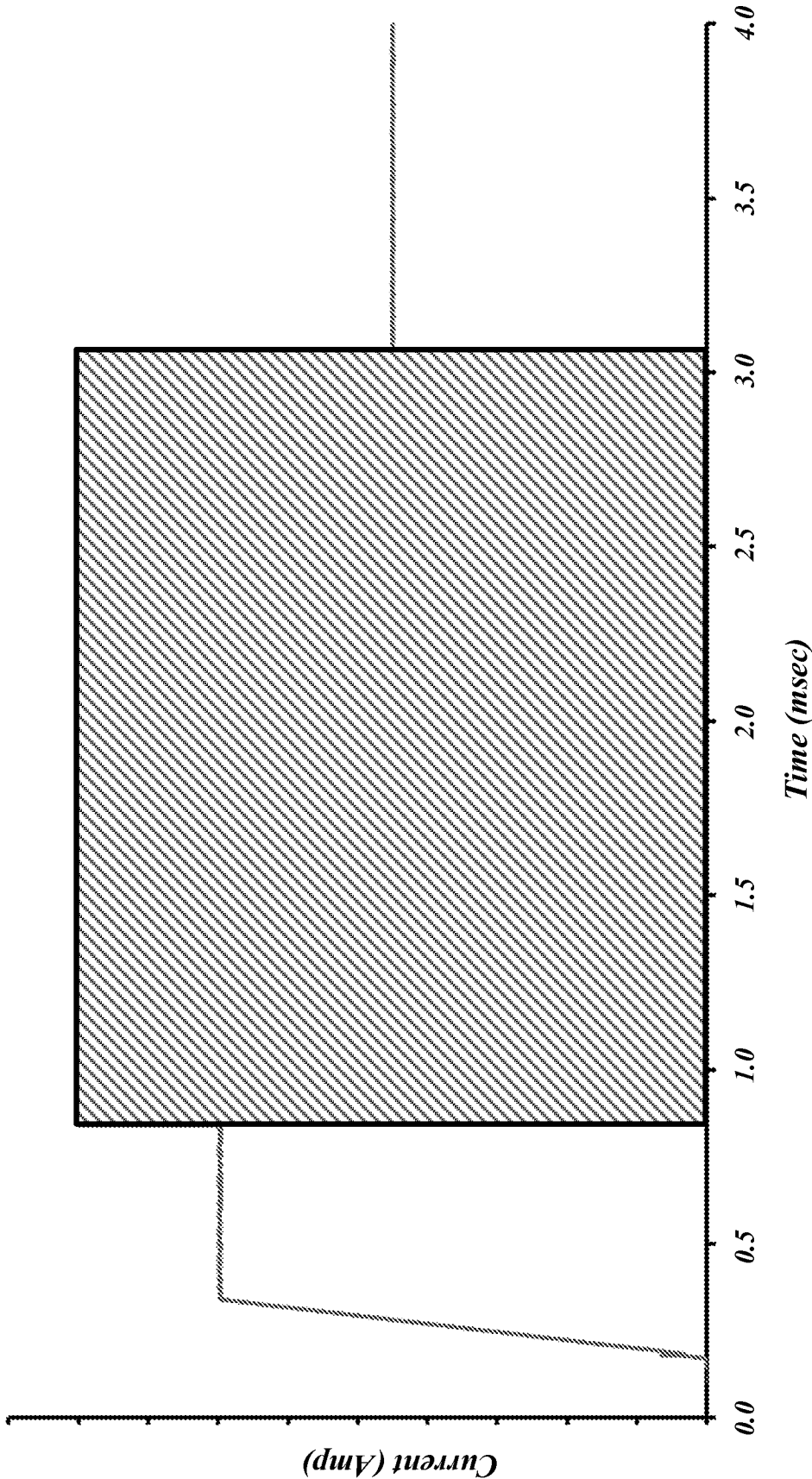


FIG. 2

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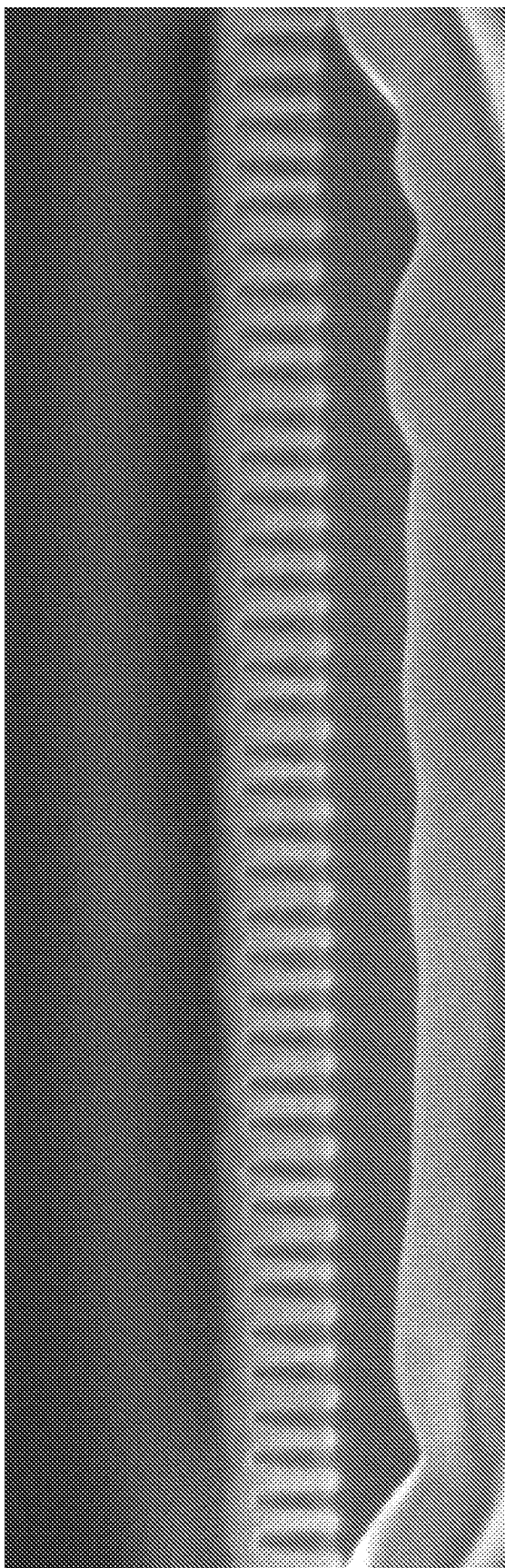


FIG. 3

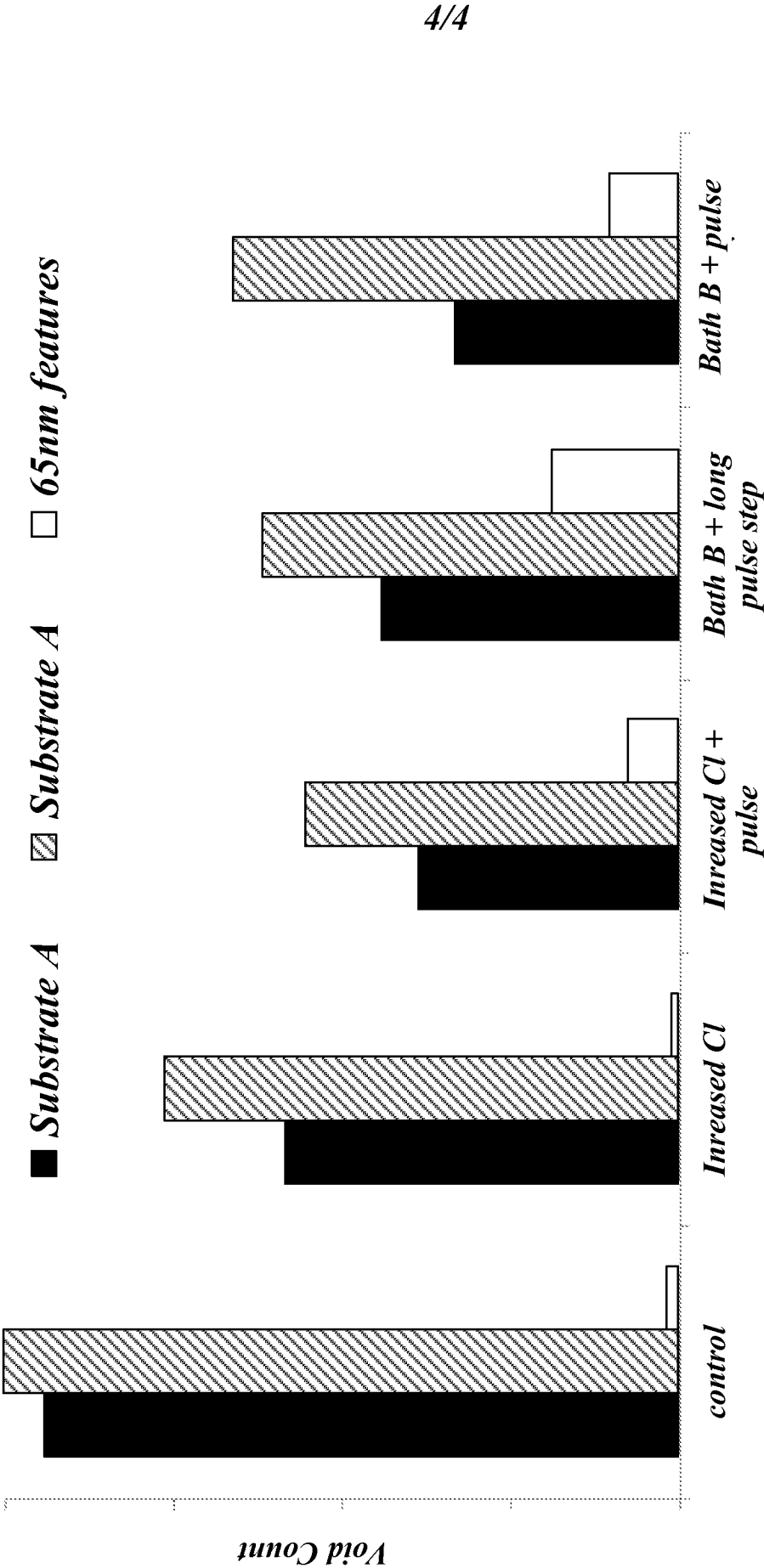


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/075133**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/28(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/28; C25D 3/38; H01L 23/48; H01L 21/288; C25D 5/02; H05H 1/00; H01L 21/44; C23C 16/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: electroplating, halide ion, electric waveform, chemistry, ramping, cation

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 7799684 B1 (JONATHAN REID et al.) 21 September 2010 See column 2, line 64 - column 3, line 16, column 7, line 41 - column 13, line 39; claims 1, 30, 33; and figure 2.	1-17
Y	US 2012-0292771 A1 (HARIKIA DELIGIANI et al.) 22 November 2012 See abstract; paragraphs [0013]-[0038], [0046]-[0052]; and figure 6.	1-17
A	US 2002-0112964 A1 (SRINIVAS GANDIKOTA et al.) 22 August 2002 See paragraphs [0017]-[0028]; claims 1-20; and figure 1.	1-17
A	KR 10-0707653 B1 (DONGBU ELECTRONICS CO., LTD.) 13 April 2007 See paragraphs [0025]-[0046]; claims 1-5; and figures 1-7.	1-17
A	US 7871676 B2 (TONY P. CHIANG et al.) 18 January 2011 See column 10, line 42 - column 12, line 67; claims 1-2; and figures 1-6.	1-17



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

28 March 2014 (28.03.2014)

Date of mailing of the international search report

31 March 2014 (31.03.2014)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/075133

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 7799684 B1	21/09/2010	None	
US 2012-0292771 A1	22/11/2012	CN 101663753 A EP 2140490 A1 JP 2010-525159 A KR 10-2009-0093985 A TW 200918690 A US 2008-0261066 A1 US 8372744 B2 WO 2008-128823 A1	03/03/2010 06/01/2010 22/07/2010 02/09/2009 01/05/2009 23/10/2008 12/02/2013 30/10/2008
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