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(54) **Title:** THREE-PHASE DETECTION MODULE

(57) **Abstract:** An apparatus includes a first optocoupler and a control module. The first optocoupler selectively allows a first current to flow from a first one of a first pair of N power supply lines to a second one of the first pair. N is an integer greater than two. The N power supply lines each provide a phase signal. The control module controls the first optocoupler and determines an occurrence of a phase failure of the phase signals based on a first signal, which is based on the first current.

THREE-PHASE DETECTION MODULE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 60/987,653 filed on 13 November 2007. The disclosure of the above application is incorporated herein by reference in its entirety.

FIELD

[0002] The present disclosure relates to three-phase power and more particularly to systems and methods for detecting conditions of a three-phase power supply.

BACKGROUND

[0003] The background description provided herein is for the purpose of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent the work is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present disclosure.

[0004] Distributing electric power in three phases is a common method of electric power transmission. Three-phase power is used to power motors and many other devices. A three-phase power system uses three alternating current (AC) voltage sources whose phases are each separated by 120 degrees. In a balanced three-phase power system, three power supply lines carry three AC signals of the same frequency (and therefore the same period), which reach their instantaneous peak values at different times. Taking a current carried by one of the three power supply lines as a reference, the other two currents are delayed in time by one third and two thirds of one period of the electrical current, respectively.

[0005] One common way to produce the three AC voltage sources is to construct an AC generator/alternator in which a rotating magnetic field passes by three sets of wire windings, each set spaced 120 degrees apart around the

circumference of the generator/alternator. A phase voltage refers to the amount of voltage measured across any one AC voltage source, such as one set wire winding in an AC generator/alternator.

[0006] The windings of a generator or of a motor can be connected to three-phase power supply lines in different configurations, including those shown in FIGs. 1-1A. FIG. 1 depicts a "Δ" (delta) configuration, while FIG. 1A depicts a "Y" configuration, also known as a star configuration. In the delta configuration, the windings are connected between the three power supply lines. In the star configuration, the windings are connected from each of the three power supply lines to a common node. The common node may be connected to a neutral line, which is present in some applications of the star configuration. The neutral line may allow lower voltage devices to be connected between one of the power supply lines and the neutral line, which results in a lower voltage than when connecting between two of the power supply lines.

SUMMARY

[0007] An apparatus includes a first optocoupler and a control module. The first optocoupler selectively allows a first current to flow from a first one of a first pair of N power supply lines to a second one of the first pair. N is an integer greater than two. The N power supply lines each provide a phase signal. The control module controls the first optocoupler and determines an occurrence of a phase failure of the phase signals based on a first signal, which is based on the first current.

[0008] In other features, the apparatus further includes second and third optocouplers that selectively allow current to flow between second and third pairs of the N power supply lines, respectively. The control module controls the second and third optocouplers. A plurality of optocouplers includes the first, second, and third optocouplers. The control module deactivates others of the optocouplers when activating one of the optocouplers. Each of the plurality of optocouplers allows current to flow while activated.

[0009] In other features, the first signal is based on the first current when the first optocoupler is activated, the first signal is based on a second current flowing from a first one of a second pair of the N power supply lines to a

second one of the second pair when the second optocoupler is activated, and the first signal is based on a third current flowing from a first one of a third pair of the N power supply lines to a second one of the third pair when the third optocoupler is activated.

[0010] In other features, the phase failure includes at least one of a phase loss, a phase order reversal, and a phase magnitude imbalance. The apparatus further includes an output optocoupler that generates the first signal based on a total current including the first current. The total current includes second and third currents from second and third optocouplers.

[0011] An apparatus includes a first optocoupler, a device, and a control module. The first optocoupler selectively allows a first current to flow from a first one of N power supply lines to a second one of the N power supply lines. N is an integer greater than two. The N power supply lines each provide a phase signal. The device allows current to flow from the second one of the N power supply lines to the first one of the N power supply lines and prevents current from flowing from the first one of the N power supply lines to the second one of the N power supply lines. The control module controls the first optocoupler and analyzes a first signal, which is based on the first current, to determine a phase failure of the phase signals.

[0012] In other features, the apparatus further includes a second optocoupler that selectively allows a second current to flow from the second one of the N power supply lines to a third one of the N power supply lines; and a third optocoupler that selectively allows a third current to flow from the third one of the N power supply lines to the first one of the N power supply lines.

[0013] In other features, the apparatus further includes an output optocoupler that receives a sum of the first, second, and third currents and that generates an output current. The first signal is based on the output current. The first, second, and third currents are zero when the first, second, and third optocouplers, respectively, are deactivated.

[0014] In other features, the apparatus further includes N Zener diodes that each allow current flow from the output optocoupler to a node of a respective one of the first, second, and third optocouplers. The N Zener diodes

each allow current flow from the node of the respective one of the first, second, and third optocouplers to the output optocoupler when a voltage applied to the Zener diode is above a predetermined threshold.

[0015] In other features, the apparatus further includes N diodes that each allow current flow from a node of a respective one of the first, second, and third optocouplers to a corresponding one of the N power supply lines. The device includes one of the N diodes. The apparatus further includes N resistances, each connected between one of the first, second, and third optocouplers and a respective one of the N power supply lines. The apparatus further includes N varistors, each connected between a respective two of the N power supply lines.

[0016] An apparatus includes N resistances, N switching devices, an output device, N unidirectional devices, and a control module. N is an integer greater than two. N switching devices each have first and second ends and each selectively electrically connect the first end to the second end. The first ends are coupled to respective ones of N power lines via the N resistances. The second ends are connected to a common node. Each of the N power lines carries a power signal having a different one of N phases. The output device is connected between the common node and a second node and generates an output signal based on a current flowing between the common node and the second node. The N unidirectional devices each allow current to flow from a node at the first end of a respective one of the N switching devices to a corresponding one of the N power lines and each inhibit current flow toward the first ends. The control module analyzes the output signal to determine a failure of the power signals and selectively generates N control signals that respectively control the N switching devices.

[0017] In other features, the apparatus further includes N Zener diodes that each allow current to flow from the second node to the node at the first end of a respective one of the N switching devices and that each selectively inhibit current flow toward the second node. Each of the N unidirectional devices includes a diode. Each of the N switching devices includes an optocoupler. The

output device includes an optocoupler. The apparatus further includes N varistors that are each connected between two of the N power lines.

[0018] A method includes receiving N power signals, each having a different one of N phases, over N power supply lines, wherein N is an integer greater than two; selectively activating a first switch to allow a first current to flow from a first one of the N power supply lines to a second one of the N power supply lines; generating a signal based on the first current; and selectively generating a phase failure signal when the signal is less than a predetermined threshold.

[0019] In other features, the method further includes controlling a motor based on the phase failure signal. The method further includes halting operation of the motor when the phase failure signal is generated. The method further includes activating the first switch for a predetermined period of time. The predetermined period is based on a duration of one cycle of one of the N power signals. The predetermined period is equal to the duration plus a predetermined value.

[0020] In other features, the method further includes selectively activating a second switch to allow a second current to flow from the second one of the N power supply lines to a third one of the N power supply lines; and selectively activating a third switch to allow a third current to flow from the third one of the N power supply lines to the first one of the N power supply lines. The method further includes deactivating remaining ones of the switches when activating one of the first, second, and third switches.

[0021] In other features, the method further includes sequentially activating the first, second, and third switches. The method further includes generating the signal based on the first, second, and third currents. The signal is proportional to a sum of the first, second, and third currents. The first, second, and third currents are zero when the first, second, and third switches, respectively, are deactivated. The method further includes generating the phase failure signal when a peak value of the signal is less than a predetermined threshold and one of the first, second, and third switches is activated.

[0022] In other features, the method further includes generating the phase failure signal when the peak value of the signal over a predetermined period is less than the predetermined threshold. The method further includes determining a first peak value of the signal when the first switch is activated; determining a second peak value of the signal when the second switch is activated; determining a third peak value of the signal when the third switch is activated; and generating the phase failure signal when a difference between the first, second, and third peak values is greater than a predetermined limit.

[0023] In other features, the method further includes activating the first switch; comparing the signal to a threshold value while the first switch is activated; after the signal exceeds the threshold value, alternately activating the second switch and the third switch; comparing the signal to the threshold value while the second switch is activated and while the third switch is activated; and generating the phase failure signal when the signal exceeds the threshold value while the third switch is activated prior to the signal exceeding the threshold value while the second switch is activated.

[0024] In other features, the method further includes activating the first switch; comparing the signal to a threshold value while the first switch is activated; after the signal exceeds the threshold value, alternately activating the second switch and the third switch; determining a first time at which the signal exceeds the threshold value while the second switch is activated; determining a second time at which the signal exceeds the threshold value while the third switch is activated; and generating the phase failure signal when the first time is after the second time.

[0025] Further areas of applicability of the present disclosure will become apparent from the detailed description, the claims and the drawings. The detailed description and specific examples are intended for purposes of illustration only and are not intended to limit the scope of the disclosure.

BRIEF DESCRIPTION OF DRAWINGS

[0026] The drawings described herein are for illustration purposes only and are not intended to limit the scope of the present disclosure in any way.

[0027] FIGs. 1-1A are exemplary schematics of motor winding connections according to the prior art;

[0028] FIG. 2 is a functional block diagram of an exemplary motor system according to the principles of the present disclosure;

[0029] FIG. 2A is a schematic diagram of an exemplary implementation of the phase module according to the principles of the present disclosure;

[0030] FIGs. 2B-2C are schematic diagrams showing exemplary current flow in the phase module of FIG. 2A;

[0031] FIGs. 3-3A are flowcharts depicting steps performed by exemplary implementations of the control module of FIG. 2 according to the principles of the present disclosure;

[0032] FIGs. 4-4C are flowcharts depicting exemplary steps performed in checking for phase loss according to the principles of the present disclosure;

[0033] FIGs. 5-5C are flowcharts depicting exemplary steps performed in checking for phase reversal according to the principles of the present disclosure; and

[0034] FIGs. 6-6A are flowcharts depicting exemplary steps performed in checking for peak voltage imbalance according to the principles of the present disclosure.

DETAILED DESCRIPTION

[0035] The following description is merely exemplary in nature and is in no way intended to limit the disclosure, its application, or uses. For purposes of clarity, the same reference numbers will be used in the drawings to identify similar elements. As used herein, the phrase at least one of A, B, and C should be construed to mean a logical (A or B or C), using a non-exclusive logical or. It should be understood that steps within a method may be executed in different order without altering the principles of the present disclosure.

[0036] As used herein, the term module may refer to, be part of, or include an Application Specific Integrated Circuit (ASIC), an electronic circuit, a processor (shared, dedicated, or group) and/or memory (shared, dedicated, or group) that execute one or more software or firmware programs, a combinational

logic circuit, and/or other suitable components that provide the described functionality.

[0037] Referring to FIG 2, a motor 102 receives three-phase power via U, V, and W power supply lines. Power signals on the U, V, and W power supply lines have phases of ΦU, ΦV, ΦW, respectively, which are different from each other by 120 degrees (2 / 3 * pi radians). A neutral line may also be connected to the motor 102. For example only, windings of the motor may be configured as shown in FIGs. 1-1A. Although three-phase power is shown, the principles of the present disclosure apply to multiphase power having more than three phases.

[0038] A control system 106 including a phase module 110 and a control module 120 also receives the U, V, and W power signals. The phase module 110 receives the U, V, and W power signals at nodes N3, N2, and N1, respectively. The phase module 110 outputs a signal S4 based on a voltage difference between two of the power signals to a control module 120. The control module 120 controls the phase module 110 using selection signals S1, S2, and S3.

[0039] Voltage differences may be referred to as line voltages. For example, line voltage UV refers to the voltage difference from power signal U to power signal V; line voltage VW refers to the voltage difference from power signal V to power signal W; line voltage WU refers to the voltage difference from power signal W to power signal U.

[0040] The control module 120 may generate the selection signals S1, S2, and S3 to select one of the line voltages. For example, by activating the selection signal S1 and deactivating the selection signals S2 and S3, the phase module 110 may output a signal as S4 based on UV. Similarly, activating the selection signals S2 and S3 cause S4 to be based on VW and WU, respectively.

[0041] The control module 120 may activate one of the selection signals for at least a predetermined period. For example, the predetermined period of time may be equal to the length of one cycle of power plus a tolerance value (for example, 3-5 milliseconds). The length of one cycle may be 20 milliseconds for 50 Hertz power or 16.7 milliseconds for 60 Hertz power.

[0042] The control module 120 analyzes signal S4 to determine if there are any problems with the incoming three-phase power. For example, the control module 120 may detect whether one of the U, V, or W power signals is missing, whether the phases of the power signals is wrong, and/or whether voltages of the power signals are imbalanced.

[0043] Referring to FIG. 2A, an exemplary implementation of the phase module 110 is shown. Power supply line U connects to a first end of a resistor R201 and a cathode of a diode D202 at a node N3; power supply line V connects to a first end of a resistor R202 and a cathode of a diode D203 at a node N2; power supply line W connects to a first end of a resistor R203 and a cathode of a diode D201 at a node N1. A varistor RV201 is connected between the node N3 and the node N1; a varistor RV202 is connected between the node N3 and the node N2; and a varistor RV203 is connected between the node N2 and the node N1. In various implementations, varistors RV201, RV202, and RV203 may be metal oxide varistors.

[0044] An anode of the diode D201 and the other end of the resistor R201 connect to a cathode of a zener diode Z201 at a node N4; an anode of the diode D202 and the other end of the resistor R202 connect to a cathode of a zener diode Z202 at a node N5; an anode of the diode D203 and the other end of the resistor R203 connect to a cathode of a zener diode Z203 at a node N6. Anodes of the zener diode Z201, the zener diode Z202, and the zener diode Z203 connect at a node N7.

[0045] The node N4 connects to a collector of an optical coupler X201; node N5 connects to a collector of an optical coupler X202; and node N6 connects to a collector of an optical coupler X203. Emitters of optical coupler X201, optical coupler X202, and optical coupler X203 connect to an anode of an optical coupler X204 at node N8. A cathode of optical coupler X204 connects to node N7.

[0046] A voltage input V201 connects through resistor R207 to anodes of the optical coupler X201, the optical coupler X202, and the optical coupler X203. A cathode of the optical coupler X201 receives the selection signal S1 at a node N31; a cathode of the optical coupler X202 receives the selection signal

S2 at a node N32; and a cathode of the optical coupler X203 receives the selection signal S3 at a node N33.

[0047] A collector of the optical coupler X204 connects to a voltage input V202. In various implementations, the voltage inputs V201 and V202 may have approximately equal voltages and may be from the same power source. An emitter of the optical coupler X204 outputs the line voltage signal S4 to the control module 120 via node N34. A resistor R204 and a capacitor C201 are connected between the node N34 and a ground potential.

[0048] A variable resistance to ground may be created at the node N34. For example, a bipolar junction transistor (BJT) Q1 may be included, where an emitter of BJT Q1 is connected to the ground potential and a collector of BJT Q1 is connected to the node N34 via a resistor R205. A base of BJT Q1 receives a signal S5 via a resistor R206. The signal S5 may be provided by the control module 120.

[0049] When the signal S5 is activated, the resistance to ground seen by the node N34 is reduced. For a given current through the optical coupler X204, reducing the resistance to ground reduces the voltage output to S4. This allows the range of the measured voltage to be changed. To maximize the precision of measurement, measured voltages should be as large as possible without reaching the voltage input V202.

[0050] The voltage range may be varied to counteract circuit changes. For example, over time, a current transfer ratio of optical couplers, such as the optical coupler X204, may decrease. The voltage range may therefore be increased to counteract this decrease in current. The voltage range may also be varied to accommodate different power voltages, such as may be used by different countries or different electrical grids. In addition, the voltage range may be adjusted when moving between power generated by delta or star configurations.

[0051] The resistors R201, R202, and R203 are current limiting resistors that limit the current input to the optical couplers X201, X202, and X203. The varistors RV201, RV202, and RV203 may absorb excessive transient

voltages between the power supply lines. The diodes Z201, Z202, and Z203 provide alternative current paths when optical couplers are deactivated.

[0052] When any of the selection signals S1, S2, or S3, is low, a current from voltage input V201 causes a light-emitting diode (LED) of the corresponding optical coupler to emit light, which energizes a base of a phototransistor, allowing current to flow from the collector to the emitter of the optical coupler. Thus, the selection signals S1, S2, or S3 are active-low.

[0053] The control module 120 may generate values for the selection signals S1, S2, or S3 corresponding to four modes. In mode 1, the selection signal S1 is active and the selection signals S2 and S3 are inactive. This causes the signal S4 to be based on line voltage UV. In various implementations, negative values of the line voltage UV will not reach the signal S4, as described in more detail below.

[0054] Because the circuit of FIG. 2A does not rely on a neutral line, the circuit can analyze power corresponding to both a star three-phase configuration, which may or may not have an associated neutral line, and a delta three-phase configuration, which does not normally have an associated neutral line. For example only, even if three-phase power was generated using a star configuration including a neutral line, the neutral line may not be present at the motor, such as when the motor's windings are in a delta configuration. The circuit of FIG. 2A may therefore be used with any three-phase power regardless of the star/delta configuration of the generating source or the consuming motor.

[0055] As shown in FIG. 2B, when the phase module 110 operates in mode 1 and the line voltage UV is positive, a current from power supply line U flows through the resistor R201, the optical coupler X201, the optical coupler X204, the zener diode Z203, the node N6, and the diode D203, reaching the power supply line V. This current activates an LED of the optical coupler X204, thereby activating a phototransistor of the optical coupler X204, producing a current. This current reaches ground, such as by the resistor R204, thereby creating a voltage at the node N34.

[0056] In mode 2, the selection signal S2 is low and the selection signals S1 and S3 are high. Current then flows from the power supply line V to

the power supply line W in a similar manner to that of mode 1. In mode 3, the selection signal S3 is low and the selection signals S1 and S2 are high, allowing current to flow from the power supply line W to the power supply line U. In mode 4, all the selection signals are high, which deactivates the optical couplers X201, X202, and X203.

[0057] The zener diodes may provide an alternative current path when the line voltage UV, the line voltage VW, or the line voltage WU are great enough and the corresponding optical coupler to the line voltage is deactivated. When the line voltage UV is positive and the optical coupler X201 is deactivated, current may flow through the zener diode Z201 in the reverse direction. This current may reach the power supply line V via the zener diode Z202 and the resistor R202 or the zener diode Z203 and the diode D203. Similar current flows are present for VW and WU.

[0058] As shown in FIG. 2C, when the line voltage UV is negative, regardless of mode, a current may flow from the power supply line V to the power supply line U. This current may flow from the power supply line V flows through the resistor R202, the diode D202 to reach the power supply line U. Similar current flows are present for negative values of VW and WU.

[0059] Referring now to FIG. 3, a flowchart illustrates exemplary control of control module 120. In step 401, the control module 120 is initialized. In step 402, control checks whether a phase loss has occurred and sends out error messages accordingly. For example only, a phase loss may be detected when one of the line voltages UV, VW, or WU is less than a predetermined threshold. For example only, if the line voltage UV remains less than the predetermined threshold over an entire power cycle, one or both of the power signals U and V may be zero or unusually low. In step 402A, if a phase loss was detected, control returns back to step 402; otherwise, control returns to step 403.

[0060] In step 403, control determines whether a phase order reversal has occurred and sends out error messages accordingly. Because the phase voltages U, V, and W are separated by 120 degrees, the line voltages UV, VW, and WU may also be out of phase by 120 degrees. Each of the line voltages will reach a peak voltage at a different time. The order in which the line voltages

reaches their peak voltage may be predetermined. A deviation from this predetermined order may cause inefficient or even damaging operation of an attached motor. For example, a motor may be configured to use line voltages reaching their peak in the following order: UV, VW, WU. If the order changes to UV, WU, VW, a phase order reversal had occurred.

[0061] In step 403A, if a phase order reversal was detected, control returns to step 403; otherwise, control goes to step 404. In step 404, control determines whether a phase magnitude imbalance has occurred and sends out error messages accordingly. A phase magnitude imbalance may be defined as any two of the line voltages differing in magnitude by more than a predetermined limit. For example only, peak magnitude values of each of the line voltages may be compared.

[0062] In step 404A, if a phase magnitude imbalance is detected, control returns to step 404; otherwise, control returns to step 402. Control may wait before returning to step 402, causing detection to be performed intermittently. This may save power at the expense of potentially slower detection of errors.

[0063] Referring now to FIG. 3A, steps 412, 413, and 414 set flags when errors occur. Steps 412A, 413A, and 414A check these flags to determine whether errors have occurred. If so, control transfers to steps 420, 421, and 422, respectively. In steps 420, 421, and 422, an appropriate error message is generated. Power supply errors may cause the motor 102 to overheat or run in an undesired manner. Based on the error message, the control module 120 may disable the motor 102 or perform other remedial action, such as decreasing a load on the motor 102 or decreasing a speed of the motor 102.

[0064] For example only, the control module 120 may instruct the motor 102 to stop operation. In various implementations, the control module 120 may stop the motor 102 from operating by tripping a circuit interruption element, such as a relay or a circuit breaker, which will cut off power from the power supply lines U, V, and W to the motor 102. In various implementations, the control module 120 may monitor the error messages and change the remedial action performed based on historical information about the error messages.

[0065] For example, individual error messages may be logged along with a timestamp. If too many error messages occur within a predetermined time window, the control module 120 may disable the motor 102. If error messages are only occasionally generated, a service indicator may be activated. The service indicator may include an illuminated light, audible indicator, and/or an electronic indication, such as a network control message, email message, text message, etc. If error messages are being generated continuously, the control module 120 may immediately disable the motor 102.

[0066] Referring to FIG. 4, a logic flow diagram illustrating general operation of an exemplary implementation of step 402 in detail is shown. In step 501, for a detection period, control sets the value of the selection signal S1 at low and the values of the selection signals S2 and S3 at high. Control module 120 detects the line voltage signal S4 received at the node 34 to determine if a high value above a predetermined threshold has been received in the detection period. In step 501A, control determines a next step based on a result of step 501; if a high value is not detected in the detection period, then either ΦU or ΦV is missing in the detection period, and control sends out an error message in step 501B, and returns to step 501; if a high value is detected, control goes to a next step.

[0067] In step 502, for a detection period, control sets the value of the selection signal S2 at low, and the values of the selection signals S1 and S3 at high. Control module 120 detects the line voltage signal S4 received at the node 34 to determine if a high value above a predetermined threshold has been received in the detection period. In step 502A, control determines a next step based on a result of step 502; if a high value is not detected in the detection period, then either ΦV or ΦW is missing in the detection period, and control sends out an error message in step 502B and returns to step 502; if a high value is detected, control goes to a next step.

[0068] In step 503, for a detection period, control sets the value of the selection signal S3 at low, and the values of the selection signals S1 and S2 at high. Control module 120 detects the line voltage signal S4 received at node N34 to determine if a high value above a predetermined threshold has been

received in the detection period. In step 503A, control determines a next step based on a result of step 503; if a high voltage is not detected in the detection period, then either ΦW or ΦU is missing in the detection period, and control sends out an error message in step 503B and returns to step 503; if a high voltage is detected, control exits step 402.

[0069] Referring to FIG. 4A, a logic flow diagram illustrating general operation of an exemplary implementation of step 412 in detail is shown. The operation shown in FIG. 4A is generally similar to the operation shown in FIG. 4. In this exemplary implantation of step 412, in step 501A if a high value above a predetermined threshold has not been detected in the detection period, control flags an error in step 511B and then enters into step 502. In step 502A if a high value above a predetermined threshold has not been detected in the detection period, control flags an error in 512B and enters into step 504. In step 503A if a high value above a predetermined threshold has not been detected in the detection period, control flags an error a 513B and exits step 412.

[0070] Referring to FIG. 4B, a logic flow diagram illustrating general operation of yet another exemplary implementation of step 412 in detail is shown. The control module 120 enters into step 412 and starts from step 551. In step 551, control resets a timer for a detection period. Next, in step 553, control sets the value of the selection signal S1 at low and the values of the selection signals S2 and S3 at high, and then senses a voltage of the line voltage signal S4 received at the node 34 representing the line voltage UV. In step 555, control determines if the sensed voltage is greater than a predetermined threshold; if yes, control enters step 561; if not, control enters step 557. In step 557, control checks the timer and determines if the predetermined period of time has lapsed; if not, control returns back to step 553; if yes, control flags an error in step 559 and enters step 561.

[0071] In step 561, control resets the timer again for the predetermined period of time. Next, in step 563, control sets the value of the selection signal S2 at low and the values of the selection signals S1 and S3 at high, and then senses a voltage of the line voltage signal S4 received at the node 34 representing the line voltage VW. In step 565, control determines if the sensed

voltage is greater than the predetermined threshold; if yes, control enters step 571; if not, control enters step 567. In step 567, control checks the timer and determines if the predetermined period of time has lapsed; if not, control returns back to step 563; if yes, control flags an error in step 569 and enters step 571.

[0072] In step 571, control resets the timer again for the predetermined period of time. Next, in step 573, control sets the value of the selection signal S3 at low and the values of the selection signals S1 and S2 at high, and then senses a voltage of the line voltage signal S4 received at the node 34 representing the line voltage WU. In step 575, control determines if the sensed voltage is greater than the predetermined threshold; if yes, control exits step 412; if not, control enters step 577. In step 577, control checks the timer and determines if the predetermined period of time has lapsed; if not, control returns back to step 573; if yes, control flags an error in step 579 and exits step 412.

[0073] Referring to FIG. 4C, a logic flow diagram illustrating general operation of another exemplary implementation of step 402 in detail is shown. The operation shown in FIG. 4C is generally similar to the operation shown in FIG. 4B. In this implantation of step 402, in step 557, control checks the timer and determines if the predetermined period of time has lapsed; if not, control returns back to step 553; if yes, control sends out an error message in step 558 and returns to step 551. In step 567, control checks the timer and determines if the predetermined period of time has lapsed; if not, control returns back to step 563; if yes, control sends out an error message in step 568 and returns to step 561. In step 577, control checks the timer and determines if the predetermined period of time has lapsed; if not, control returns back to step 573; if yes, control sends out an error message in step 578 and returns to step 571.

[0074] Referring to FIG. 5, a logic flow diagram illustrating an exemplary implementation of step 403 in detail is shown. In step 601, control sets the selection signal S3 at low and the selection signals S2 and S1 at high, and detects the line voltage signal S4 representing the line voltage UV received at the node N34. In step 601A, control determines if a high voltage above a predetermined threshold has been detected in a detection period; if not, control can send out an error message in step 604 and then return to step 601; If yes,

control goes to step 602. In step 602, control sets the selection signal S3 at high, and initially sets one of the selection signal S2 and the selection signal S1 at high and the other at low and then alternates the values of the selection signal S1 and the selection signal S2 rapidly in a detection period. At the same time, control detects the value of line voltage signal S4.

[0075] In step 602A, control determines a next step based on a result of step 602. If a first high voltage above a predetermined threshold of the line voltage signal S4 is detected at a time when the selection signal S2 is low, then the phase of the line voltage VW follows the phase of line voltage UV before the phase of WU; control can decide this is a correct phase sequence and exit step 403. If the first high voltage above a predetermined threshold of line voltage signal S4 is detected at a time when the selection signal S1 is low, then the phase of the line voltage WU follows the phase of the line voltage UV before the phase of the line voltage VW; control can decide this is not a correct phase sequence, send out an error message in step 604, and return to step 601.

[0076] In the above described steps, control is configured to consider the correct phase sequence as the phase of line voltage VW following the phase of line voltage UV and the phase of line voltage WU following the phase of line voltage VW. It is understood, however, that the correct phase sequence can be alternatively defined as, e.g., the phase of line voltage WU following the phase of line voltage UV and the phase of line voltage VW following the phase of line voltage WU; control can be configured accordingly. It is also understood that in step 601, control can be configured to set the selection signal S2 or the selection signal S1 at low, and the other two selection signals at high, and thus detect the line voltage signal S4 representing the line voltage VW or the line voltage WU; accordingly, in steps 602 and 602A, control can be configured to determine if the phase of line voltage WU or line voltage UV follows.

[0077] The exemplary implementation shown in FIG. 5 can be modified such that instead of sending an error message and returning to step 601, control flags an error in step 604 and then exits step 403.

[0078] Referring to FIG. 5A, a logic flow diagram illustrating an exemplary implementation of step 413 is shown. A wait period can be defined

as the time interval between peak values of two consecutive phase voltage in normal operation of the three-phase power supply (e.g., approximately one third of a cycle of the power supply). Control module 120 resets a timer in step 651. In step 653, control sets the value of the selection signal S1 at low and the values of the selection signals S2 and S3 at high, and then senses a voltage of the line voltage signal S4 received at node 34 representing the line voltage UV. In step 655, control determines if the sensed voltage is greater than a predetermined threshold; if yes, control enters step 661; if not, control enters step 657. In step 657, control checks the timer and determines if a detection period has lapsed; if not, control returns back to step 653; if yes, control flags an error in step 659 and then exits step 413.

[0079] Control module 120 resets the timer in step 661. In step 663, control sets the value of the selection signal S2 at low and the values of the selection signals S1 and S3 at high, and then senses a voltage of the line voltage signal S4 received at node 34 representing line voltage VW. In step 665, control determines if the sensed voltage is greater than a predetermined threshold; if yes, control exits step 413; if not, control enters step 667. In step 667, control checks the timer and determines if a wait period plus a tolerance period has lapsed; if not, control returns back to step 663; if yes, control flags an error in step 669 and then exits step 413.

[0080] Referring to FIG. 5B, a logic flow diagram illustrating general operation of another exemplary implementation of step 403 in detail is shown. The operation shown in FIG. 5B is generally similar to the operation shown in FIG. 5A. Instead of flagging an error in step 659 and step 669, control can send out an error message in step 658 and step 668. After executing steps 658 and 668, control returns to step 651.

[0081] Referring to FIG. 5C, a logic flow diagram illustrating general operation of another exemplary implementation of step 413 in detail is shown. Control module 120 resets a timer in step 671. In step 673, control sets the value of the selection signal S1 at low and the values of the selection signals S2 and S3 at high, and then senses a voltage of the line voltage signal S4 received at the node 34 representing the line voltage UV. In step 675, control determines

if the sensed voltage is greater than a predetermined threshold; if yes, control enters step 683; if not, control enters step 677. In step 677, control checks the timer and determines if a detection period has lapsed; if not, control returns back to step 673; if yes, control flags an error in step 699 and then exits step 413.

[0082] In step 683, control sets the value of the selection signal S2 at low and the values of the selection signals S1 and S3 at high, and then senses a voltage of the line voltage signal S4 received at node 34 representing the line voltage VW. In step 685, control determines if the sensed voltage is greater than a predetermined threshold; if yes, control can determine this is a correct sequence and exit the operation of step 413; if not, control enters step 689. In step 689, control sets the value of the selection signal S3 at low and the values of the selection signals S1 and S2 at high, and then senses a voltage of the line voltage signal S4 received at the node 34 representing the line voltage WU.

[0083] In step 691, control determines if the sensed voltage is greater than a predetermined threshold; if yes, control has detected a high value of the line voltage WU before a high value of the line voltage VW, and control can determine this is not a correct sequence, flag an error in step 699 and exit the operation of step 413; if not, control enters step 695. In step 695, control checks the timer to determine if the detection period has lapsed; if not, control returns to step 683; if yes, control has not detected either the line voltage VW or the line voltage WU in the detection period, and thus control flags an error in step 699 and exits the operation of step 413.

[0084] Referring to FIG. 6, a logic flow diagram illustrating step 404 in detail is shown. In step 701, control set the selection signal S3 at high for a detection period and detects a peak value of line voltage signal S4 representing the line voltage UV. In step 702, control set the selection signal S2 at high for a detection period and detects a peak value of the line voltage signal S4 representing the line voltage VW. In step 703, control set the selection signal S1 at high for a detection period and detects a peak value of the line voltage signal S4 representing the line voltage WU.

[0085] In step 704, control compares the peak values of the line voltage signal S4 detected for the line voltage UV, the line voltage VW, and the

line voltage WU and determines if a difference between selected two peak values is less than a predetermined tolerance. If the difference exceeds the tolerance, control sends out an error message in step 706 and returns to step 701; if the differences are within the tolerance, control exits step 404

[0086] Referring to FIG. 6A, a logic flow diagram illustrating a general operation of an exemplary implementation of step 414 in detail is shown. The operation shown in FIG. 6A is generally similar to the operation shown in FIG. 6. Instead of sending out an error message in step 706, control can flag an error in step 707 and then exit step 414.

[0087] The description herein is merely exemplary in nature and, thus, variations that do not depart from the gist of that which is described are intended to be within the scope of the disclosure. Such variations are not to be regarded as a departure from the spirit and scope of the disclosure.

CLAIMS

What is claimed is:

1. An apparatus comprising:

a first optocoupler that selectively allows a first current to flow from a first one of a first pair of N power supply lines to a second one of the first pair, wherein the N power supply lines each provide a phase signal, and wherein N is an integer greater than two; and

a control module that controls the first optocoupler and that determines an occurrence of a phase failure of the phase signals based on a first signal, which is based on the first current.

2. The apparatus of claim 1 further comprising second and third optocouplers that selectively allow current to flow between second and third pairs of the N power supply lines, respectively, and wherein the control module controls the second and third optocouplers.

3. The apparatus of claim 2 wherein a plurality of optocouplers includes the first, second, and third optocouplers, wherein the control module deactivates others of the optocouplers when activating one of the optocouplers, and wherein each of the plurality of optocouplers allows current to flow while activated.

4. The apparatus of claim 2 wherein the first signal is based on the first current when the first optocoupler is activated, the first signal is based on a second current flowing from a first one of a second pair of the N power supply lines to a second one of the second pair when the second optocoupler is activated, and the first signal is based on a third current flowing from a first one of a third pair of the N power supply lines to a second one of the third pair when the third optocoupler is activated.

5. The apparatus of claim 1 wherein the phase failure comprises at least one of a phase loss, a phase order reversal, and a phase magnitude imbalance.

6. The apparatus of claim 1 further comprising an output optocoupler that generates the first signal based on a total current including the first current.

7. The apparatus of claim 6 wherein the total current includes second and third currents from second and third optocouplers.

8. An apparatus comprising:

a first optocoupler that selectively allows a first current to flow from a first one of N power supply lines to a second one of the N power supply lines, wherein the N power supply lines each provide a phase signal, and wherein N is an integer greater than two;

a device that allows current to flow from the second one of the N power supply lines to the first one of the N power supply lines and that prevents current from flowing from the first one of the N power supply lines to the second one of the N power supply lines; and

a control module that controls the first optocoupler and that analyzes a first signal, which is based on the first current, to determine a phase failure of the phase signals.

9. The apparatus of claim 8 further comprising:

a second optocoupler that selectively allows a second current to flow from the second one of the N power supply lines to a third one of the N power supply lines; and

a third optocoupler that selectively allows a third current to flow from the third one of the N power supply lines to the first one of the N power supply lines.

10. The apparatus of claim 9 further comprising an output optocoupler that receives a sum of the first, second, and third currents and that generates an output current, wherein the first signal is based on the output current, and wherein the first, second, and third currents are zero when the first, second, and third optocouplers, respectively, are deactivated.

11. The apparatus of claim 10 further comprising N Zener diodes that each allow current flow from the output optocoupler to a node of a respective one of the first, second, and third optocouplers.

12. The apparatus of claim 11 wherein the N Zener diodes each allow current flow from the node of the respective one of the first, second, and third optocouplers to the output optocoupler when a voltage applied to the Zener diode is above a predetermined threshold.

13. The apparatus of claim 9 further comprising N diodes that each allow current flow from a node of a respective one of the first, second, and third optocouplers to a corresponding one of the N power supply lines, wherein the device comprises one of the N diodes.

14. The apparatus of claim 9 further comprising N resistances, each connected between one of the first, second, and third optocouplers and a respective one of the N power supply lines.

15. The apparatus of claim 8 further comprising N varistors, each connected between a respective two of the N power supply lines.

16. An apparatus comprising:

N resistances, wherein N is an integer greater than two;

N switching devices that each have first and second ends and that each selectively electrically connect the first end to the second end, wherein the first ends are coupled to respective ones of N power lines via the N resistances and wherein the second ends are connected to a common node, wherein each of the N power lines carries a power signal having a different one of N phases;

an output device that is connected between the common node and a second node and that generates an output signal based on a current flowing between the common node and the second node;

N unidirectional devices that each allow current to flow from a node at the first end of a respective one of the N switching devices to a corresponding one of the N power lines and that each inhibit current flow toward the first ends; and

a control module that analyzes the output signal to determine a failure of the power signals and that selectively generates N control signals that respectively control the N switching devices.

17. The apparatus of claim 16 further comprising N Zener diodes that each allow current to flow from the second node to the node at the first end of a respective one of the N switching devices and that each selectively inhibit current flow toward the second node.

18. The apparatus of claim 16 wherein each of the N unidirectional devices comprises a diode.

19. The apparatus of claim 16 wherein each of the N switching devices comprises an optocoupler.

20. The apparatus of claim 16 wherein the output device comprises an optocoupler.

21. The apparatus of claim 16 further comprising N varistors that are each connected between two of the N power lines.

22. A method comprising:

receiving N power signals, each having a different one of N phases, over N power supply lines, wherein N is an integer greater than two;

selectively activating a first switch to allow a first current to flow from a first one of the N power supply lines to a second one of the N power supply lines;

generating a signal based on the first current; and

selectively generating a phase failure signal when the signal is less than a predetermined threshold.

23. The method of claim 22 further comprising controlling a motor based on the phase failure signal.

24. The method of claim 23 further comprising halting operation of the motor when the phase failure signal is generated.

25. The method of claim 22 further comprising activating the first switch for a predetermined period of time, wherein the predetermined period is based on a duration of one cycle of one of the N power signals.

26. The method of claim 25 wherein the predetermined period is equal to the duration plus a predetermined value.

27. The method of claim 22 further comprising:

selectively activating a second switch to allow a second current to flow from the second one of the N power supply lines to a third one of the N power supply lines; and

selectively activating a third switch to allow a third current to flow from the third one of the N power supply lines to the first one of the N power supply lines.

28. The method of claim 27 further comprising deactivating remaining ones of the switches when activating one of the first, second, and third switches.

29. The method of claim 28 further comprising sequentially activating the first, second, and third switches.

30. The method of claim 27 further comprising generating the signal based on the first, second, and third currents.

31. The method of claim 30 wherein the signal is proportional to a sum of the first, second, and third currents.

32. The method of claim 30 wherein the first, second, and third currents are zero when the first, second, and third switches, respectively, are deactivated.

33. The method of claim 30 further comprising generating the phase failure signal when a peak value of the signal is less than a predetermined threshold and one of the first, second, and third switches is activated.

34. The method of claim 33 further comprising generating the phase failure signal when the peak value of the signal over a predetermined period is less than the predetermined threshold.

35. The method of claim 30 further comprising:

determining a first peak value of the signal when the first switch is activated;

determining a second peak value of the signal when the second switch is activated;

determining a third peak value of the signal when the third switch is activated; and

generating the phase failure signal when a difference between the first, second, and third peak values is greater than a predetermined limit.

36. The method of claim 30 further comprising:

activating the first switch;

comparing the signal to a threshold value while the first switch is activated;

after the signal exceeds the threshold value, alternately activating the second switch and the third switch;

comparing the signal to the threshold value while the second switch is activated and while the third switch is activated; and

generating the phase failure signal when the signal exceeds the threshold value while the third switch is activated prior to the signal exceeding the threshold value while the second switch is activated.

37. The method of claim 30 further comprising:

activating the first switch;

comparing the signal to a threshold value while the first switch is activated;

after the signal exceeds the threshold value, alternately activating the second switch and the third switch;

determining a first time at which the signal exceeds the threshold value while the second switch is activated;

determining a second time at which the signal exceeds the threshold value while the third switch is activated; and

generating the phase failure signal when the first time is after the second time.

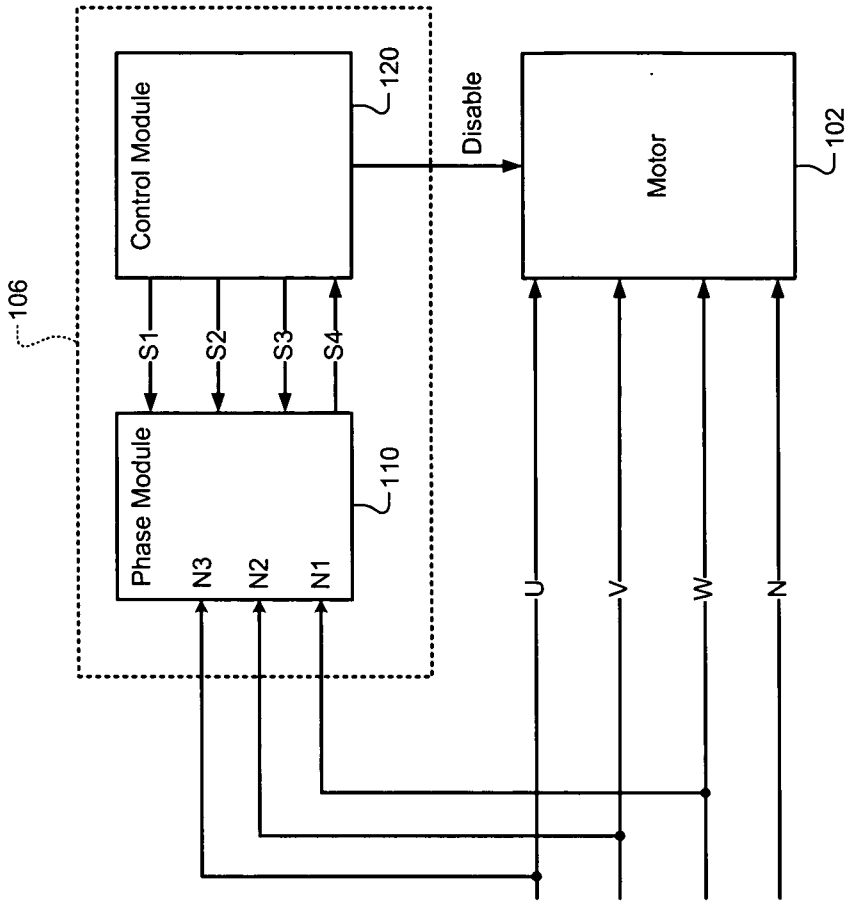


FIG. 2

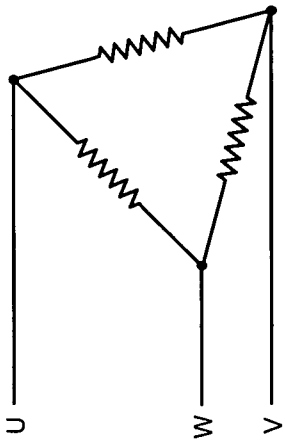


FIG. 1
Prior Art

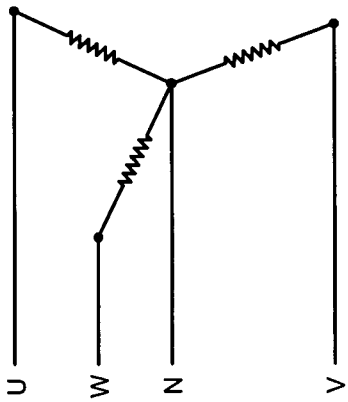


FIG. 1A
Prior Art

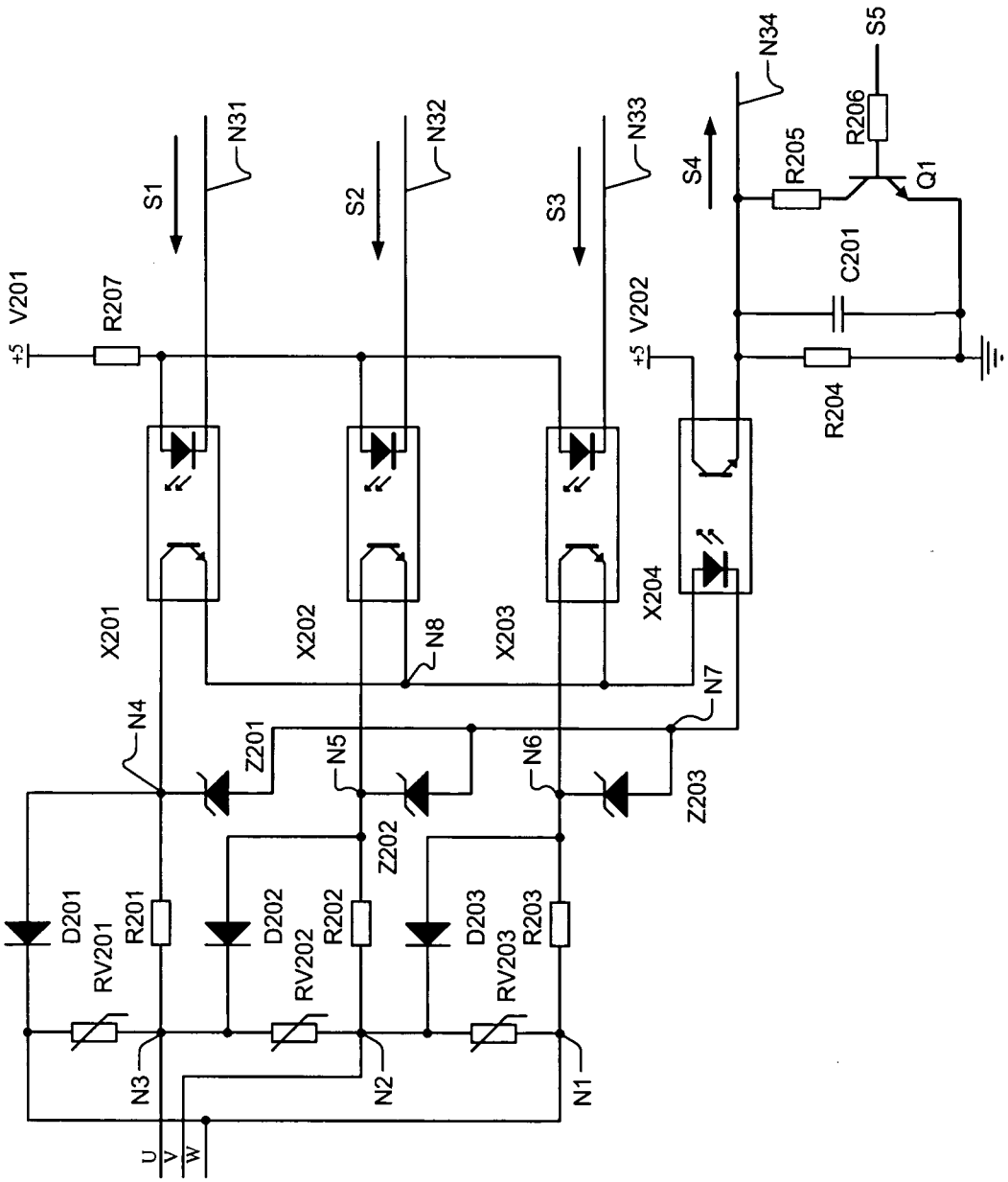

S1
S2
S3
S4
S5
N31
N32
N33
N34
V201
+5
R207
V202
+5
R205
R206
Q1
C201
R204
X201
X202
X203
X204
N8
N7
N4
N5
N6
Z201
Z202
Z203
D201
D202
D203
R201
R202
R203
RV201
RV202
RV203
N3
N2
N1
U
V
W

FIG. 2A

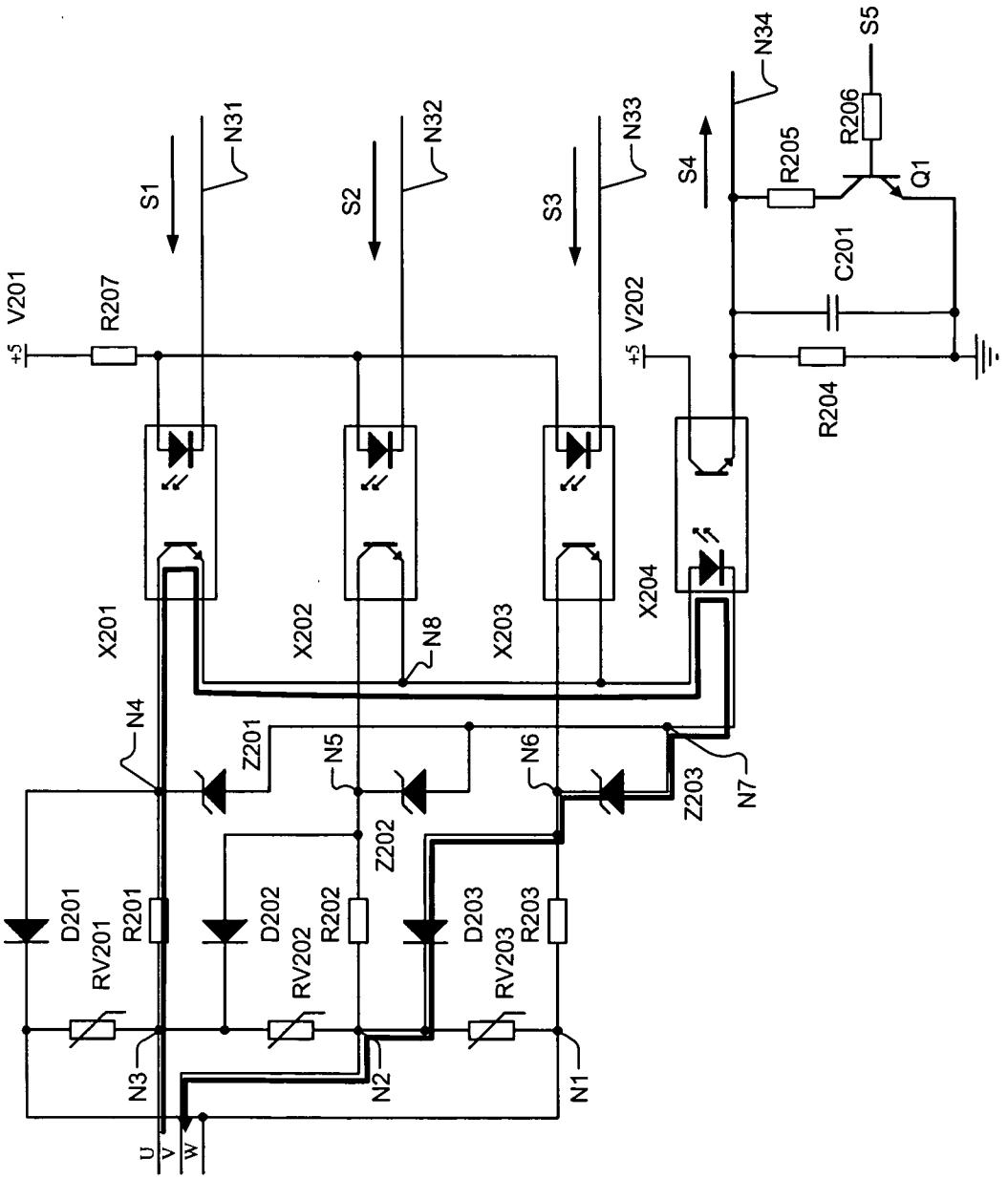

S1
S2
S3
S4
S5
N31
N32
N33
N34
V201
V202
+5
R207
R205
R206
Q1
C201
R204
X201
X202
X203
X204
N8
N4
N5
N6
N7
Z201
Z202
Z203
D201
D202
D203
R201
R202
R203
RV201
RV202
RV203
N3
N2
N1
U
V
W

FIG. 2B

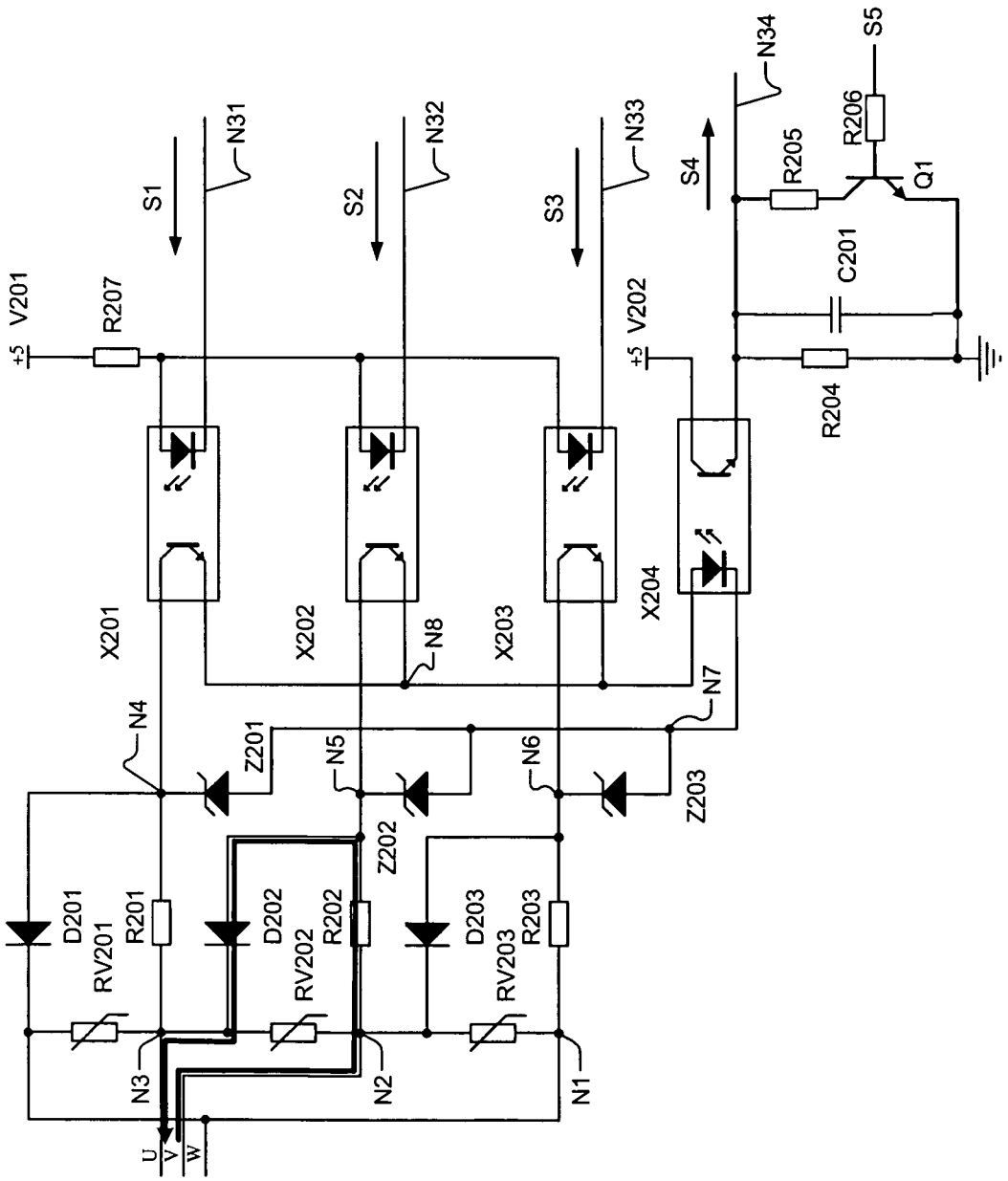

+5
V201
R207
S1
N31
S2
N32
S3
N33
S4
N34
S5
R205
R206
Q1
C201
V202
R204
X201
X202
X203
X204
N8
N7
N4
N5
N6
Z201
Z202
Z203
D201
RV201
R201
D202
RV202
R202
D203
RV203
R203
N3
N2
N1
U
V
W

FIG. 2C

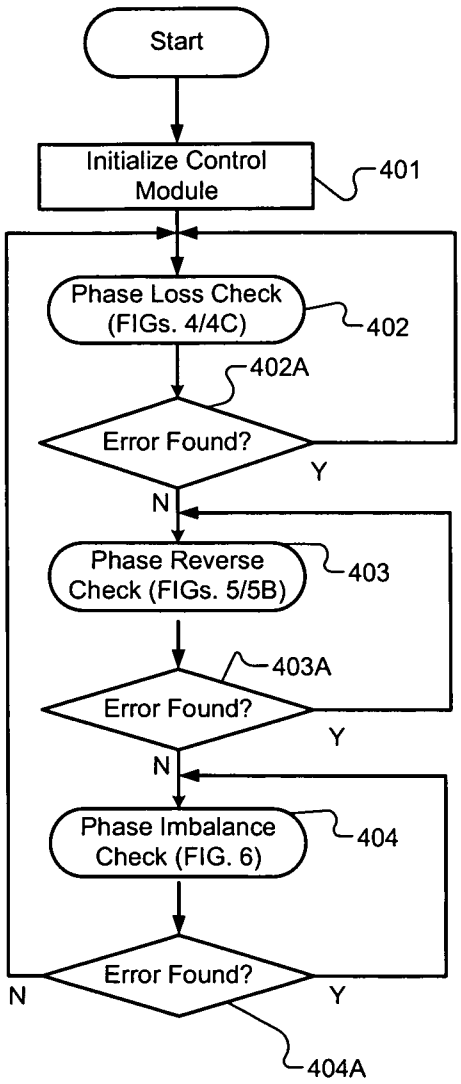

Start
Initialize Control Module
401
Phase Loss Check (FIGs. 4/4C)
402
402A
Error Found?
Y
N
Phase Reverse Check (FIGs. 5/5B)
403
403A
Error Found?
Y
N
Phase Imbalance Check (FIG. 6)
404
Error Found?
N
Y
404A

FIG. 3

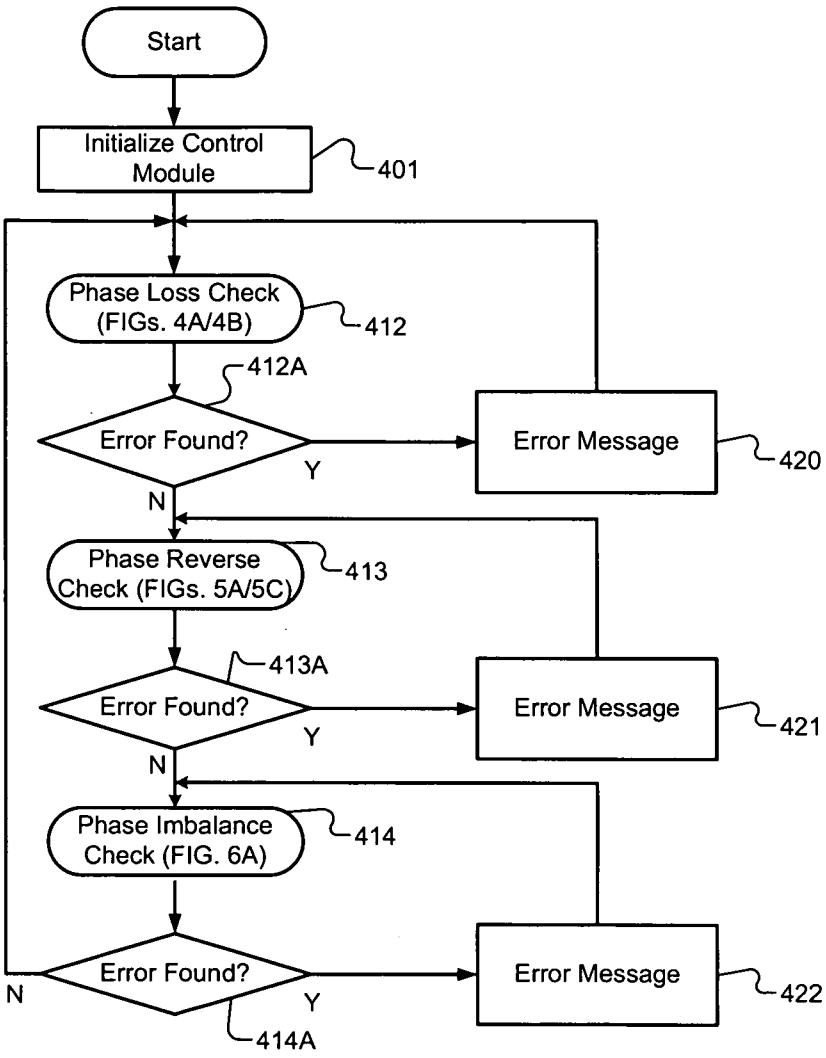

Start
Initialize Control Module
401
Phase Loss Check (FIGs. 4A/4B)
412
412A
Error Found?
Y
Error Message
420
N
Phase Reverse Check (FIGs. 5A/5C)
413
413A
Error Found?
Y
Error Message
421
N
Phase Imbalance Check (FIG. 6A)
414
Error Found?
N
Y
Error Message
422
414A

FIG. 3A

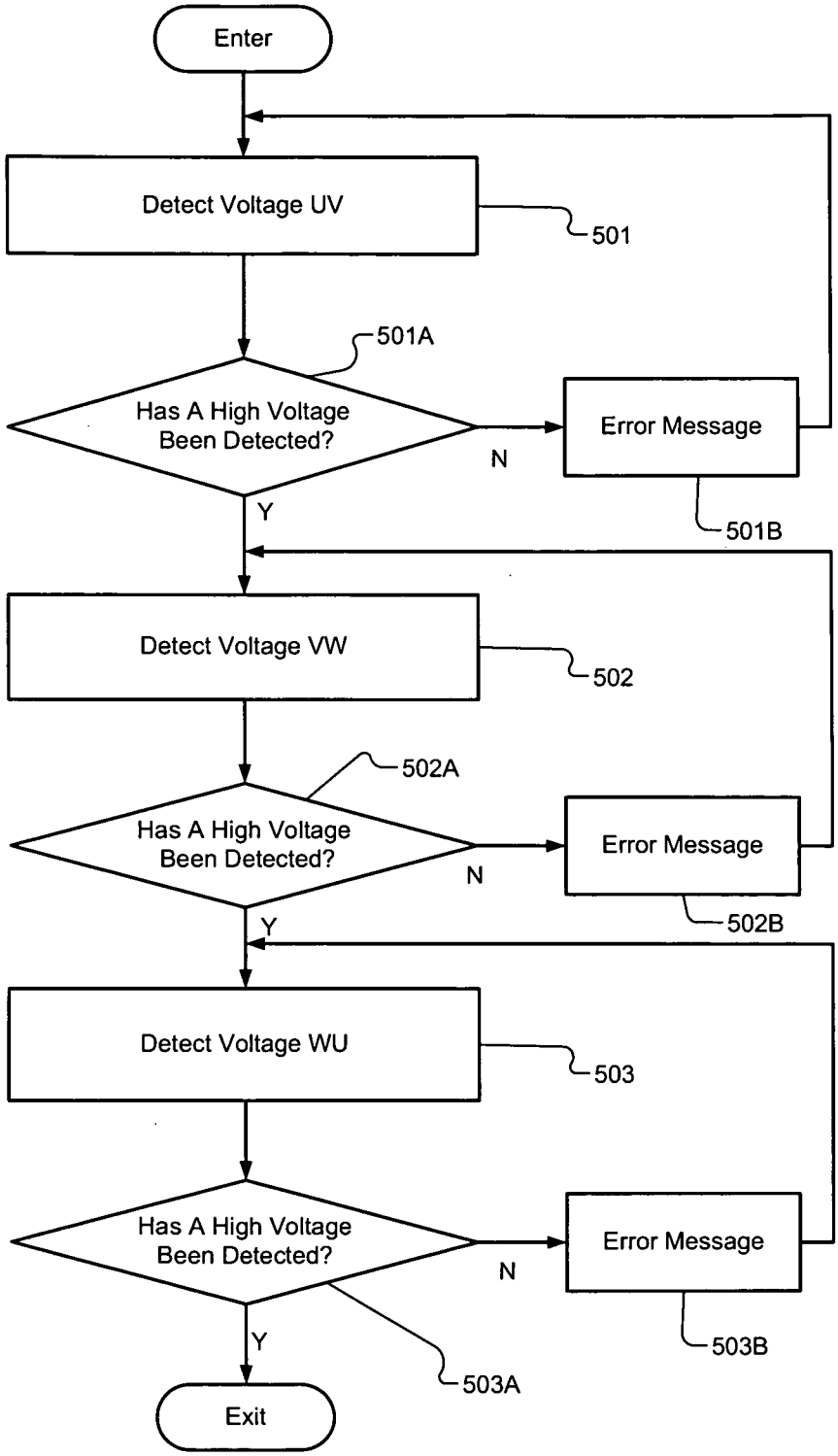

Enter
Detect Voltage UV
501
501A
Has A High Voltage Been Detected?
N
Error Message
501B
Y
Detect Voltage VW
502
502A
Has A High Voltage Been Detected?
N
Error Message
502B
Y
Detect Voltage WU
503
Has A High Voltage Been Detected?
N
Error Message
503B
Y
503A
Exit

FIG. 4

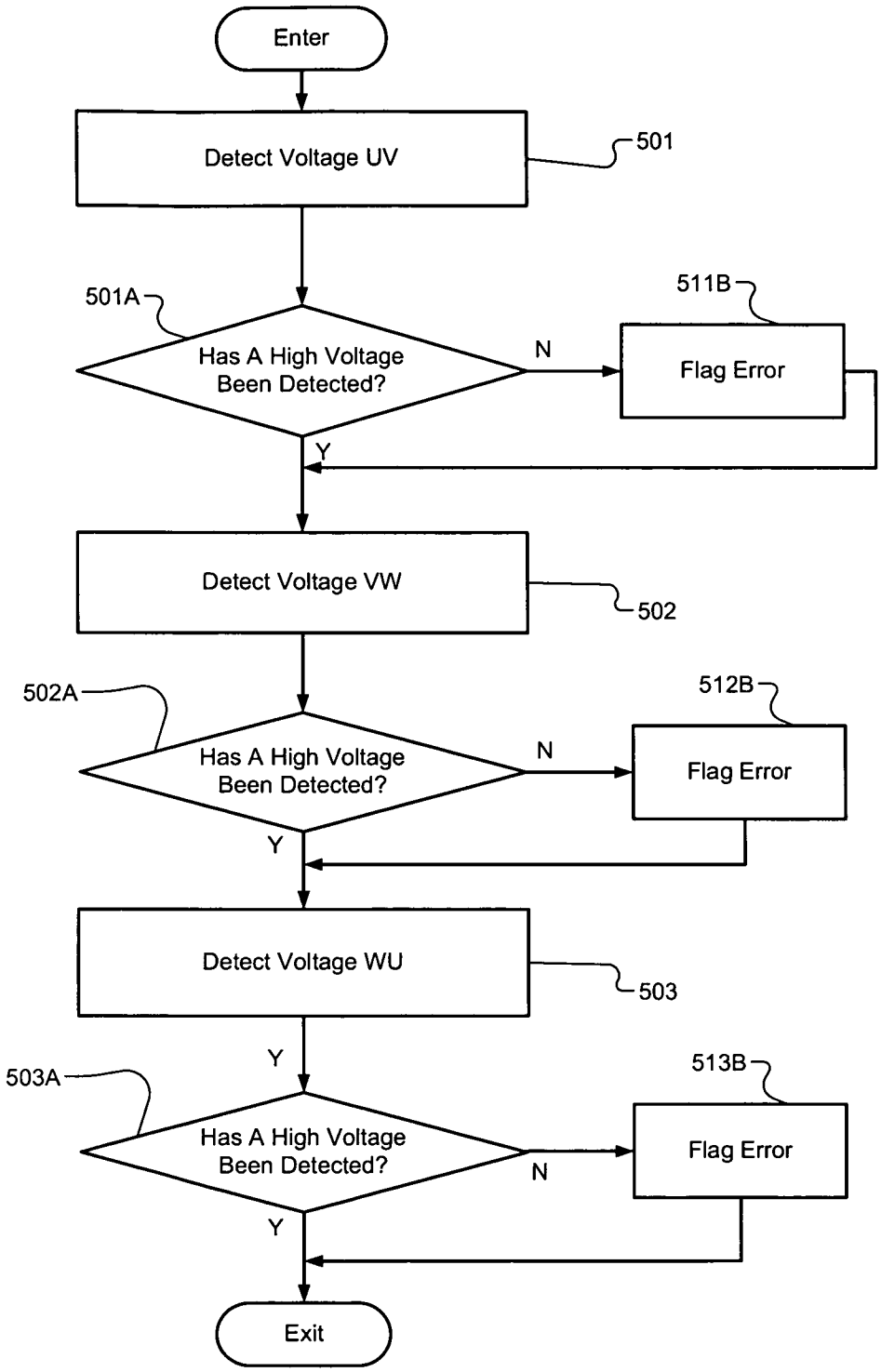

Enter
Detect Voltage UV
501
501A
Has A High Voltage Been Detected?
N
511B
Flag Error
Y
Detect Voltage VW
502
502A
Has A High Voltage Been Detected?
N
512B
Flag Error
Y
Detect Voltage WU
503
Y
503A
Has A High Voltage Been Detected?
N
513B
Flag Error
Y
Exit

FIG. 4A

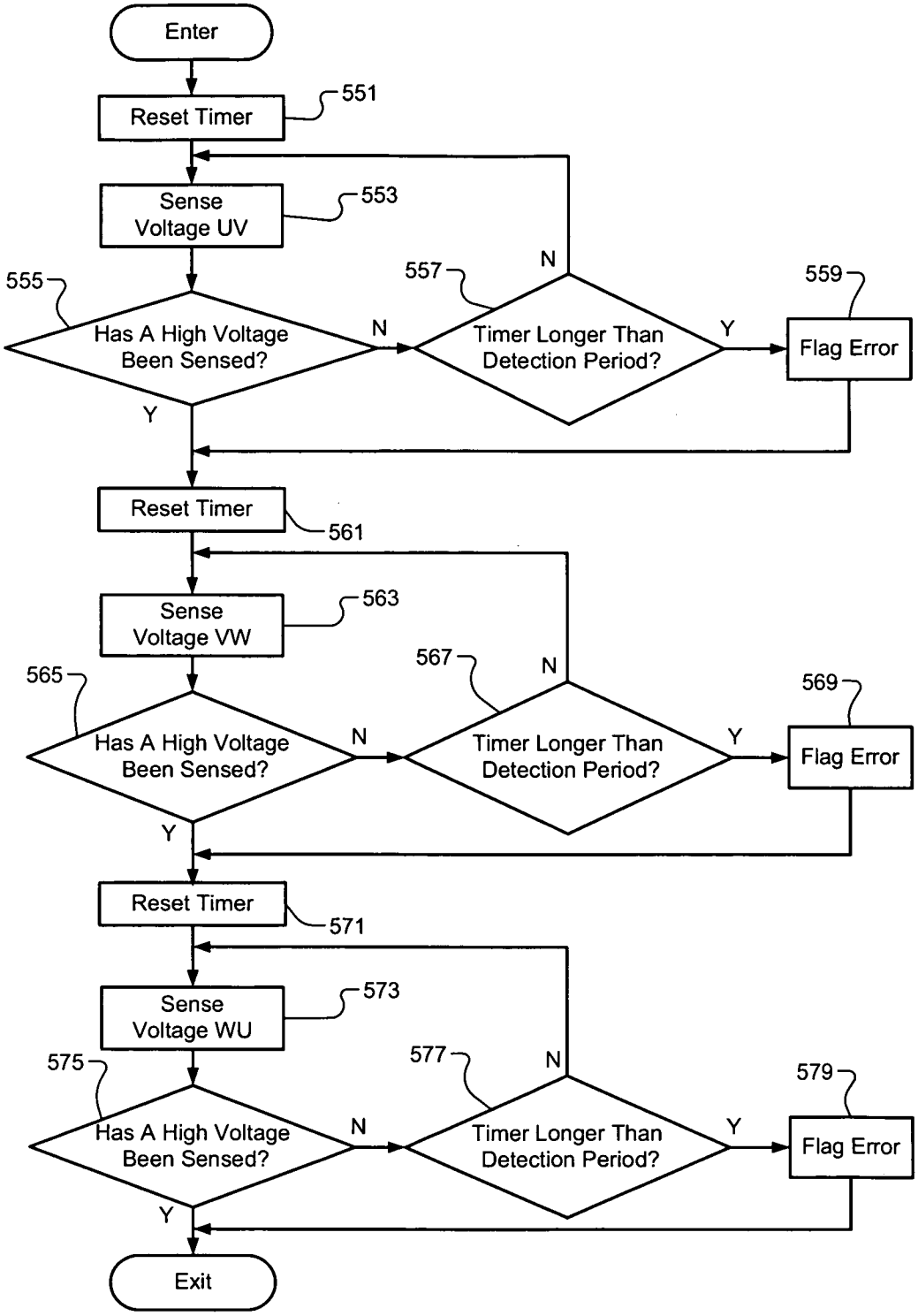

Enter
Reset Timer
551
Sense Voltage UV
553
555
Has A High Voltage Been Sensed?
N
557
Timer Longer Than Detection Period?
N
Y
559
Flag Error
Y
Reset Timer
561
Sense Voltage VW
563
565
Has A High Voltage Been Sensed?
N
567
Timer Longer Than Detection Period?
N
Y
569
Flag Error
Y
Reset Timer
571
Sense Voltage WU
573
575
Has A High Voltage Been Sensed?
N
577
Timer Longer Than Detection Period?
N
Y
579
Flag Error
Y
Exit

FIG. 4B

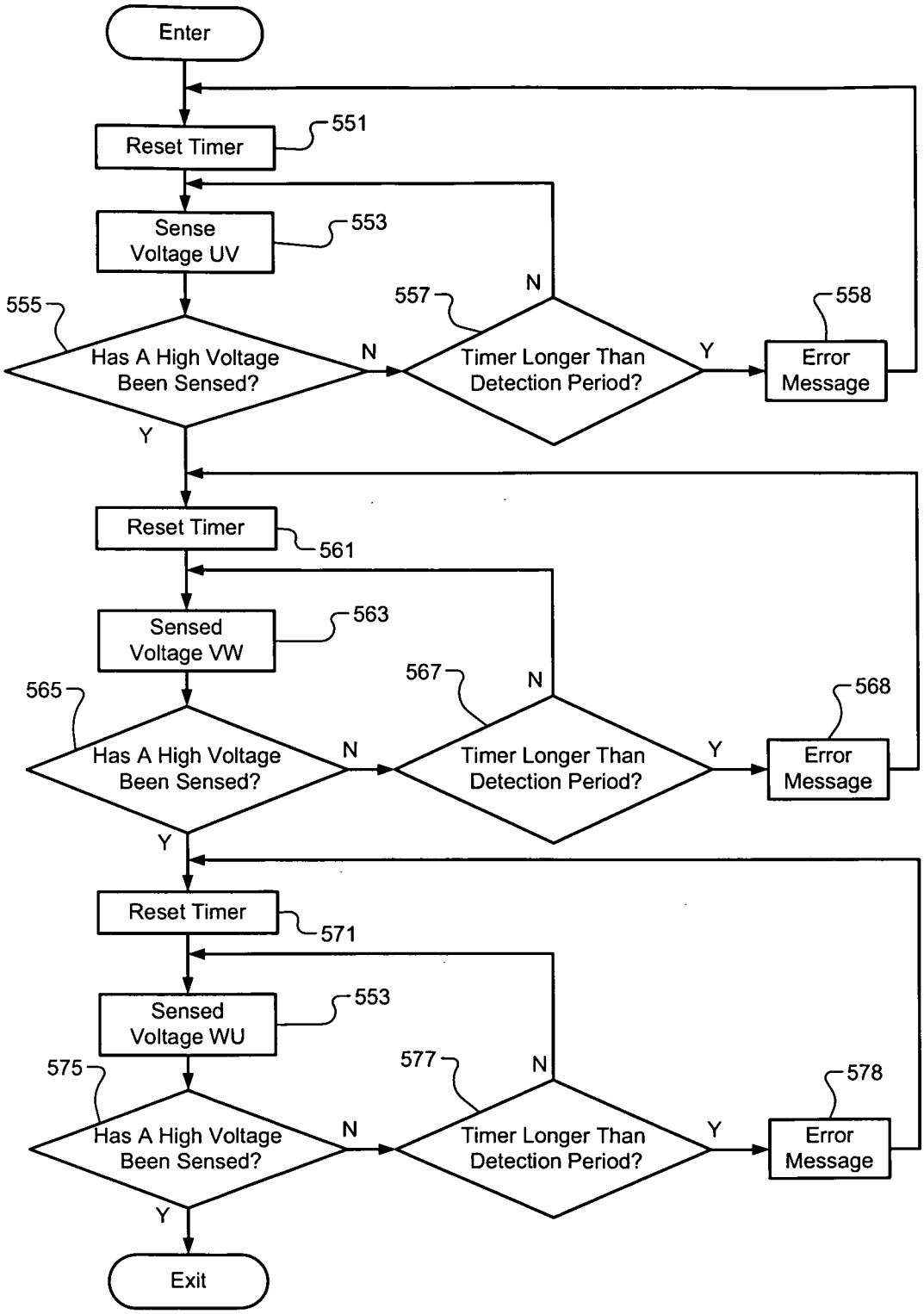

Enter
Reset Timer
551
Sense Voltage UV
553
555
Has A High Voltage Been Sensed?
N
557
Timer Longer Than Detection Period?
N
Y
558
Error Message
Y
Reset Timer
561
Sensed Voltage VW
563
565
Has A High Voltage Been Sensed?
N
567
Timer Longer Than Detection Period?
N
Y
568
Error Message
Y
Reset Timer
571
Sensed Voltage WU
553
575
Has A High Voltage Been Sensed?
N
577
Timer Longer Than Detection Period?
N
Y
578
Error Message
Y
Exit

FIG. 4C

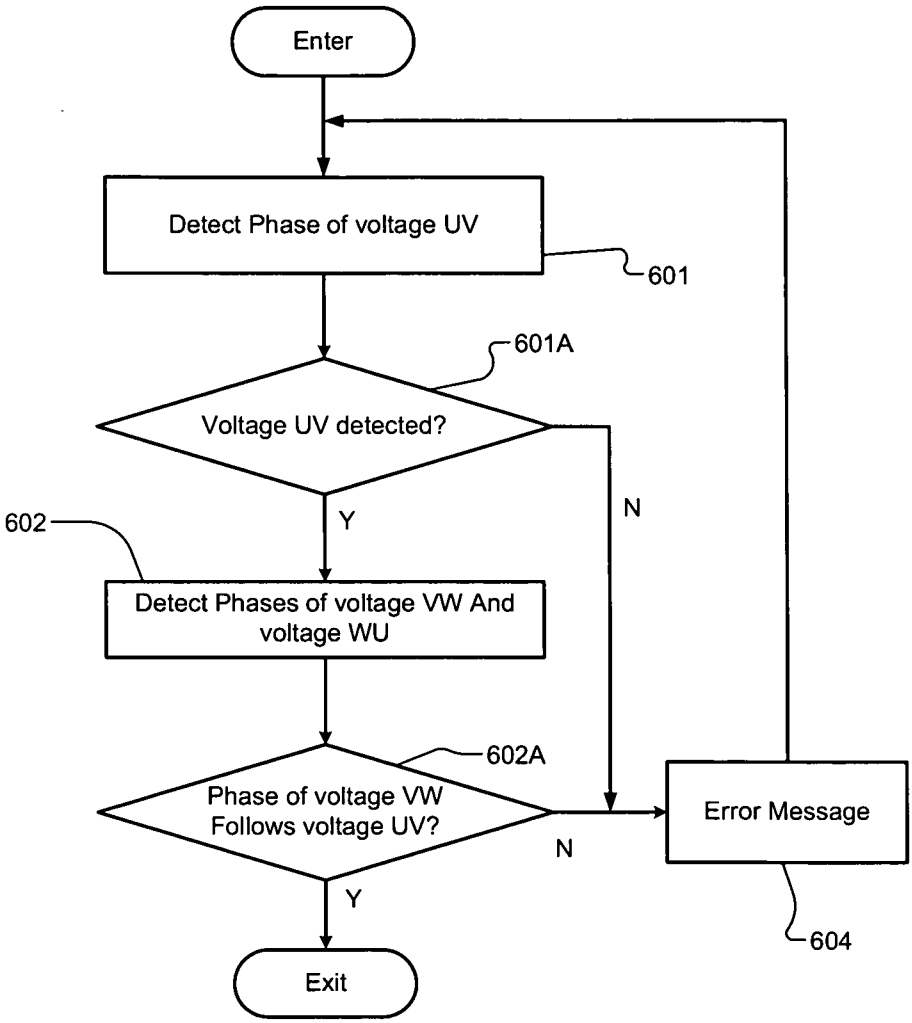

Enter
Detect Phase of voltage UV
601
601A
Voltage UV detected?
N
Y
602
Detect Phases of voltage VW And voltage WU
602A
Phase of voltage VW Follows voltage UV?
N
Error Message
Y
604
Exit

FIG. 5

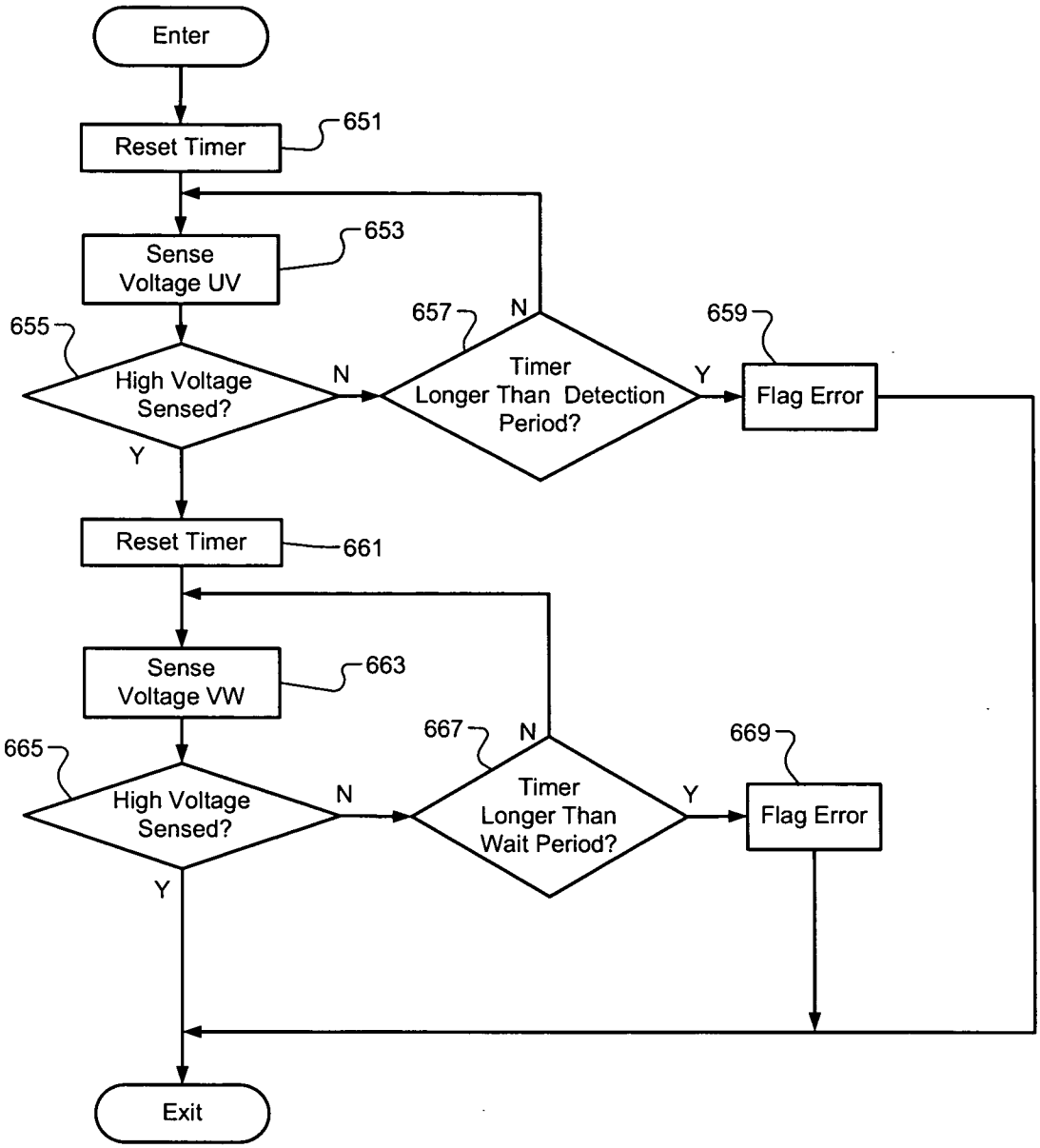

Enter
Reset Timer
651
Sense Voltage UV
653
655
High Voltage Sensed?
N
657
N
Timer Longer Than Detection Period?
Y
659
Flag Error
Y
Reset Timer
661
Sense Voltage VW
663
665
High Voltage Sensed?
N
667
N
Timer Longer Than Wait Period?
Y
669
Flag Error
Y
Exit

FIG. 5A

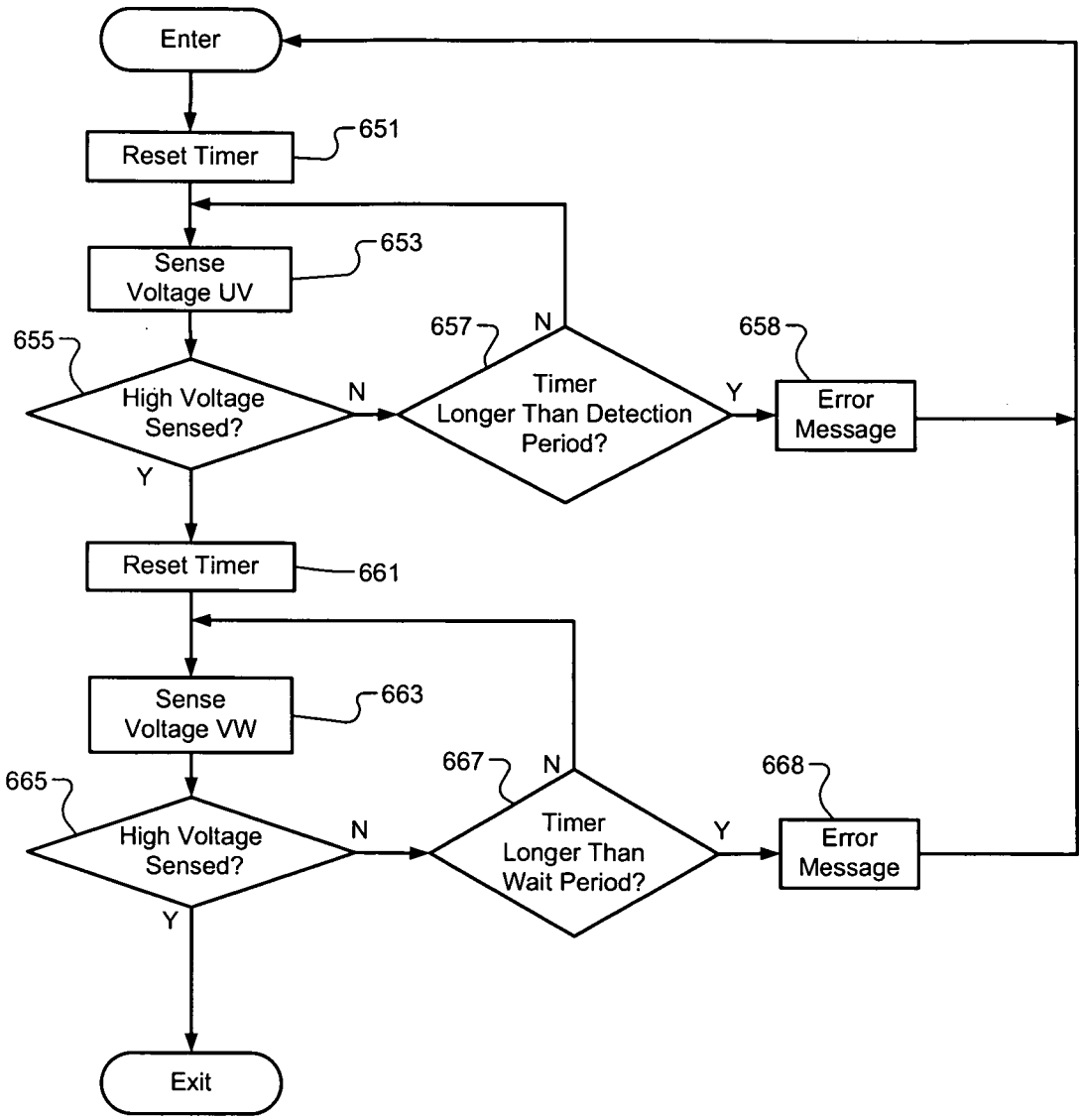

Enter
Reset Timer
651
Sense Voltage UV
653
655
High Voltage Sensed?
N
Y
657
N
Timer Longer Than Detection Period?
Y
658
Error Message
Reset Timer
661
Sense Voltage VW
663
665
High Voltage Sensed?
N
Y
667
N
Timer Longer Than Wait Period?
Y
668
Error Message
Exit

FIG. 5B

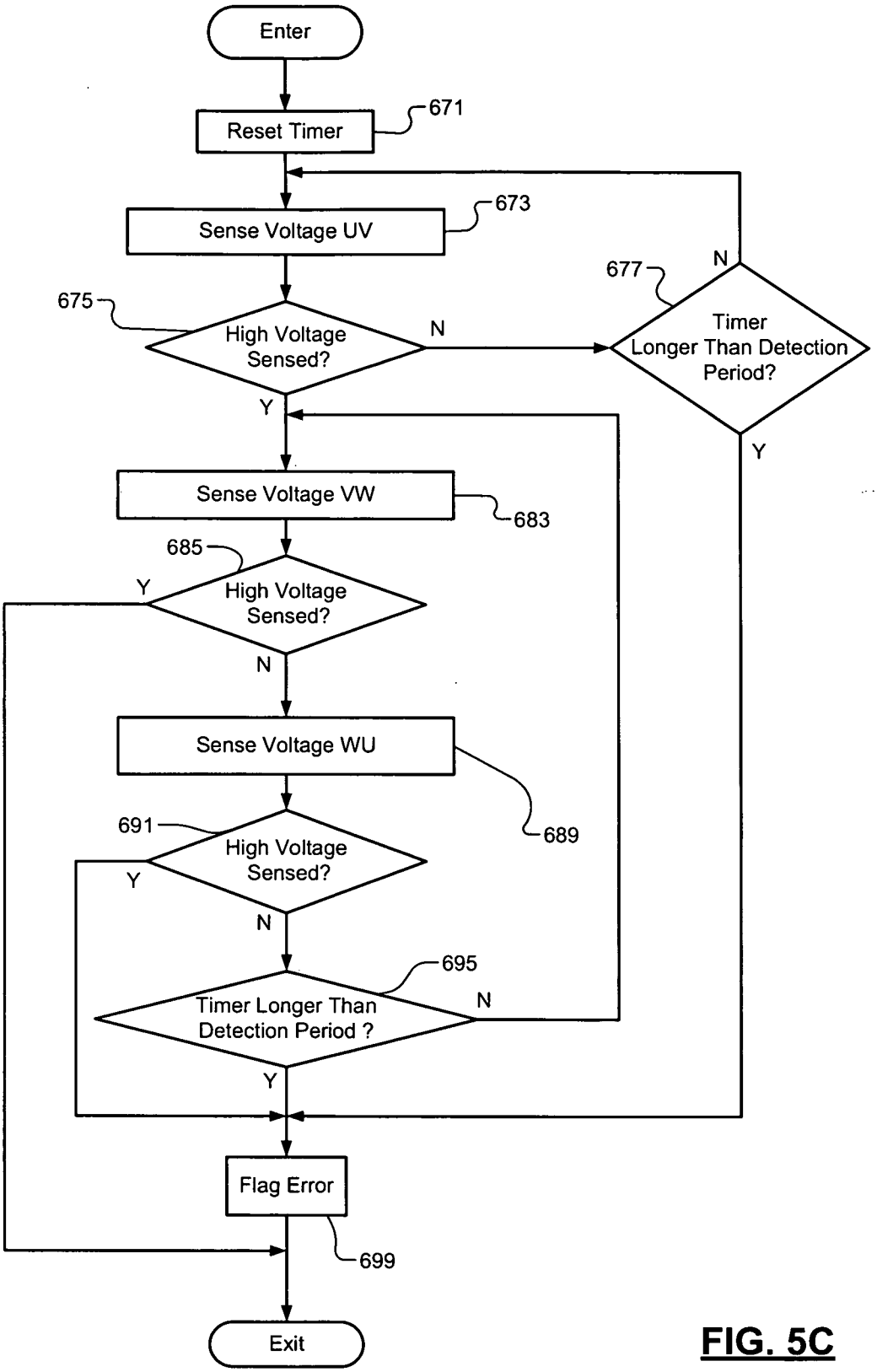

Enter
Reset Timer
671
Sense Voltage UV
673
675
High Voltage Sensed?
N
677
Timer Longer Than Detection Period?
N
Y
Y
Sense Voltage VW
683
685
High Voltage Sensed?
Y
N
Sense Voltage WU
689
691
High Voltage Sensed?
Y
N
695
Timer Longer Than Detection Period ?
N
Y
Flag Error
699
Exit

FIG. 5C

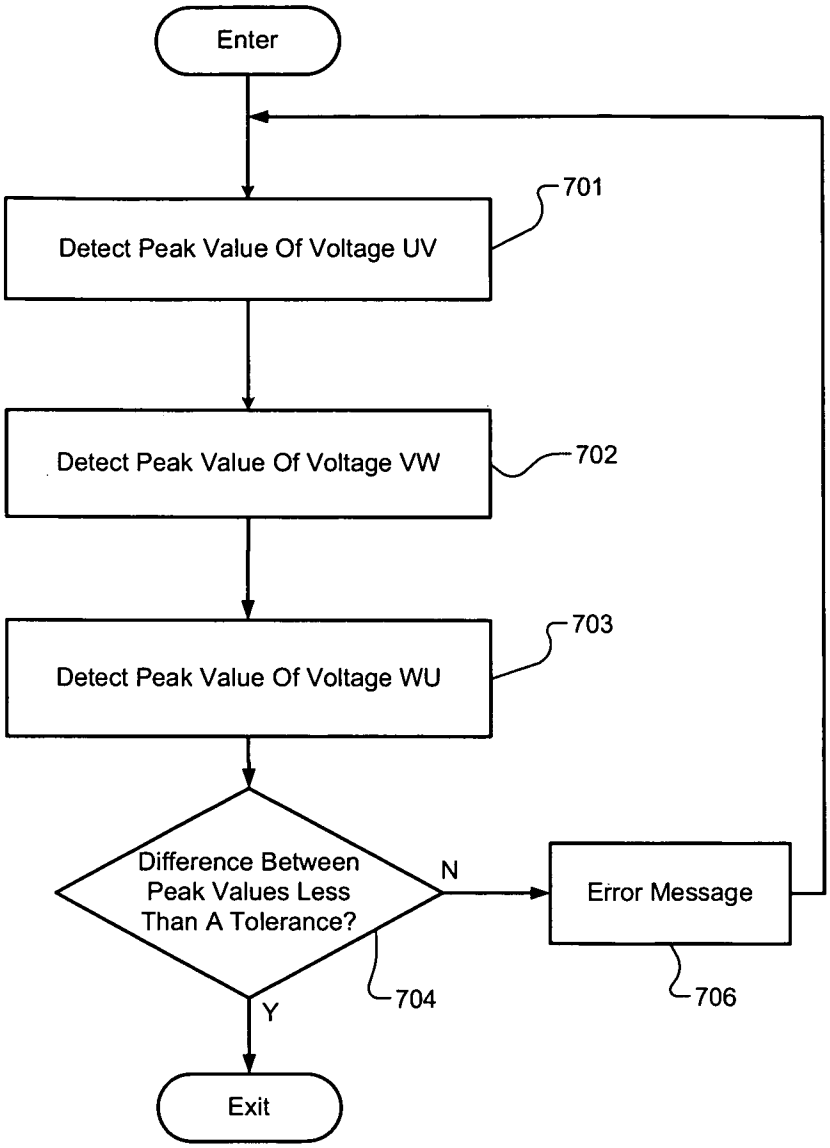

Enter
Detect Peak Value Of Voltage UV
701
Detect Peak Value Of Voltage VW
702
Detect Peak Value Of Voltage WU
703
Difference Between Peak Values Less Than A Tolerance?
N
Error Message
704
706
Y
Exit

FIG. 6

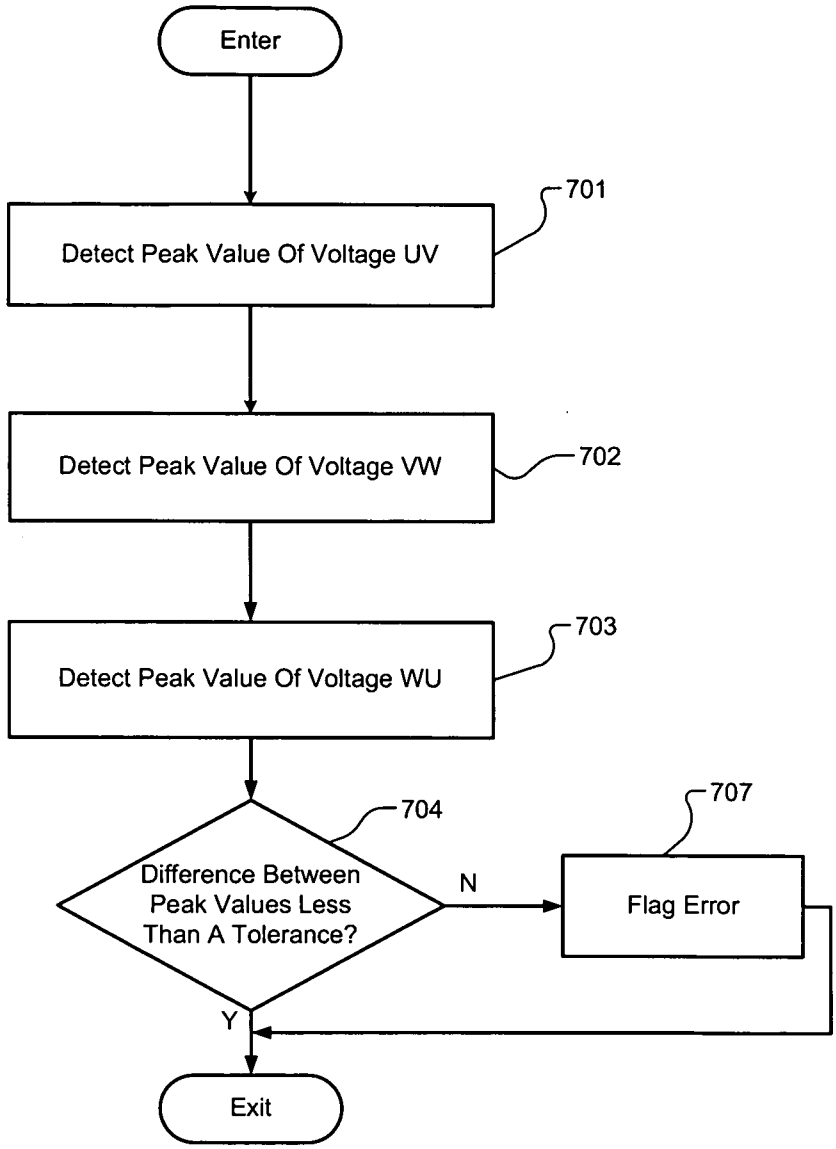

Enter
701
Detect Peak Value Of Voltage UV
702
Detect Peak Value Of Voltage VW
703
Detect Peak Value Of Voltage WU
704
Difference Between Peak Values Less Than A Tolerance?
N
707
Flag Error
Y
Exit

FIG. 6A