

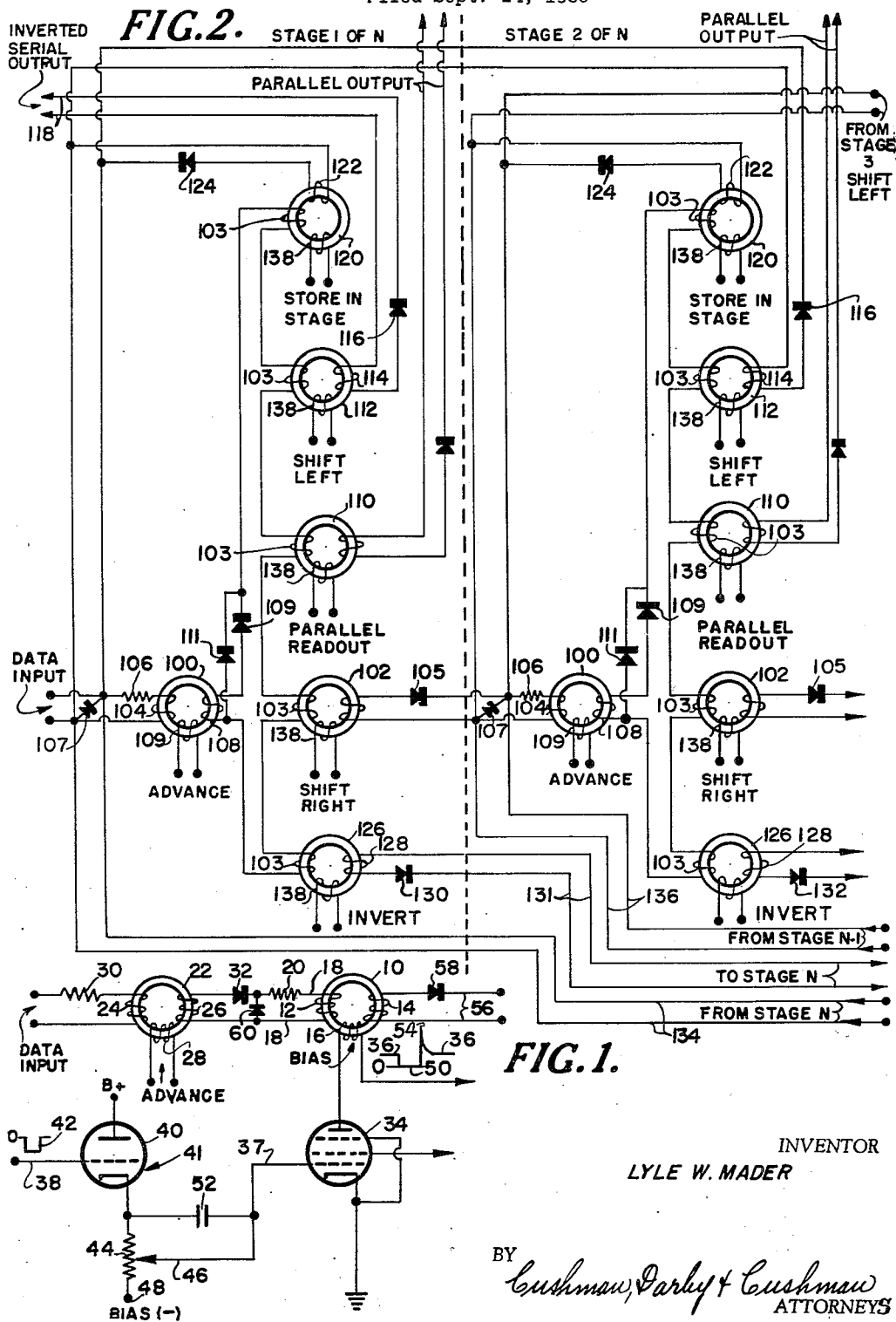
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MAGNETIC CORE DEVICES

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MAGNETIC CORE DEVICES

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This invention relates to magnetic devices which utilize the hysteresis characteristic of magnetic materials as means for switching or gating data and the like in a shifting register.

The value of saturable reactors comprised of suitably wound small cores of ferromagnetic material as storage and logical elements in electronic data handling systems is being increasingly recognized, particularly because of their miniature size, low power requirements, dependability and their ability to retain stored information for long periods of time in spite of power failure. The cores of such reactor elements are able to store binary information in the form of residual magnetization after the cores are magnetized to saturation in either of two directions. The saturation can be achieved by passing either a constant direct current or a pulse current through a winding on the core. When a current is applied to a winding on the core to create a magnetomotive force in the sense opposite to the pre-existing flux direction, the core is driven to saturation in the opposite polarity, provided that the magnetomotive force exceeds a certain critical value. The total change in flux accompanying this shift in flux direction occurs in a relatively short time, thereby inducing a sizable voltage pulse across any winding on the core, which pulse may be utilized to drive other saturable reactor elements to saturation in a predetermined polarity or in a variety of other ways. On the other hand, magnetizing pulses applied to a saturable reactor element which drive it further into saturation in the same direction as that of the residual flux produce a change in flux which is small compared to that created in reversing the flux polarity and so induce correspondingly small voltage pulses in windings on the core.

In order to achieve a large ratio between the voltage pulses induced when a saturable magnetic reactor element is driven to the opposite polarity as compared to that obtained when driving it to saturation in its original polarity, its core material is preferably one having at least a quasi-rectangular hysteresis characteristic so that the residual flux density is a relatively large percentage of the flux density present during the application of a saturating magnetomotive force. A number of suitable magnetic materials are available such as Deltamax, ultrathin 4-79 Permalloy and ferromagnetic ferrites. In order to improve high-frequency response by reducing eddy current losses, metallic ferro-alloys are preferably used in thin strips which may be wrapped around ceramic spools while ferrite cores may be molded and windings placed directly thereon, inasmuch as ferrites are relatively free from eddy current effects.

The core of a saturable reactor element may be held in one direction of residual magnetization by subjecting it to a continuous magnetomotive force in the pre-existing flux direction such as that produced by passing a direct current through a winding on the core. This biasing current may be readily adjusted so that the maximum magnetomotive force created by an information or data sig-

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nal is insufficient to both balance out the biasing magnetomotive force and to switch the element to the opposite polarity. Normally, the biasing current will retain the magnetization of a saturable reactor element in the polarity arbitrarily designated as the binary digit "00." The opposite polarity of the residual magnetization of such a core will be referred to as the "1" state. Removal of the biasing current for a definite interval then allows the element either to be switched to the state of opposite polarity, designated as the "1" state, or held in the "0" state according to the information applied thereto during that interval. Following this interval the information is read out by reapplying the bias, assuming that such reapplication creates a sufficient magnetomotive force to switch the core of the element, if necessary, back to the "0" state. This is conveniently accomplished by reapplying the bias in a manner such that a surge of current results. Consequently, the saturable reactor element may function as a binary gate which blocks the flow of information until the biasing current is momentarily removed to allow one digit of binary information to be stored in its core. Reapplication of the bias induces a voltage in an output winding on the core indicative of the digit stored.

Since current required to shift the magnetic core of the saturable reactor element is comparatively small, several saturable reactors may be driven by the output of one saturable reactor, and in this manner a multi-functioning stage of a shifting register may be built. That is, one of the driven saturable reactors may be utilized to shift the data presented thereto to a succeeding and like stage of the register, a second saturable reactor may shift the data to a preceding stage, a third saturable reactor may provide read out of the data in the stage, a fourth saturable reactor may re-store the information within its stage, and a fifth saturable reactor may be provided for each stage to shift the contents of the register end for end.

It is accordingly an object of this invention to provide novel means for gating digital information or data in a shifting register by using saturable reactor elements.

Normally in the use of saturable reactor elements as gates, two separate sources of control are required, one to allow information to be advanced into the gate and a second to drive the information out. It is accordingly an object of this invention to provide each stage of a multi-stage shifting register with magnetic gates each of which utilizes a single source of bias both to control the passage of information and to provide means for advancing the information out in a usable form.

Information may be accepted by a magnetic gate embodying the principles of this invention in the form of a relatively small current compared to the amplitude of the current surge. An object of this invention is then to provide each stage of a shifting register with magnetic gates which incidentally may act as amplifiers and as storage devices.

It is another object of this invention to provide a shifting register comprised of saturable reactor elements in which the stored information may be so gated as to be held in place, inverted, advanced in either direction, or read out in parallel.

These and other objects of the invention will be apparent and best understood from the following description and claims when considered in connection with the exemplary drawings, in which:

Figure 1 is a schematic diagram illustrating the basic principles of gating information through a single stage, dual element, saturable reactor shifting register in the practice of this invention; and

Figure 2 is a schematic diagram of two of N stages of a novel shifting register which is capable of shifting

data serially in either direction, holding the data in place, inverting it or gating the data out in parallel.

The cores of the saturable reactor elements are shown in the drawings to be toroidal in shape. However, the shape of the cores is not critical so long as adequate coupling is achieved between the core and its windings. Toroidal cores are especially satisfactory in this respect, and incidentally produce a minimum external field. Each reactor which functions as a magnetic gate in the practice of this invention is provided with a data receiving input winding, an output winding, and a control winding. When these windings are connected to windings on other magnetic cores in a circuit, unidirectional impedance devices such as semi-conducting diodes are included in the connecting leads to serve a dual purpose of preventing signals from being transmitted from the input windings of one saturable reactor element to the output winding of another element or from being transmitted from the output winding of an element when that element is being switched from a given state of remanent magnetization to the opposite polarity.

Referring now to Figure 1, wherein there is illustrated the basic components of a shifting register according to the invention, there is shown a toroidal-shaped saturable reactor element 10 which is provided with an input winding 12, an output winding 14, and a control winding 16. The input winding 12 is connected by lines 18 via resistor 20 and diode 32 to a source of data such as saturable reactor element 22. Reactor 22 also has an input winding 24, an output winding 26 and a control winding 28, with the input winding 24 being connected via resistor 30 to a source of data (not shown) represented by the presence or absence of current pulses. Upon the presentation of a current pulse representing a binary digit "1" to winding 24, the core of reactor 22 will be shifted to its arbitrarily designated "0" state. However, winding 26 will not provide an output to winding 12 of the saturable reactor 10 since diode 32 is orientated to allow substantial current flow only in a direction opposite that tended to be induced in winding 26 by a change of the core to its 0 magnetization state. Diode 32 will, however, allow current to flow to winding 12 when an "advance" pulse is applied to control winding 28 to switch the state of the core of reactor 22 to its 1 polarity. In the practice of this invention advance pulses are applied to winding 28 periodically and in an interlaced fashion with the data pulses to winding 24.

The control winding 16 of saturable reactor 10 is connected to a source of bias such as tube 34 so that reactor 10 is normally biased to an arbitrarily designated 0 magnetization state. In order to shift reactor 10 to its opposite 1 state, the amplitude on bias winding 16 must be reduced, preferably to zero, since the magnitude of the bias from tube 34 is made sufficient to counteract any input on winding 12. The bias may be completely interrupted by connection of winding 16 in series with the plate circuit of biasing tube 34 which is normally conducting to cause a biasing current 36 to flow. In an actual embodiment, a steady biasing current 36 of 25 milliamperes was found sufficient to prevent signals arriving on lines 18 from switching the state of element 10, assuming that element 10 is initially magnetized to its 0 state. Biasing tube 34 is controlled by the level of potential on lead 37 which in turn is controlled by the potential on the grid lead 38 of tube 40. If tube 40 is initially conducting, a negative voltage (e. g. pulse 42) on lead 38 will cut it off and cause the voltage drop across the resistance of potentiometer 44 to reduce so that the movable arm 46, regardless of its position on the resistance of potentiometer 44, will assume a negative potential with respect to ground because of the negative bias applied at terminal 48. Therefore, line 37 and the potential of the control grid of tube 34 will become negative and cut off tube 34 as illustrated in the waveform at 50. By removing the negative pulse on lead 38, tube 40

of the cathode follower circuit 41 again becomes conducting, thereby causing the potential of line 37 to go positive so that a current again flows through control winding 16. However, a coupling condenser 52 between the cathode of tube 40 and the control grid of tube 34 causes a sharp leading edge to the plate current pulse 54 from tube 34 when tube 34 is brought to conduction. This surge of current 54 may be several times the amplitude of the steady biasing current, and thus it can apply sufficient magnetomotive force to saturable reactor element 10 to switch its magnetization state after which the steady state biasing current 36 again takes over to hold element 10 in that same state until its subsequent removal allows data arriving on lines 18 to again change the state of element 10. It will be appreciated by those familiar with the art that the amplitude and duration of the current surge on line 37, and therefore of pulse 54, is dependent upon the RC time constant of capacitor 52 and potentiometer 44 and so can be varied by adjusting the latter. It has been found that a current surge 54 of 75 milliamperes is satisfactory. Diode 60 shunts lines 18 so that any current induced in winding 12 by the current surge 54 in winding 16 is prevented from affecting the state of the core of reactor 22.

It follows that in the circuit of Figure 1, saturable reactor 22 is a storage element and saturable reactor 10 is a gating element for the transfer of data from storage element 22 to the output line 56 of element 10 according to the voltage on lead 38. Suppose that the static residual magnetization of element 10 is initially in that state arbitrarily designated to correspond to the binary digit "0" and that biasing tube 34 is conducting to cause current to flow through winding 16 such that the magnetomotive force created thereby is in that same direction as the vector representing the aforementioned residual magnetization. Assuming that the biasing current through winding 16 is sufficiently large, data signals on lines 18 cannot cancel the bias, and element 10 remains in the 0 state until a negative potential is applied at lead 38. This cuts off the biasing current 36 and allows a signal of the proper polarity on lines 18 to switch the element 10 to the 1 state. However, no output appears on line 56 since diode 58 is orientated to prevent a substantial output therefrom. Removal of the negative potential from lead 38 produces a current surge 54 through winding 16 which drives the element 10 back to the 0 state to induce a relatively large voltage across winding 14 for producing a pulse of current through diode 58 to line 56. Of course, if no signal is applied to lines 18, or if the polarity of the signal is such that element 10 is driven further into its 0 state, reapplication of the bias from tube 34 produces a negligible voltage across winding 14, assuming that element 10 is of fabricated material characterized by a generally rectangular hysteresis loop.

The circuit of Figure 1 not only possesses gating action but incidentally may act as an amplifier. Information or data signals on lines 18 may be of minimum amplitude, just sufficient to switch the state of saturable reactor 10, while tube 34 may be driven hard to cause a relatively large pulse to appear on line 56. Accordingly, the output on line 56 may be used directly without further amplification whereas an amplifier is usually required in the output of most electronic gates. It should be noted that a large number of saturable reactor elements may be included in the plate circuit of biasing tube 34 if it is desired to control the gating action of such elements uniformly.

Reference is now made to Figure 2 in which the serial shifting register illustrated in Figure 1 is improved to form a multi-stage shifting register capable of shifting data serially in either direction, re-storing the data in each of its stages while the data is being otherwise utilized, inverting the data, and/or gating the data out from the different stages in parallel. Only the first and second stages of an N stage shifting register is illustrated in Figure 2,

but it will be apparent that the other of the N stages is similar to those shown and described.

Each stage possesses a single saturable reactor 100 for storage of data, plus one gating saturable reactor for each of its functions. The illustrated shifting register is provided with a set of five gating saturable reactors, however, it will be understood that such representation is only for the purposes of example, and that a shifting register may employ more or less gating elements to accomplish the particular functions desired.

Saturable reactor 100 of each stage is employed to store and shift the data presented to its input winding 104 via resistor 106 from the output of the preceding stage. The output from winding 108 of the storage elements 100 is presented via diode 109 in series to the input windings 103 of the several gating saturable reactors 102, 110, 112, 120 and 126 each of which has a control winding 138 supplied with bias in the same manner as described for winding 16 of Figure 1. Gating reactor 102 shifts data to the right through output diode 105 and presents it to the input winding 104 of the next stage. Diode 107 is a shunting diode which prevents current induced in winding 104 by application of the advance pulses to control winding 109 from affecting the state of magnetization of the reactor 102 of the preceding stage. Diode 111 does the same as between the input winding 103 and reactor 100 within each stage.

Saturable reactor 110 is provided to allow parallel read out from the storage element 100. Upon reduction and reapplication of the bias to the control windings 138 of all the reactors 110, there will appear on the parallel output lines an indication of the contents of the whole register.

Saturable reactor 112 of stage 2 and succeeding stages has its output winding 114 connected via diode 116 to the input winding 104 of storage element 100 of the preceding stage to permit the data stored in a storage element 100 to be shifted to the left to the next lower stage. That is, assuming a 1 to be stored in element 100 of stage 2, an output from element 112 of stage 2 provides a 1 in element 100 of stage 1. Element 112 of stage 1 has an output line 118 which may provide an "inverted" serial output. That is, upon successive left shiftings the output on line 118 would represent the data stored in the register in a reverse order, with the lower order digits being read first.

If during the time that parallel read out is being taken from elements 110, or if any other gating function destroys the state of element 100, and it is desired to maintain the pre-existing state in elements 100, a saturable reactor 120 with its output winding 122 may be connected via diodes 124 to the input winding 104 of the saturable reactor 100 in the same stage. In this manner utilization of the data stored in the elements 100 will, in effect, be non-destructive.

Under certain conditions it is desirable to invert the order of the data in the several stages of the register. For example, teletype information is usually transmitted with its higher order data first, but computers normally require that the data be received with its lower order digits first. With a saturable reactor 126 in each stage, the order of the data may be inverted or reversed, that is, the contents of the register may be shifted end for end. The output winding 128 of reactor 126 of the first stage is coupled by diode 130 in line 131 to the input winding 104 of the last or Nth stage (not shown); the output winding 128 of reactor 126 in the second stage is coupled by diode 132 to the next-to-last or (N-1)th stage (not shown); the output winding of the "Invert" reactor of the third stage (not shown) is coupled to the input storage reactor of the (N-2)th stage, etc. Also the "Invert" output of the Nth stage is coupled to the input of storage reactor 100 of the first stage by line 134; the "Invert" output of the (N-1)th stage is coupled to

input of the storage reactor 100 of stage 2 by line 136; the "Invert" output of the (N-2)th stage is coupled to the storage reactor input of the third stage, etc. In this manner the information stored in the first stage may be shifted to the Nth stage and vice versa, while the data stored in the second stage is shifted to the (N-1)th stage and vice versa, etc., to inter-change the contents of the register end for end.

As mentioned above, it is to be understood that a shifting register need not contain all of the saturable reactors illustrated and described, since seldom, if ever, will all five functions be required of a shifting register. Normally, two or three of the functions are sufficient. For example, a shifting register containing three gating elements per stage could be fabricated, and then readily modified to form any three of the functions by merely changing the appropriate connections. Thus the invention readily lends itself to production-line techniques.

Since only a comparatively small amount of current is necessary to hold the gating elements 102, 110, 112, 120 and 126 in their 0 state, one biasing tube, such as tube 34, may be connected to serve several gating elements. For example, one biasing tube may provide biasing current for all the "Shift Right" reactors 102 in the register, a second biasing tube may provide bias for all the "Parallel Readout" reactors 110, a third biasing tube may provide bias for all the "Shift Left" reactors 112 in the register, etc. In this way, the separate functions may be controlled by a negative pulse (such as pulse 42 at lead 38, Figure 1), applied to the cathode follower circuit preceding each of the biasing tubes.

Modifications of this invention not described herein will become apparent to those skilled in the art. Therefore, it is intended that the matter contained in the foregoing description and the accompanying drawings be interpreted as illustrative and not limitative, the scope of the invention being defined in the appended claims.

What is claimed is:

1. A stage of an N stage data shifting register, the stage comprising a plurality of saturable cores each of which has an input winding, a control winding, an output winding and a unidirectional current conducting device connected with the output winding, magnetic storage means having an input and output for receiving the data to be stored and shifted, means interconnecting said storage means output with each of said plurality of saturable core input windings, one of said plurality of saturable cores being adapted for coupling from its output winding to the succeeding stage, and a plurality of amplitude controllable biasing means connected respectively to the control windings of said saturable cores for gating the output from said storage means, the arrangement being such that during the biasing of the saturable cores no outputs occur therefrom, but upon a decrease in the amplitude of the bias for any one saturable core after an input thereto an output therefrom occurs.

2. Apparatus as in claim 1 wherein a second one of said plurality of saturable cores is coupled at its output winding to read out the data stored in said storage means.

3. Apparatus as in claim 1 wherein a second one of said plurality of saturable cores is adapted for coupling at its output winding to the input of the preceding stage.

4. Apparatus as in claim 1 wherein a second one of said plurality of saturable cores is coupled at its output winding to the input of said storage means to re-store the data within said stage while the amplitude of the bias on another of said saturable cores is reduced to permit an output therefrom.

5. Apparatus as in claim 1 wherein a second one of said plurality of saturable cores is coupled at its output winding to the input of said storage means, and a third one of said plurality of saturable cores is coupled at its output winding to read out the data stored in said storage

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means, said second one saturable core being operable to re-store the data in said storage means.

6. Apparatus as in claim 1 wherein a second one of said plurality of saturable cores is adapted for coupling at its output winding to the input of another stage.

7. A data shifting register comprising N stages each including a like plurality of saturable reactors each of which have an input winding, a control winding, an output winding and a unidirectional current conducting device connected with the output winding, each stage further including magnetic storage means having an input and an output for receiving the data to be stored, means interconnecting said storage means output with each of said plurality of saturable reactor input windings within said stages respectively, one of said plurality of saturable reactors in each stage being coupled from its output winding to the input of the storage means of the succeeding stage to shift the data to the next higher order stage, and a plurality of amplitude controllable biasing means connected respectively to the control windings of said saturable reactors in each stage for gating the output from the storage means associated therewith, the arrangement being such that during the biasing of the saturable reactors no outputs occur therefrom but upon a decrease in the amplitude of the bias for any one saturable reactor after an input thereto an output therefrom occurs.

8. Apparatus as in claim 7 wherein a second one of said plurality of saturable reactors in each stage is

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coupled at its output winding to read out the data stored in said storage means of the respective stages.

9. Apparatus as in claim 7 wherein a second one of said plurality of saturable reactors in each stage other than the first stage is coupled at its output winding to the input of the storage means of the preceding stage to shift the data to the next lower order stage.

10. Apparatus as in claim 7 wherein a second one of said plurality of saturable reactors in each stage is coupled at its output winding to the input of the storage means associated respectively therewith to re-store the data within each stage while the amplitude of the bias on another of said saturable reactors in each stage is reduced to permit an output therefrom.

11. Apparatus as in claim 7 wherein a second one of said plurality of saturable reactors in each stage is coupled at its output winding to the input of the storage means associated respectively therewith to re-store the data within each stage, and a third one of said cores in each stage is coupled at its output winding to read out the data stored in said storage means in parallel with read out from the other stages.

12. Apparatus as in claim 7 wherein a second one of said plurality of saturable reactors in each stage is coupled at its output winding to the input of a storage means in another stage, the coupling being such that the order of data stored in each stage is inverted.

No references cited.