(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
23 September 2010 (23.09.2010)

PCT

(10) International Publication Number
WO 2010/108030 A3

(51) **International Patent Classification**:
H03F 1/26 (2006.01) ***H03F 3/45*** (2006.01)
H03F 3/193 (2006.01)

(21) **International Application Number**:
PCT/US2010/027855

(22) **International Filing Date**:
18 March 2010 (18.03.2010)

(25) **Filing Language**: English

(26) **Publication Language**: English

(30) **Priority Data**:
12/407,704 19 March 2009 (19.03.2009) US

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(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

[Continued on next page]

(54) **Title**: COMMON-GATE COMMON-SOURCE AMPLIFIER

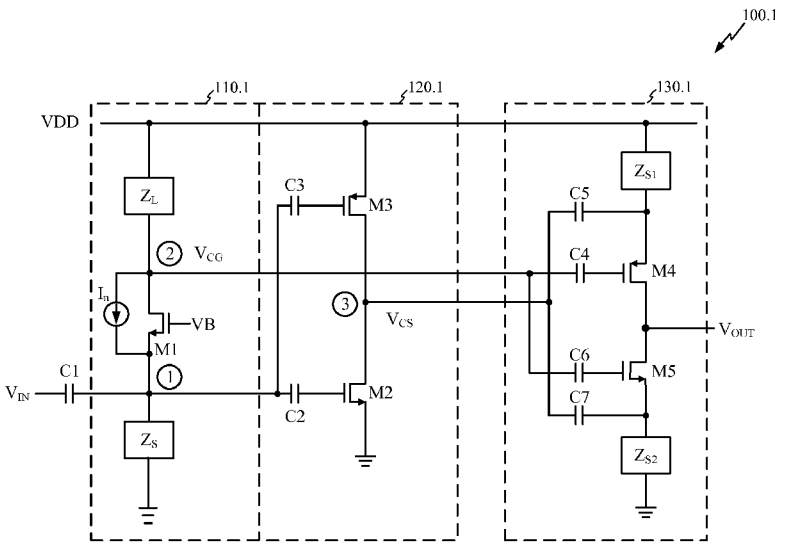

FIG 2

(57) **Abstract**: Techniques for integrating a common-source and common-gate amplifier topology in a single amplifier design. In one aspect, an input voltage is provided to both a common- source amplifier and a common-gate amplifier. The output voltages of the common- source amplifier and the common-gate amplifier are provided to a difference block for generating a single-ended voltage proportional to the difference between the output voltages. When applied to the design of, e.g., low-noise amplifiers (LNA's), the disclosed techniques may offer improved noise performance over the prior art.

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— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(88) Date of publication of the international search report:
25 November 2010

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/027855

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F1/26 H03F3/193 H03F3/45
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	BLAAKMEER S C ET AL: "A wideband Noise-Canceling CMOS LNA exploiting a transformer" RADIO FREQUENCY INTEGRATED CIRCUITS (RFIC) SYMPOSIUM, 2006 IEEE, IEEE, PISCATAWAY, NJ, USA LNKD- DOI:10.1109/RFIC.2006.1651110, 11 June 2006 (2006-06-11), pages 137-140, XP010925159 ISBN: 978-0-7803-9572-5	1,7,10, 11,17, 20,21
Y	page 3, left-hand column, line 42 - line 44; figure 3	23
A		8
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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 September 2010	05/10/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Kurzbauer, Werner

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/027855

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	the whole document	2-5, 11-15, 21,22
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X	DONG-GU IM ET AL: "A Wide-Band CMOS Variable-Gain Low Noise Amplifier for Multi-Standard Terrestrial and Cable TV Tuner" RADIO FREQUENCY INTEGRATED CIRCUITS (RFIC) SYMPOSIUM, 2007 IEEE, IEEE, PISCATAWAY, NJ, USA, 1 June 2007 (2007-06-01), pages 621-624, XP031113107 ISBN: 978-1-4244-0530-5 page 622, right-hand column; figure 2	1
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A,P	page 15, right-hand column; figure 5	2-5, 12-15,22

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/027855

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	WO 03/021768 A1 (MOTOROLA INC [US]) 13 March 2003 (2003-03-13) page 5; figures 1,2 page 6, line 17 - line 23	1,6,7,10 2-4,8, 11-14, 18,21,22
Y	STEPHAN C BLAAKMEER ET AL: "The Blixer , a Wideband Balun-LNA-I/Q-Mixer Topology" IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE SERVICE CENTER, PISCATAWAY, NJ, US LNKD-DOI:10.1109/JSSC.2008.2004866, vol. 43, no. 12, 1 December 2008 (2008-12-01), pages 2706-2715, XP011238672 ISSN: 0018-9200 the whole document	6,7,16, 17
A	US 5 777 514 A (MITTAL ROHIT [US] ET AL) 7 July 1998 (1998-07-07) figure 2	6-8,10, 16-18,20
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INTERNATIONAL SEARCH REPORT

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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A,P	ZHIQUN LI ET AL: "40-Gb/s, 0.18-Î 1/4 m CMOS Front-End Amplifier for VSR Parallel Optical Receiver" PHOTONICS AND OPTOELECTRONICS, 2009. SOPO 2009. SYMPOSIUM ON, IEEE EXPRESS CONFERENCE PUBLISHING, PISCATAWAY, NJ, USA, 14 August 2009 (2009-08-14), pages 1-4, XP031524445 ISBN: 978-1-4244-4412-0 figure 4	1
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A	US 7 120 427 B1 (ADAMS ANDREW R [AU] ET AL) 10 October 2006 (2006-10-10) figure 7	23
A	US 2006/068749 A1 (ISMAIL ALY [US] ET AL) 30 March 2006 (2006-03-30) the whole document	23
A	US 6 806 744 B1 (BELL MARSHALL J [US] ET AL) 19 October 2004 (2004-10-19) the whole document	6,16

INTERNATIONAL SEARCH REPORT

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Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☒ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-5, 11-15, 21, 22

A method for amplifying an input voltage to produce a single-ended output voltage, the method comprising:
amplifying the input voltage using a common-gate amplifier to generate a common-gate output voltage;
amplifying the input voltage using a common-source amplifier to generate a common-source output voltage; and
generating the difference between the common-gate output voltage and the common-source output voltage using a difference block to produce the single-ended output voltage,
wherein generating the difference comprising:
coupling the common-gate output voltage to the gate (source) of a first difference transistor; and
coupling the common-source output voltage to the source (gate) of the first difference transistor;
the single-ended output voltage being coupled to the drain of the first difference transistor and a corresponding apparatus.

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2. claims: 6, 16

A method for amplifying an input voltage to produce a single-ended output voltage, the method comprising:
amplifying the input voltage using a common-gate amplifier to generate a common-gate output voltage;
amplifying the input voltage using a common-source amplifier to generate a common-source output voltage; and
generating the difference between the common-gate output voltage and the common-source output voltage using a difference block to produce the single-ended output voltage,
wherein generating the difference comprising:
coupling the common-gate output voltage to the gate of a first difference transistor of a differential pair, the differential pair further comprising a second difference transistor having a source coupled to the source of the first difference transistor, the differential pair further comprising respective loads coupled to the drains of the first and second difference transistors, the differential pair further comprising a tail current source;
coupling the common-source output voltage to the gate of the second difference transistor; and
converting the differential voltage between the drains of the first and second difference transistors to the single-ended output voltage and a corresponding apparatus.

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3. claims: 7, 8, 17, 18

A method for amplifying an input voltage to produce a single-ended output voltage, the method comprising:

amplifying the input voltage using a common-gate amplifier to generate a common-gate output voltage;
amplifying the input voltage using a common-source amplifier to generate a common-source output voltage; and
generating the difference between the common-gate output voltage and the common-source output voltage using a difference block to produce the single-ended output voltage, the amplifying the input voltage using a common-gate amplifier comprising coupling the input voltage to the source of a common-gate transistor, the source of the common-gate transistor further coupled to a source impedance, the drain of the common-gate transistor further coupled to a load impedance and a corresponding apparatus.

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4. claims: 9, 19

A method for amplifying an input voltage to produce a single-ended output voltage, the method comprising:
amplifying the input voltage using a common-gate amplifier to generate a common-gate output voltage;
amplifying the input voltage using a common-source amplifier to generate a common-source output voltage; and
generating the difference between the common-gate output voltage and the common-source output voltage using a difference block to produce the single-ended output voltage, the amplifying the input voltage using a common-source amplifier comprising:
coupling the input voltage to the gate of a first common-source transistor, the drain of the first common-source transistor coupled to the drain of a second common-source transistor, the second common-source transistor being complementary to the first common-source transistor; and
coupling the input voltage to the gate of the second common-source transistor and a corresponding apparatus.

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5. claims: 10, 20

A method for amplifying an input voltage to produce a single-ended output voltage, the method comprising:
amplifying the input voltage using a common-gate amplifier to generate a common-gate output voltage;
amplifying the input voltage using a common-source amplifier to generate a common-source output voltage; and
generating the difference between the common-gate output voltage and the common-source output voltage using a difference block to produce the single-ended output voltage, the amplifying the input voltage using a common-source amplifier comprising buffering the output of the common-source amplifier using a cascoded transistor and a corresponding apparatus.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

6. claim: 23

A device for wireless communications, the device comprising a TX LO signal generator, at least one baseband TX amplifier, an upconverter coupled to the TX LO signal generator and the at least one baseband TX amplifier, a TX filter coupled to the output of the upconverter, a power amplifier (PA) coupled to the TX filter, an RX LO signal generator, an RX filter, a downconverter coupled to the RX LO signal generator and the RX filter, a low-noise amplifier (LNA) coupled to the RX filter, and a duplexer coupled to the PA and the LNA, the LNA amplifying an output voltage of the duplexer to produce a single-ended output voltage, the LNA comprising:
a common-gate amplifier configured to amplify the output voltage of the duplexer to generate a common-gate output voltage;
a common-source amplifier configured to amplify the output voltage of the duplexer to generate a common-source output voltage;
a difference block configured to generate a difference between the common-gate output voltage and the common-source output voltage to produce the single-ended output voltage.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2010/027855

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