



(51) International Patent Classification:
C23C 16/458 (2006.01)

(21) International Application Number:
PCT/EP2009/058387

(22) International Filing Date:
3 July 2009 (03.07.2009)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
08159693.4 4 July 2008 (04.07.2008) EP

(71) Applicants (for all designated States except US): **ABB TECHNOLOGY AG** [CH/CH]; Affolternstrasse 44, CH-8050 Zürich (CH). **ZIMMERMANN, Andreas** [CH/CH]; Baumgartenweg 1, CH-5702 Niederlenz (CH).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **AKURATI, Kranthi** [IN/CH]; Marktmattenstrasse 10, CH-5600 Lenzburg (CH). **KUNOW, Magnus** [DE/CH]; Fünflindenstrasse 2, CH-5600 Lenzburg (CH). **JERVIS, Ron** [GB/CH]; Zollweg 2c, CH-5034 Suhr (CH).

(74) Agent: **ABB**; ABB Schweiz AG, Intellectual Property (CH-LC/IP), Brown Boveri Strasse 6, CH-5400 Baden (CH).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: DEPOSITION METHOD FOR PASSIVATION OF SILICON WAFERS

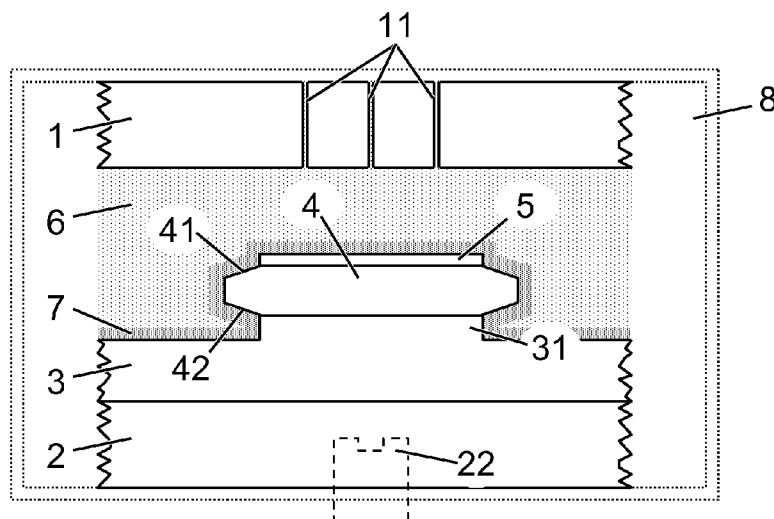


Fig. 2

(57) Abstract: A substrate (4) is mounted onto an elevated substrate support (31) of a substrate carrier plate (3). The substrate carrier plate with the substrate is then placed in a plasma reactor (8). Due to the elevated substrate support, both opposite sides of the substrate are exposed to the plasma (6) and are therefore coated with an electrical passivation layer (7).

Deposition Method for Passivation of Silicon Wafers

DESCRIPTION

Background of the Invention

Subject matter disclosed herein relates generally to the technical field of high-voltage, high-power semiconductors and, in particular, to a method and an apparatus for a single-step double-sided deposition of an electrical passivation layer on semiconductor wafers for power semiconductors.

In general, bipolar power semiconductors, such as diodes, thyristors, GTOs and GCTs, are made from silicon wafers. After these silicon wafers have undergone different implantation, diffusion, photolithographic and metallization processes, they are cut to circular discs and a negative or positive bevel is ground on the high-voltage blocking pn-junction(s). These bevels usually need to be protected with an electric passivation layer. One of the currently used state of the art passivation materials is amorphous hydrogenated carbon (a-C:H, also known as Diamond-like carbon DLC) which is typically deposited in a Plasma Enhanced Chemical Vapor Deposition (PECVD) process inside a parallel plate plasma reactor, but could generally be deposited in PECVD reactors of other geometries or by ion beam, sputtering, cathodic arc, pulsed laser deposition or low pressure CVD.

A simplified picture of the general PECVD process is given in Fig. 1. The silicon wafer is in contact with the second, lower electrode inside the reaction chamber via a substrate carrier plate. The hydrocarbon precursor gas (e.g., methane, acetylene) enters the reaction chamber of the plasma reactor through openings in the first, upper electrode, is ionized by radiofrequency, and forms the bulk plasma. The edge plasma layer is the space where the plasma ions get accelerated into the direction of the substrate and substrate carrier plate due to a DC bias voltage applied between the two electrodes.

The common process is to put the silicon wafers inside a recess on an aluminum substrate carrier plate as depicted in Fig. 1. This substrate carrier plate does not only act as a holder for the silicon wafers (substrate), it also establishes the disc's thermal

and electrical contacts to the actively cooled second (lower) electrode in the reaction chamber. The bevel on the silicon wafer facing the first (upper) electrode is exposed to the a-C:H depositing plasma while the remaining upper surface of the silicon wafer is covered by an aluminum shadow mask. Active cooling of the silicon wafer during the depositing process is necessary to avoid passivation layers with unsatisfactory electrical properties. Thermal degradation of a-C:H is reported in "Diamond-like amorphous carbon", by J. Robertson, Materials Science and Engineering: R: Reports 37, (2002) 129.

Silicon wafers with two high voltage blocking pn-junctions (e.g., a thyristor) may have one negative bevel ground on each of its opposite sides. With the common process described above, only the upper bevel is coated with a-C:H in a single process run. As a result, manual flipping-over of the silicon wafer and a second a-C:H deposit-process run are required. Since the bevel coated in the second process step is put into the recess face-down during the first process step in an unprotected and very sensitive state, said bevel is at a high risk of being contaminated resulting in a reduced blocking yield.

Summary of the Invention

It is one object of the invention to reveal a single-step method for the deposition of an double-sided deposition as an electrical passivation layer, such as a homogeneous a-C:H layer, on two sides of a wafer. It is a further object of the invention, to improve an existing deposition apparatus to allow such a single-step process for the deposition of an electrical passivation layer on a semiconductor wafer.

The inventive method is based on Plasma Enhanced Chemical Vapor Deposition (PECVP) in combination with an improved substrate-holder apparatus. In particular, the inventive method comprises the step of mounting a silicon wafer on an elevated substrate support of a substrate carrier plate and placing the substrate carrier plate with the silicon wafer in a plasma reactor. The substrate support is formed such that the wafer is placed on the substrate support only with its central area of the second main side being in contact to the substrate support. Due to such an elevated substrate support, both opposite sides of the silicon wafer are exposed to the plasma and are therefore coated with an electrical passivation layer. By the electrical passivation layer the wafer is electrically inactivated in the area of the electrical passivation layer (The

inventive passivation layer is not completely electrically inactive while it is partially conductive.).

The inventive method is advantageous over former methods as a-C:H-layers are deposited on two sides of the wafer, e.g. a silicon wafer, in one process step, either both on the two sides of one silicon wafer or on two silicon wafers stacked back to back. The wafer comprises a first main side with a first bevel on the border of the first main side and a second main side, which has a central area and a second bevel on the border of the second main side surrounding the central area, which second main side is arranged opposite the first main side. The wafer is mounted on a substrate support of a substrate carrier plate, which substrate support is formed such that the wafer is placed on the substrate support only with its central area of the second main side being in contact to the substrate support. Then the substrate carrier plate is placed with the wafer in a reaction chamber of a plasma reactor. Thereby, the first and second bevels are exposed simultaneously to the plasma in order to create the electrical passivation layer. In an exemplary embodiment, amorphous hydrogenated carbon is applied as the plasma to form the electrical passivation layer onto the wafer.

In order to avoid deteriorated heat transfer which may occur due to the increased distance between the silicon wafer carried on the elevated substrate support of the substrate carrier plate and the actively cooled lower electrode, the invention also relates to a combination of said novel substrate carrier plate design and an improved silicon wafer cooling mechanism. This allows for reasonable heat dissipation, which is crucial for the deposition process, since more graphite-like carbon layers with unsatisfactory electrical properties may be deposited at substrate temperatures above approximately 200 °C.

The described invention highlights the significance of a pedestal-like substrate carrier plate instead of a recess. Therefore, both sides of a silicon wafer are exposed to the plasma. Nevertheless, homogeneous deposition is highly non-trivial, especially for the bevel adjacent to the lower electrode. As both even plasma flux-rates and homogeneous electric fields are necessary for the deposition of uniform a-C:H-layers, mushroom-shaped (e.g. concave, upside down truncated cone, etc.) designs of the elevated substrate supports tend to be advantageous over purely cylindrical designs.

In yet another embodiment, the invention also relates to adjusted deposit-process parameters of the DC bias voltage.

Brief Description of the Drawings

A more complete understanding of the invention may be gained by reference to the following detailed description when taken in conjunction with the accompanying drawings wherein:

Fig. 1 schematically shows an assembly with a silicon wafer within a parallel plate reactor in a prior art single sided deposition process,

Fig. 2 schematically shows an assembly with a silicon wafer on an inventive elevated substrate support within a parallel plate reactor,

Fig. 3 shows in more detail the assembly of Fig. 2, with a first embodiment (cylindrical) of the inventive elevated substrate support,

Fig. 4 shows in more detail the assembly of Fig. 2, with a second embodiment (truncated cone) of the inventive elevated substrate support, and

Fig. 5 schematically shows an assembly with stacked silicon wafers on inventive elevated substrate supports within a parallel plate reactor.

Description of the Preferred Embodiments

Fig. 1 provides a schematic drawing of a parallel plate reactor used in a prior art PECVD-process with a pair of parallel plate electrodes 1 and 2, reaction chamber 8, bulk plasma 6, edge plasma layer 7, silicon wafer 4, shadow mask 5, and substrate carrier plate 3 with recess 33. Electron energy (plasma) is used as the activation method to enable a-C:H deposition on the silicon wafer. The hydrocarbon precursor gas (e.g., methane, acetylene) enters the reaction chamber 8 through openings 11 in the upper electrode 1. It is ionized by radiofrequency and forms the bulk plasma 6. The edge plasma layer 7 is the space in the reaction chamber 8 where plasma ions get accelerated to the silicon wafer or substrate carrier plate due to a DC bias voltage that has been applied between the two electrodes 1 and 2. The silicon wafer 4 as a substrate is put inside a recess 33 on a substrate carrier plate 3. This substrate carrier plate 3 does not only act as a mechanical substrate holder, but it also establishes thermal and electrical contacts between the silicon wafer and the lower electrode 2 in the reaction chamber 8 of the plasma reactor. One bevel on the silicon wafer that is to be passivated is facing the upper electrode 1. This bevel is exposed to the a-C:H depositing plasma 6 and/or 7. Areas on the top surface of the silicon wafer that are not

subject to passivation are covered by a shadow mask 5. In the current process, only the upper bevel is coated with a-C:H in a single process run. As a result, manual flipping-over of the silicon wafer and a second a-C:H deposit-process run are required for silicon wafer with two high voltage blocking pn-junctions, that have one bevel on each opposite side (e.g., a thyristor). As mentioned above, the bevel coated in the second process step is put into the recess 33 face-down (in an unprotected and therefore very sensitive state) during the first process step and is therefore at a high risk of being contaminated resulting in a reduced blocking yield.

Fig. 2 provides a schematic drawing of an improved version of a parallel plate reactor used in the inventive one-step double-sided PECVD-process. The apparatus differs from the one used in Fig. 1 in so far that a newly developed substrate carrier plate 3 is used. This plate is preferably made of electrically and thermally conducting material, such as aluminum or another metal. The silicon wafer (substrate) is no longer placed inside a recess in the substrate carrier plate 3, in order to overcome the limitation of only single-sided a-C:H-deposition. Instead, the silicon wafer is placed on top of a "mushroom-like" or "pedestal-like" protrusion, which is referred to as elevated substrate support 31. The wafer is placed on the substrate carrier plate 3 with a contact area of such a design, that the second main side of the wafer is in contact to the substrate carrier plate 31 and the first and second bevels are not covered or enclosed or encased by the substrate carrier plate 31.

Said elevated substrate support 31 is arranged on top of the substrate carrier plate 3, integrated in the substrate carrier plate 3 or optionally as a separate part. This substrate carrier plate does not only act as a mechanical substrate holder for the silicon wafer, but it also establishes thermal and electrical contacts between the silicon wafer and the lower electrode 2 in the reaction chamber 8. By lifting the position of the silicon wafer, flow of plasma, which again is created from precursor gases flowing into the reaction chamber 8 through the parallel plate electrode 1, is no longer limited to the upper bevels 41 of the silicon wafer substrate. The a-C:H-deposition simultaneously occurs on the upper bevels 41 and lower bevels 42 of the silicon wafer. The non-coatable upper surface areas of the silicon wafer are again covered by a shadow mask 5. To indirectly limit the temperature of the silicon wafer to a level below approximately 200 °C, the bottom electrode 2 is actively cooled, e.g. by a water cooling device 22 running at a temperature of about 15 to 20 °C.

Fig. 3 provides a more detailed view of a first embodiment of an inventive “pedestal-like” elevated substrate support 31 of the substrate carrier plate 3 with the wafer, e.g. a silicon wafer, on top. Ions from the bulk plasma 6 get accelerated to the silicon wafer 4 in the edge plasma layer 7 near the surfaces that are electrically connected to the bottom electrode 2. Homogeneous a-C:H deposition on the silicon wafer 4 at different regions A and B is highly non-trivial especially for the lower bevel on the silicon wafer. The reason is that evenly distributed plasma flux-rates and homogeneous electric fields are necessary for the deposition of uniform a-C:H-layers. However, except for extremely small plasma edge layer thicknesses, the plasma-flux density as well as the accelerating electric field can differ for regions A and B resulting in slightly inhomogeneous a-C:H deposition in these regions. To a certain extent, such inhomogenities can be compensated for by a slight tuning of the process parameters, as the plasma edge layer thickness scales with the square root of the DC bias voltage which can be decreased to a minimum of approximately 500 Volts. This minimal DC bias voltage may vary for some reactors, as it is dependant of many different parameters.

Fig. 4 provides a more detailed view of a second embodiment of the inventive substrate carrier plate 3, in particular the elevated substrate support 31. Instead of using a mere cylindrical protrusion as elevated substrate support 31 of the substrate carrier plate 3, an additional rotated cut at the base leads to a concave cross-section of the elevated substrate support 31. Regarding this type of geometrical profile, these elevated substrate supports are herein referred to as “mushroom-shaped”. Possible geometrical cut, mushroom shaped, profiles are not limited to straight lines. In principle, any geometrical profile of the elevated substrate support 31 can be used, e.g. concave, upside down truncated cone, etc., provided that plasma flux-rates are sufficiently high and electric/ magnetic fields on the bottom bevels of the silicon wafer are such as to provide a deposition rate as homogeneous as possible. In these cases, homogeneous a-C:H deposition on the silicon wafer 4 at different regions A and B is facilitated. Remaining possible inhomogenities can again be compensated for by a slight tuning of the process parameters, as the plasma edge layer thickness scales with the square root of the DC bias voltage which can be decreased to a minimum of approximately 500 V. Improved and more direct cooling of the silicon wafer is optionally achieved by active cooling with a cooling device 32 arranged in or adjacent to the substrate carrier plate 3

or in or adjacent to the elevated substrate support 31 of the substrate carrier plate. As cooling device, water cooling can be used, operating for example at a temperature of 15 to 20 °C. This optimized in-situ cooling strategy in combination with an optional pre-cooling procedure of the silicon wafer and/ or the substrate carrier plate leads to a maximal process temperature of the silicon wafer of below 200 °C. In order to further reduce the temperature of the silicon wafer during the deposition process cooling means are optionally arranged in the shadow mask, which is covering an upper surface of the silicon wafer. As mentioned above, satisfactory heat dissipation is crucial for the deposition process as silicon wafer temperatures above 200 °C may lead to the deposition of graphite-like carbon layers with unsatisfactory electrical properties.

In order to properly align, i.e. concentrically align, silicon wafer 4 and elevated substrate support 31 of the substrate carrier plate 3, aligning or centering means can be used prior to loading the assembly into the reaction chamber of the plasma reactor.

Optionally, as schematically shown in Fig. 5, additional silicon wafers 4' may be stacked on top of the one silicon wafer 4 carried on the elevated substrate support 31. Between adjacent silicon wafers 4 and 4' in the stack, an elevated substrate support 31' is arranged, in order to allow homogeneous a-C:H deposition on adjacent silicon wafers. Optionally, this additional elevated substrate support may be omitted, to allow back-to-back stacking of two silicon wafers, each with only one high voltage blocking pn-junction, such as diodes, GTOs and GCTs, and therefore only one bevel to be passivated.

Optionally, cooling means may be arranged within the additional elevated substrate supports 31' and/ or the shadow mask 5, arranged on top of the stack. Optionally, there is an electrically conducting connection 34 arranged between the additional elevated substrate supports 31' and one or several or all of the parts, which are electrically connected to the lower electrode 2, i.e. the elevated substrate support 31, the substrate carrier plate 3 or the lower electrode 2 itself.

List of Reference Symbols

1, 2	Electrodes
22	cooler
3	substrate carrier plate
31, 31'	Elevated Substrate support
32	cooler
33	recess
34	electrically conducting connection
4, 4'	Si-disc/ substrate
41	Upper bevel
42	Lower bevel
5	Shadow mask
6	bulk plasma
7	edge plasma layer
8	Reaction chamber of plasma reactor

PATENT CLAIMS

1. Method for applying double-sided deposition (7) of amorphous hydrogenated carbon onto a silicon wafer (4), which wafer (4) comprises a first main side with a first bevel on the border of the first main side and a second main side, which has a central area and a second bevel on the border of the second main side surrounding the central area, which second main side is arranged opposite the first main side, comprising the steps of mounting the wafer (4) on a substrate support (31) of a substrate carrier plate (3), which substrate support (31) is formed such that the wafer (4) is placed on the substrate support (31) only with its central area of the second main side being in contact to the substrate support (31), and placing the substrate carrier plate with the wafer (4) in a reaction chamber (8) of a plasma reactor, wherein the first and second bevels are exposed simultaneously to a plasma (6) in order to create the deposition (7), wherein amorphous hydrogenated carbon is applied as the plasma.
2. Method as in claim 1, wherein the temperature within the wafer is kept below 200 °C during the deposition process.
3. Method as in claim 1, wherein the wafer (4) is cooled prior to being mounted on the substrate carrier plate (3) or wherein the substrate carrier plate (3) is cooled prior to being placed in the reaction chamber (8) or wherein the wafer (4) and the substrate carrier plate (3) are being placed in the reaction chamber (8).
4. Method as in one of the claims 1, wherein the reaction chamber (8) comprises two parallel plate electrodes (1, 2) and wherein the wafer (4) is being actively cooled during the deposition process by cooling means (22) arranged in the electrodes (2) of the reaction chamber (8) or wherein the wafer (4) is being actively cooled during the deposition process by cooling means (32) arranged in the substrate carrier plate (3) or the substrate support (31) of the substrate carrier plate (3).
5. Substrate carrier plate (3) for carrying a silicon wafer (4) for the manufacturing of a semiconductor device during a deposition process for depositing a double-sided deposition (7) on the surface of the wafer (4) in a plasma reactor chamber (8), which wafer (4) comprises a first main side with a first bevel on the border of the first main side and a second main side, which has a central area and a second bevel on the border of the second main side surrounding the central area, which second main

side is arranged opposite the first main side, characterized in, that said substrate carrier plate (3) comprises a substrate support (31) for carrying the wafer (4), which substrate support (31) is formed such that the wafer (4) can be placed on the substrate support (31) only with its central area of the second main side being in contact to the substrate support (31).

6. Substrate carrier plate as in claim 5, comprising a cylindrical substrate support (31) or comprising a substrate support (31), which has a surface area in a surface plane, on which the central area of the wafer can be placed, and which substrate carrier plate (3) has a cross-section, which diminishes with distance from the surface plane at least up to a first depth.
7. Substrate carrier plate as in one of the claims 5 or 6, comprising several substrate supports (31) each for carrying a wafer (4).
8. Substrate carrier plate as in one of claims 5 to 7, said substrate support (31) being a separate part which is attached to said substrate carrier plate (3).
9. Substrate carrier plate as in one of claims 5 to 8, wherein said substrate carrier plate (3) comprises a substrate support (31), on which a first wafer can be carried, and at least one further wafer can be stacked on the first wafer.
10. Substrate carrier plate as in claim 9, wherein an additional substrate support (31') can be arranged between adjacent wafers (4, 4') in the stack, the wafers from each pair of neighbored wafers being separated from each other by an additional substrate support (31').
11. Substrate carrier plate as in claim 10, wherein cooling means (32) are arranged in said additional substrate support (31').
12. Substrate carrier plate as in one of claims 10 or 11, wherein an electrically conducting connection (34) is arranged between said additional substrate support (31') and the substrate support (31) and/ or the substrate carrier plate (3) and/ or the substrate carrier plate (3) carrying electrode (2).
13. Deposition apparatus for depositing a double-sided deposition (7) on a silicon wafer (4), comprising two parallel plate electrodes (1, 2) inside a reaction chamber (8) of a plasma reactor, a substrate carrier plate (3) according to any of the claims 3 to 6

with at least one wafer (4) placed on the substrate support (31), which substrate carrier plate (3) can be placed on one of the electrodes (2).

14. Deposition apparatus as in claim 13, comprising cooling means (22, 32) for cooling the wafer (4) during the deposition process.
15. Deposition apparatus as in claim 14, said cooling means (22) being arranged in or adjacent to said substrate carrier plate (3) carrying electrode (2).
16. Deposition apparatus as in one of claims 14 or 15, wherein said cooling means (32) are arranged in said substrate carrier plate (3) or in said substrate support (31) of the substrate carrier plate (3) or wherein said cooling means (32) are arranged in a shadow mask (5) covering said wafer (4) on the surface facing the other of the two plate electrodes (1).

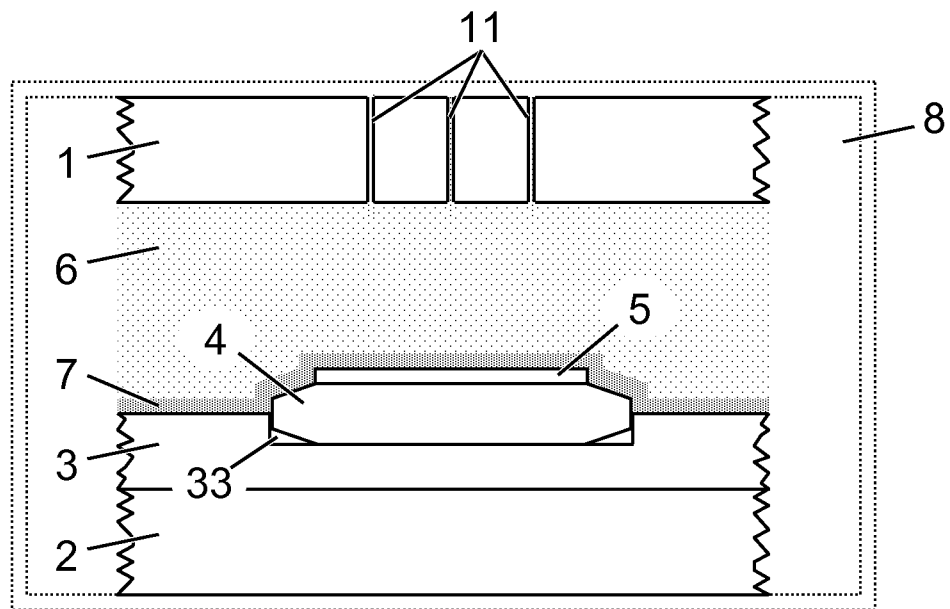


Fig. 1

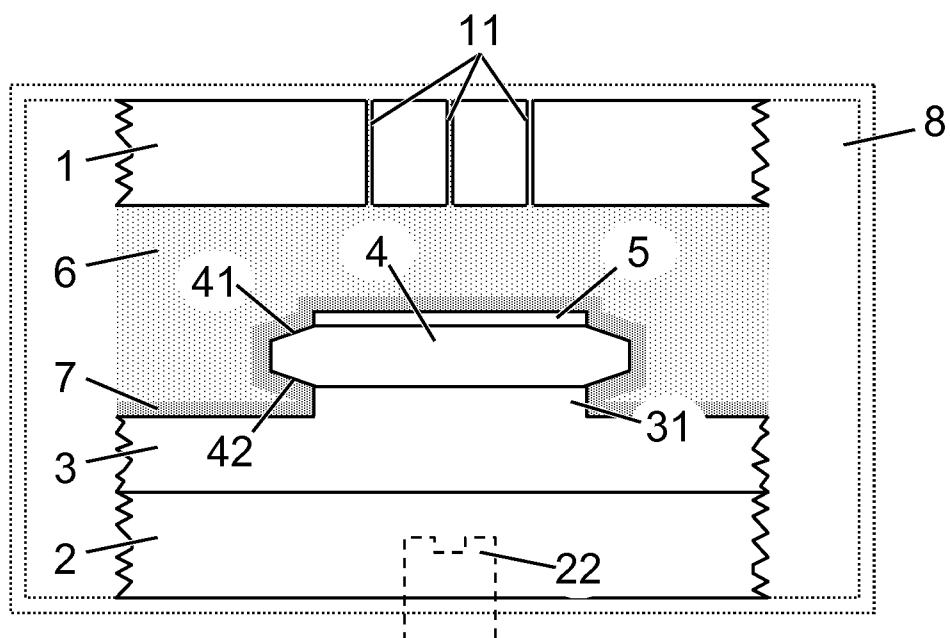


Fig. 2

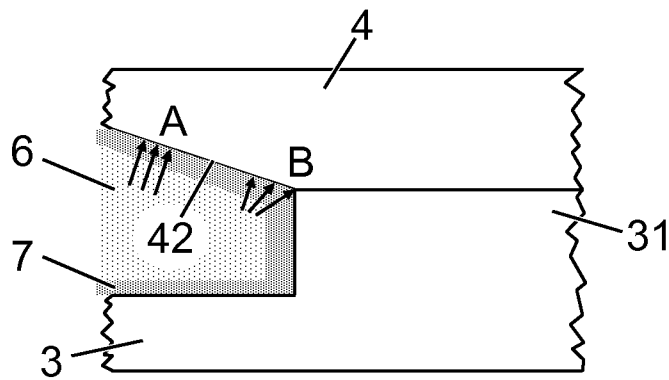


Fig. 3

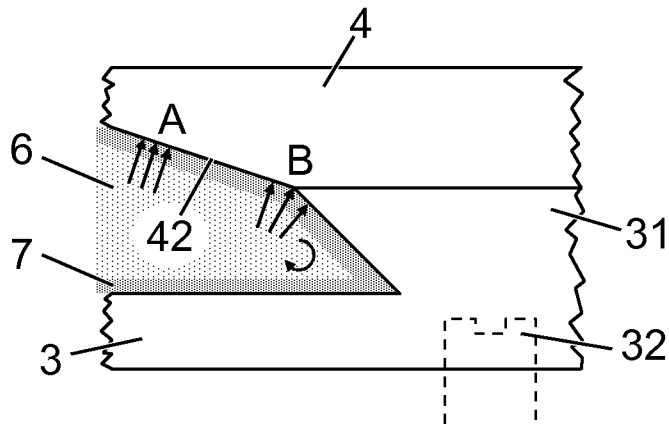


Fig. 4

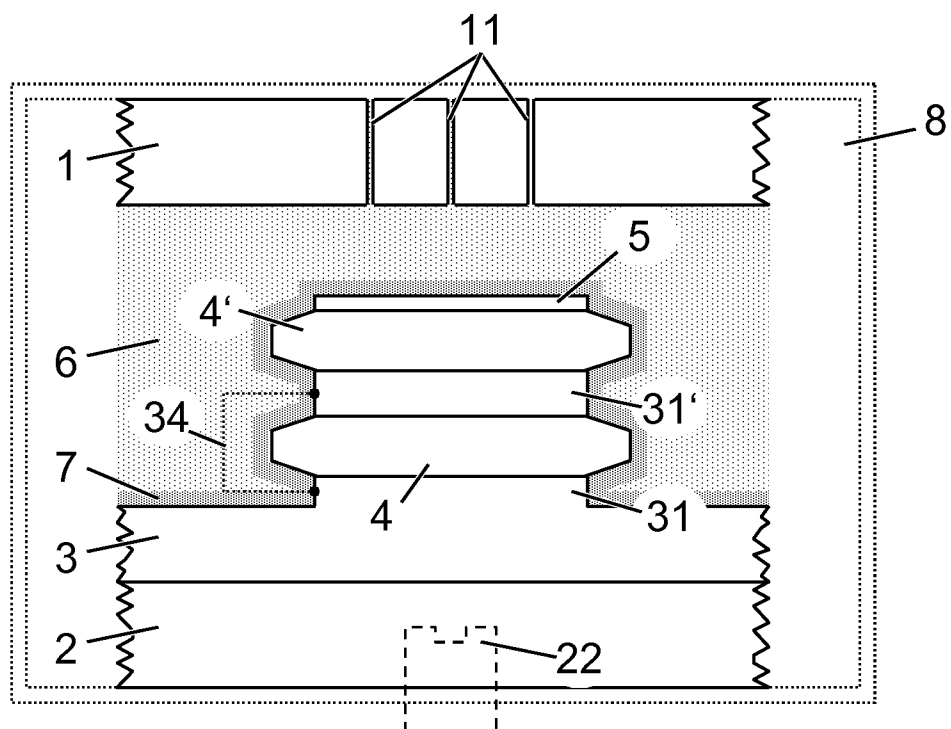


Fig. 5

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2009/058387

A. CLASSIFICATION OF SUBJECT MATTER

INV. C23C16/458

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

C23C H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 023 405 A (SHAMOUILIAN SHAMOUIL [US] ET AL) 8 February 2000 (2000-02-08) column 1, lines 30-37 column 5, line 25 - column 6, line 27; figure 1a column 6, line 28 - line 44; figures 1a-1c column 10, line 35 - column 11, line 20	5-8, 13-16
A	the whole document	1-5, 8, 9, 15-20
X	US 5 384 008 A (SINHA ASHOK [US] ET AL) 24 January 1995 (1995-01-24) column 3, line 30 - column 6, line 24; figures 4-7	5-8, 13
A	the whole document	1-4, 9-12, 14-16
	----- -/--	

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- *G* document member of the same patent family

Date of the actual completion of the international search

6 August 2009

Date of mailing of the international search report

18/08/2009

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel: (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Keller, Jan

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/058387

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005/284371 A1 (MCFADDEN ROBERT S [US] ET AL) 29 December 2005 (2005-12-29) paragraphs [0016] - [0036]; figures 4,6A,6B	5-8,13
A	the whole document	1-4, 9-12, 14-16
A	----- WOLF S, TAUBER R N: "Silicon Processing for the VLSI Era, Volume 1: Process technology" 1986, LATTICE PRESS, SUNSET BEACH, CALIFORNIA, USA, XP002500748 page 171 - page 174; figure 8	5-16
A	----- WIDMANN D, MADER H, FRIEDRICH H: "Technologie hochintegrierter Schaltungen, 2. Auflage" 1996, SPRINGER-VERLAG, XP002500749 page 13 - page 21; figure 3.1.6a	5-16
A	----- US 2007/243652 A1 (BOUR DAVID [US] ET AL) 18 October 2007 (2007-10-18) the whole document	1-16

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2009/058387

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 6023405	A	08-02-2000	US 6557248 B1	06-05-2003
US 5384008	A	24-01-1995	NONE	
US 2005284371	A1	29-12-2005	CN 1961097 A	09-05-2007
			DE 112005001470 T5	16-04-2009
			WO 2006012048 A2	02-02-2006
US 2007243652	A1	18-10-2007	NONE	