(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
26 October 2006 (26.10.2006)

PCT

(10) International Publication Number
WO 2006/111203 A1

(51) International Patent Classification:
H01L 21/28 (2006.01) *H01L 29/49* (2006.01)
H01L 29/51 (2006.01)

(21) International Application Number:
PCT/EP2005/051784

(22) International Filing Date: 21 April 2005 (21.04.2005)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **FREESCALE SEMICONDUCTOR, INC.** [US/US]; 7700 West Parmer Lane, Austin, TX 78729 (US).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **KAUSHIK, Vidya** [US/BE]; Europalaan 17, B-1560 Hoeilaart (BE).

(74) Agent: **WHARMBY, Martin, Angus**; c/o Impetus IP Ltd, Grove House, Lutyens Close, Chineham Court, Basingstoke, Hampshire RG24 8AG (GB).

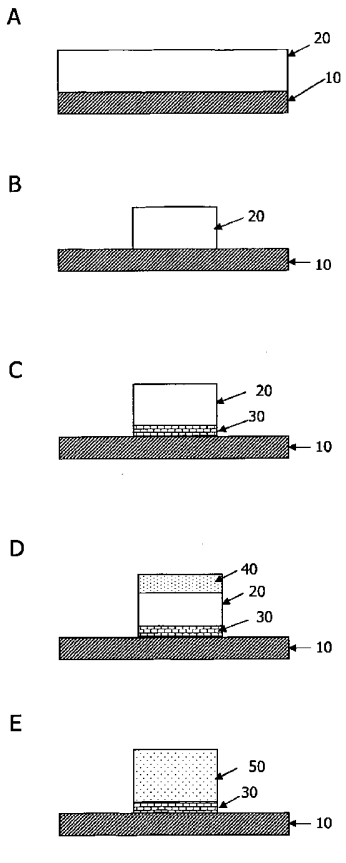
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *with amended claims*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) **Title:** METHOD OF FABRICATING A MOS DEVICE WITH NON-SiO_2 GATE DIELECTRIC



(57) **Abstract:** A polycrystalline silicon layer (20) is deposited on a gate dielectric (10) and then a portion thereof is re-oxidised so as to form a thin layer of oxide (30) between the poly-Si layer and the underlying gate dielectric. Subsequently, the poly-Si layer is converted to a fully-silicided form (50) so as to produce a FUSI gate. The gate dielectric can be a high-k material, for example a Hf-containing material, or SION, or another non-SiO_2 dielectric. The barrier oxide layer (30) is preferably less than 1 nm thick.

WO 2006/111203 A1

Method Of Fabricating A MOS Device with Non-SiO_2 Gate Dielectric

The present invention relates to the field of integrated circuit device manufacture. More particularly, the present invention relates to the manufacture of metal-oxide-silicon (MOS) devices and the like, notably such devices employing high dielectric constant (high-k) gate dielectric or, more generally, non-SiO_2 gate dielectric, that is, gate dielectric materials which do not behave as classic SiO_2 dielectric does, even if based on SiO_2 (thus including doped SiO_2 dielectrics).

The continuing drive for greater scaling of integrated circuit devices has lead to a desire to replace the SiO_2 that is traditionally used as gate dielectric in MOS devices. The Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors (ITRS) 2004 specifies that MOSFET devices used in CMOS will require a gate-oxide equivalent thickness (EOT) less than 1.4 or 1.5 nm when these devices are scaled so as to have gate lengths below 65nm, dropping to 0.8 nm or less by 2010. This would be very hard, if not impossible, to achieve using SiO_2 gate dielectric because it would require the use of a SiO_2 gate dielectric layer only a few atoms thick. Moreover, because of quantum mechanical direct tunnelling, leakage current increases as the thickness of the SiO_2 gate dielectric decreases.

Accordingly, high-k dielectric materials have been attracting attention for use as gate dielectric materials, notably in applications where low gate leakage current is desired. High-k dielectric materials are those having a dielectric constant, k greater than that of silicon nitride, i.e. $k>7$. Some high-k dielectric materials under consideration include oxides and silicates of metals such as tantalum (Ta), zirconium (Zr) and hafnium (Hf). A number of existing

proposals involve use of gate dielectric materials containing Hf, notably, HfO_2, HfO_2/SiN, HfSiON and HfAlO.

Difficulties arise when it is desired to use high-k dielectric materials, instead of SiO_2, as gate dielectric. In particular, SiO_2 is compatible both with the Si substrate and with existing fabrication processes. In order to be able to use a high-k dielectric material, or indeed other non-SiO_2 dielectric materials, as the gate dielectric, it is necessary to overcome potential problems due to chemical bonding effects and difficulties arising from the desirability of integrating the new material into existing fabrication processes.

For example, in recent years MOSFET gate electrodes have habitually been made of polycrystalline silicon (poly-Si). Various problems arise when high-k dielectric materials (or other non-SiO_2 dielectrics) are used as gate dielectric materials with poly-Si gates.

In particular, when using poly-Si on non-SiO_2 gate dielectric, carrier mobility in the MOSFET device can be low. Moreover, the threshold voltage, Vt, is different from that observed when SiO_2 dielectric is used with poly-Si gate electrodes: typically Vt is -0.3 V for poly-Si on SiO_2 whereas it is typically in the range -0.6 to -0.9 V for poly-Si on high-k gate dielectric. Furthermore, when poly-Si is used with high-k gate dielectric it is generally observed that the threshold voltage, Vt, for PMOS devices is too high, (because of Fermi-level pinning of the gate work function).

One approach that has been tried in view of the above-mentioned problems is to convert the poly-Si gate electrode material to silicide, for example NiSi or CoSi, thus forming a fully-silicided (or "FUSI") gate electrode. This can be considered to be a metal-like gate electrode. This approach has the advantage of avoiding the poly-depletion effect that is observed when using

poly-Si gate electrodes, thus reducing the equivalent oxide thickness (EOT) at the gate. Certain proposals have used Hf-based materials (notably HfSiON, HfO_2 and HfO_xN_y) as a high-k gate dielectric material in association with FUSI gate electrodes.

However, when FUSI gate electrodes are used with high-k gate dielectric materials the following problem arises: there is insufficient PMOS/NMOS Vt modulation (asymmetric Vt and higher-than-target Vt values).

In view of the above problems, various researchers have concluded that it is preferable to use SiON rather than high-k dielectric materials when selecting a material for use as the gate dielectric for a CMOS device having a FUSI-gate. (SiON was already being considered as a replacement for SiO_2 gate dielectrics as an intermediate step on the way to changing to high-k dielectric materials, in view of the fact that a SiON film has a dielectric constant of about 4 to 8, depending upon the proportions of O and N therein.) However, it is generally found that the leakage current is undesirably high in devices using FUSI-gate electrodes on SiON gate dielectrics.

An alternative approach that has been tried in order to overcome the problems involved in using high-k gate dielectric with poly-Si gate electrodes is to modify the interface between the high-k gate dielectric and the poly-Si gate electrode, for example by adding barrier layers (or "capping layers") between the gate dielectric and the poly-Si gate electrode. However, this approach has not been particularly successful – even when a variety of different materials and deposition techniques were used to form the barrier layers on the high-k material, there was no reduction, or inadequate reduction, in the observed Vt shift when the gate stack structure was subsequently completed by a poly-Si gate electrode, and/or carrier mobility was degraded. In some cases the

capping technique was unsuitable for making NMOS devices. Also, introduction of capping layers causes undesirable increase in the EOT.

The inadequacy of capping for tackling Vt shift can be seen from Fig.1. In Fig.1 there is a plot of gate length (expressed as Ldrawn) against Vt for a number of different PMOSFET structures all using poly-Si gate electrodes. These PMOSFET structures constitute comparative examples for use in demonstrating the improvements achieved using the present invention.

The first comparative example is a PMOSFET structure using a SiO_2 gate dielectric 2.5 nm thick; the results for this first comparative example are indicated using hollow squares in Fig.1. The second comparative example is a PMOSFET structure using a HfO_2 gate dielectric 3 nm thick topped by a SiN_x capping layer 1 nm thick; the results for this second comparative example are indicated using hollow triangles in Fig.1. The third comparative example is a PMOSFET structure using a HfO_2 gate dielectric 2.5 nm thick topped by a $HfSiO_x$ capping layer 1 nm thick; the results for this third comparative example are indicated using hollow circles in Fig.1.

As seen from Fig.1, the Vt shift for HfO_2 or $HfSiO_x$ gate dielectric with polysilicon gates, relative to SiO_2 is unacceptably high. Further, the Vt difference is maintained for large and smaller gate lengths.

Poor results are seen for capped high-k dielectric materials used with poly-Si gate electrodes even when the high-k dielectric is capped with SiO_2.

The present inventor has postulated that the reason for the disappointing results that are observed in gate stacks using poly-Si gate electrodes and high-k dielectrics with caps is that the capping layers are formed on the gate dielectric layer before the poly-Si layer has been deposited. In

other words, at the time when the capping layers are formed there is not yet an interface between the high-k dielectric material and the poly-Si.

The present invention provides a new method of fabricating MOS devices comprising FUSI gates, as defined in the appended claims.

The present invention further provides a MOS device comprising FUSI gates, as defined in the appended claims.

In the preferred embodiments of the present invention, a poly-Si layer is formed on a gate dielectric layer and then a layer of oxide is produced between the poly-Si and the gate dielectric, notably by a lateral re-oxidation process.

The formation of the thin oxide layer after the poly-Si has already been deposited on the gate dielectric releases Fermi-level pinning of the gate work function, enabling lower threshold voltages (Vt) to be obtained for smaller gates. As a result, a desired work function modulation can be achieved.

Because the lateral reoxidation process has been found to release Fermi-level pinning and reduce Vt shift it is believed that the thin layer of oxide formed by this process is generated by oxidation of the poly-Si.

Although the reoxidation process leads to an increase in the EOT at the gate, a CETinv (Capacitance equivalent thickness in inversion) reduction can be obtained by use of a FUSI gate – in other words, by converting the poly-Si layer into a fully-silicided form. Thus, the increase in EOT from a physically thicker dielectric is compensated by the absence of polysilicon depletion using a metal-like FUSI gate, so that overall there is little or no increase in CETinv under transistor operation conditions of inversion.

In certain of the preferred embodiments of the invention, the reoxidation process forms a particularly thin oxide layer between the gate electrode and gate dielectric, notably a layer having a thickness less than 10 angstroms (< 1 nm).

In certain of the preferred embodiments of the invention, the gate dielectric is a high-k dielectric material, for example a Hf-containing material.

An advantage of fabricating MOS devices using FUSI gate electrodes on high-k gate dielectrics is that this enables further scaling of ULSI devices to be achieved whilst still using existing fabrication equipment. This avoids the need to introduce dual metal gate electrode devices, which could require significant changes in the machinery used in ULSI device fabrication processes.

The above and other features and advantages of the present invention will become apparent from the following description of a preferred embodiment thereof, given by way of example, and illustrated in the accompanying drawings, in which:

Figure 1 is a graph illustrating how Vt changes as gate lengths are scaled down in various comparative examples that are PMOSFET structures which do not make use of the present invention;

Figure 2 illustrates schematically the main steps of a method for forming a CMOS device according to one preferred embodiment of the present invention, in which Figs.2A to 2E illustrate respective different steps in the method;

Figure 3 illustrates formation of a SiO_2 barrier layer in a MOS device gate stack structure according to a CMOS device fabrication technique of a first preferred embodiment of the present invention, in which:

Fig.3A shows the gate stack structure in an initial stage, and

Fig.3B shows the gate stack structure at a subsequent stage; and

Figure 4 is a graph illustrating how Vt changes as gate lengths are scaled down in various PMOSFET structures fabricated using a reoxidation method according to the preferred embodiment of the invention, in which:

Fig.4A shows results obtained for a first group of PMOSFET structures based on the first group of comparative examples, and

Fig.4B shows results obtained for a second group of PMOSFET structures.

The preferred embodiment of the present invention will now be described with reference to Figures 2 to 4. In this description, it will be assumed that the method according to the preferred embodiment is being used to fabricate the gate stack structure of a MOSFET device. However, it is to be understood that the present invention is not limited to use in the fabrication of MOSFET devices.

As shown in Fig.2A, a layer of gate dielectric 10 is formed on a substrate 1 (not shown in Fig.2, but see Fig.3). The substrate 1 will typically be silicon and may have an overlying layer 5 of SiO_2 or the like (also not shown in Fig.2) for example to enhance mobility in or to enable the deposition of the gate dielectric 10. In the preferred embodiment of the invention this gate dielectric 10 is formed of a high-k dielectric material, notably a Hf-containing material, e.g. HfO_2. Any convenient process can be used for forming the gate dielectric layer 10, including, but not limited to: atomic-level chemical vapour deposition (ALCVD), metal organic chemical vapour deposition (MOCVD), etc, with any appropriate post-processing, e.g. post-deposition annealing. However, if the post-processing treatment results in a reduction in the ability of oxygen to diffuse through the high-k dielectric material forming layer 10 then the reoxidation conditions have to be adjusted in order to compensate. Typically, the gate dielectric layer 10 will have a thickness of 1nm to 10nm depending on the dielectric constant.

If desired, a capping layer (not shown) can be formed on the gate dielectric 10 before the subsequent processing. This will be appropriate, notably, when the high-k material forming the gate dielectric layer 10 acts as a barrier to penetration of oxygen (e.g. because of a post-deposition treatment such as plasma nitridation). According to the present invention it is desirable that the top few angstroms of the gate dielectric allow oxygen to pass therethrough (so as to oxidize the bottom few angstroms of the polysilicon gate and form the thin 'special' layer that releases the Fermi level pinning, as explained further below). Thus, in a case where there is poor oxygen diffusion through the high-k material forming the gate dielectric layer 10 it can be advantageous to deposit a cap layer formed of a small amount of HfO_2, or another excellent oxygen conductor (this will help achieve reoxidation at a lower temperature or more rapidly).

A poly-Si layer 20 is formed by any convenient process, for example: chemical vapour deposition (CVD), plasma-assisted CVD, sputtering, etc., on the gate dielectric 10 (or on its capping layer, if applicable). At this stage, the poly-Si layer 20 will typically have a thickness of 10nm to 200nm. The technique used for depositing the poly-Si layer is not critical to the success of the invention. However, from a practical viewpoint, it is preferred to use a deposition technique that results in formation of a layer of fine-grained or columnar crystalline poly-Si (so as to oxidize rapidly during the lateral reoxidation step discussed below).

The poly-Si layer 20 is patterned in accordance with the desired dimensions of the gate electrode, to produce a structure as illustrated schematically in Fig.2B. Typically, after patterning, the poly-Si layer will have a length in the range 25 to 100nm depending on the technology node.

Any convenient process can be used for patterning the poly-Si layer 20, for example, in some cases a standard dry etch process can be used. If the

gate dielectric layer 10 is formed of a high-k material then the standard dry etch process can be modified in a known manner so as to ensure removal of the high-k dielectric from areas exposed during etching of the gate electrode, without creation of a recess in the underlying Si substrate.

After the gate electrode patterning has been performed, a controlled lateral oxidation process is performed in order to produce a barrier layer 30 of silicon dioxide (SiO_2) at the interface between the poly-Si material 20 and the gate dielectric 10, as shown in Fig.2C. The thickness of the oxide layer 30 is determined by the process conditions that are applied during the oxidation process.

A lateral reoxidation process can successfully produce a thin SiO_2 layer 30 between the HfO_2 gate dielectric 10 and the poly-Si layer 20. This is illustrated in Fig.3, which shows images produced using a transmission electron microscope (TEM). The images of Fig 3 were produced from a wafer that was processed, after polysilicon patterning, in a conventional high temperature 700-900°C thermal oxidation step.

Fig.3A shows the interface between the HfO_2 gate dielectric layer 10 and the poly-Si layer 20 before the lateral reoxidation process is performed. Fig.3B shows the interface after completion of the lateral reoxidation process. The barrier oxide layer 30 is labelled in Fig.3B.

In the example illustrated by Fig.3, the barrier layer 30 has a thickness of 0.8 nm (8 Angstroms). This is greater than the desired thickness but serves to demonstrate that the lateral reoxidation process is effective to produce a layer of SiO_2 between the high-k dielectric layer 10 and the overlying poly-Si layer 20.

To produce a SiO_2 layer of a sufficiently low thickness for practical application, grown by lateral oxidation, between the polysilicon and the high-k layers, it is advisable to use a low temperature 500-700°C oxidation in a batch-wafer furnace or a 600-800°C rapid thermal oxidation in a single wafer tool. Since it is difficult to estimate the thickness of laterally-grown SiO_2 on device wafers, the oxidation condition is verified on bare Si monitor wafers that are oxidized using the same conditions as the device wafers. The thickness of the laterally-grown SiO_2 will be much lesser than that grown on a bare SiO_2 wafer.

Further, the oxidation condition will depend on the gate dielectric material, particularly the oxygen diffusion properties of the material. Rapid lateral diffusion of oxygen through the dielectric layer will allow a shorter time and/or lower temperature oxidation sequence. HfO_2 allows fast diffusion of the oxygen laterally, while Hf-silicate allows slower diffusion. HfSiON will likely allow very slow oxygen diffusion, thereby requiring stronger (higher temperature or longer time) oxidation conditions. An oxidation condition that produces a target SiO_2 layer of 1-2nm on a bare silicon wafer is optimal for growing a thin SiO_2 layer between the gate dielectric layer 10 and the poly-Si layer 20 by lateral oxidation.

According to the preferred embodiment of the present invention, the thickness of the oxide barrier layer 30 should be related to the gate length. The extent of lateral oxidation across a patterned poly-Si line has a strong dependence on the oxidation temperature, partial pressure, time of oxidation, the permeability of oxygen through the dielectric, and a weak dependence on the oxidation rate of the polysilicon grain. The relationship is mathematically complex, but it has been found that the oxidation thickness saturates at a value determined by the diffusion limitation.

More particularly, it has been found to be advantageous to set the thickness of the oxide layer 30 to less than 10 angstroms (1 nm), for example to a value of 6 angstroms.

In principle, a minimum SiO_2 layer that is 1 monolayer or ~0.3nm thick will be sufficient to release the Fermi-level pinning and bring the Vt values for poly-Si on non-SiO_2 dielectric close to that of poly-Si on SiO_2. However, in practice, it may be difficult to ensure the uniform growth of a 0.3nm layer of SiO_2 by lateral reoxidation. As a practical matter, it is simple to set the oxidation conditions with the aim of producing a 0.5nm +/- 0.1nm SiO_2 layer. A SiO_2 layer of this thickness gives the benefit of Vt-shift reduction while only causing a limited increase in the EOT. This increase in EOT can be compensated by converting the poly-Si layer 20 to a fully-silicided form, making it possible to take advantage of the poly depletion gain (~0.4nm) obtained from use of the metal-like FUSI gate. With this choice of thickness and process conditions, the benefit of Vt reduction, or Vt matching with SiO_2 and poly depletion, can be achieved.

The subsequent steps in the method according to the preferred embodiment of the present invention (illustrated in Figs.2D to 2F) relate to the conversion of the poly-Si layer 20 to a fully-silicided form so as to constitute a FUSI gate electrode. However, before continuing with the description of these subsequent steps in the preferred method, it is useful to consider the properties of MOS devices based on the gate stack structure of Fig.2C, that is, devices having poly-Si gate electrodes.

The present inventor has found that the devices fabricated using the method according to the preferred embodiment of the invention have a reduced Vt shift as the gate length is scaled down. This improvement in device

performance is due to the thin barrier layer of oxide 30 that is produced by the above-described lateral reoxidation process.

The improved V_t shift can be seen from a consideration of Fig.4. Fig.4 relates to devices having the barrier oxide layer 30 produced by reoxidation (as described above), but poly-Si gate electrodes.

In Fig.4A there is a plot of gate length against Vt for a first group of PMOSFET structures fabricated using the method according to the above-described preferred embodiment as described so far, as well as for the first comparative example that uses a 2.5nm SiO_2 gate dielectric with a poly-Si gate electrode. This first group of PMOSFET structures according to the invention is based on the first group of comparative examples discussed above.

The first example according to the invention is a PMOSFET structure based on the above-described second comparative example; it uses a HfO_2 gate dielectric 3 nm thick (without a SiN_x capping layer) and, between the poly-Si gate electrode and the gate dielectric layer, there is an SiO_2 barrier layer formed by lateral oxidation under process conditions in a batch furnace so as to give a 2 nm thick SiO_2 layer on a bare wafer at 700°C. The exact thickness of this layer on the device wafer is seen by XTEM later. The results for this first example are indicated using hollow circles in Fig.4A.

The second example according to the invention is a PMOSFET structure based on the above-described third comparative example; it uses a HfO_2 gate dielectric 2.5 nm thick topped by a $HfSiO_x$ capping layer 1 nm thick and, between the poly-Si gate electrode and the gate dielectric layer, there is an SiO_2 barrier layer formed by lateral oxidation under process conditions in a

batch furnace so as to give a 2 nm thick barrier layer 30 at 700°C. The results for this second example are indicated using hollow triangles in Fig.4A.

A comparison of the results shown in Fig.1 for the 2nd Comparative Example (triangles) with the results shown in Fig.4A for the 1st Example (circles), shows that the lateral-oxidation-grown layer SiO_2 between the HfO_2 gate dielectric and the poly-Si gate electrode results in a reduction in the Vt-shift observed when using this high-k dielectric material. The reduction in Vt-shift is particularly apparent at shorter gate lengths.

A comparison of the results shown in Fig.1 for the 3rd Comparative Example (circles) with the results shown in Fig.4A for the 2nd Example (triangles), shows that, once again, the lateral-oxidation-grown SiO_2 between the $HfSiO_x$-capped HfO_2 gate dielectric and the poly-Si gate electrode results in a reduction in the Vt-shift observed when using this high-k dielectric material, especially at shorter gate lengths.

Fig. 4A demonstrates the concept that the Vt reduction by lateral oxidation is in fact realizable for the case where a furnace batch-wafer oxidation step was used. However, the thickness of the lateral-reoxidation-grown layer 30 in these examples is likely to be greater than necessary. Accordingly, the experiment was repeated using a rapid thermal oxidation single-wafer tool, which used a shorter time and lower temperature, enabling a thinner SiO_2 layer to be realized. Monitor wafer data showed that, in the repeated experiment, the EOT increase was < 0.8nm. This experiment showed that the effect of Vt reduction by lateral oxidation can be achieved using a thinner layer of SiO_2 also, with 1 monolayer being the theoretical limit.

In Fig.4B there is a plot of gate length against Vt for a second group of PMOSFET structures fabricated using the reoxidation method employed in the

above-described preferred embodiment, as well as for the first comparative example. This second group of PMOSFET structures all use a gate dielectric layer which is formed of a HfO_2 layer 2.5nm thick topped by a 1nm HfSiO capping layer, and all use poly-Si gate electrodes.

The third example is a PMOSFET structure having, between the HfSiO dielectric-capping layer and the poly-Si gate electrode, a laterally-grown SiO_2 layer (grown under rapid thermal oxidation conditions at 800°C and 1 Torr for 34 seconds - conditions which grow a 1nm oxide layer on a bare Si wafer). The results for this third example are indicated using hollow upright triangles in Fig.4B.

The fourth example is a PMOSFET structure having, between the HfSiO dielectric-capping layer and the poly-Si gate electrode, a laterally-grown SiO_2 layer (grown under rapid thermal oxidation conditions at 800°C and 1 Torr for 68 seconds – conditions which grow a <2nm thick oxide layer on a bare Si wafer). The results for this fourth example are indicated using hollow circles in Fig.4B (that is, triangles whose lower side is horizontal in the figure).

The fifth example is a PMOSFET structure having, between the HfSiO dielectric-capping layer and the poly-Si gate electrode, an oxide layer 30 formed by in-situ steam generation (ISSG) in a cold wall rapid thermal processing chamber, with the wafer held at 800°C for 26 seconds in N_2O at 12.5 Torr pressure (targeted to grow 1nm nominally on a bare Si wafer). The results for this fifth example are indicated using hollow sideways triangles in Fig.4B (that is, triangles whose lower side is inclined to the horizontal).

The sixth example according to the invention is a PMOSFET structure having, between the HfSiO dielectric-capping layer and the poly-Si gate electrode, an oxide layer 30 formed by ISSG in a cold wall rapid thermal

processing chamber, with the wafer held at 800°C for 52 seconds in N_2O at 12.5 Torr. The results for this sixth example are indicated using hollow diamonds in Fig.4B.

Fig 4B shows that even shorter oxidation sequences that occur with rapid thermal oxidation conditions are effective to achieve lateral oxidation resulting in Vt shift reduction.

The above results demonstrate that the formation of a thin oxide barrier layer between the high-k dielectric and the poly-Si electrode is effective to release Fermi-level pinning and provide an acceptable work function modulation. Moreover, poly depletion is improved. However, even when the thickness of the oxide barrier layer is minimized the creation of this oxide barrier layer leads to an increase of around 0.4 nm in the EOT at the gate. Accordingly, it is desirable to adopt some measure to counteract this increase in EOT.

It is known that devices using FUSI gates on high-k dielectrics or SiON have a significantly lower CETinv than comparable devices using poly-Si gates. In particular, a reduction in CETinv of around 0.3 nm can be seen in devices having FUSI gate electrodes compared to devices having poly-Si gate electrodes.

According to the preferred embodiments of the present invention, after the oxide barrier layer 30 has been formed, the poly-Si layer 20 is converted to a fully-silicided form to produce a FUSI-gate electrode, thereby reducing the EOT of the device.

Returning to Fig.2, the process for converting the poly-Si layer 20 to a FUSI gate electrode layer will now be described. After the barrier oxide layer 30 has been formed, a metal layer 40, typically nickel (Ni) or cobalt (Co), is deposited on the poly-Si layer 20, as indicated in Fig.2D. Typically, the nickel

layer is deposited by sputtering. It is deposited all over the wafer including the poly-Si and the surrounding active source/drain regions. Normally a spacer will be between the gate and the source/drain areas (so that silicidation occurs at the gate and the source and drain regions but not over the spacer, thus preventing a conductive path between the gate and source-drain regions).

The resulting gate stack structure is sintered typically at temperatures between 300-500°C whereby the metal species diffuses into the poly-Si, reacting with it fully (down to the interface with the barrier oxide 30). This produces a fully-silicided layer 50, as indicated in Fig.2E, whereby to produce the finished gate stack structure (ready for connection of contacts).

The layer 50 can have any desired thickness compatible with the poly-Si process. The thickness of the metallic layer 40 (e.g. Ni) is adjusted in dependence on the thickness of the poly-Si layer 20 so as to give full silicidation of the poly-silicon. The techniques and conditions necessary to produce FUSI gate electrodes are well-known to the skilled person and so no further details will be given here.

It has been found that the method according to the preferred embodiment of the present invention can produce MOS devices that have FUSI gate electrodes and high-k gate dielectric with adequate work function modulation. This makes it feasible to use devices having FUSI electrodes at the 65nm and 45nm technology nodes. Thus, it will still be possible to use conventional fabrication equipment even when ULSI device features are scaled down to 45/65 nm. More particularly, known processes and equipment can be used to implement the various steps of the present invention, with only minor adaptations being required in processing conditions for reoxidation or silicidation steps (whereby to ensure compatibility of these processes with the gate dielectric material and whereby to form a thin lateral-oxidation-grown SiO_2 layer).

Although the present invention has been described above with reference to a particular preferred embodiment, it is to be understood that the invention is not limited by reference to the specific details of this preferred embodiment. More specifically, the person skilled in the art will readily appreciate that, modifications and developments can be made in the preferred embodiment without departing from the scope of the invention as defined in the accompanying claims.

For example, in the above-described preferred embodiment a thin oxide layer is grown between a poly-Si layer formed on a high-k dielectric, notably a Hf-containing high-k dielectric. However, the present invention can be applied to grow an oxide layer between a poly-Si layer formed on other high-k dielectric materials, and on other non-SiO_2 dielectric materials, such as a SiON gate dielectric layer.

Furthermore, in the above-described preferred embodiment of the invention, the poly-Si layer was patterned to form the desired shape of the gate electrode before the lateral reoxidation step was performed. However, alternative approaches are possible. For example, a super-thin layer of poly-Si may be deposited over the dielectric layer 10 on the wafer, then fully oxidized, and then thinned down to an allowable thickness by etching.

Moreover, although the present invention has been described above in terms of embodiments relating to the fabrication of a gate stack structure for a MOSFET device, the present invention is applicable to the fabrication of other devices, notably devices where threshold voltage control is important but is harder to achieve when the dielectric is changed from SiO_2 to a non-SiO_2 dielectric (e.g. a high-k dielectric).

CLAIMS

1. A method of fabricating a MOS device, comprising the steps of:
forming a layer of gate dielectric material on a substrate; and
forming a layer of polycrystalline silicon on said gate dielectric layer;
characterised by comprising the step of forming a layer of oxide between said polycrystalline silicon layer and said gate dielectric layer after said layer of polycrystalline silicon has been formed on said layer of gate dielectric material.

2. The MOS device fabrication method of claim 1, wherein said oxide-layer formation step comprises process steps adapted to cause the formation of an oxide layer having a thickness of less than 1 nm.

3. The MOS device fabrication method of claim 1 or 2, and comprising the step of converting said polycrystalline silicon to a fully-silicided form.

4. The MOS device fabrication method of claim 1, 2 or 3, wherein said gate dielectric material is a high-k dielectric material.

5. The MOS device fabrication method of claim 4, wherein said gate dielectric material is a Hf-containing material.

6. The MOS device fabrication method of claim 1, 2 or 3, wherein said gate dielectric material is SiON.

7. A MOS device fabricated according to the method of any one of claims 3 to 6, comprising a gate dielectric and a FUSI gate electrode, wherein there is a layer of oxide between the gate electrode and the gate dielectric.

8. A MOS device according to claim 7, wherein the oxide layer between the gate electrode and the gate dielectric is less than 1 nm thick.

9. A MOS device according to claim 7 or 8, wherein the gate dielectric comprises a layer of high-k dielectric material.

10. A MOS device according to claim 7 or 8, wherein the gate dielectric comprises a layer of SiON.

AMENDED CLAIMS

[received by the International Bureau on 29 March 2006 (29.03.2006);
original claims 1-10 replaced by amended claims 1-9 (2 pages)]

1. A method of fabricating a MOS device, comprising the steps of:
forming a layer of gate dielectric material on a substrate; and
forming a layer of polycrystalline silicon on said gate dielectric layer;
characterised by comprising the steps of:
forming a layer of oxide between said polycrystalline silicon layer and said gate dielectric layer after said layer of polycrystalline silicon has been formed on said layer of gate dielectric material, and
converting said polycrystalline silicon to a fully-silicided form.

2. The MOS device fabrication method of claim 1, wherein said oxide-layer formation step comprises process steps adapted to cause the formation of an oxide layer having a thickness of less than 1 nm.

3. The MOS device fabrication method of claim 1 or 2, wherein said gate dielectric material is a high-k dielectric material.

4. The MOS device fabrication method of claim 3, wherein said gate dielectric material is a Hf-containing material.

5. The MOS device fabrication method of claim 1 or 2, wherein said gate dielectric material is SiON.

6. A MOS device fabricated according to the method of any one of claims 1 to 5, comprising a gate dielectric and a FUSI gate electrode, wherein there is a layer of oxide between the gate electrode and the gate dielectric.

7. A MOS device according to claim 6, wherein the oxide layer between the gate electrode and the gate dielectric is less than 1 nm thick.

8. A MOS device according to claim 6 or 7, wherein the gate dielectric comprises a layer of high-k dielectric material.

9. A MOS device according to claim 6 or 7, wherein the gate dielectric comprises a layer of SiON.

FIG.1

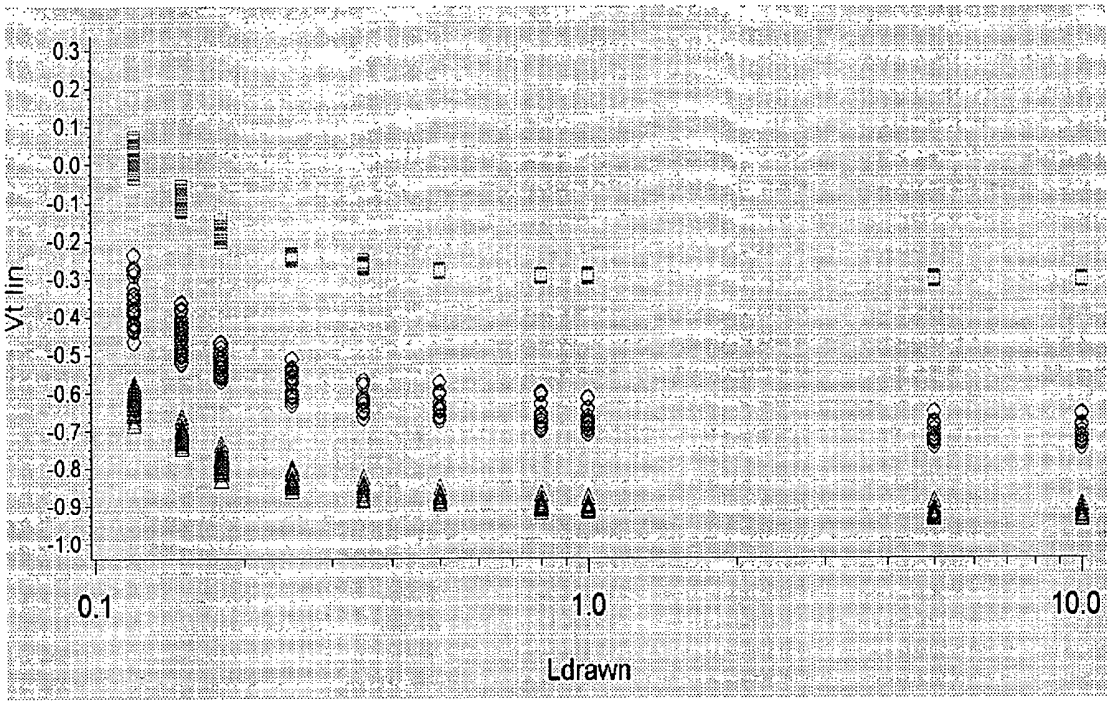

0.3
0.2
0.1
0.0
-0.1
-0.2
-0.3
-0.4
-0.5
-0.6
-0.7
-0.8
-0.9
-1.0
Vt lin
0.1
1.0
10.0
Ldrawn

FIG.4A

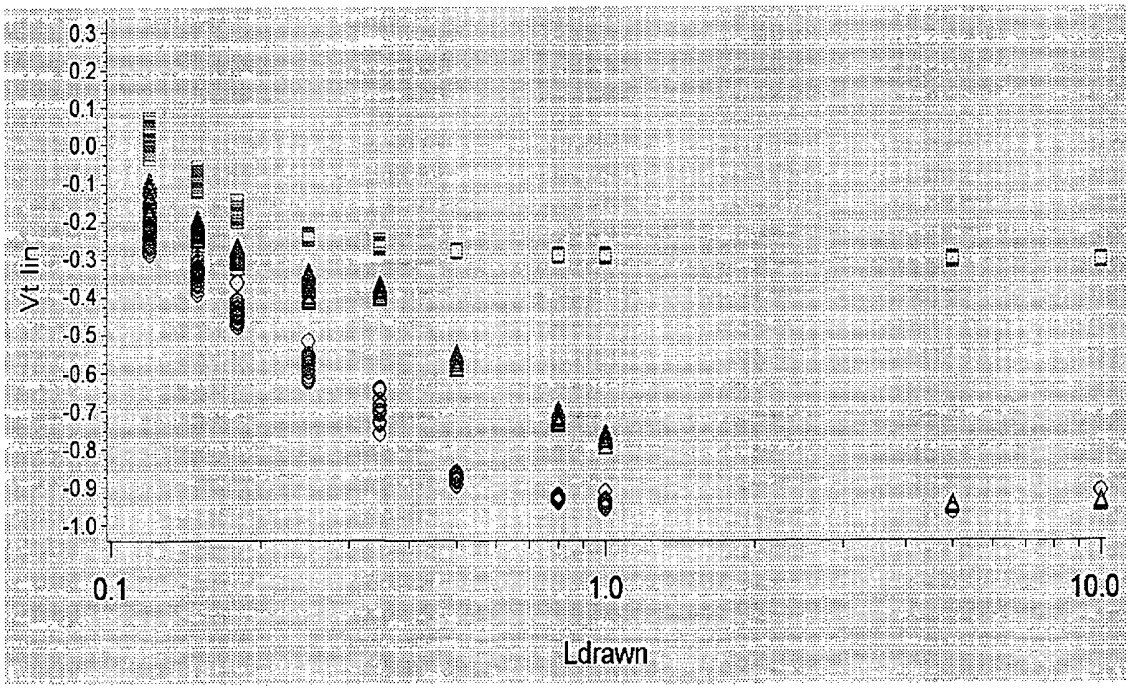

0.3
0.2
0.1
0.0
-0.1
-0.2
-0.3
-0.4
-0.5
-0.6
-0.7
-0.8
-0.9
-1.0
Vt lin
0.1
1.0
10.0
Ldrawn

FIG.2A

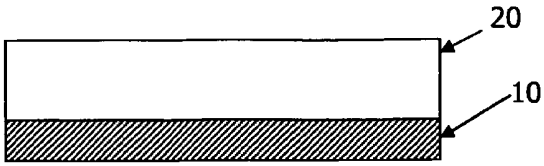


FIG.2B

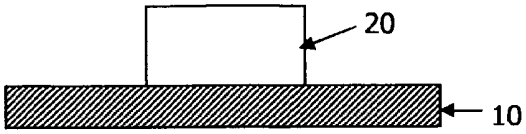


FIG.2C

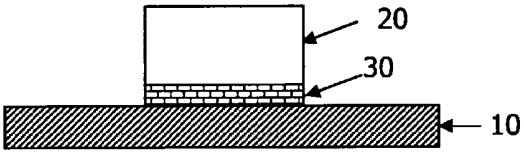


FIG.2D

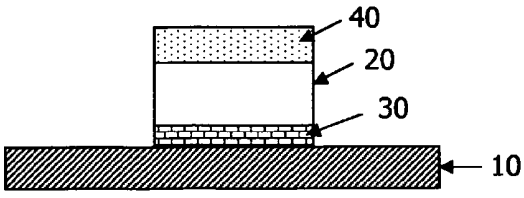


FIG.2E

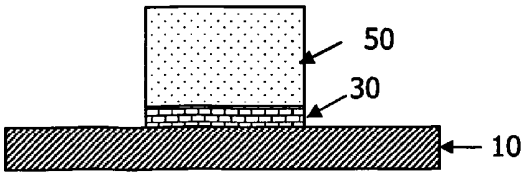


FIG.3A

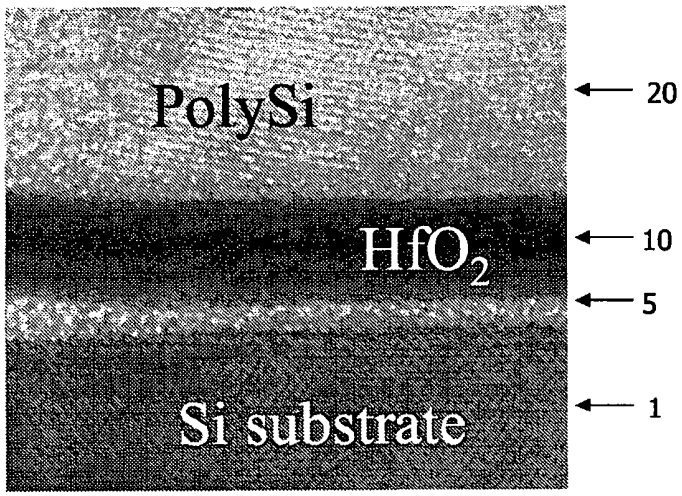

PolySi
HfO_2
Si substrate
20
10
5
1

FIG.3B

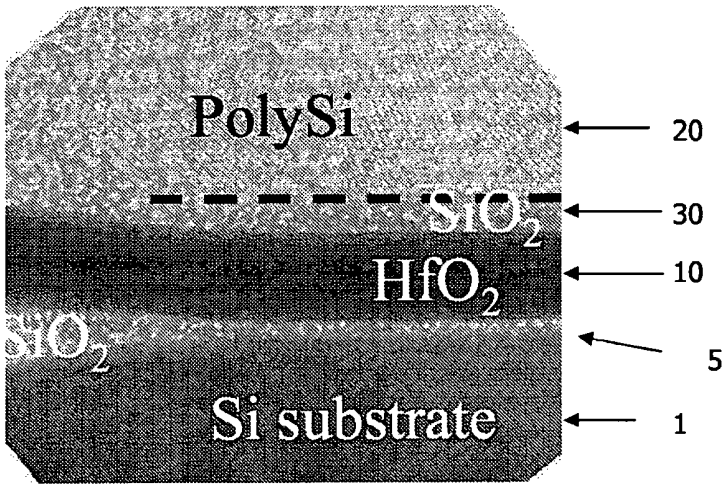
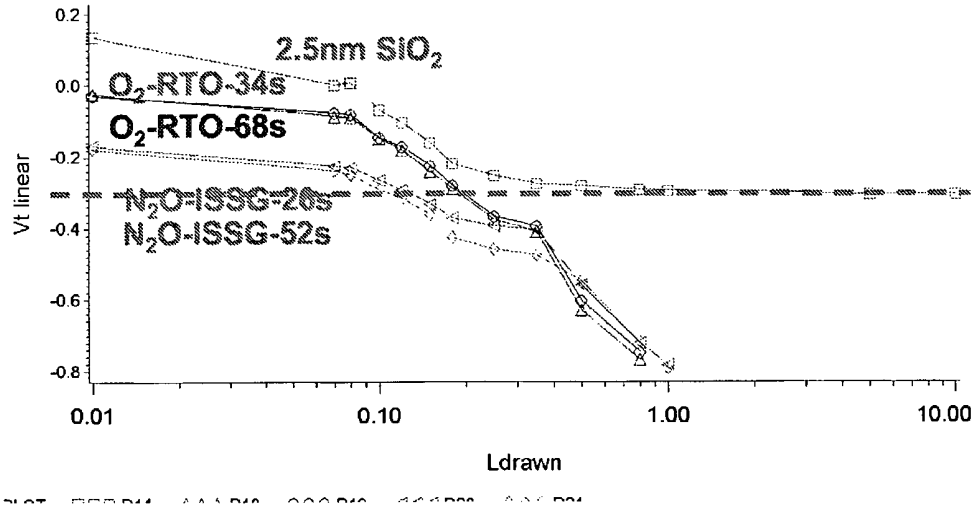

PolySi
SiO_2
HfO_2
SiO_2
Si substrate
20
30
10
5
1

FIG.4B


2.5nm SiO2
O2-RTO-34s
O2-RTO-68s
N2O-ISSG-26s
N2O-ISSG-52s
Vt linear
0.2
0.0
-0.2
-0.4
-0.6
-0.8
0.01
0.10
1.00
10.00
Ldrawn

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP2005/051784

A. CLASSIFICATION OF SUBJECT MATTER
H01L21/28 H01L29/51 H01L29/49

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	HOBBS C ET AL: "80 nm poly-si gate CMOS with Hf02 gate dielectric" INTERNATIONAL ELECTRON DEVICES MEETING 2001. IEDM. TECHNICAL DIGEST. WASHINGTON, DC, DEC. 2 - 5, 2001, NEW YORK, NY : IEEE, US, 2 December 2001 (2001-12-02), pages 3011-3014, XP010575209 ISBN: 0-7803-7050-3 figures 2,5 ----- -/--	1-10

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 December 2005	13/12/2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Nesso, S

Form PCT/ISA/210 (second sheet) (January 2004)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KUBICEK S ET AL: "Investigation of poly-Si/HfO2 gate stacks in a self-aligned 70nm MOS process flow" EUROPEAN SOLID-STATE DEVICE RESEARCH, 2003 33RD CONFERENCE ON. ESSDERC '03 SEPT. 16-18, 2003, PISCATAWAY, NJ, USA,IEEE, 16 September 2003 (2003-09-16), pages 251-254, XP010676621 ISBN: 0-7803-7999-4 paragraph '0002!	1-10
A	HOBBS C ET AL: "Sub-quarter micron Si-gate CMOS with ZrO2 gate dielectric" VLSI TECHNOLOGY, SYSTEMS, AND APPLICATIONS, 2001. PROCEEDINGS OF TECHNICAL PAPERS. 2001 INTERNATIONAL SYMPOSIUM ON APR 18-20, 2001, PISCATAWAY, NJ, USA,IEEE, 18 April 2001 (2001-04-18), pages 204-207, XP010551429 ISBN: 0-7803-6412-0 the whole document	1-10
A	MORISAKI Y ET AL: "ELECTRICAL PROPERTIES OF SIN/HFO2/SION GATE STACKS WITH HIGH THERMAL STABILITY" IEICE TRANSACTIONS ON ELECTRONICS, ELECTRONICS SOCIETY, TOKYO, JP, vol. E87-C, no. 1, January 2004 (2004-01), pages 37-43, XP001185940 ISSN: 0916-8524 paragraph '0002!; figure 2	1-10
A	US 6 287 897 B1 (GOUSEV EVGENI ET AL) 11 September 2001 (2001-09-11) figures 1-4	1-10
A	US 5 712 208 A (TSENG ET AL) 27 January 1998 (1998-01-27) the whole document	1-10
A	US 5 382 533 A (AHMAD ET AL) 17 January 1995 (1995-01-17) figures 2-4	1-10

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/EP2005/051784

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6287897 B1	11-09-2001	JP 3519056 B2	12-04-2004
		JP 2001274393 A	05-10-2001
		TW 517332 B	11-01-2003
US 5712208 A	27-01-1998	NONE	
US 5382533 A	17-01-1995	NONE	