

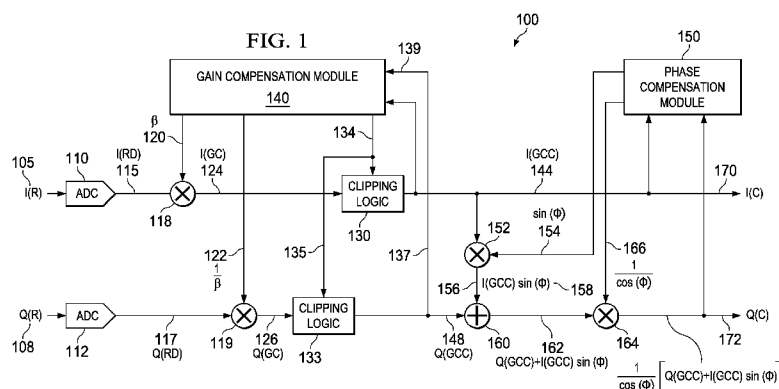


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- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
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[Continued on next page]

(54) Title: BLIND I/Q MISMATCH COMPENSATION APPARATUS AND METHODS

(57) **Abstract:** Apparatus and methods perform gain, clipping, and phase compensation in the presence of I/Q mismatch in quadrature RF receivers. Gain and phase mismatch are exacerbated by differences in clipping between I & Q signals in low resolution ADCs. Signals in the stronger channel arm are clipped differentially more than weaker signals in the other channel arm. Embodiments herein perform clipping operations during iterations of gain mismatch calculations in order to balance clipping between the I and Q channel arms (105 and 108, respectively). Gain compensation coefficients (120 and 122) are iteratively converged, clipping levels are established, and data flowing through the network (100) is gain and clipping compensated. A compensation phase angle and phase compensation coefficients (154 and 166) are then determined from gain and clipping compensated sample data. The resulting phase compensation coefficients are applied to the gain and clipping compensated receiver data (144 and 148) to yield a gain, clipping, and phase compensated data stream (on 170 and 172).

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BLIND I/Q MISMATCH COMPENSATION APPARATUS AND METHODS

[0001] This relates to apparatus and methods associated with electronic circuits, including RF receiver gain and phase mismatch compensation processing.

Background Information

BACKGROUND

[0002] Quadrature radio frequency (RF) signal transmission and reception exploits the concept that a single carrier wave may carry two independent data streams, provided that the data streams modulate the carrier in quadrature. For example, one of the data streams may modulate the carrier as a sine function and the other data stream may modulate the carrier as a cosine function. In any case, the two modulation streams must have a phase offset of 90° with respect to each other. The quadrature data streams are typically referred to as I data and Q data, representing an in-phase data stream and a data stream that is in quadrature with the in-phase data stream, that is, at a phase angle of 90° thereto.

[0003] A quadrature RF receiver splits the received signal into two paths, referred to herein as an “I arm” and a “Q arm.” The I signal is down-converted by mixing the received signal with an I-arm local oscillator (LO) carrier signal. The Q signal is likewise down-converted by mixing the received signal with a Q-arm LO carrier. Ideally, the Q-arm LO signal is of precisely the same magnitude as the I-arm LO signal and is exactly 90° out of phase with the I-arm LO signal. In actual practice, the I and Q arm LO signals often vary somewhat in magnitude and drift in phase away from perfect quadrature, creating a problem referred to as I/Q mismatch. Other factors such as non-ideal low-pass filter characteristics may also contribute to I/Q mismatch.

[0004] I/Q mismatch results in extraneous LO energy components in the image spectrum and the subsequent down-conversion of image spectrum interference. Said differently, I/Q mismatch results in decreased image rejection performance and lower SNRs.

[0005] In the presence of gain and phase mismatch, I and Q LO carriers may be mathematically modeled as:

$$C_I(t) = \cos(\omega t + \theta); \quad C_Q(t) = -\beta \sin(\omega t + \theta + \phi)$$

where ϕ represents phase mismatch between the two LO carriers and where β represents gain mismatch between the two LO carriers.

[0006] The resulting received, down-converted I and Q signals may be represented as:

$$\begin{aligned} I_R(t) &= I(t) \\ Q_R(t) &= \beta(Q(t) \cos \phi - I(t) \sin \phi) \end{aligned}$$

It is noted that the I and Q signals are not independent in the presence of I/Q mismatch as they are when in ideal quadrature with each other. Rather, the Q signal now includes an I signal component.

[0007] The gain imbalance β is estimated as:

$$\beta = \sqrt{\frac{\text{variance}(Q_R^2)}{\text{variance}(I_R^2)}} = \sqrt{\frac{\sigma_{Q_R}^2}{\sigma_{I_R}^2}}$$

[0008] The phase imbalance ϕ is estimated as:

$$\phi = \sin^{-1} \left(\frac{E[I_R \cdot Q_R] - E[I_R] \cdot E[Q_R]}{\sigma_{I_R} \sigma_{Q_R}} \right)$$

SUMMARY

[0009] Embodiments and methods herein perform gain and phase imbalance compensation in an RF quadrature receiver in the presence of non-linearities. Such non-linearities may be introduced in analog and/or digital sections of a quadrature receiver.

As an example used hereinunder, one such non-linearity may result from signal clipping in an analog-to-digital converter (ADC) used to digitally sample I and Q signals for further upstream digital processing. Some embodiments determine a clipping threshold associated with data samples in the I arm, the Q arm, or both. The clipping threshold is then applied to received and converted data in the I arm and/or the Q arm such as to balance a statistical distribution between data in the two arms.

[0010] Some embodiments and methods herein perform gain and phase imbalance compensation in an RF quadrature receiver in the presence of analog-to-digital (ADC) clipping artifacts. Q-arm/I-arm gain imbalance manifests itself as a difference in average AC signal power between I and Q signals as presented at the inputs of their respective ADCs. For purposes of convention in this disclosure, a positive gain imbalance shall mean that the average AC signal power in the Q arm is greater than the average AC signal power in the I arm. Likewise a stronger average AC signal power in the I arm shall be referred to herein as a negative gain imbalance. The higher-power arm, whether I-arm or Q-arm, shall be referred to as being “dominant.”

[0011] Data sample values at the output of an ADC should faithfully represent the gain imbalance in the analog signal at the ADC input at sampling time, assuming ADC clipping levels greater than peak signal levels. Conversely, an ADC with insufficient dynamic range will exacerbate the I/Q mismatch problem by disproportionately clipping whichever quadrature arm is dominant with respect to gain imbalance. Such difference in clipping complicates the task of gain and phase imbalance compensation. Gain imbalance as calculated from I and Q data sample averages is underestimated in the presence of clipping. The underestimation occurs because proportionally more signal power is lost through clipping from the dominant arm than from the lower-power arm. Clipping also biases phase imbalance estimates as a consequence of poor I/Q statistical correlation at time instances when I, Q, or both are clipped.

[0012] ADC hardware with sufficient dynamic range to prevent clipping in a high dynamic range signal environment may be too expensive to match the design goals

for a particular receiver type. Embodiments herein include clipping functions in the I and Q arms. The clipping functions perform additional clipping operations on data values in the non-dominant arm in order to balance clipping artifacts between the two arms. Balanced clipping and the balancing of other non-linearities in the I arm and Q arm contribute to matching statistical data distribution functions in the I and Q arms. Aligned data distribution functions associated with the receiver arms contribute to accurate gain & phase imbalance estimates. These embodiments and methods enable the use of lower-cost ADCs with correspondingly lower dynamic range. They may be particularly useful in RF receivers designed to process signals of high Peak-to-Average ratio (PAR) such as WLAN receivers and receivers processing highly Gaussian noise content such as GPS receivers

[0013] Embodiments herein iteratively estimate and apply gain compensation. Clipping levels are re-balanced at the start of each gain compensation iteration as further described below. Following convergence of the gain and clipping functions after a preset number of iterations, gain and clipping-corrected I and Q signals appear at inputs to a phase compensation portion of the gain and phase compensation network. The phase compensation network operates on one or more sets of I and Q data appearing at the phase compensation network output. A phase angle mismatch estimate calculated from the latter data is used to compensate for phase mismatch by subtracting the appropriate I signal component from the time-correlated Q signal and by factoring the Q signal according to the amount of phase mismatch.

[0014] Thus, apparatus and methods herein perform gain, clipping, and phase compensation and balancing according to various temporal sequences. Sequencing between gain/compensation training and normal live-data receiver operation may proceed variously according to system design requirements. In some embodiments, a full set of training sequences may be performed at receiver power-on or reset, or at the occurrence of some appropriate triggering event. For example, training sequences may be initiated upon sensing receiver temperature or supply voltage changes or other operating parameter conditions that could modify receiver channel gain/phase

characteristics. Some embodiments may perform full or partial training sequences continuously or at fixed intervals. Training sequence data may be discarded in some cases and/or passed on to subsequent stages during periods when the receiver is online and therefore expected to produce usable data at receiver outputs. Some embodiments herein may time-sample a live data stream for purposes of periodic or continuous gain and/or phase compensation in the presence of ADC-induced clipping.

[0015] Within certain constraints, embodiments herein may implement various schemes of sequencing between the functions of determining a gain compensation coefficient β and applying functions of ϕ to a gain and clipping compensated incoming data stream. In general, a selected or predetermined number of iterations of data capture and analysis yield a β and a scaled clipping level that will have converged to acceptably accurate values. These methods are recursive in that sample data is captured at the output of the gain/clipping portion of the method or network. Thus, a data sample used in the calculation of a new-iteration β value will itself have been factored by the previous-iteration β value and will have been artificially clipped by the previous-iteration scaled clipping level. It is noted, however, that some sequences of I data or Q data may be factored and/or clipped by a unity gain value, as further described below. For example, sample data used in the first iteration of β may be factored and clipped by a unity gain value, given that no value may yet exist for β .

[0016] According to these disclosed methods, gain compensation estimation uses clipping balancing at each iteration, as mentioned. The phase angle estimation and compensation scheme uses input data that has been gain and clipping compensated using the converged value of β . Consequently, embodiments herein determine and apply phase compensation during a sequence following gain/clipping training. Phase training yields the compensation phase angle ϕ . ϕ is converged to an accuracy that is dependent upon the number of data samples used to calculate ϕ but not dependent upon a number of iterations of calculations using different data sets. Thus, embodiments herein may perform phase training iteratively using multiple data sets or may perform a single calculation of ϕ following the acquisition of a larger single data set. It is noted that some

embodiments may perform clipping-compensated gain compensation in the absence of phase compensation. It is also noted that gain and/or phase compensation may be applied by the compensation network at any time in the future based upon previously-determined values of β and ϕ .

[0017] The invented structures and methods provide for gain, clipping, and phase compensation in the presence of I/Q mismatch exacerbated by differential clipping in low resolution I and Q ADCs. Improved image rejection performance may enhance receiver operation.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] FIG. 1 is a diagram of a gain and phase compensation network according to various example embodiments of the invention.

[0019] FIG. 2 is a flow diagram representing a method of performing gain and phase compensation in an RF quadrature receiver according to various example sequences.

[0020] FIG. 3 is a block diagram of a gain compensation module in a gain and phase compensation network according to various example embodiments.

[0021] FIG. 4 is a block diagram of a clipping logic module in a gain and phase compensation network according to various example embodiments.

[0022] FIG. 5 is a block diagram of a phase compensation module in a gain and phase compensation network according to various example embodiments.

[0023] FIG. 6 is a detailed flow diagram representing a method of performing gain and phase compensation in an RF quadrature receiver according to various example sequences.

[0024]

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0025] FIG. 1 is a diagram of a gain and phase compensation network 100 according to various example embodiments of the invention. Down-converted and filtered analog signals I(R) 105 and Q(R) 108 are received at ADCs 110 and 112,

respectively. The ADC's 110 and 112 convert the analog signals I(R) 105 and Q(R) 108 to digitally sampled data streams I(RD) 115 and Q(RD) 117, respectively.

[0026] The compensation network 100 includes an I-arm multiplier 118 and a Q-arm multiplier 119 communicatively coupled to the ADCs 110 and 112, respectively. The I-arm multiplier 118, the Q-arm multiplier 119, or both, factor one or more sets of received data samples from the I-arm data stream I(RD) 115 and/or the Q-arm data stream Q(RD) 117. I-arm data samples, if factored, are factored by a gain compensation coefficient β appearing at a multiplier input 120. Q-arm data samples, if factored, are factored by a gain compensation coefficient $1/\beta$ appearing at a clipping logic module input 122. Gain-compensated sets of I data and Q data samples I(GC) 124 and Q(GC) 126 result.

[0027] The compensation network 100 also includes an I-arm clipping logic module 130 communicatively coupled to the multiplier 118 and a Q-arm clipping logic module 133 communicatively coupled to the multiplier 119. The clipping logic modules 130 and 133 perform clipping operations on the gain compensated set of I data samples I(GC) 124, the gain compensated set of Q data samples Q(GC) 126, or both. "Clipping operations," in the context of the instant disclosure, means factoring data values whose magnitude is greater than a specified clipping level. In some embodiments, affected data values may be factored down to the specified clipping level. However, this disclosure contemplates other clipper factoring schemes as may be applicable to various clipping imbalances introduced by various ADC technologies and other receiver non-linearities. Clipping level information appears at the inputs 134 and 135 of the clipping logic modules 130 and 133, respectively. Gain and clipping compensated I data samples I(GCC) and Q data samples Q(GCC) result at the outputs 144 and 148 of the clipping logic modules 130 and 133, respectively.

[0028] The compensation network 100 further includes a gain compensation module 140 communicatively coupled to the multipliers 118 and 119 and to the clipping logic modules 130 and 133. The gain compensation module 140 buffers samples I(GCC) and Q(GCC) at the start of each of a first set of iterations corresponding to the

gain compensation function. The gain compensation module 140 processes the buffered data samples to determine an estimated gain compensation coefficient β , as further described below. The factor β or $1/\beta$ is associated with the gain compensation functions performed by the multiplier 118 in the I arm, the multiplier 119 in the Q arm, or both. At the start of the first iteration, a value for β will not yet be available. The gain compensation module 140 may thus process an uncompensated set of I(GCC) and Q(GCC) data to produce the first estimate of β .

[0029] The gain compensation module 140 also utilizes β and known ADC characteristics to establish a clipping threshold to send to clipping logic modules 130 and 133. The clipping threshold is associated with a clipping compensation function performed by clipping logic modules 130 and 133 following frequency conversion and ADC conversion and as further described below.

[0030] The compensation network 100 also includes a phase compensation module 150 communicatively coupled to the clipping logic module outputs 144 and 148. The phase compensation module 150 is also communicatively coupled to the compensation network 100 outputs 170 and 172. From the latter outputs, the phase compensation module buffers a set of gain, clipping, and phase compensated I and Q data samples at the start of each of a second set of iterations. It is noted that the first set of iterations is associated with obtaining converged gain and clipping compensation coefficients, as described above.

[0031] The phase compensation module 150 calculates an estimated phase compensation angle ϕ using the compensated data samples, as further described below. The phase compensation module 150 may directly estimate the phase imbalance compensation factor or may calculate trigonometric functions of ϕ to be used as factors to perform further compensation operations on the Q arm. Specifically, the phase compensation module 150 provides the factor $\sin(\phi)$ on control line 154 to the multiplier 152. The factor $I(\text{GCC}) * \sin(\phi)$ represents the component of I that was subtracted from Q as a consequence of the original I/Q mismatch with clipping. The latter factor is summed back into Q(GCC) at the summing junction 160 in order to perform this portion

of the compensation, resulting in the intermediate results $Q(GCC) + I(GCC) * \sin(\phi)$ at node 162. Finally, this intermediate result is factored in multiplier 164 by $1/\cos(\phi)$. The latter factor appears at input 166 from the phase compensation module 150. These operations compensate the Q-arm data to further conform I-arm and Q-arm data distribution functions.

[0032] FIG. 2 is a flow diagram representing a method 200 of performing gain and phase compensation in a trained RF quadrature receiver according to various example sequences. For purposes of this disclosure, "trained RF quadrature receiver" means that one or more iterations of gain, clipping, and/or phase compensation operations have been performed on sampled data to determine compensation coefficients and that the resulting compensation coefficients are currently applied in a compensation network such as the network 100 previously described.

[0033] The method 200 commences at blocks 205 and 210 with receiving a digitized sample of a down-converted I-arm signal and a digitized sample of a down-converted Q-arm signal (e.g., the digitized samples $I(RD)$, $Q(RD)$ of the down-converted signals $I(R)$, $Q(R)$, respectively, of FIG. 1).

[0034] The method 200 includes determining whether a previously calculated $\text{variance}(Q)$ value is greater than a corresponding previously calculated $\text{variance}(I)$ value, at block 215. If so, the method 200 includes factoring $I(RD)$ by a unity gain factor to obtain $I(GC)$, at block 218. The method 200 also includes factoring $Q(RD)$ by a gain compensation coefficient $1/\beta$ to obtain a gain compensated value $Q(GC)$, at block 220. In the case of $\text{variance}(Q)$ greater than $\text{variance}(I)$, the method 200 also includes performing clipping compensation by factoring certain but not all gain compensated I data values $I(GC)$. For all $|I(GC)|$ greater than $1/\beta * (\text{ADC_full-scale_value})$, the method 200 includes reducing $I(GC)$ to $1/\beta * (\text{ADC_full-scale_value})$ to obtain $I(GCC)$, at block 225. It is noted that clipping compensation may find nothing to clip from $Q(GC)$ data in this case, because $Q(GC)$ data has already been gain compensated down to the clipping threshold or below. Thus, in the latter case, $Q(GCC)$ is equal to $Q(GC)$.

[0035] If a previously calculated ratio of variance(Q) / variance(I) is less than one, the method 200 includes factoring Q(RD) by a unity gain factor to obtain Q(GC), at block 228. The method 200 also includes factoring I(RD) by a gain compensation coefficient β to obtain a gain compensated value I(GC), at block 230. To perform clipping balancing in the case of the previously calculated ratio of variance(Q) / variance(I) less than one, for all $|Q(GC)|$ greater than $\beta * (ADC_full-scale_value)$, the method 200 includes reducing Q(GC) to $\beta * (ADC_full-scale_value)$ to obtain Q(GCC), at block 235. It is noted that clipping compensation may find nothing to clip from I(GC) data in this case, because I(GC) data has already been gain compensated down to the clipping threshold or below. Thus, in the latter case, values of I(GCC) are equal to corresponding values of I(GC).

[0036] The method 200 continues at block 240 with noting that gain and clipping compensated I(GCC) values may pass through a phase compensation network (e.g. the phase compensation network of FIG. 1 at output 170) in an unaltered state. That is, again referring to FIG. 1, I(GCC) is equal to I(GC).

[0037] The method 200 includes factoring I(GCC) by $\sin(\phi)$ to obtain a phase correction component $I(GCC) * \sin(\phi)$, at block 245. The method 200 also includes adding $I(GCC) * \sin(\phi)$ to Q(GCC) to obtain an intermediate Q value $Q(GCC) + I(GCC) * \sin(\phi)$, at block 250. It is noted that Q(t) acquired a negative I(t) component during the process of being down-converted using non-ideal LOs. Here, the method 200 algebraically sums the $I(GCC) * \sin(\phi)$ factor out of the Q data stream. The method 200 also includes factoring $[Q(GCC) + I(GCC) * \sin(\phi)]$ by $1/\cos(\phi)$ to obtain a phase compensated Q value Q(C), at block 255.

[0038] FIG. 3 is a block diagram of a gain compensation module 140 in a gain and phase compensation network according to various example embodiments. The gain compensation module 140 includes I and Q sample buffers 310 and 312 to accept gain and clipping compensated sets of I and Q data samples for processing. The gain compensation module 140 also includes a sample buffer logic module 315 communicatively coupled to the I and Q sample buffers 310 and 312. The sample buffer

logic module 315 gates gain and clipping compensated sets of I and Q data samples into the I and Q sample buffers 310 and 312 at the start of a gain compensation iteration.

[0039] The gain compensation module 140 also includes an average total power module 320 communicatively coupled to the I and Q sample buffers 310 and 312. The average total power module 320 performs a first set of mathematical operations on the I and Q data samples as further described below. The first set of mathematical operations results in a value $I(\text{AVG_TOTAL})$ of average total power in the I arm and a value $Q(\text{AVG_TOTAL})$ of average total power in the Q arm.

[0040] The gain compensation module 140 further includes an average DC power module 324 communicatively coupled to the I and Q sample buffers 310 and 312. The average DC power module 324 performs a second set of mathematical operations on the I and Q data samples as further described below. The second set of mathematical operations results in a value $I(\text{AVG_DC})$ of average DC power in the I arm and a value $Q(\text{AVG_DC})$ of average DC power in the Q arm.

[0041] The gain compensation module 140 also includes a variance power module 328 communicatively coupled to the average total power module 320 and to the average DC power module 324. The variance power module 328 subtracts $I(\text{AVG_DC})$ from $I(\text{AVG_TOTAL})$ to obtain a variance(I) of average AC signal power in the I arm. The variance power module 328 also subtracts $Q(\text{AVG_DC})$ from $Q(\text{AVG_TOTAL})$ to obtain a variance(Q) of average AC signal power in the Q arm. The gain compensation module 140 also includes an I, Q variance power comparator 330 communicatively coupled to the variance power module 328. The I, Q variance power comparator 330 determines whether the I arm or the Q arm is gain-dominant. Gain dominance determines whether gain factoring or clipping balancing is applied to the I arm or Q arm.

[0042] The gain compensation module 140 also includes a previous gain compensation estimate buffer 340 communicatively coupled to the variance power module 328. The previous gain compensation estimate buffer 340 stores a cumulative gain compensation estimate $\beta(\text{PREV})$ calculated during previous iterations. The gain compensation module 140 further includes a gain compensation estimation module 342

communicatively coupled to the variance power module 328 and to the previous gain compensation estimate buffer 340. The gain compensation estimation module 342 calculates the square root of the ratio of variance(Q) to variance(I) to obtain a current gain compensation estimate $\beta(\text{CURRENT})$. The gain compensation estimation module 342 also adds $\beta(\text{CURRENT})$ to $\beta(\text{PREV})$ to obtain a cumulative gain compensation estimate $\beta(\text{CUMULATIVE})$. $\beta(\text{CUMULATIVE})$ or its reciprocal is presented at output 350 to be used as a factoring coefficient by the multipliers 118 and 119 of FIG. 1, subject to additional criteria described below. $\beta(\text{CUMULATIVE})$ is also stored in the previous gain compensation estimate buffer 340 as a new $\beta(\text{PREV})$ for use in the next iteration.

[0043] The gain compensation module 140 also includes a clipping threshold estimation module 344 communicatively coupled to the variance power module 328. The clipping threshold estimation module 344 calculates a clipping logic threshold value proportional to a product of $\beta(\text{CUMULATIVE})$ and an ADC full-scale value. The ADC full-scale value is stored in a buffer 346 communicatively coupled to the clipping threshold estimation module 344. The resulting clipping logic threshold value is sent to the clipping logic modules 130 and 133 of FIG. 1 on output 354 to balance clipping levels in the I and Q arms at each iteration during gain compensation convergence.

[0044] The gain compensation module 140 further includes an iteration control module 360 communicatively coupled to the sample buffer logic module 315 and to the gain compensation estimation module 342. The iteration control module 360 controls successive iterations of compensated data sampling, gain compensation estimation, and clipping threshold estimation. A buffer 362 is communicatively coupled to the iteration control module 362 store a number of iterations of P as specified by design criteria to achieve a desired level of convergence of the gain compensation coefficient $\beta(\text{CUMULATIVE})$.

[0045] FIG. 4 is a block diagram of a clipping logic module 400 in a gain and phase compensation network according to various example embodiments. The clipping logic module 400 includes clipping level logic 405 to calculate a clipping level. The

clipping level logic 405 receives the cumulative gain compensation estimate $\beta(\text{CUMULATIVE})$ at an input 415 and a value 420 representing maximum ADC signal range at an input 422. Both values are received from the gain compensation module 140. The clipping level is calculated as the absolute value of the largest digital value capable of representation by the applicable ADC factored by $\beta(\text{CUMULATIVE})$. For example, assume a six-bit ADC capable of a maximum value of $|(2^6)/2| = 32$. If $\beta(\text{CUMULATIVE})$ were equal to 0.75, the clipping level logic 405 would, in this example, calculate the clipping level as $32 * 0.75 = 24$.

[0046] The clipping logic module 400 also includes a comparator 425 communicatively coupled to the clipping level logic 405. The comparator 425 receives a gain compensated sample value $I(\text{GC})$ or $Q(\text{GC})$ and compares the sample value to the clipping level. The clipping logic module 400 further includes a clipper 430 coupled to the comparator 425. The clipper 430 factors the magnitude of the gain compensated sample value down to the clipping level if the gain compensated sample value exceeds the clipping level. A gain and clipping level compensated output value $I(\text{GCC})$ or $Q(\text{GCC})$ appears at the output 440 of the clipping logic module 400.

[0047] FIG. 5 is a block diagram of a phase compensation module 150 in a gain and phase compensation network according to various example embodiments. The phase compensation module 150 operates on clipping-corrected data. That is, I-arm and Q-arm signal distributions are normalized with respect to each other as received at the phase compensation portion of the network 100. Phase compensation is more accurate as a result.

[0048] The phase compensation module 150 includes a compensated data sampling and power calculation module 505. The compensated data sampling and power calculation module 505 includes I and Q sample buffers 510 and 512, a sample buffer logic module 515, total power and DC power modules 520 and 524, and a variance power module 528. The included modules operate as previously described with reference to the gain compensation module 140 to obtain a variance(I) of average AC signal power in the I arm and a variance(Q) of average AC signal power in the Q arm. It

is noted, however, that the modules 510, 512, 515, 520, 524 operate on data samples from the I(C) and Q(C) outputs 170 and 172 of the gain, clipping, and phase compensation network 100 of FIG. 1.

[0049] The phase compensation module 150 also includes a standard deviation module 530 communicatively coupled to the compensated data sampling and power calculation module 505. The standard deviation module 530 calculates a standard deviation of I $\sigma(I)$ as a square root of the variance(I) and a standard deviation of Q $\sigma(Q)$ as a square root of the variance(Q).

[0050] The phase compensation module 150 further includes an I-dot-Q expectation module 540 communicatively coupled to the compensated data sampling and power calculation module 505. The I-dot-Q expectation module 540 calculates a mathematical expectation $E[I \cdot Q]$ of the dot product of the I data samples and the Q data samples.

[0051] The phase compensation module 150 also includes I and Q expectation modules 544 and 548 communicatively coupled to the compensated data sampling and power calculation module 505. The I and Q expectation modules 544 and 548 calculate mathematical expectations $E[I]$ and $E[Q]$ of the I and Q data samples, respectively.

[0052] The phase compensation module 150 also includes a biased phase estimation module 550 communicatively coupled to the I-dot-Q expectation module 540 and to the standard deviation module 530. The biased phase estimation module 550 calculates a DC-biased phase angle compensation estimate $\phi(\text{CURRENT_BIASED})$ equal to $\arcsin \{E[I \cdot Q] / \sigma(I) * \sigma(Q)\}$.

[0053] A DC phase estimation module 552 is communicatively coupled to the I expectation module 544, the Q expectation module 548, and the standard deviation module 530. The DC phase estimation module 552 calculates a DC component $\phi(\text{DC})$ of the DC-biased phase angle compensation estimate $\phi(\text{CURRENT_BIASED})$. The DC component $\phi(\text{DC})$ is equal to an arcsine of a dot product of the expectation $E[I]$ and the expectation $E[Q]$ divided by $\sigma(I) * \sigma(Q)$.

[0054] The phase compensation module 150 also includes a phase angle determination module 555 communicatively coupled to the biased phase estimation module 550 and to the DC phase estimation module 552. The phase angle determination module 555 subtracts $\phi(\text{DC})$ from $\phi(\text{CURRENT_BIASED})$ to obtain a current unbiased phase correction angle $\phi(\text{CURRENT_UNBIASED})$. The phase angle determination module 555 also adds $\phi(\text{CURRENT_UNBIASED})$ to a cumulative phase estimate $\phi(\text{PREV})$ accrued from previous iterations to obtain $\phi(\text{CUMULATIVE})$. $\phi(\text{CUMULATIVE})$ is made available to the phase compensation network on output 556. A previous phase angle estimation module 558 stores the cumulative previously calculated phase estimate $\phi(\text{PREV})$ between iterations.

[0055] The phase compensation module 150 further includes an iteration control module 560 communicatively coupled to the compensated data sampling and power calculation module and to the phase angle determination module 555. The iteration control module 560 controls successive iterations of compensated data sampling and phase angle compensation estimation. A buffer 562 stores a desired number of iterations, R. It is noted, however, that some embodiments may determine the phase compensation angle in a single iteration, as previously described.

[0056] FIG. 6 is a detailed flow diagram representing a method 600 of performing gain and phase compensation in an RF quadrature receiver according to various example sequences. The method 600 includes performing a first set of iterations to determine an estimated gain compensation coefficient associated with a gain compensation function in a receiver I arm, Q arm, or both. The method 600 also includes determining a clipping threshold associated with a clipping compensation function in the I arm, the Q arm, or both.

[0057] Each iteration operates on a gain and clipping compensated set of I data samples and Q data samples. The samples are captured at the I and Q data outputs of a gain and clipping compensation network associated with the receiver (e.g., the outputs 144 and 148 of FIG. 1) following frequency conversion and ADC conversion. The

samples are buffered for processing during a sampling period at the start of each iteration.

[0058] The method 600 also includes factoring a set of received I data samples and received Q data samples using the gain compensation function. A current gain compensated set of I data and Q data samples results. The method 600 further includes performing clipping operations on the current gain compensated set of I data samples and Q data samples using the clipping compensation function. A current gain and clipping compensated set of I data samples and Q data samples results. The latter samples are used as input data to a next one of the first set of iterations. One skilled in the art will note that this portion of the method 600 is recursive with regard to sample data sets following the first set captured and processed.

[0059] Following completion of the first set of iterations, the method 600 proceeds with determining a phase correction angle ϕ and coefficients associated with a phase compensation function in the Q-arm of the quadrature receiver channel. The phase correction angle ϕ is determined from one or more gain and clipping compensated sets of I data samples and one or more sets of gain, clipping, and phase compensated Q data samples. The method 600 also includes using the phase compensation function in the Q-arm to factor one or more gain and clipping compensated Q data samples. A corresponding number of Q data samples compensated for gain and phase mismatch in the presence of ADC clipping result.

[0060] Referring to FIG. 6A, the method 600 commences at block 605 with initiating a gain and phase compensation training sequence. The method 600 continues at block 608 with buffering N samples of I-arm data I(GCC) and N samples of Q-arm data Q(GCC) as received at gain compensation network outputs (e.g. the outputs 144 and 148 of FIG. 1). The method 600 includes mathematically squaring each I sample and each Q sample individually, at block 610. The method 600 also includes adding the squared I samples together and dividing by N to obtain a value I(AVG_TOTAL) of average total signal power in the I arm during the sampling period, at block 612. The method 600 further includes adding the squared Q samples together and dividing by N to

calculate a value $Q(\text{AVG_TOTAL})$ of average total signal power in the Q arm during the sampling period, at block 614.

[0061] The method 600 continues at block 616 with adding all non-squared I samples together, dividing by N, and squaring to obtain a value $I(\text{AVG_DC})$ of average power of a DC signal component in the I arm during the sampling period. The method 600 also includes adding all non-squared Q samples together, dividing by N, and squaring to obtain a value $Q(\text{AVG_DC})$ of average power of a DC signal component in the Q arm during the sampling period, at block 618.

[0062] The method 600 includes subtracting $I(\text{AVG_DC})$ from $I(\text{AVG_TOTAL})$ to obtain a variance(I) representing an average AC signal power in the I arm, at block 620. The method 600 further includes subtracting $Q(\text{AVG_DC})$ from $Q(\text{AVG_TOTAL})$ to obtain a variance(Q) representing an average AC signal in the Q arm, at block 622.

[0063] The method 600 proceeds at block 624 with dividing the variance(Q) by the variance(I) to obtain a ratio of variances and finding a square root of the ratio of variances to obtain a current estimate $\beta(\text{CURRENT})$ of a gain compensation coefficient β .

[0064] The method 600 also includes adding a prior cumulative total $\beta(\text{PRIOR})$ of previously-calculated gain compensation estimates to $\beta(\text{CURRENT})$ to obtain a new cumulative gain compensation estimate $\beta(\text{CUMULATIVE})$, at block 626.

[0065] The method 600 continues at block 630 with determining whether previously-calculated variance(Q) is greater than variance(I). If not, the method 600 includes adjusting I-arm gain compensation to $\beta(\text{cumulative})$, at block 632. In this case the method 600 also includes setting a clipping logic threshold value. The clipping threshold value is set equal to a product of $\beta(\text{cumulative})$ and a full-scale value associated with ADCs used to convert the I and Q signals, at block 634.

[0066] If previously-calculated variance(Q) is greater than variance(I), the method 600 includes adjusting the Q arm gain compensation to $1/\beta(\text{cumulative})$, at block 636. The method 600 also, in this case, includes setting the clipping logic threshold value equal to a product of $1/\beta(\text{cumulative})$ and the ADC full-scale value, at block 638.

[0067] The method 600 continues at block 640 with determining whether a predetermined number P of gain compensation iterations have occurred. If P iterations have not occurred, the method 600 includes incrementing a gain iteration counter by one, at block 642, and initiating another iteration, at block 644. The method 600 repeats at block 608 with buffering a new set of N samples of I arm data $I(GCC)$ and N samples of Q arm data $Q(GCC)$ from gain compensation network outputs and determining updated values for β (cumulative) and clipping logic coefficients.

[0068] If the predetermined number of gain compensation iterations P has occurred, the method 600 continues at block 650 with starting a phase correction sequence. The phase correction sequence commences at block 652 with buffering M samples of gain, clipping, and phase-compensated I-arm data and M samples of gain, clipping, and phase-compensated Q-arm data (e.g., as received at phase compensation network outputs $I(C)$ and $Q(C)$ of FIG. 1);

[0069] The method 600 proceeds with mathematically squaring each I sample and each Q sample, at block 654. The method 600 also includes adding the squared results of all I data samples and dividing by M to obtain a value $I(AVG_TOT)$ of average total I-arm signal power in I-arm data, at block 656. The method 600 further includes adding the squared results of all Q data samples and dividing by M to obtain a value $Q(AVG_TOTAL)$ of average total Q-arm signal power in Q-arm data, at block 658.

[0070] The method 600 also includes adding all I samples together, dividing the resulting sum by M , and squaring the quotient to obtain a value $I(AVG_DC)$ of average power of a DC signal component in the I arm, at block 660. Likewise the method 600 includes adding all Q samples together, dividing the resulting sum by M , and squaring the quotient to obtain a value $Q(AVG_DC)$ of average power of a DC signal component in the Q arm, at block 662.

[0071] The method 600 continues at block 664 with subtracting the average I arm DC signal component $I(AVG_DC)$ from total I signal power $I(AVG_TOTAL)$ to obtain a variance(I) corresponding to average AC signal power in the I arm. Likewise,

the method 600 includes subtracting the average Q arm DC signal component $Q(\text{AVG_DC})$ from total Q signal power $Q(\text{AVG_TOTAL})$ to obtain a variance(Q) corresponding to average AC signal power in the Q arm, at block 668.

[0072] The method 600 also includes determining a square root of the variance(I) to obtain a standard deviation of I, $\sigma(I)$, at block 670. Likewise the method 600 includes determining a square root of the variance(Q) to obtain a standard deviation of Q $\sigma(Q)$, at block 672.

[0073] The method 600 includes multiplying each I, Q sample pair, summing the resulting products, and dividing by M to obtain $E[I \cdot Q]$, an expectation of a dot product of I and Q, at block 676. The method 600 also includes dividing $E[I \cdot Q]$ by a product of $\sigma(I)$ and $\sigma(Q)$ to obtain the trigonometric sine of a current DC-biased phase error estimate $\phi(\text{CURRENT_BIASED})$, at block 678.

[0074] The method 600 also includes summing all I sample values and dividing the result by M to obtain $E[I]$, an expectation of I, at block 680. The Q samples are also summed and divided by M to obtain $E[Q]$, an expectation of Q, at block 681.

[0075] The method 600 continues at block 682 with multiplying $E[I]$ by $E[Q]$ and dividing the result by the product of $\sigma(I)$ and $\sigma(Q)$ to obtain the sine of a DC bias component $\phi(\text{DC})$ of $\phi(\text{CURRENT_BIASED})$.

[0076] The method 600 includes subtracting $\phi(\text{DC})$ from $\phi(\text{CURRENT_BIASED})$ to obtain a current, unbiased phase correction estimate $\phi(\text{CURRENT_UNBIASED})$, at block 684.

[0077] The method 600 further includes adding $\phi(\text{CURRENT_UNBIASED})$ to a previous phase estimate $\phi(\text{PREV})$ to obtain a new cumulative phase correction estimate $\phi(\text{CUMULATIVE})$, at block 686.

[0078] The method 600 also includes configuring the phase compensation network to factor the Q arm by $[1/\text{COS}(\phi(\text{CUMULATIVE}))] * [Q(\text{GCC} + I(\text{GCC}) * \text{SIN}(\phi(\text{CUMULATIVE})))]$ at block 688.

[0079] The method 600 continues with comparing the phase iteration index R to a maximum iteration index, $R(\text{MAX})$, at block 690. If the maximum number of

iterations has not occurred, the method 600 includes incrementing the index R, at block 692, and initiating an additional phase angle correction iteration, at block 694. It is noted that R(MAX) may be set equal to 1 in some example sequences in order to implement a single-iteration phase angle correction estimate and associated coefficients.

[0080] If $R = R(\text{MAX})$, the method 600 includes awaiting another gain/phase correction training sequence opportunity as triggered by an expiration of a timeout period or other selected trigger parameter(s), at block 696.

[0081] Modules and components described herein may include hardware circuitry, optical components, single or multi-processor circuits, memory circuits and/or computer-readable media with computer instructions encoded therein/thereon capable of being executed by a processor, including non-volatile memory with firmware stored therein, but excluding non-functional descriptive matter, and combinations thereof, as desired by the architects of the apparatus 100, 140, 150, and 400 and the methods 200 and 600 and as appropriate for particular implementations of various embodiments.

[0082] Apparatus and methods described herein may be useful in applications other than determining gain, clipping, and phase training coefficients and applying them in an RF quadrature receiver. Other applications may exist for the described methods and apparatus. Examples of the apparatus 100, 140, 150, and 400 and the methods 200 and 600 are intended to provide a general understanding of the flow of various sequences and the structures of various embodiments. They are not intended to serve as complete descriptions of all elements and features of apparatus and systems that might make use of these sequences and structures.

[0083] The various embodiments may be incorporated into electronic circuitry used in lighting control systems, computers, communication and signal processing circuitry, single-processor or multi-processor modules, single or multiple embedded processors, multi-core processors, data switches, and application-specific modules including multi-layer, multi-chip modules, among others. Such apparatus and systems may further be included as sub-components within a variety of electronic systems, such as televisions, cellular telephones, personal computers (e.g., laptop computers, desktop

computers, handheld computers, tablet computers, etc.), workstations, radios, video players, audio players (e.g., MP3 (Motion Picture Experts Group, Audio Layer 3) players), vehicles, medical devices (e.g., heart monitor, blood pressure monitor, etc.), set top boxes, and others.

[0084] Apparatus and methods described herein perform quadrature RF receiver gain, clipping, and phase compensation in the presence of I/Q mismatch exacerbated by differential clipping in low resolution I and Q ADCs. Improved image rejection performance may result.

[0085] Those skilled in the art will appreciate that modifications may be made to the described embodiments, and also that many other embodiments are possible, within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. A quadrature signal processing method, comprising:
 - determining a clipping threshold associated with data samples in at least one of an I arm or a Q arm in a quadrature receiver channel following frequency conversion and analog-to-digital (ADC) conversion; and
 - applying the clipping threshold to received and converted data in the I arm or the Q arm such as to balance a statistical distribution between data in the I arm and data in the Q arm.
2. The method of claim 1, further comprising:
 - during a first set of iterations, determining, from a gain and clipping compensated set of I data samples and Q data samples captured during a sampling period at a start of each iteration, an estimated gain compensation coefficient associated with a gain compensation function in at least one of the I arm or the Q arm and a clipping threshold associated with a clipping compensation function in at least one of the I arm or the Q arm of the quadrature receiver channel following frequency conversion and analog-to-digital (ADC) conversion;
 - factoring a set of received I data samples and Q data samples using the gain compensation function to obtain a current gain compensated set of I data and Q data samples; and
 - performing clipping operations on the current gain compensated set of I data samples and Q data samples using the clipping compensation function to obtain a current gain and clipping compensated set of I data samples and Q data samples to use as input data to a next one of the first set of iterations.
3. The method of claim 2, further comprising:
 - following completion of the first set of iterations, determining, from at least one gain and clipping compensated set of I data samples and at least one gain, clipping, and phase compensated set of Q data samples, a phase correction angle ϕ and coefficients

associated with a phase compensation function in the Q-arm of the quadrature receiver channel; and

factoring at least one gain and clipping compensated Q data sample using the phase compensation function in the Q-arm to obtain a Q data sample compensated for gain and phase mismatch in the presence of ADC clipping.

4. The method of claim 2, further comprising:

buffering N samples of I-arm data $I(GCC)$ and N samples of Q-arm data $Q(GCC)$ as received at gain compensation network outputs;

mathematically squaring each I sample and each Q sample;

adding squared I samples together and dividing by N to obtain a value $I(AVG_TOTAL)$ of average total signal power in the I arm during the sampling period;

adding squared Q samples together and dividing by N to calculate a value $Q(AVG_TOTAL)$ of average total signal power in the Q arm during the sampling period;

adding all non-squared I samples together, dividing by N, and squaring to obtain a value $I(AVG_DC)$ of average power of a DC signal component in the I arm during the sampling period;

adding all non-squared Q samples together, dividing by N, and squaring to obtain a value $Q(AVG_DC)$ of average power of a DC signal component in the Q arm during the sampling period;

subtracting $I(AVG_DC)$ from $I(AVG_TOTAL)$ to obtain a variance(I) representing an average AC signal power in the I arm; and

subtracting $Q(AVG_DC)$ from $Q(AVG_TOTAL)$ to obtain a variance(Q) representing an average AC signal in the Q arm.

5. The method of claim 4, further comprising:

dividing the variance(Q) by the variance(I) to obtain a ratio of variances;

finding a square root of the ratio of variances to obtain a current estimate $\beta(\text{current})$ of a gain compensation coefficient β ; and

adding a prior cumulative total $\beta(\text{prior})$ of previously-calculated gain compensation estimates to at least one of $\beta(\text{current})$ or a function of $\beta(\text{current})$ to obtain a new cumulative gain compensation estimate $\beta(\text{cumulative})$.

6. The method of claim 5, further comprising:

adjusting I-arm gain compensation to $\beta(\text{cumulative})$ if the variance(Q) is less than the variance(I);

setting a clipping logic threshold value equal to a product of $\beta(\text{cumulative})$ and a full scale value associated with analog-to-digital converters (ADCs) used to convert the I and Q signals if the variance(Q) is less than the variance(I);

adjusting the Q arm gain compensation to $1/\beta(\text{cumulative})$ if the variance(Q) is greater than or equal to the variance(I); and

setting the clipping logic threshold value equal to a product of $1/\beta(\text{cumulative})$ and the ADC full-scale value if the variance(Q) is greater than or equal to the variance(I).

7. The method of claim 6, further comprising:

determining whether a predetermined number of gain compensation iterations have occurred;

if the predetermined number of gain compensation iterations has not occurred, incrementing a gain iteration counter by one;

buffering a new set of N samples of I arm data I(GCC) and N samples of Q arm data Q(GCC) from gain compensation network outputs;

determining updated values for $\beta(\text{cumulative})$ and clipping logic coefficients;

if a predetermined number of gain compensation iterations have occurred, continuing with a phase correction sequence.

8. The method of claim 1, further comprising:

buffering M samples of gain-compensated, clipping-corrected, and phase-compensated I-arm data and M samples of gain-compensated, clipping-corrected, and

phase-compensated Q-arm data as received at phase compensation network outputs $I(C)$ and $Q(C)$;

mathematically squaring each I sample, summing the squares, and dividing by M to obtain a value $I(AVG_TOTAL)$ of average total I-arm signal power in I-arm data;

mathematically squaring each Q sample, summing the squares, and dividing by M to obtain a value $Q(AVG_TOTAL)$ of average total Q-arm signal power in Q-arm data;

9. The method of claim 8, further comprising:

adding all I samples together, dividing by M, and squaring to obtain a value $I(AVG_DC)$ of average power of a DC signal component in the I arm;

adding all Q samples together, dividing by M, and squaring to obtain a value $Q(AVG_DC)$ of average power of a DC signal component in the Q arm;

Subtracting the average I arm DC signal component $I(AVG_DC)$ from total I signal power $I(AVG_TOTAL)$ to obtain a variance(I) corresponding to average AC signal power in the I arm;

determining a square root of the variance(I) to obtain a standard deviation of $\sigma(I)$;

Subtracting the average Q arm DC signal component $Q(AVG_DC)$ from total Q signal power $Q(AVG_TOTAL)$ to obtain a variance(Q) corresponding to average AC signal power in the Q arm;

determining a square root of the variance(Q) to obtain a standard deviation of $\sigma(Q)$.

10. The method of claim 9, further comprising:

multiplying each I, Q sample pair, summing resulting products, and dividing by M to obtain $E[I \cdot Q]$, an expectation of a dot product of I and Q;

dividing $E[I \cdot Q]$ by a product of $\sigma(I)$ and $\sigma(Q)$ to obtain a trigonometric sine of a DC-biased current phase error estimate $\phi(CURRENT_BIASED)$.

11. The method of claim 10, further comprising:
 - summing all I sample values and dividing by M to obtain $E[I]$, an expectation of I;
 - summing all Q sample values and dividing by M to obtain $E[Q]$, an expectation of Q;
 - multiplying $E[I]$ by $E[Q]$ and dividing the result by a product of $\sigma(I)$ and $\sigma(Q)$ to obtain a sin of a DC bias component $\phi(DC)$ of $\phi(CURRENT_BIASED)$.
12. The method of claim 11, further comprising:
 - subtracting $\phi(DC)$ from $\phi(CURRENT_BIASED)$ to obtain a current, unbiased phase correction estimate $\phi(CURRENT_UNBIASED)$;
 - add $\phi(CURRENT_UNBIASED)$ to a previous phase estimate $\phi(PREV)$ to obtain a new cumulative phase correction estimate $\phi(CUMULATIVE)$.
13. The method of claim 12, further comprising:
 - configuring the phase compensation network to factor the Q arm by a phase compensation factor $[1/\cos(\phi(CUMULATIVE))] * [Q(GCC) - I(GCC) * \sin(\phi(CUMULATIVE))]$;
 - comparing the phase iteration index R to R(MAX);
 - incrementing R if R is less than R(MAX) and performing an additional phase compensation iteration operation; and
 - awaiting another gain/phase correction training sequence opportunity as triggered by an expiration of a timeout period or other selected receiver trigger parameter(s) if $R = R(MAX)$.
14. A quadrature signal processing method, comprising:
 - receiving a digitized sample I(RD) of a down-converted I-arm signal I(R) and a digitized sample Q(RD) of a down-converted Q-arm signal Q(R);
 - factoring Q(RD) by a gain compensation coefficient $1/\beta$ to obtain a gain compensated value Q(GC) if a previously calculated ratio of $\text{variance}(Q) / \text{variance}(I)$ is greater than one, otherwise applying a unity gain factor to Q(RD) to obtain Q(GC);

factoring $I(RD)$ by a gain compensation coefficient β to obtain a gain compensated value $I(GC)$ if the previously calculated ratio of $\text{variance}(Q) / \text{variance}(I)$ is less than one, otherwise applying a unity gain factor to $I(RD)$ to obtain $I(GC)$;

if the previously calculated ratio of $\text{variance}(Q) / \text{variance}(I)$ is greater than one and the absolute value of $I(GC)$ is greater than $1/\beta * (\text{ADC_full-scale_value})$, reducing $I(GC)$ to $1/\beta * (\text{ADC_full-scale_value})$ to obtain $I(GCC)$;

if the previously calculated ratio of $\text{variance}(Q) / \text{variance}(I)$ is less than one and the absolute value of $Q(GC)$ is greater than $\beta * (\text{ADC_full-scale_value})$, reducing $Q(GC)$ to $\beta * (\text{ADC_full-scale_value})$ to obtain $Q(GCC)$;

factoring $I(GCC)$ by a first phase imbalance correction factor $\sin \phi$;

algebraically adding $I(GCC) * \sin \phi$ to the gain and clipping corrected Q value $Q(GCC)$ to obtain an independent Q value $[Q(GCC) + (I(GCC) * \sin \phi)]$; and

factoring $[Q(GCC) + (I(GCC) * \sin \phi)]$ by a second phase imbalance correction factor $1/\cos(\phi)$ to obtain a phase compensated Q value $Q(C)$.

15. A quadrature signal processing apparatus, comprising:

a gain compensation module to calculate, from a gain and clipping compensated set of I data samples and Q data samples captured at a start of each of a first set of iterations, an estimated gain compensation coefficient associated with a gain compensation function in each of an I arm and a Q arm and a clipping threshold associated with a clipping compensation function in the I arm and the Q arm of a quadrature receiver channel following frequency conversion and analog-to-digital (ADC) conversion;

an I -arm multiplier and a Q -arm multiplier communicatively coupled to the gain compensation module to factor at least one of a set of received I data samples or received Q data samples to obtain the gain compensated set of I data and Q data samples;

an I -arm clipping logic module and a Q -arm clipping logic module communicatively coupled to the gain compensation module to perform clipping operations on at least one of the gain compensated set of I data samples or the gain compensated set of Q data samples to obtain a current gain-compensated and clipping-

corrected set of I data samples and Q data samples to use as input data to a next one of the first set of iterations; and

a phase compensation module communicatively coupled to compensated I data and Q data outputs of the quadrature signal processing apparatus to calculate, from a gain, clipping, and phase-compensated set of I data samples and Q data samples captured at a start of each of a second set of iterations, a first estimated phase compensation factor to be used to add a negative I-arm signal component back into Q-arm data and a second estimated phase compensation factor for factoring resulting Q-arm data to further conform I-arm and Q-arm data distribution functions.

16. The apparatus of claim 15, wherein the gain compensation module further comprises:

I and Q sample buffers to accept the gain and clipping compensated set of I and Q data samples;

a sample buffer logic module communicatively coupled to the I and Q sample buffers to gate the gain and clipping compensated set of I and Q data samples into the I and Q sample buffers;

an average total power module communicatively coupled to the I and Q sample buffers to perform a first set of mathematical operations on the I and Q data samples to obtain a value $I(\text{AVG_TOTAL})$ of average total power in the I arm and a value $Q(\text{AVG_TOTAL})$ of average total power in the Q arm;

an average DC power module communicatively coupled to the I and Q sample buffers to perform a second set of mathematical operations on the I and Q data samples to obtain a value $I(\text{AVG_DC})$ of average DC power in the I arm and a value $Q(\text{AVG_DC})$ of average DC power in the Q arm; and

a variance power module communicatively coupled to the average total power module and to the average DC power module to subtract $I(\text{AVG_DC})$ from $I(\text{AVG_TOTAL})$ to obtain a variance(I) of average AC signal power in the I arm and to subtract $Q(\text{AVG_DC})$ from $Q(\text{AVG_TOTAL})$ to obtain a variance(Q) of average AC signal power in the Q arm.

17. The apparatus of claim 16, wherein the gain compensation module further comprises:

a previous gain compensation estimate buffer to store a previously-calculated cumulative gain compensation estimate $\beta(\text{PREV})$;

a gain compensation estimation module coupled to the previous gain compensation estimate buffer to obtain a square root of a ratio of variance(Q) to variance(I) to obtain a current gain compensation estimate $\beta(\text{CURRENT})$ and to combine $\beta(\text{CURRENT})$ with $\beta(\text{PREV})$ to obtain a cumulative gain compensation estimate $\beta(\text{CUMULATIVE})$;

a clipping threshold estimation module communicatively coupled to the variance power module to obtain a clipping logic threshold value proportional to a product of $\beta(\text{CUMULATIVE})$ and an ADC full-scale value; and

an iteration control module communicatively coupled to the sample buffer logic module and to the gain compensation estimation module to control successive iterations of compensated data sampling, gain compensation estimation, and clipping threshold estimation.

18. The apparatus of claim 15, wherein the phase compensation module comprises:

a compensated data sampling and power calculation module to obtain a variance(I) of average AC signal power in the I arm and a variance(Q) of average AC signal power in the Q arm;

a standard deviation module communicatively coupled to the compensated data sampling and power calculation module to obtain a standard deviation of I $\sigma(I)$ as a square root of the variance(I) and to obtain a standard deviation of Q $\sigma(Q)$ as a square root of the variance(Q);

an I-dot-Q expectation module communicatively coupled to the compensated data sampling and power calculation module to obtain a mathematical expectation $E[I \cdot Q]$ of a dot product of the I data samples and the Q data samples;

an I expectation module communicatively coupled to the compensated data sampling and power calculation module to obtain a mathematical expectation $E[I]$ of the I data samples; and

a Q expectation module communicatively coupled to the compensated data sampling and power calculation module to obtain a mathematical expectation $E[Q]$ of the Q data samples.

19. The apparatus of claim 18, wherein the phase compensation module further comprises:

a biased phase estimation module communicatively coupled to the I-dot-Q expectation module and to the standard deviation module to obtain a DC-biased phase angle compensation estimate $\phi(\text{CURRENT_BIASED})$ equal to an arcsine $\{E[I \cdot Q] / \sigma(I) * \sigma(Q)\}$;

a DC phase estimation module communicatively coupled to the I expectation module, the Q expectation module, and the standard deviation module to obtain a DC component $\phi(\text{DC})$ of the DC-biased phase angle compensation estimate $\phi(\text{CURRENT_BIASED})$ equal to an arcsine of a dot product of the expectation $E[I]$ and the expectation $E[Q]$ divided by $\sigma(I) * \sigma(Q)$;

a previous phase angle estimation module to store a previously calculated phase estimate $\phi(\text{PREV})$;

a phase angle determination module communicatively coupled to the biased phase estimation module and to the DC phase estimation module to subtract $\phi(\text{DC})$ from $\phi(\text{CURRENT_BIASED})$ to determine a current unbiased phase correction angle $\phi(\text{CURRENT_UNBIASED})$ and to add $\phi(\text{CURRENT_UNBIASED})$ to the previously-calculated phase estimate $\phi(\text{PREV})$ to obtain $\phi(\text{CUMULATIVE})$; and

an iteration control module communicatively coupled to the compensated data sampling and power calculation module and to the phase angle determination module to control successive iterations of compensated data sampling and phase angle compensation estimation.

20. The apparatus of claim 15, wherein the I-arm and Q-arm clipping logic modules further comprise:

clipping level logic to receive the cumulative gain compensation estimate β (CUMULATIVE) and a maximum ADC range from the gain compensation module and to calculate a clipping level;

a comparator to compare a gain compensated sample value to the clipping level; and

a clipper to decrease a magnitude of the gain compensated sample value to the clipping level if the gain compensated sample value exceeds the clipping level.

21. A quadrature signal processing apparatus, comprising:

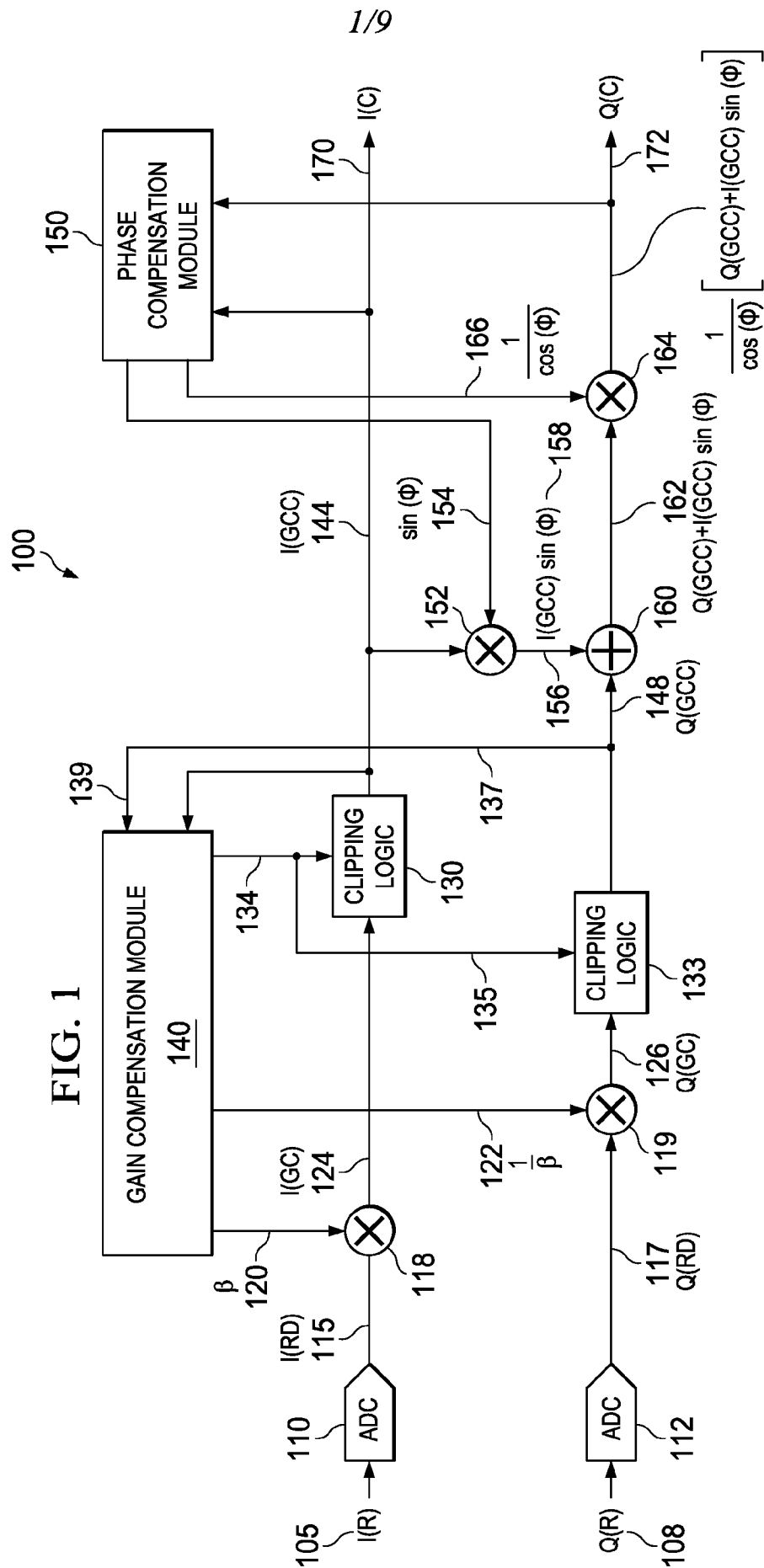
a gain compensation module to calculate, from a gain and non-linear artifact compensated set of I data samples and Q data samples captured at a start of each of a first set of iterations, an estimated gain compensation coefficient associated with a gain compensation function in each of an I arm and a Q arm and a non-linear artifact balancing coefficient associated with a non-linear artifact balancing compensation function in the I arm and the Q arm of a quadrature receiver channel following frequency conversion and analog-to-digital (ADC) conversion;

an I-arm multiplier and a Q-arm multiplier communicatively coupled to the gain compensation module to factor at least one of a set of received I data samples or received Q data samples to obtain the gain compensated set of I data and Q data samples;

an I-arm non-linear artifact processor and a Q-arm non-linear artifact processor communicatively coupled to the gain compensation module to perform non-linear artifact balancing operations on at least one of the gain compensated set of I data samples or the gain compensated set of Q data samples to obtain a current gain-compensated and non-linear artifact balanced set of I data samples and Q data samples to use as input data to a next one of the first set of iterations; and

a phase compensation module communicatively coupled to compensated I data and Q data outputs of the quadrature signal processing apparatus to calculate, from a gain and phase-compensated and non-linear artifact balanced set of I data samples and Q

data samples captured at a start of each of a second set of iterations, a first estimated phase compensation factor to be used to add a negative I-arm signal component back into Q-arm data and a second estimated phase compensation factor for factoring resulting Q-arm data to further conform I-arm and Q-arm data distribution functions.



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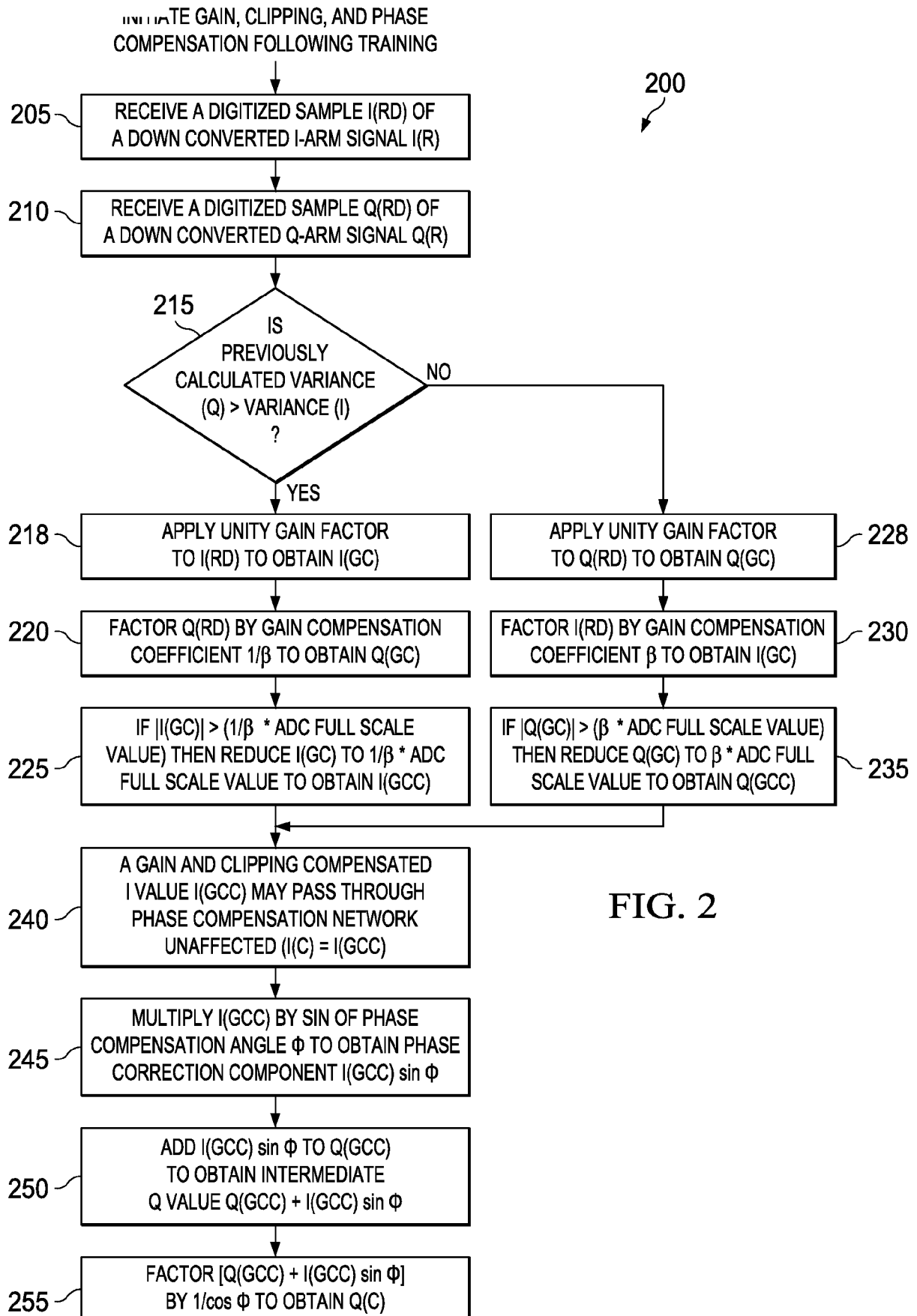


FIG. 2

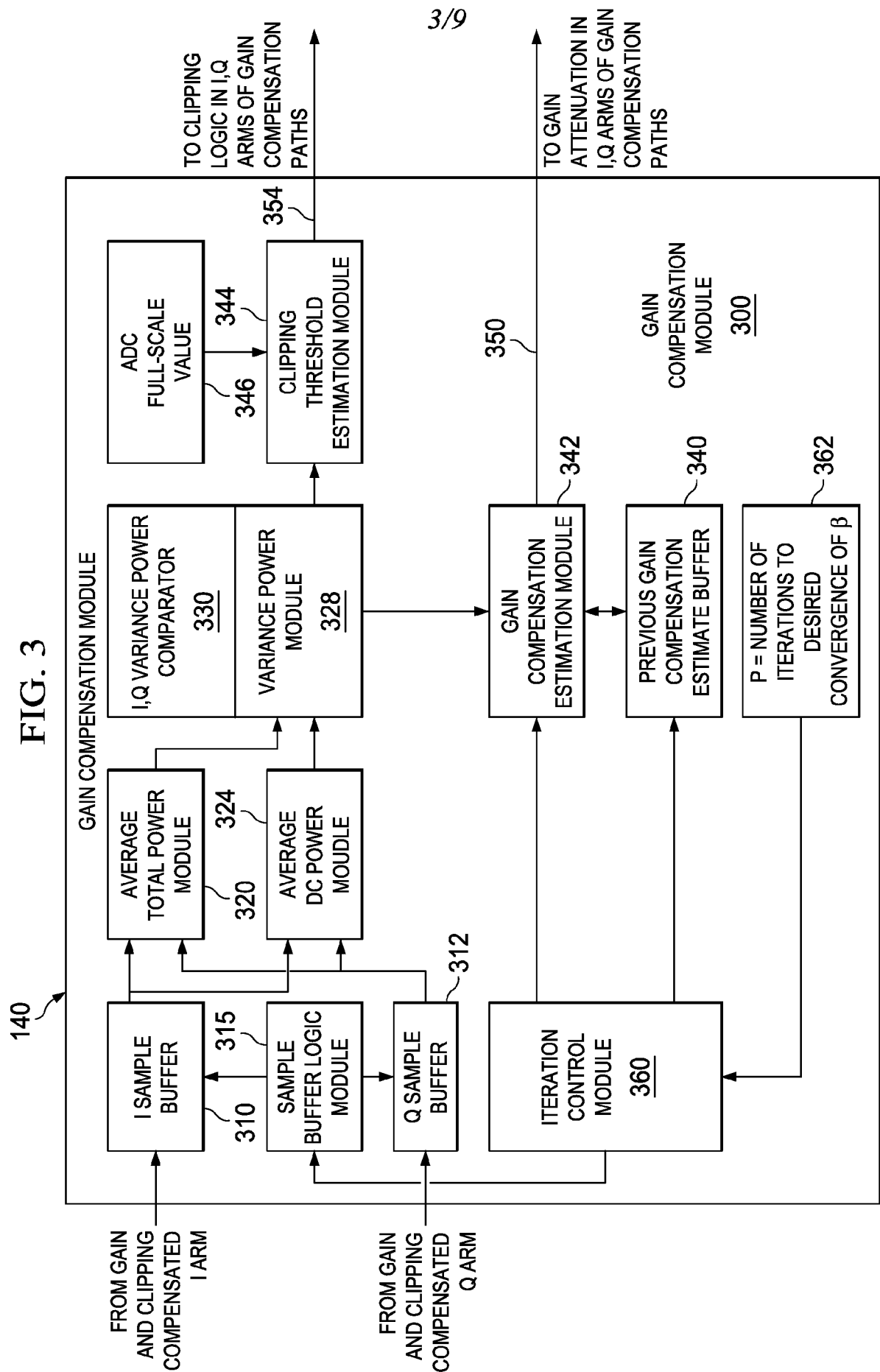
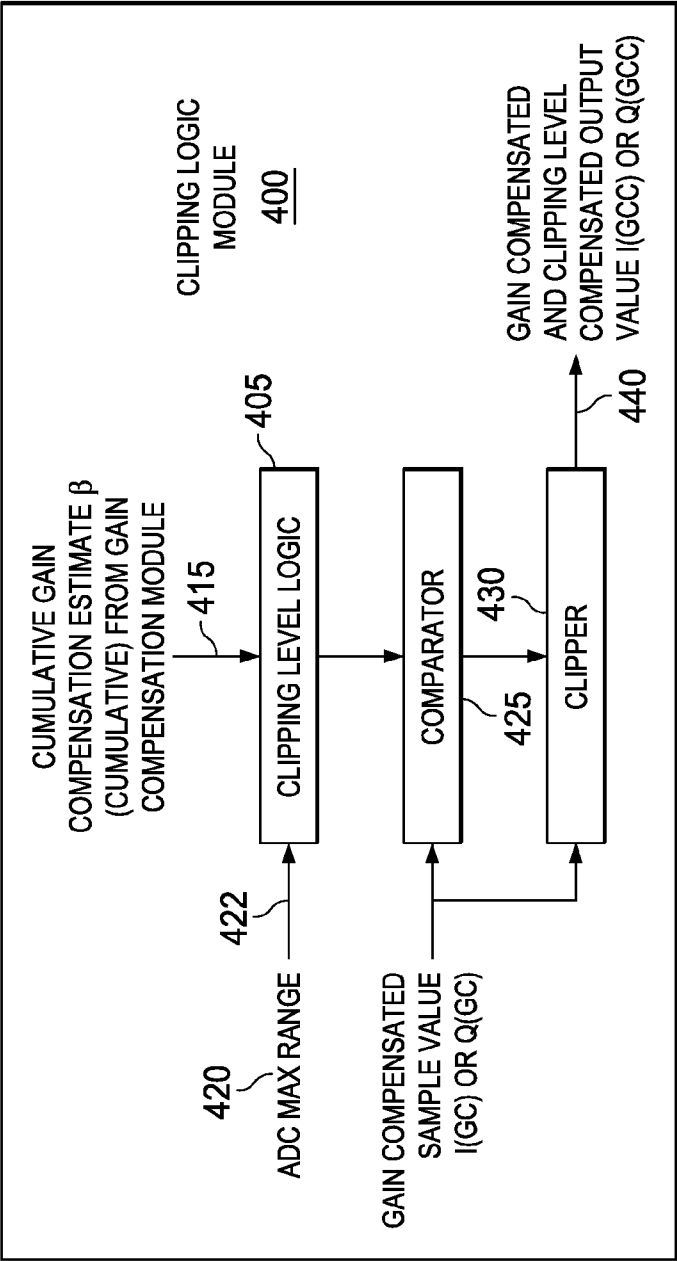
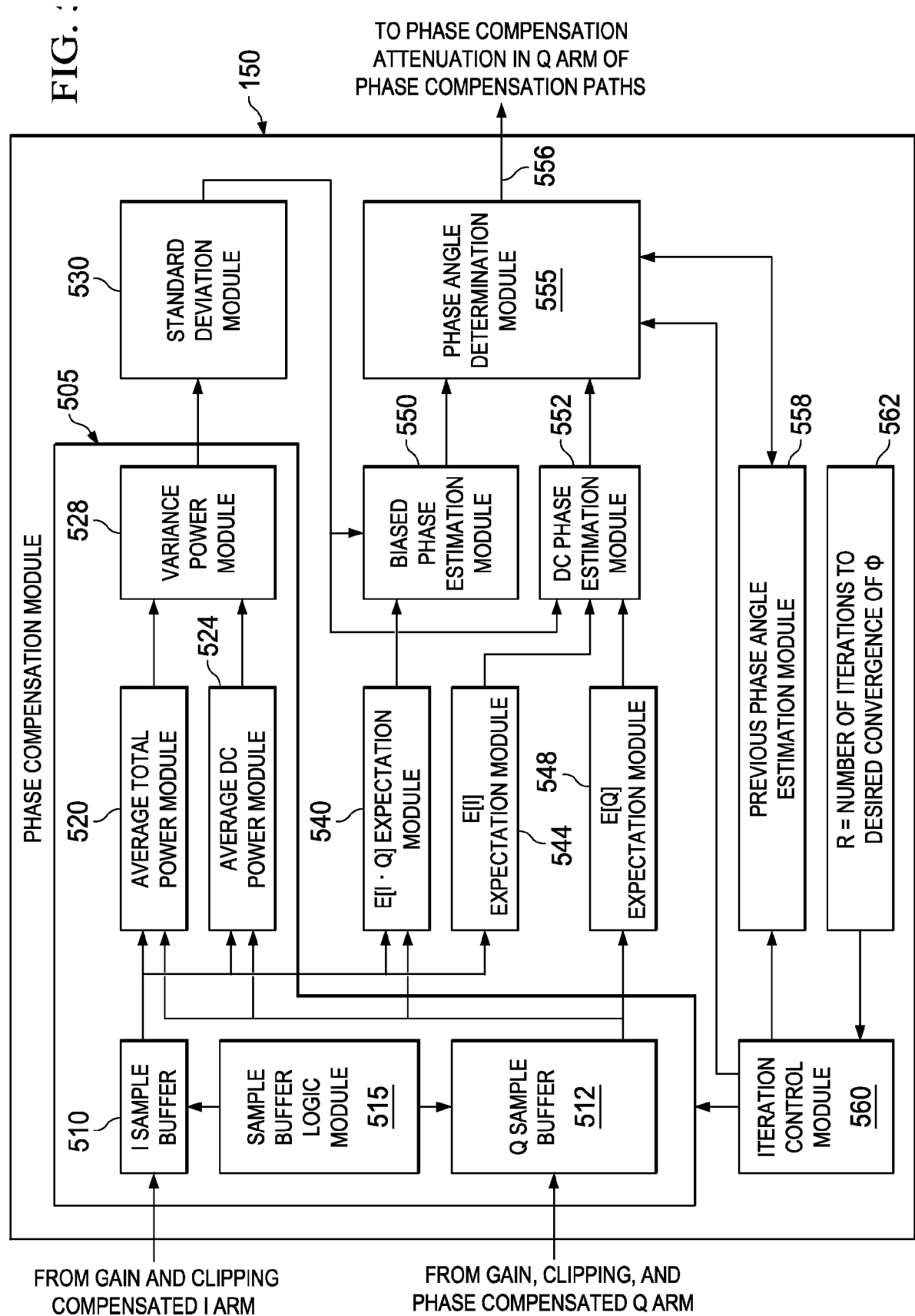


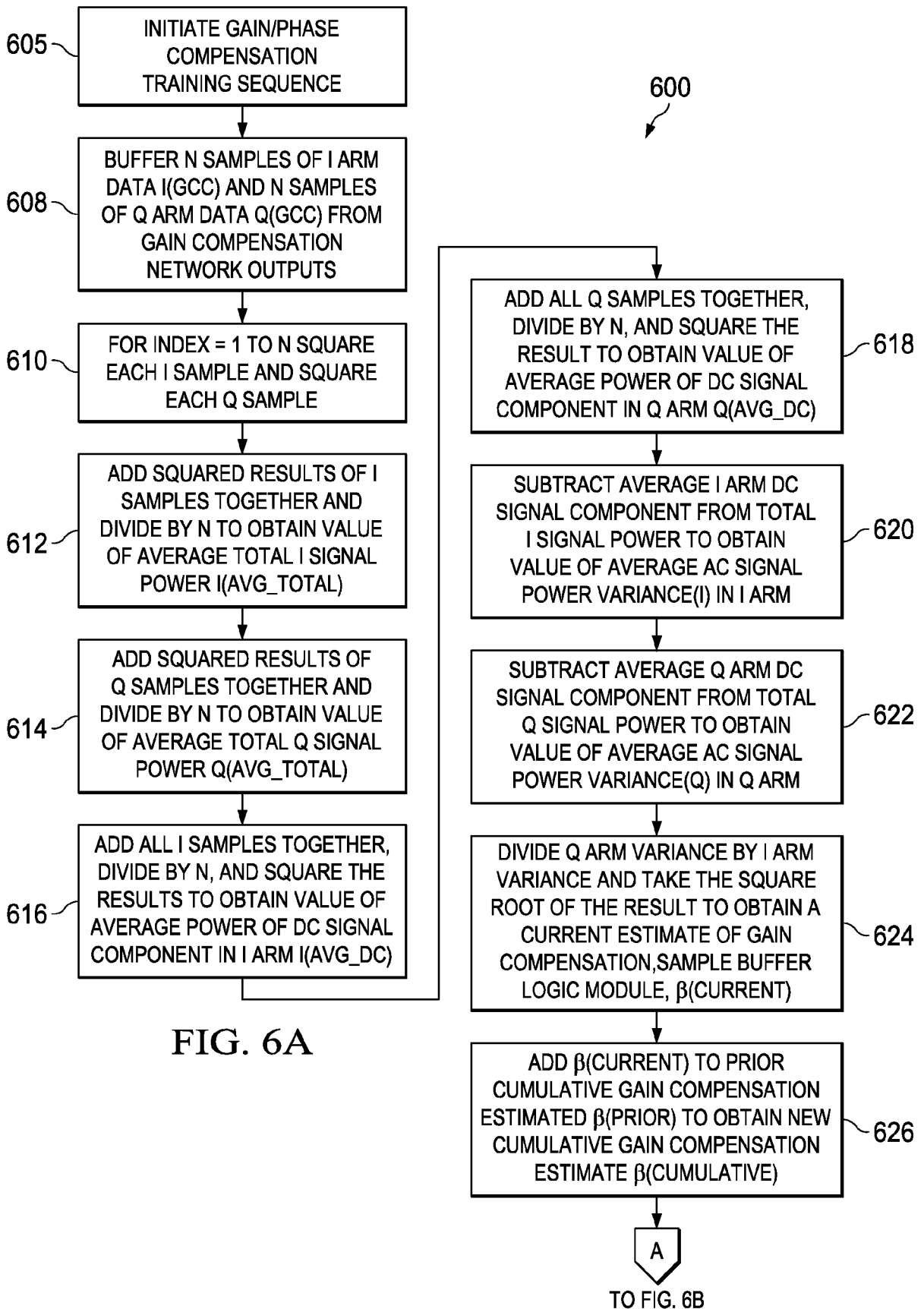
FIG. 4



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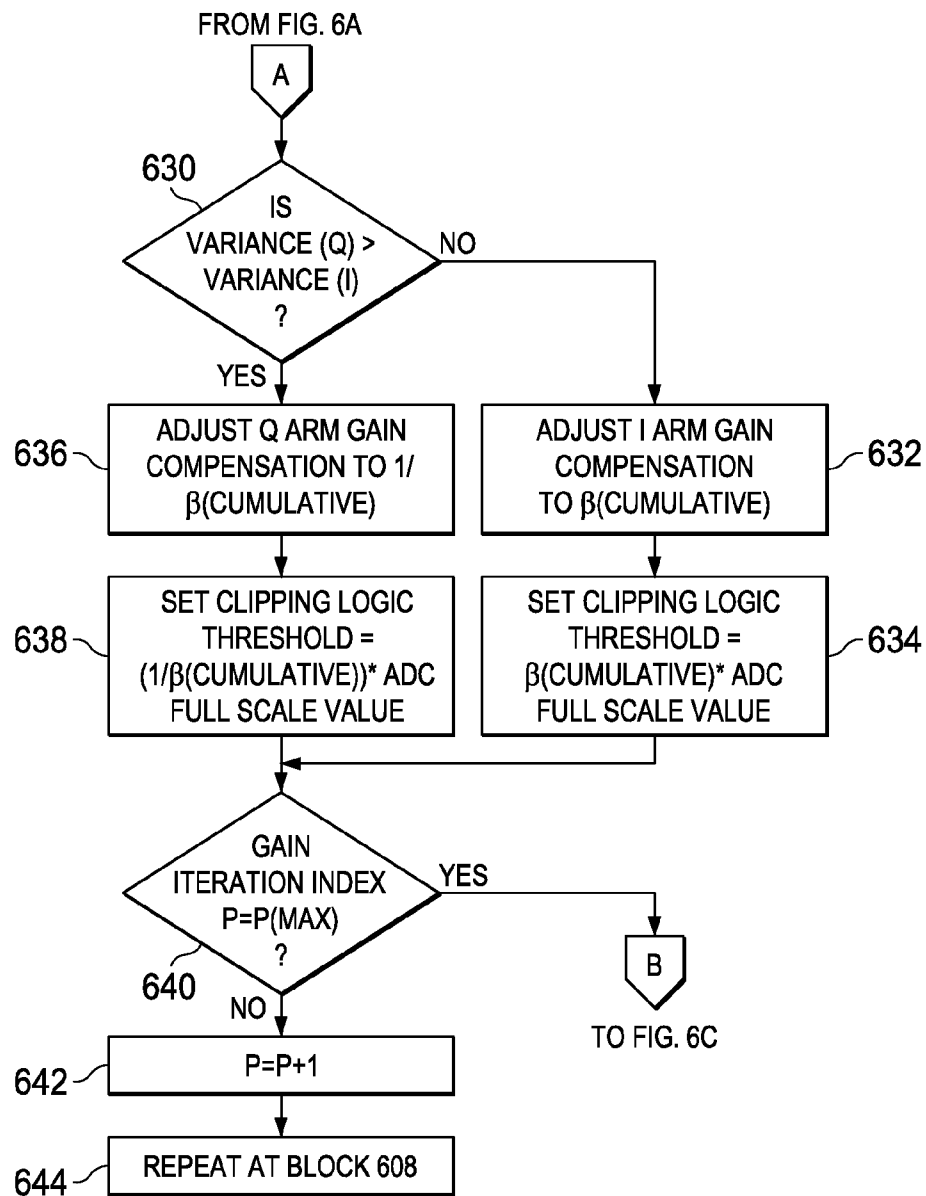


FIG. 6B

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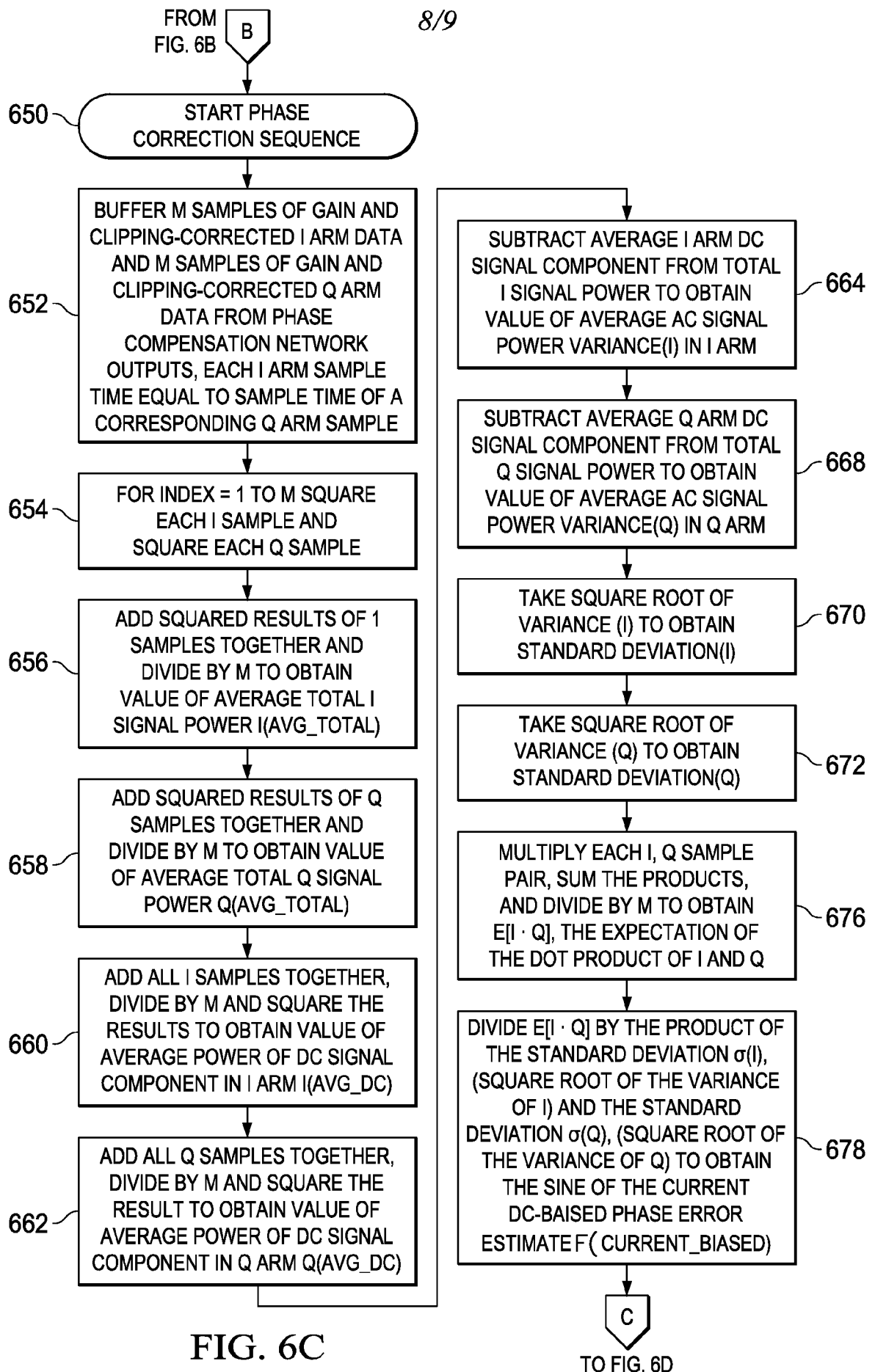


FIG. 6C

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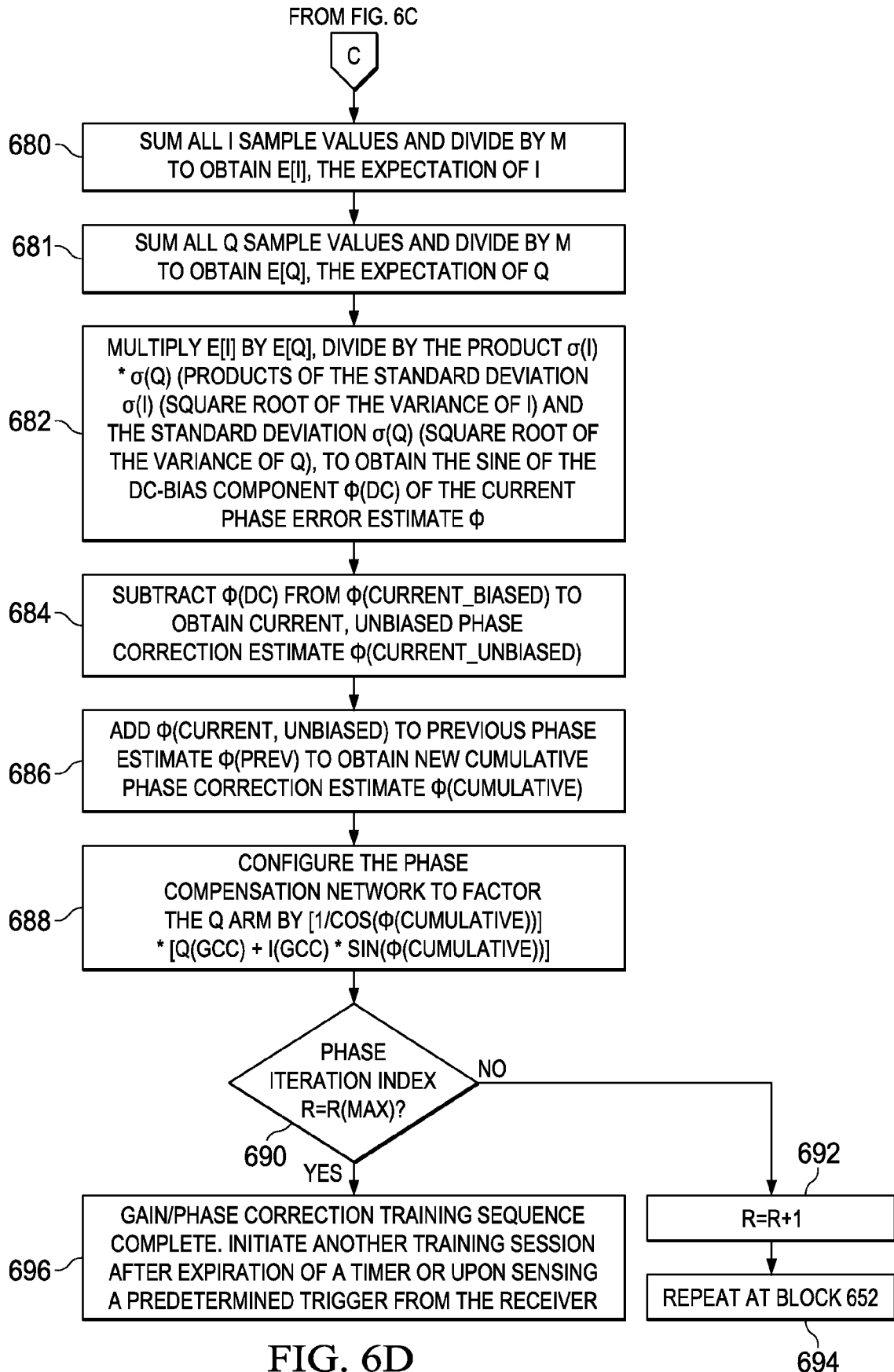


FIG. 6D

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/054636**A. CLASSIFICATION OF SUBJECT MATTER****H04L 25/03(2006.01)i, H04L 25/12(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04L 25/03; H01Q 11/12; H03C 1/62; H03H 11/16; H04B 1/16; H04B 1/10; H03F 1/32; H04B 1/04; H04L 25/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: quadrature signal, clipping threshold, ADC conversion, I/Q mismatch, compensation

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012-0028594 A1 (YADUNANDANA RAO et al.) 02 February 2012 See paragraphs 13-16, 21; claims 1-3; and figures 1, 2.	1
A		2-21
A	US 2003-0104792 A1 (YOSHIAKI DOI) 05 June 2003 See paragraphs 24-29; claim 1; and figure 4.	1-21
A	US 2009-0221255 A1 (JUN MA et al.) 03 September 2009 See paragraphs 10, 39-48; and figure 5.	1-21
A	US 2002-0041208 A1 (HAJIME HAMADA et al.) 11 April 2002 See paragraphs 17-20; claims 1, 3; and figure 1.	1-21
A	US 2007-0232250 A1 (THOMAS SUN et al.) 04 October 2007 See paragraphs 47, 65-66; and figures 3, 13.	1-21



Further documents are listed in the continuation of Box C.



See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

22 November 2013 (22.11.2013)

Date of mailing of the international search report

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/054636

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