April 6, 1965 R. O. BARBER ETAL 3,177,420

THREE-PHASE TRANSISTORIZED OSCILLATOR POWER SUPPLY

Filed Oct. 7, 1960 5 Sheets-Sheet 1

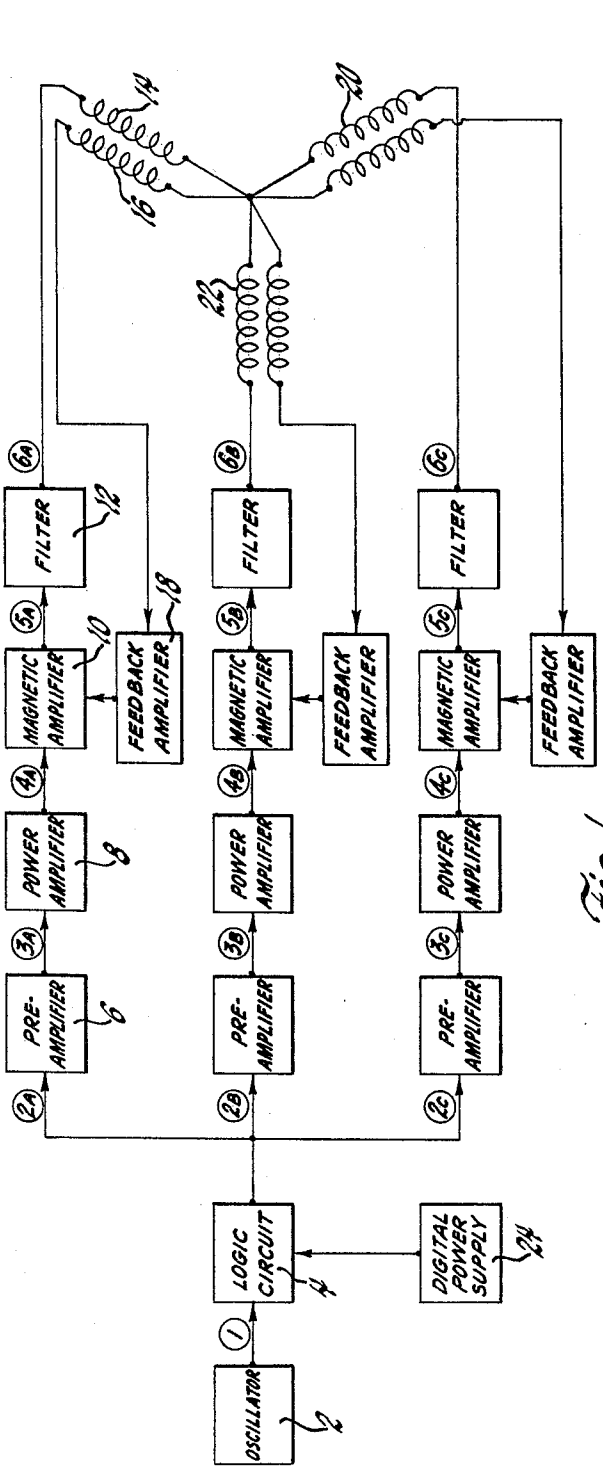


FIG. 1

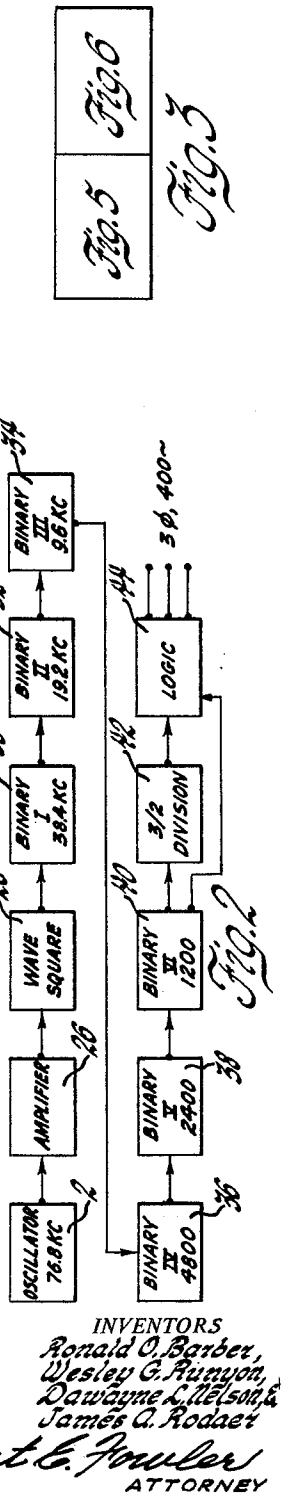


FIG. 2

FIG. 3 = FIG. 5 + FIG. 6

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Filed Oct. 7, 1960 5 Sheets-Sheet 2

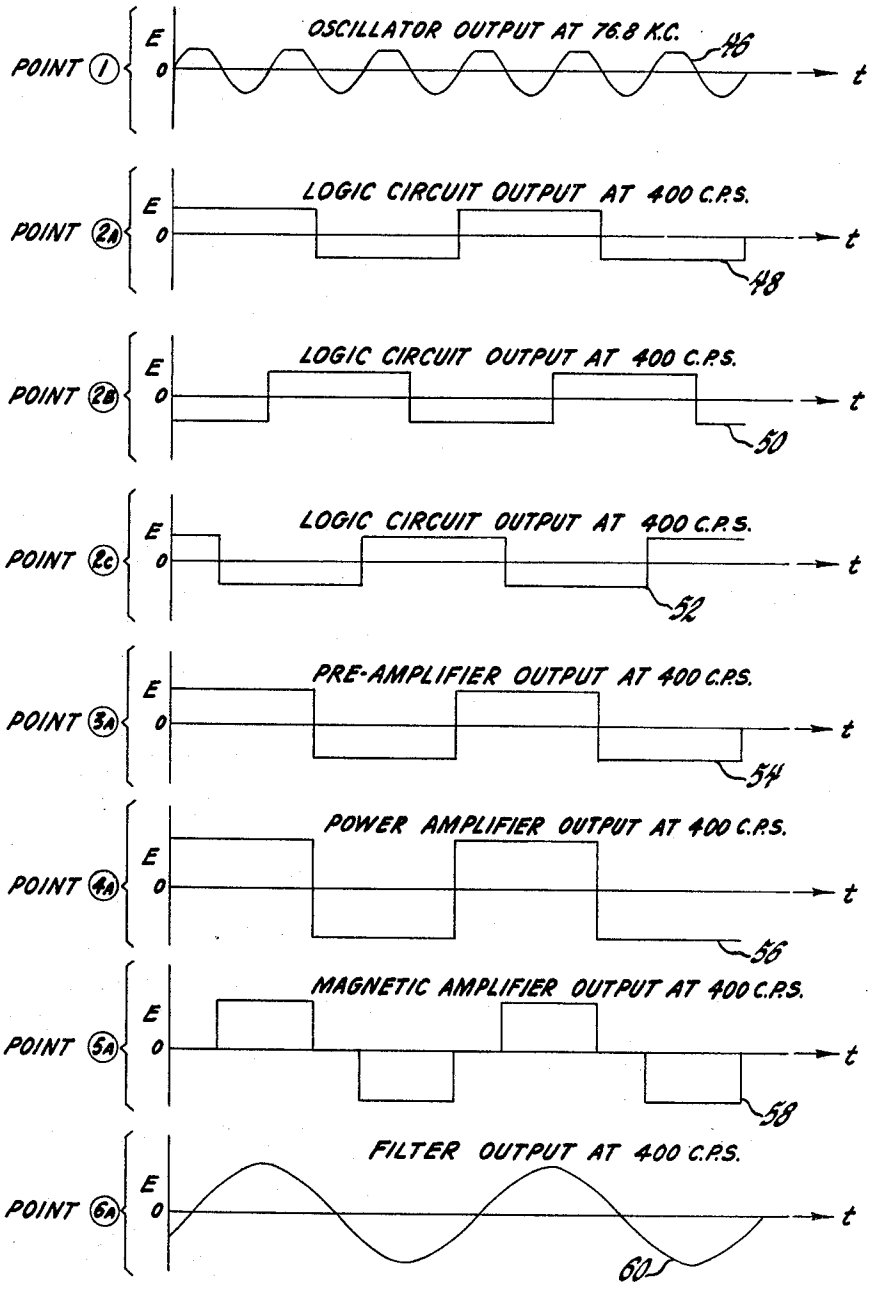


Fig. 4

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THREE-PHASE TRANSISTORIZED OSCILLATOR POWER SUPPLY

Filed Oct. 7, 1960 5 Sheets-Sheet 3

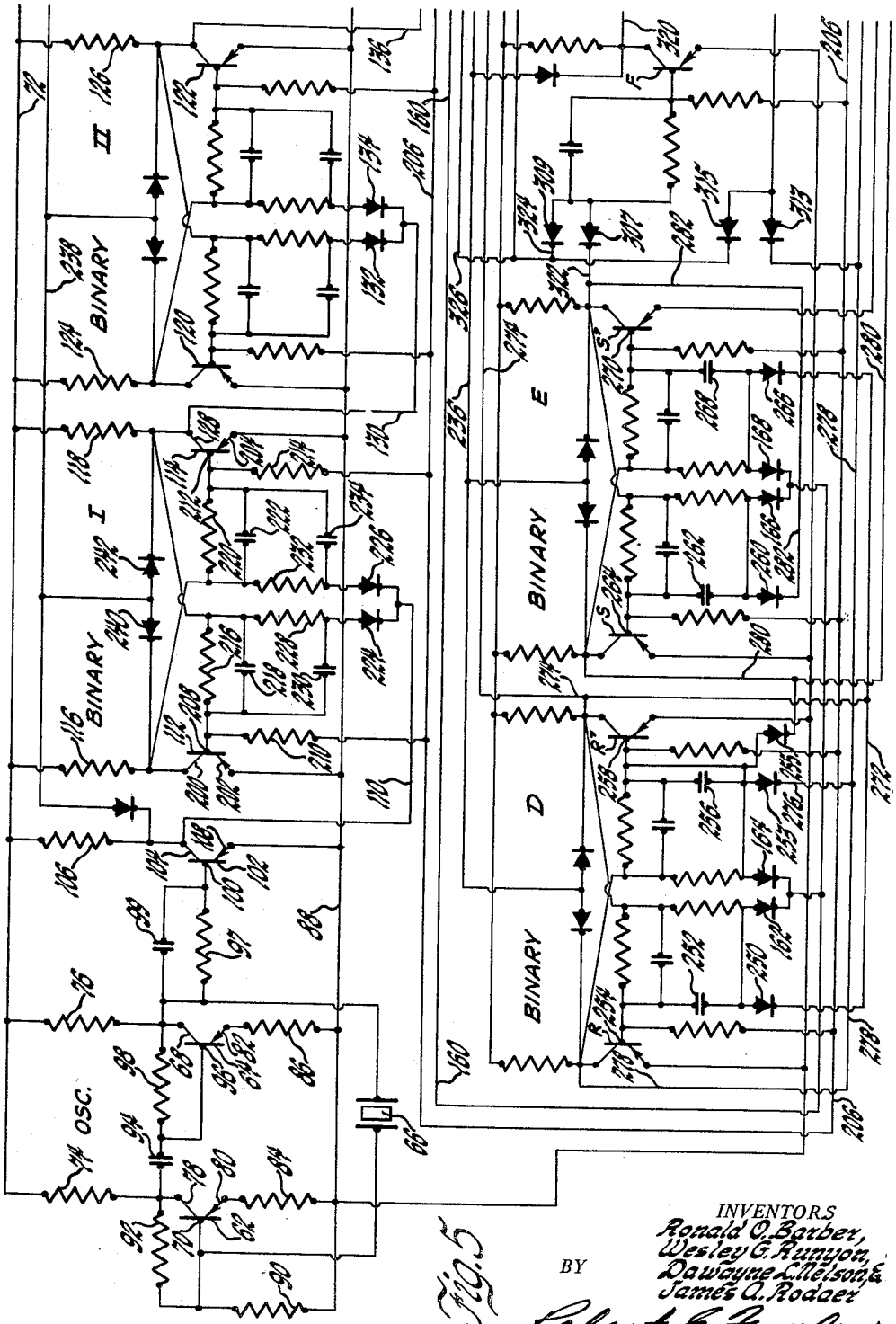


FIG. 5

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THREE-PHASE TRANSISTORIZED OSCILLATOR POWER SUPPLY

Filed Oct. 7, 1960 5 Sheets-Sheet 4

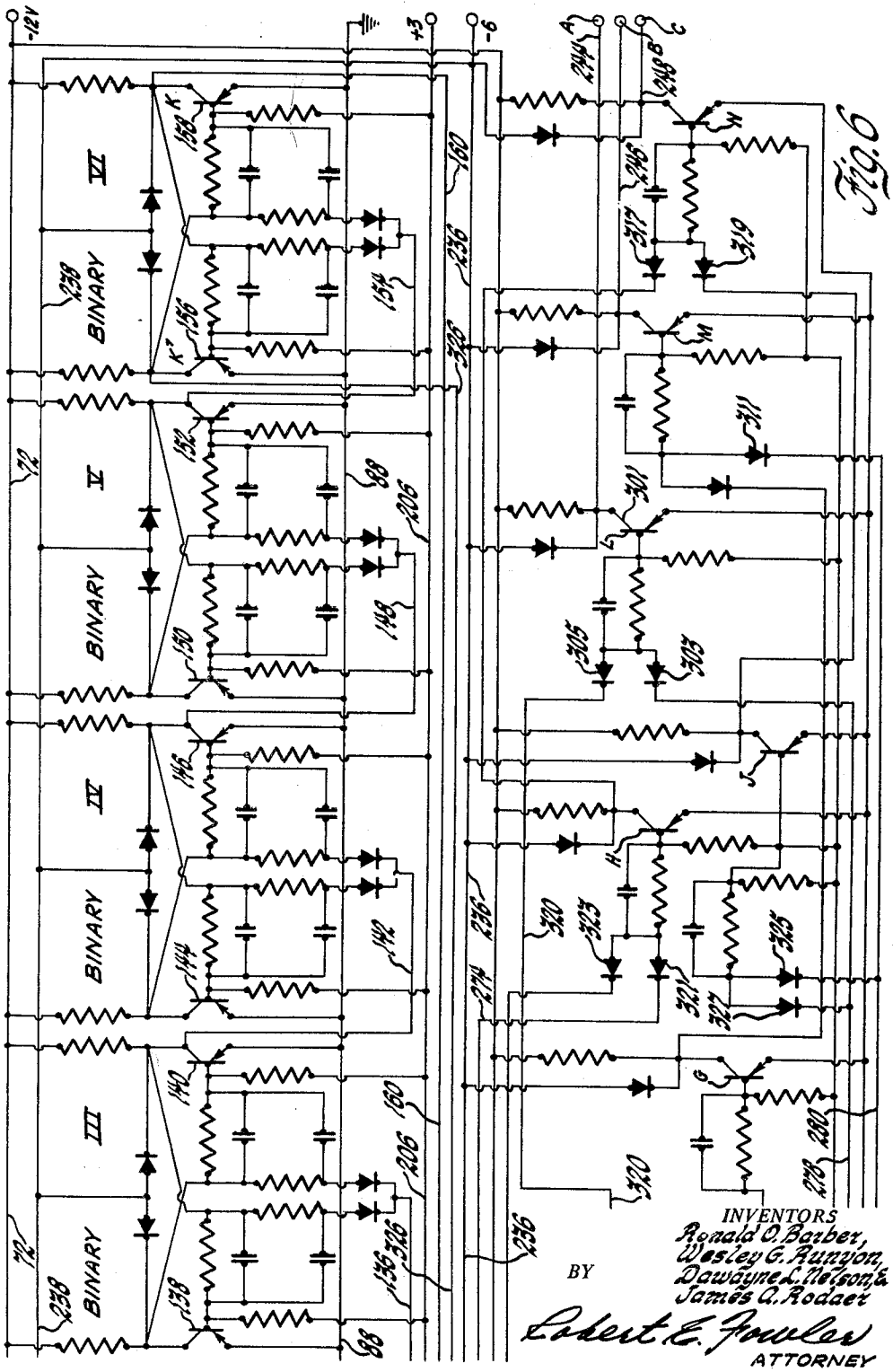


FIG. 4

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THREE-PHASE TRANSISTORIZED OSCILLATOR POWER SUPPLY

Filed Oct. 7, 1960 5 Sheets-Sheet 5

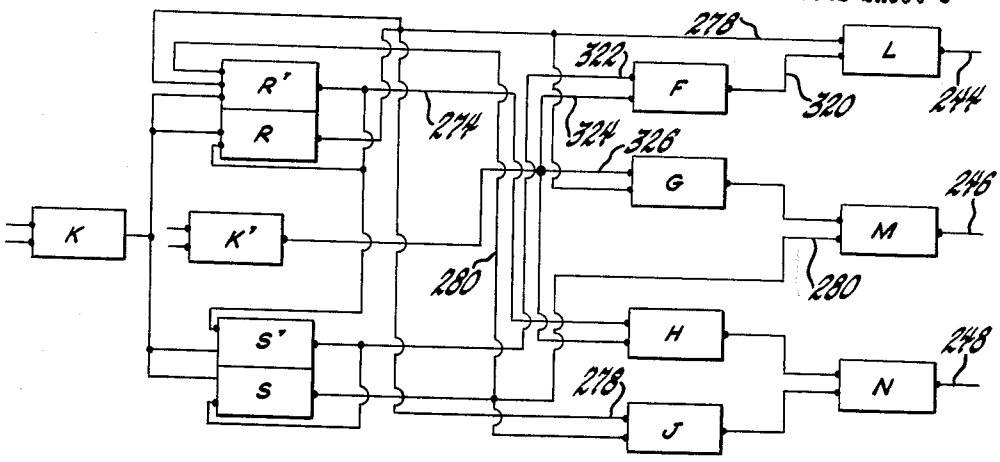


Fig. 7

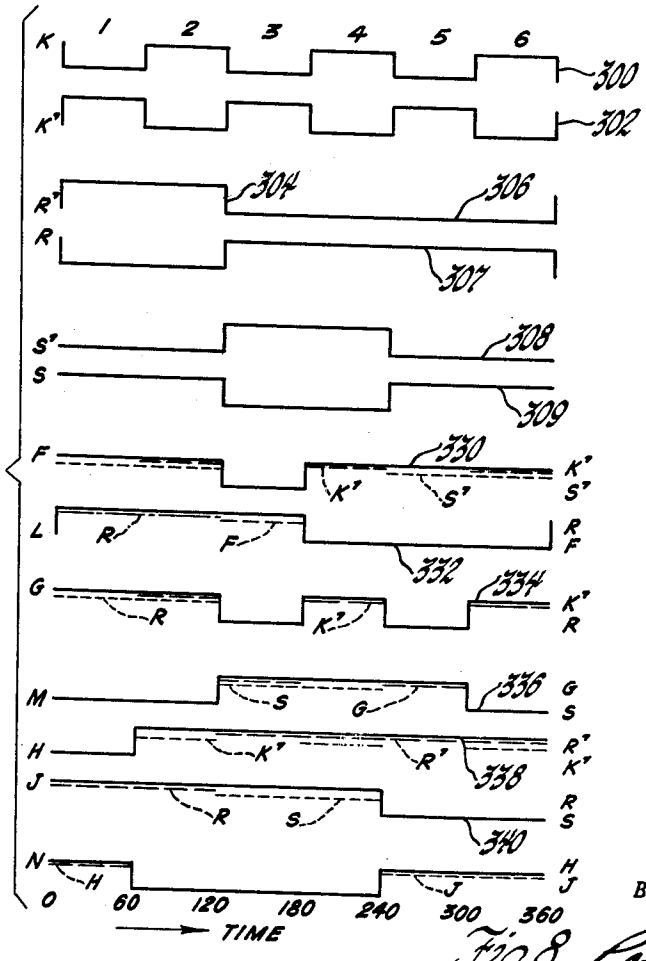


Fig. 8

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United States Patent Office 3,177,420 Patented Apr. 6, 1965

3,177,420

THREE-PHASE TRANSISTORIZED OSCILLATOR POWER SUPPLY

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Filed Oct. 7, 1960, Ser. No. 61,282
7 Claims. (Cl. 321—5)

This invention relates to a static inverter power supply system for providing precisely displaced three-phase alternating current power from a direct current power supply. Specifically it relates to a static inverter system for providing 400 cycle three-phase alternating current power from a 25 to 30 volt direct current source which has primary utility in aircraft installations but which can be used in any other similar installation where there is a need for such equipment. Inverters for producing single phase alternating current power from a direct current source are not uncommon but difficulties arise when precisely displaced three-phase power is required from the direct current power source and it is the object of the present invention to provide such an inverter system.

In the present instance a high frequency oscillator powered by a direct current source is used as the basic power source, the output of which is divided down through a series of binary dividers or counters to a suitable frequency which is then applied to a ternary divider to provide the desired output frequency and thence through logic gate circuits to a three-phase output where accurate and precise spacing is maintained at all times between the three phases.

The objects and advantages of this invention will be better understood from the following description with reference to the figures of the accompanying drawings in which:

FIGURE 1 is a block diagram illustrating the components of the complete inverter system;

FIG. 2 is a block diagram illustrating the components of the basic oscillator, frequency division section and logic gate section for supplying three-phase power;

FIG. 3 is a diagram illustrating the manner in which FIGS. 5 and 6 fit together;

FIG. 4 is a series of graphs illustrating the wave shapes of the voltage obtained at various indicated locations;

FIG. 5 is a portion of the detailed circuit diagram of the oscillator, binary counter, divider and logic section of our inverter;

FIG. 6 is the remainder of that detailed circuit diagram of our inverter which should be considered together with FIG. 5 as shown in FIG. 3;

FIG. 7 is a block diagram illustrating the clock and gate controls for developing the precisely spaced three-phase output; and,

FIG. 8 is a graph showing the relative timed clock and gate conditions to develop the precisely phased three-phase output.

Referring first to FIG. 1 there is shown therein a high frequency oscillator 2 which serves as the main source of high frequency current. This is, of course, supplied with direct current power from the power supply 24 in order to drive the same and is in this case a crystal controlled oscillator which operates at a very accurate frequency output. The output of the oscillator is fed into a section which may be termined a frequency division or splitting section for dividing down the frequency of the power and which terminates in a gate logic circuit providing a three-phase output. This is shown in FIG. 1 as a block identified as logic circuit 4 but actually it includes much more than a pure logic circuit as will be clear from the following detailed description.

The output of the logic circuit block 4 is actually three-phase power and each phase is connected individually through a pre-amplifier, power amplifier, magnetic amplifier and filter of its own to a final output winding. This is illustrated in FIG. 1 by three separate channels identified as A, B and C. For example, the channel identified as A has a pre-amplifier 6 which is connected to the output of the first phase from the logic circuit 4 and which is in turn connected to a power amplifier 8, thence through a magnetic amplifier 10 and a filter 12 to an output winding 14. Inductively associated with the output winding 14 in a Y connection in a feedback winding 16 which is connected to a feedback amplifier 18 and thence into the magnetic amplifier to control the amount of amplification. Each of the other phases are exactly the same as the first but amplify and control the voltage flowing through its phase at 120 electrical degree displacement from the others The output of these three together are applied to the output windings 14, 20 and 22 to drive whatever equipment it is desired with alternating current power. The power supply indicated at 24 is shown connected into the logic circuit but it actually provides power for the whole system.

Referring now more particularly to FIG. 2 which specifically illustrates how the high frequency of the oscillator is divided or broken down into a suitable lower output frequency, the block units of FIG. 2 from the oscillator 2 on are all elements included in block 4 identified as the logic circuit in FIG. 1. In this instance the oscillator has been designed to operate at a fixed frequency of 76.8 kc. in order to provide a final output frequency of 400 cycles. As mentioned the oscillator is crystal controlled so that it maintains a very accurate frequency. The output of the oscillator is applied first to an amplifier section 26 where the 76.8 kc. signal is amplified. The signal is then squared by section 28 to square up the sinusoidal wave and applied to binary I or first frequency dividing circuit 30 which divides the frequency in half. The output of this binary I circuit has, therefore, a frequency of 38.4 kc. In succession the signal is then sent through a series of dividing circuits binary II–32, binary III–34, binary IV–36, binary V–38 and lastly binary VI–40. Through this succession of frequency divisions the frequency is changed from 38.4 kc. to 19.2 kc., 9600 cycles, 4800 cycles, 2400 cycles and lastly 1200 cycles, respectively, as labeled on the blocks. It is obvious that from the output of the last binary VI–40 means must be provided to reduce the frequency from 1200 to 400 cycles and at the same time provide a three-phase output precisely spaced at 120 electrical degrees. This is accomplished in two steps, first through a ternary division section 42 which reduces the frequency to 400 cycles and thence through a gate logic circuit 44 which properly switches the output to three-phase output lines at the correct time. The final output of this chain is, therefore, a precisely spaced three-phase 400 cycle output. These would be the signals applied to the different channels A, B and C as indicated in FIG. 1.

FIG. 3 is merely included to show how FIGS. 5 and 6 should be laid together in order to form a complete circuit diagram.

Referring now more particularly to FIG. 4 there are shown in that figure graphs of the shape of the various voltage wave forms found at different points indicated numerically in the general circuit, FIG 1. The voltage wave form as shown in the first graph 46 of FIG. 4 appears at the output of the oscillator circuit 2 at point indicated as 1. It is to be noted that this is not a complete sinusoidal wave voltage but that the positive half waves have been clipped to form more of a square wave

indicating that the wave has passed through the square wave section 28. At point 2A there is obtained a 400 cycle square wave voltage as shown at 48 and it is indicated by being labeled 2A at the left in FIG. 4. This voltage is indicated as going positive at time zero, reverse at 180 electrical degrees to negative, reverse again to positive at 360 electrical degrees, etc. The 400 cycle voltages appearing at 2B and 2C are shown in the next two succeeding graphs 50 and 52 which are likewise labeled 2B and 2C to indicate where they appear. At time zero the voltage at 2B is indicated as being negative but it goes positive at 120 degrees, thus lagging phase A by that amount, remains there for additional 180 degrees, then back positive again showing a phase displacement to the first phase shown at 2A of 120 degrees. In like manner the curve 52 showing the shape of the voltage applied to the C channel and specifically to point 2C is shown to be on positive at time zero, to go negative at 60 degrees and to remain there for 180 degrees, reversing to positive to again indicate the proper 120 degrees spacing of the three phases A, B and C at points 2A, 2B and 2C, respectively.

The following graphs in FIG. 4 indicate the further changes in the wave form as the voltage progresses only through the A channel since the same results would obtain in each of the other two channels and the discussion would be repetitive. Therefore, following the voltage waves through channel A alone, when the wave reaches the point 3A we find that the amplitude of the wave indicated at 54 has increased since it has passed through the pre-amplifier 6 but that its shape and phase is the same as it was in wave form 48 and it is only the amplitude that has varied. Output voltage wave form 54, labeled pre-amplifier output, is then applied to the power amplifier 8 and the resultant wave shown at 56, indicated as appearing at point 4A, is, as would be expected, merely an additional amplitude increase. The effect of magnetic amplifier 10 and the resultant wave form appearing at point 5A, FIG. 1, is indicated at 58, FIG. 4, and in this case it is seen that this is a stabilized regulated wave whose amplitude is controlled to give only a desired output, the feedback preventing the output from exceeding a certain value. In order now to return the square wave appearing at the output of the magnetic amplifier to the sinusoidal form in which it is desired to use the same, the square wave form 58 appearing at point 5A is applied to the input of the filter 12 which smooths it out and, therefore, at point 6A there is obtained a substantially sinusoidal output wave 60 which appears on the output winding 14 for use in desired apparatus. The same amplification, squaring and smoothing occurs in each one of the other channels B and C as each applies its output in desired phased relation to output coils 20 and 22, respectively, obtaining precisely spaced three-phase power at 400 cycles from the output windings 14, 20 and 22.

Referring now more particularly to the detail circuit of the static inverter shown in FIGS. 5 and 6, the power oscillator 2 consists of two transistors 62 and 64 which are controlled by a quartz crystal 66 connected in feedback relation between the collector electrode 68 or out put of transistor 64 and the base electrode 70 or input of transistor 62. These two transistors are properly biased by being supplied with power from power line 72 whose terminal at the extreme right of FIG. 6 is connected to a source of power of —12 volts as indicated. This power line 72 is connected through resistances 74 and 76 to the collector electrodes 78 and 68 of the transistors 62 and 64, respectively. The emitter electrodes 80 and 82 of the transistors 62 and 64 are connected through biasing resistors 84 and 86 to ground line 88 whose righthand terminal in FIG. 6 is marked "ground." A resistance 90 is connected between the base electrode 70 of transistor 62 and ground and a further biasing resistor 92 is connected between the collector electrode 78 and base electrode 70. The resistances 74, 92 and 90 provide a voltage divider for supplying the proper bias voltages to the transistor 62. The collector electrode 78 of the transistor 62 is connected through a condenser 94 to the base electrode 96 of the transistor 64 and a biasing resistor 98 is connected between the collector electrode 68 and the base electrode 96 of this transistor. This is a two stage oscillator, the first stage 62 acting as the main oscillator and the second stage 64 functioning as an amplifier and phase inverter so that the feedback signal through the crystal is in the proper phase. This oscillator supplies power at a frequency of 76.8 kc. and has a sine wave output which is applied to the input or base electrode 100 of the transistor 102 in the next stage through coupling resistance 97 shunted by condenser 99.

The transistor 102 acts as both an amplifier and as a wave squaring stage and is connected directly across between the power line 72 and the ground line 88, its collector electrode 104 being connected to the power line through biasing resistance 106 and its emitter electrode 108 being directly connected to ground line 88. The sine wave output of the oscillator 2 applied to the first stage including transistor 102 is amplified and since this stage is designed to be turned on and off rapidly it also squares the signal to produce an amplified square wave signal.

It is next desired to reduce the frequency of the signal and this square wave output from transistor 102 is applied to line 110 connected directly to the collector electrode 104 of transistor 102 and to the input of the first binary counting circuit indicated previously as binary I consisting of two transistors 112 and 114. These binary circuits are used only for frequency division and are conventional binary or flip-flop circuits, one half of the circuit conducting on each cycle to cut the frequency output in half. Power is supplied to this binary circuit from power supply line 72 through resistors 116 and 118. Resistor 116 is connected to collector 200 of transistor 112 and its emitter 202 is directly connected to ground line 88. In a symmetrical manner collector 128 of transistor 114 is connected to resistor 118 and emitter 204 of transistor 114 is connected to ground line 88. It is desired to maintain the base electrodes of these two transistors at a slight positive bias and as illustrative line 206 is in this case indicated as being connected to a source of power of +3 volts. Base electrode 208 of transistor 112 is connected to line 206 through resistor 210 and base electrode 212 of transistor 114 is similarly connected to line 206 through resistor 214. Base electrode 208 of transistor 112 is cross-connected to collector 128 of transistor 114 through resistor 216 which is shunted by condenser 218. Symmetrically, base electrode 212 of transistor 114 is cross-connected to collector 200 of transistor 112 through a resistor 220 shunted by condenser 222.

The input line 110 to this binary stage is commonly connected to two control diodes 224 and 226. Diode 224 is also connected through a resistor 228 to one end of resistor 216 and through a condenser 230 to base 208 of transistor 112. Symmetrically, diode 226 is connected through resistor 232 to one end of resistor 220 and through a condenser 234 to base 212 of transistor 114. A power supply line 236 is permanently connected to a —6 volt source and this line and its tie line 238 connected thereto are directly connected to a pair of diodes 240 and 242 in the binary I circuit. The diode 240 is also connected to the collector electrode 200 of transistor 112 and diode 242 is connected to collector 128 of transistor 114. These diodes are called clamping diodes and prevent the specific collector electrode to which each is connected from going below —6 volts under any condition. It might be mentioned here that lines 236 and 238 are connected through diodes to all of the collectors of all of the stages of the inverter from the amplifier and wave squaring section on.

Binary I operates as a flip-flop circuit, that is one side conducts while the other is off and each negative going signal causing a switching from the non-conducting to the conducting state and vice versa. Assuming that transistor 114 is conducting and that transistor 112 is cut off, the application of a negative pulse to line 110 causes a charging of gate condenser 218 which drives the base 208 negative to turn on transistor 112. Turning transistor 112 on makes the base 212 of transistor 114 positive which turns it off. The next negative pulse again causes the base 212 to go negative to turn transistor 114 on and 112 off so that with every alternate negative pulse transistor 114 conducts which provides a one-half frequency output.

A similar binary or flip-flop circuit including transistors 120 and 122, previously identified as binary II, follows next in order but will not be described in detail as its circuitry is the same as binary I. These transistors 120 and 122 are supplied from the power line through resistances 124 and 126 and the signal output from the first binary counting circuit is supplied to binary II from the collector electrode 128 of transistor 114 through line 130 and thence alternately through rectifiers 132 and 134 and their associated gate circuits to the base circuits of the transistors 120 and 122. This pair of transistors again divides the frequency in two and applies the output to line 136 which couples into the next binary group, binary III, including transistors 138 and 140. The output of binary III is coupled through line 142 to binary IV including transistors 144 and 146 for further frequency division and that output again applied to coupling line 148 into binary V including transistors 150 and 152. Through these five binary counters or frequency dividers the frequency has been reduced from 76.8 kc. to 2400 cycles. This, however, is not quite low enough so it is necessary to utilize one last stage of frequency division which is provided by binary VI coupled to binary V through line 154. Binary VI includes transistors 156 and 158 and on the collector electrodes of transistors 156 and 158 a frequency of 1200 cycles is now obtained and applied through line 160 to the input of the ternary division or three halves division.

The purpose of the remainder of the circuitry shown in FIGS. 5 and 6 is to reduce the frequency of the power to 400 cycles and to divide it into three-phase power. In order to accomplish this two additional binary circuits identified as D and E are provided together with seven transistor gates identified as F, G, H, J, L, M and N. These all combine to develop on line 244 electrical voltage for a first phase A as was indicated in FIG. 1, on line 246 power for phase B which is precisely spaced at 120 degrees and on line 248 power for phase C. Line 160 is commonly coupled to the input of the two binary circuits indicated as D and E, since it is connected directly to a pair of rectifiers 162 and 164 in the binary circuit D and also to two input rectifiers 166 and 168 in the input circuit of the binary E. In this binary portion of the circuit it is desired to develop signals to control the transistor gate switching means F, G, H, J, L, M and N to give a 400 cycle output on the three properly phased and timed transmission lines 244, 246 and 248. The output of binary VI, 1200 cycles, triggers both binary D and E and together therewith provides conductive signals in proper phased relation to control switching means for the desired three-phase output as will now be described. Binary circuits D and E are not exactly like binary circuits I–IV, nor are they like each other. They are all substantially alike but are designed to require more factors to be present before switching occurs. The differences are the addition in binary D of a control signal diode 250 connected through condenser 252 to base 254 of transistor R and two control signal diodes 253 and 255 connected in parallel and through condenser 256 to the base 258 of transistor R'. In a similar manner in binary E control diode 260 is connected through condenser 262 to base

electrode 264 of transistor S and a control diode 266 is connected through condenser 268 to base 270 of transistor S'. Conductor 272 interconnects diode 250 of binary D with diode 266 of binary E. A tie line 274 connected to conductor 272 is connected to the collector electrode of transistor R' and then extends on to the input of transistor H. Diode 253 is connected through tie line 276 to conductor 278. Conductor 278 extends from the collector of transistor R to the input circuits of transistors G, J and L. The last diode 255 in binary D is connected to line 280 which extends from the collector of transistor S to the inputs of transistors J and M. Control diode 260 of binary E is connected through line 282 to the collector of transistor S' and to the input of transistor F.

It is desired to have each of the binaries D and E operate at a 400 cycle repetitive rate but as will be evident from the following detailed description it will not be a balanced wave. These two outputs, together with the control of the last regular binary VI, control the seven gate circuits in a manner to be described to provide the three-phase output.

In order to obtain a 400 cycle pulse in the D and E binary circuits, control switching must be built in as described. Logic equations can also be written which enable a clearer understanding of the operation. It has been worked out that if the following conditions are present the binary circuits D and E will produce a 400 cycle repetitive signal from a 1200 cycle input. The operating logic equations are; let R' be turned on when R is on, S' is on, and the master pulse from the last binary such as binary VI is applied, which can be called K. To indicate this, a point adjacent the collector of transistor 158 is labeled K and a similar location adjacent the collector of transistor 156 labeled K'. The equation can then be written for binary D;

$$R'=RS'K \tag{1}$$

On the other hand R' is turned off at any time that it is on and the master pulse is applied or

$$R'_0=RK \tag{2}$$

Equations can also be written for the E binary

$$S'=R'K \tag{3}$$
$$S'_0=S'K \tag{4}$$

which states that S' is turned on any time that R' is on and the master pulse is applied or that S' is turned off at any time that it is on and the master pulse is applied. It is to be further pointed out that only negative going pulses actuate the binaries.

Referring now to FIG 8 there is illustrated therein how the two binaries D and E produce the 400 cycle unbalanced waves from the 1200 cycle output of binary VI with the described logic controls by the control diodes to provide the equation logic. The first graph 300 at the top of FIG. 8 illustrates the voltage at point K. This is a 1200 cycle wave voltage since this is a point in binary VI. The second curve 302 is the inverse of that voltage appearing at opposite point K' since when one side is on or conducting the other is off. At time zero it is assumed that both R and S' are off and when K falls or goes negative at zero all factors of Equation 1 are met and R' is turned on as shown at 304 in the third graph 306. At 60° K. goes positive but this does not cause any change since only negative pulses cause switching and R' stays on. However, at 120° K. again goes negative. This time Equation 2 applies and R' is turned off. At this same instant, however, the same master pulse is applied to S'. S' has been off since it could not turn on with the first negative pulse at zero time since R' was off. At 120°, however, momentarily R' is on after the negative pulse is applied before it turns off and this permits S' to switch on as shown on curve 308. S' will remain on until the next negative going pulse of K at 240 and will turn off at that point as shown in graph 308, FIG. 8. However, R'

cannot turn back on at this point as one of the requisites of Equation 1 was that S be off before it could turn on and it, therefore, remains off for next negative going pulse to repeat. This provides unbalanced pulses at R' and S' repeating at a 400 cycle rate. Curves of the other half of each binary R and S are, of course, the inverse of R' and S' and are shown at 307 and 309 on FIG. 8.

Having now developed the various timed pulses which are produced at the various binary outputs shown at locations K, K', R', R, S' and S it is now desired to describe how these pulses control the seven gates to apply the proper output voltages on lines 244, 246 and 248 for a full three-phase output. In order to assist in the understanding, this portion of the circuit diagram has been diagrammatically re-drawn and is shown in FIG. 7 and the transistor gates are indicated therein by the letters which previously defined the transistors in the circuit of FIGS. 5 and 6.

Referring now specifically to FIG. 7, there is shown therein the three-phase output lines 244, 246 and 248 which are also labeled phase A, phase B and phase C. From FIG. 6 it is seen that phase A is controlled primarily by transistor L since it is directly connected to the collector 301 thereof. Transistor L is in turn controlled by either one of two signals, one from the binary terminal R through control diode 303 and the other from the output of transistor F through diode 305. If either one of these inputs goes negative, transistor L will conduct and allow voltage to appear from the −12 volt power supply on the line. This is diagrammatically shown in FIG. 7 by the two lines extending from the rectangular-shaped representation L to the left. The first line 278 connects the transistor L directly with the output of transistor R and as this point goes negative will cause the same to conduct. The transistor L is also connected through line 320 to the output of transistor F.

Transistor F on the other hand is also controlled by two signal voltages. One of these is the voltage appearing at binary terminal S' and is applied through diode 307. The connection is shown on FIG. 7 as line 322. The other control signal for gate transistor F is the voltage appearing at the 1200 cycle master pulse binary K' and is applied through diode 309. The connecting line is shown on both FIGS. 5 and 7 at 324. Therefore, when either of these points K' and S' go negative, gate transistor L will be driven into conduction and the pattern of the wave form so generated will later be specifically described.

In like manner the wave form appearing on output line 246, phase B is controlled primarily by gate transistor M. Transistor M in turn is controlled through diode 311 by the pulse appearing at location S through line 280. Transistor M is also controlled by a second gate transistor G which is gated by the pulses appearing at R and K' through diodes 313 and 315, respectively. These signals are applied through lines 278 and 326.

Lastly, the voltage wave appearing on line 248 for phase C is primarily controlled by gate transistor N which in turn is controlled by a pair of gate transistors H and J through diodes 317 and 319. H is in turn controlled by the pulses appearing at R' and K' through diodes 321 and 323 and their associated lines 274 and 326, respectively. Transistor J, on the other hand is controlled by the pulses appearing at points S and R applied through diodes 325 and 327 and lines 280 and 278, respectively. As before mentioned, whenever a negative going signal appears at any one of the control points R, R', S, S' or K or K' then any particular gate connected thereto is opened and the opening of one portion of a gate is sufficient to allow conduction for the system controlled thereby.

Referring now to the lower group of curves shown in FIG. 8, an explanation will follow as to how, through these described pulses and gates the desired signal shape is obtained for each phase, precisely spaced from the others. The first two graphs or curves to be considered are identified at the lefthand side as F and L. These represent the "Off" and "On" cycles for these two gate transistors and, therefore, the wave form that is created or gated thereby. The wave form passed by F is shown as curve 330 and the following discussion will describe how this is developed.

As mentioned above the gate will be open at any time that the pulses applied thereto go negative. The 360 degree cycle is divided into six different portions of 60° each, marked across the top of the whole diagram in FIG. 8 with zero time at the left and these portions will, therefore, be referred to hereafter by their associated numbers. It is noted on FIG. 7 that transistor F is controlled by the voltage at K' and the voltage at S'. Beginning at time zero and considering only K', K' from curve 302 is noted as being negative at time periods 2, 4 and 6. Therefore, transistor F would be on during these periods due to this pulse. This is indicated to curve 330 by the long dash line in these sections labeled at the righthand side K'. During this cycle S' from curve 308 is also negative during periods 1 and 2 and 5 and 6. This is indicated on curve F by the short dash lines in these squares just below the main curve labeled S at the right. It is now evident that transistor F will be on at all times except during time period 3 which is from 120 to 180 electrical degrees and during that period it will be off. This is shown in curve 330.

So far, therefore, transistor L connected thereto and controlled by F and the current on line 244 would be on for only 60 electrical degrees out of the whole cycle. It is, therefore, necessary to further open transistor L for an additional 120° adjacent the first sixty to form a uniform 180° "On" cycle. This is accomplished by triggering transistor L also through R. Referring back to curve 307 it is noted that in the curve for point R this point goes negative at time zero and stays negative for 120° which is indicated by the dash and dot lines under curve 332 for transistor L. Also transistor F is turned on for time period 3 as before described and indicated by the dash line so there is now obtained an "On" period of 180° from zero to 180 and an "Off" period of 180° from 180 to 360. This provides the voltage on phase A and is a 400 cycle voltage, a third of the original 1200.

In like manner curve 334 is developed to illustrate the "On" and "Off" periods of transistor G which assists in the control of the voltage developed for phase B. In this instance, from FIG. 7 it is noted that transistor G is controlled by pulses from R and K'. Referring to the curve 302 we again note that K' is negative in time periods 2, 4 and 6. This is indicated by the long dash lines across these time periods for curve 334 indicated by K' at the right of the curve. This transistor will, therefore, be turned on by this pulse during these periods. It is also controlled by R and referring to curve 307 we note that R is negative during time periods 1 and 2 and this is indicated by the short dash lines extending across these time periods. This pulse tends to turn on transistor G during time periods 1 and 2. The fact that it has already been turned on by the pulse from the point K' during time period 2 makes no difference. As a result of these two control pulses transistor G is turned on during time periods 1, 2, 4 and 6 and off during periods 3 and 5. Referring back again to FIG. 7, since transistor G controls final gate transistor M for phase B an additional control pulse must be obtained to fill in the gap in time period 4. This is obtained from point S. Specifically referring now to curve 336 identified also as M and again remembering that transistor M will be conductive only when negative pulses are applied thereto, it is found that M will have negative pulses applied thereto during time periods 3 and 5 from transistor G as shown in curve 334 and as identified in curve 336 by the long dash lines,

and it will also have applied thereto negative control pulses directly from point S and by referring to the curve representing the voltages at that location we see from curve **309** that those voltages go negative during time periods 3 and 4 which is indicated by the short dash lines. Therefore, while there is some overlap we now find that the transistor M will be nonconductive during time periods 1 and 2, conduct through time periods 3, 4 and 5, and be non-conductive during time period 6. This again gives us our desired wave form of 180 degrees on and 180 degrees off and it is to be further noted that it is spaced 120 electrical degrees from phase A.

In similar manner the voltage appearing on phase C will now be developed and it is here noted that two control gate transistors are used to control the final transistor. There will be developed, therefore, a curve for both gate transistors H and J. The curve for transistor H is shown at **338** and by reference back to FIG. 7 it is noted that transistor H is controlled by the pulses appearing on R' and K'. By reference to curve **306** it is noted that R' is negative during time periods 3, 4, 5 and 6. This is indicated just under curve **338** by the long dash lines identified as R' at the right. This transistor is also controlled by the pulses appearing at K' and by reference to curve **302** it is noted that K' is negative during time periods 2, 4 and 6. This is indicated by the short dash lines appearing across those time periods and identified as K' at the right-hand side. The step curve **338**, therefore, indicates an "Off" period for time period 1 and an "On" period for the other five periods of the cycle. The last curve to be developed is curve **340** which relates to the operation of gate transistor J. Gate transistor J is shown in FIG. 7 as controlled by the pulses appearing at points S and R. By reference to curve **307** representing R it is found that this is negative during time periods 1 and 2 which would turn on transistor J and this is indicated for curve **340** by the long dash lines under the main curve and identified by R on the righthand side. Reference to curve **309** indicating the condition at the S point shows that S is negative during time periods 3 and 4 and this is indicated by the short dash lines during those time periods and the letter S at the right. When these two transistors H and J combine to control transistor N it will be noted that there is a negative pulse available during time period 1 due to transistor H as shown by the long dash line and H in the righthand side and also during 5 and 6 due to transistor J as shown by the short dash lines and J on the righthand side to cause the transistor N to conduct and the rest of the time it is off. This produces the third phase for phase C which is again spaced 120 electrical degrees from the other two.

The result of these timed and gated circuits is, therefore, a three-phase precisely spaced current on the three output lines **244**, **246** and **248** which is fed into the three lines identified as A, B and C phases and as shown in FIG. 1 each further amplified and finally appears as a full three-phase 400 cycle output.

What is claimed is:

1. A system for generating three-phase alternating current power comprising, a source of direct current power, a high frequency oscillator connected to said source of direct current power and having an output circuit, binary frequency dividing means connected to the output circuit of the oscillator and dividing the high frequency of the alternating current from the oscillator in even multiples to a lower value, a three halves division section connected to the output of the binary frequency dividing means to provide further frequency division, a three-phase power line and gating means connected to the three-phase line, to the output of the binary frequency dividing means, and to each portion of the three halves division section to so gate the flow of current to the three-phase line as to produce a properly spaced three-phase power output.

2. A system for generating three-phase alternating current power comprising a source of direct current power, a high frequency oscillator connected to the source of direct current power and providing a high frequency alternating current output, means for dividing the frequency in even multiples connected to the high frequency oscillator to reduce the frequency of the output thereof, means for dividing the frequency in odd multiples connected to the output of the first-named means for further dividing the frequency, a three-phase output line and a plurality of gating means connected to the three-phase output line and to each portion of the outputs of the both of the means for dividing the frequency to provide a three-phase output.

3. In a system for generating three-phase alternating current power comprising a source of direct current power, a high frequency oscillator connected to said source of direct current power and providing a high frequency alternating current output, frequency dividing means connected to the oscillator to provide both even multiple division and odd multiple division frequencies, a three-phase power line and a plurality of gating circuits connected to the three-phase power line and to the output of the even and to each portion of the odd multiple division means to produce three-phase power on the three-phase lines.

4. In a system for generating three-phase alternating current power comprising a source of direct current power, a high frequency oscillator connected to said source of direct current power and providing a high frequency alternating current output, binary frequency dividing means connected to the oscillator output to reduce the frequency of the alternating current in even steps to a relatively low frequency, ternary frequency dividing means connected to the output of the binary frequency dividing means to provide a plurality of dephased signals having an output frequency of one-third of the output frequency of the binary frequency dividing means, a three-phase power line, a plurality of gating circuits connected to the three-phase power line and to the output of the binary frequency dividing means and to each portion of the ternary frequency dividing means to so gate the signals from these points as to produce three-phase power on the three-phase line.

5. In a system for generating three-phase alternating current power comprising a source of direct current power, a high frequency oscillator connected to said source of direct current power and providing a high frequency alternating current output, binary frequency dividing means connected to the oscillator output to reduce the frequency of the alternating current in even steps to a relatively low frequency, ternary frequency dividing means connected to the output of the binary frequency dividing means to provide a plurality of dephased signals having an output frequency of one-third of the output frequency of the binary frequency dividing means, a three-phase power line, a plurality of gating circuits connected to the three-phase power line and to the output of the binary frequency dividing means and to each portion of the ternary frequency dividing means to so gate the signals from these points as to produce a three-phase power on the three-phase line, amplifier means connected to each line of the three-phase power line to independently amplify the voltage in each phase, filter means connected to each amplifier means to convert the square wave output of the amplifier means into sine wave form and three-phase output connections to combine the output of all filters.

6. In a system for generating three-phase alternating current power comprising a source of direct current power, a high frequency oscillator connected to said source of direct current power and providing a high frequency alternating current output, binary frequency dividing means connected to the oscillator output to reduce the frequency of the alternating current in even steps to a relatively low frequency, ternary frequency dividing means con-

nected to the output of the binary frequency dividing means to provide a plurality of dephased signals having an output frequency of one-third of the output frequency of the binary frequency dividing means, a three-phase power line, a plurality of gating circuits connected to the three-phase power line and to the output of the binary frequency dividing means and to each portion of the ternary frequency dividing means to so gate the signals from these points as to produce three-phase power on the three-phase line, amplifier means connected to each line of the three-phase power line to independently amplify the voltage in each phase, filter means connected to each amplifier means to convert the square wave output of the amplifier into sine wave form, stabilizing feedback means from the filter output to each amplifier means to regulate each phase independently, and three-phase output connections to combine the outputs of all filter means.

7. In a system for generating three-phase alternating current power comprising a source of direct current power, a high frequency oscillator connected to said source of direct current power and providing a high frequency alternating current output, binary frequency divider means connected to the output of the high frequency oscillator to reduce the frequency of the alternating current in even steps to 1200 cycles, a pair of binary circuits commonly connected to the output of the binary frequency divider means and simultaneously provided with

signals therefrom to form a ternary divider section, said pair of binary circuits being cross connected so that between the 1200 cycle signals supplied by the binary frequency divider means and the cross connection, each of the pair of binary circuits operates at a frequency of 400 cycles with an unbalanced wave, three separate conductive lines, and a plurality of gating circuits connected to the 1200 cycle output and each binary circuit with 400 cycle output and to the three lines, to so time conduction periods as to produce on those lines properly phased three-phase power.

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