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FORM 1

SPRUSON & FERGUSON

APPLICATION ACCEPTED AND AMENDMENTS ALLOWED 18.12.90

COMMONWEALTH OF AUSTRALIA

PATENTS ACT 1952

APPLICATION FOR A STANDARD PATENT

Siemens Aktiengesellschaft, incorporated in the Federal Republic of Germany, of Wittelsbacherplatz 2, 8000 Muenchen, FEDERAL REPUBLIC OF GERMANY, hereby apply for the grant of a standard patent for an invention entitled:

Method and Arrangement for Generating a Correction Signal in a Digital Timing Recovery Device

which is described in the accompanying complete specification.

Details of basic application(s):-

Basic Applic. No:	Country:	Application Date:
P3739834.2	DE	24 November 1987
P3805259.8	DE	19 February 1988

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DATED this TWENTY FIRST day of NOVEMBER 1988

Siemens Aktiengesellschaft

By: M.J. Anderson

Registered Patent Attorney

TO: THE COMMISSIONER OF PATENTS
OUR REF: 78231
S&F CODE: 61890

S003809 5845/2 23/11/88

SPRUSON & FERGUSON

COMMONWEALTH OF AUSTRALIA
THE PATENTS ACT 1952

AUSTRALIA
CONVENTION
STANDARD
& PETTY PATENT
DECLARATION

DECLARATION IN SUPPORT OF A CONVENTION APPLICATION FOR A PATENT

In support of the Convention Application made for a patent for an invention entitled:

Title of Invention

Method and Arrangement for Generating a Correction Signal in a Digital Timing Recovery Device

Full name(s) and address(es) of Declarant(s)

I/~~We~~ Fraser Patison Old

care of Spruson & Ferguson
St Martins Tower, 31 Market Street,
Sydney, New South Wales 2000, Australia

do solemnly and sincerely declare as follows:-

Full name(s) of Applicant(s)

+. ~~I am/We are the applicant(s) for the patent~~

(or, in the case of an application by a body corporate)

1. I am/We ~~are~~ authorised by

Siemens Aktiengesellschaft

the applicant(~~s~~) for the patent to make this declaration on its/~~their~~ behalf.

2. The basic application(s) as defined by Section 141 of the Act ~~was~~/were made

Basic Country(ies)

in Federal Republic of Germany

Priority Date(s)

on 24 November, 1987 and 19 February, 1988

Basic Applicant(s)

both by Siemens Aktiengesellschaft

~~3. I am/We are the actual inventor(s) of the invention referred to in the basic application(s)~~

Full name(s) and address(es) of inventor(s)

(or where a person other than the inventor is the applicant)

3. IMRE SARKOEZI

of Karl Witthalm Street 42,
8000 Muenchen 70,
Federal Republic of Germany

~~(respectively)~~

is/~~are~~ the actual inventor(~~s~~) of the invention and the facts upon which the applicant(~~s~~) is/~~are~~ entitled to make the application are as follows:

Set out how Applicant(s) derive title from actual inventor(s) e.g. The Applicant(s) is/are the assignee(s) of the invention from the inventor(s)

The said applicant is the assignee of the actual inventor.

4. The basic application(s) referred to in paragraph 2 of this Declaration ~~was~~/were the first application(s) made in a Convention country in respect of the invention(s) the subject of the application.

Declared at Sydney this 15th day of November, 1988

.....
Signature of Declarant(s)

SFP4 To: The Commissioner of Patents 1/81

(12) PATENT ABRIDGMENT (11) Document No. AU-B-25863/88
(19) AUSTRALIAN PATENT OFFICE (10) Acceptance No. 594593

(54) Title
METHOD AND ARRANGEMENT FOR GENERATING A CORRECTION SIGNAL IN A DIGITAL TIMING RECOVERY DEVICE

International Patent Classification(s)
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SPRUSON & FERGUSON

(56) Prior Art Documents
AU 24415/88 H04L 25/40 7/00
AU 582317 81809/87 H04L 25/40 7/00 5/200

(57) A phase sensor for carrying out the method is also claimed.

CLAIM

1. Method for generating a correction signal in a digital timing recovery device upon reaching a defined phase spacing between a digital signal and a first data auxiliary clock pulse associated therewith, said first data auxiliary clock pulse representing a selectio. of one clock pulse from a plurality of clock pulses having the same frequency, wherein the plurality of clock pulses have fixed and equal phase relationship with respect to each other, said frequency is somewhat greater or smaller then the bit rate of the digital signal characterized in that the data auxiliary clock pulse is sampled with the leading edge of the pulse of the digital signal until an edge of a selected edge type of the data auxiliary clock pulse is detected by means of a change in state during the sampling, and in that the correction signal is then triggered.

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FORM 10

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COMPLETE SPECIFICATION

(ORIGINAL)

FOR OFFICE USE:

Class Int Class

Complete Specification Lodged:
Accepted:
Published:

Priority:

Related Art:

This document contains the amendments made under Section 49 and is correct for printing.

Name and Address of Applicant: Siemens Aktiengesellschaft
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8000 Muenchen
FEDERAL REPUBLIC OF GERMANY

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Level 33 St Martins Tower, 31 Market Street
Sydney, New South Wales, 2000, Australia

Complete Specification for the invention entitled:

Method and Arrangement for Generating a Correction Signal in a Digital Timing Recovery Device

The following statement is a full description of this invention, including the best method of performing it known to me/us

5845/3

Abstract

Method and arrangement for generating a correction signal for a digital timing recovery device.

This method is intended to allow phase sensors which can be realized in integrated technology with the minimum possible outlay.

In a sample and hold circuit (3), a data auxiliary clock pulse (DHT1), which applies as a recovered clock pulse of a digital signal (DS1) and the clock pulse frequency of which, which is somewhat greater or smaller than the bit rate of this digital signal (DS1), is sampled by said digital signal. If a trailing edge of a pulse of this data auxiliary clock pulse (DHT1) is established thereby via a change in state, the sample and hold circuit (3) outputs a correction request signal (K1) which triggers in a downstream device (6) a correction signal (K) which is synchronous to the data auxiliary clock pulse (DHT1).

This method is used in digital timing recovery devices.

Fig. 1.

Method and arrangement for generating a correction signal for a digital timing recovery device.

The invention relates to a method for generating a correction signal in a digital timing recovery device upon reaching a defined phase spacing between a digital signal and a first data auxiliary clock pulse associated therewith which represents a selection changing with the phase spacing of one of several auxiliary clock pulses having the same frequency, which is somewhat greater or smaller than the bit rate of the digital signal, and having the same phase spacing between each other.

A method of this kind is the basis of two earlier proposals. According to a first one Australian Patent Application No. 81809/87 a phase sensor outputs a correction signal when the effective edge of the data auxiliary clock pulse approaches an edge of the digital signal at less than a fixed time interval. For this purpose it requires a delay device. In the second one Australian Patent Application No. 24415/88 the correction signal is obtained when the effective flanks of the digital signal match a special clock pulse likewise derived from an auxiliary clock pulse and having the same frequency as the data auxiliary clock pulse and displaced with respect to the latter by a certain value in the phase.

The object of the invention is to disclose a method which can be realized without delay device and also without a special clock pulse and which can hence be carried out in integrated circuit technology also for bit rates equal to or greater than 34 Mbit/s.

According to one aspect of the present invention there is disclosed a method for generating a correction signal in a digital timing recovery device upon reaching a defined phase spacing between a digital signal and a first data auxiliary clock pulse associated therewith, said first data auxiliary clock pulse representing a selection of one clock pulse from a plurality of clock pulses, having the same frequency, wherein the plurality of clock pulses have fixed and equal phase relationship with respect to each other, said frequency is somewhat greater or smaller then the bit rate of the digital signal characterized in that the data auxiliary clock pulse is sampled with the leading edge of the pulse of the digital signal until an edge of a selected edge type of the data auxiliary clock pulse is detected by means of a change in state during the sampling, and in that the correction signal is then triggered.

It is advantageous if the sampling is blocked

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for the duration of the correction signal.

It is furthermore advantageous if a symmetrical pulse is selected as the first data auxiliary clock pulse and if, for the detection, the edge type where the edges have the defined phase spacing of 0.5 UI (Unit Interval) is selected.

The defined phase spacing or the fixed time interval is used as a gauge, the measured phase spacing or time interval between the effective edges of the data auxiliary clock pulse and the leading edges of the pulses of the digital signal continuously changing in a defined range. When the measured spacing reaches the gauge, the correction signal is triggered.

Arrangements for carrying out this method can be found in the device claims.

The invention will be explained in more detail with reference to exemplary embodiments.

Figure 1 shows a block circuit diagram of the phase sensor according to the invention for a binary digital signal,

Figure 2 shows a pulse diagram for explaining the function of the phase sensor according to Figure 1,

Figure 3 shows a block circuit diagram of the phase sensor according to the invention for a bipolar digital signal,

Figure 4 shows the block circuit diagram of a commercially available D flip-flop with test inputs and

Figure 5 shows in detail a first phase sensor according to the invention,

Figure 6 shows a pulse diagram for explaining the first phase sensor,

Figure 7 shows in detail a second phase sensor according to the invention and

Figure 8 shows a pulse diagram for explaining the second phase sensor.

Figure 1 shows a phase sensor according to the invention for a binary digital signal DS1 with a sample and hold circuit 3 and a device 6 for generating the correction signal K. Figure 2 shows the associated

pulses.

The leading edges of the digital signal DS1 at input 1 move depending on the sign of the frequency deviation with respect to the data auxiliary clock pulse DHT1 at input 2 from clock pulse period to clock pulse period either only to the left or only to the right of these selected trailing edges. In Figure 2 they move only to the right, as is indicated by dashes, until the present phase position represented by a solid line is reached. In each clock pulse period, the data auxiliary clock pulse DHT1 is sampled with the leading effective edge of the pulses of the digital signal DS1. By evaluating the samples, the trailing edge of the data auxiliary clock pulse DHT1 is detected. Upon detection of the state change of the samples at time t1, a correction request signal K1 is generated at connection 4. The favourable phase spacing of 0.5 UI between the effective leading edges of the data auxiliary clock pulse DHT1 and the leading edge of the pulses of the digital signal DS1 is obtained from the spacing between the trailing and the leading edge of a period of the data auxiliary clock pulse DHT1. The symmetry of the data auxiliary clock pulse DHT1 must be great for the required position. This can be realized for the most part independently of the tolerances. In the device 6, the correction signal K is generated at output 7 synchronously to the data auxiliary clock pulse DHT1.

In contrast to the second earlier proposal, this is achieved without a special clock pulse derived from the auxiliary clock pulse.

Figure 3 shows a phase sensor according to the invention for a bipolar digital signal with the half-waves DS2a and DS2b. The first half-wave DS2a is supplied to the sample and hold circuit 3. A further sample and hold circuit 10 is introduced for the second half-wave DS2b. The device 6a for generating the correction signal K has two inputs for the correction request signals K1 and K2 from both sample and hold circuits 3 and 10. It carries out an OR operation on both correc-

tion request signals K1 and K2.

Figure 4 shows the block circuit diagram of a commercially available D flip-flop with test inputs. Besides the D flip-flop 16, it contains an inverter 12, AND gates 13 and 14 and an OR gate 15.

Besides a D input, a clock pulse input CP, a reset input $\overline{R}$ and a Q output and a $\overline{Q}$ output, a test input TI and a test enable input TE are provided.

Figure 5 shows in detail a phase sensor according to the invention which can be used in a timing recovery device working with negative frequency deviation. The circuit part witn the solid lines is required for a binary digital signal DS1. For a bipolar digital signal DS2a, DS2b, the circuit part with the dashed lines is additionally required. The arrangement consists of sample and hold circuits with simple D flip-flops 3a and 10a and a device 6a1 for generating the correction signal K. The latter contains a first stage with a NAND gate 17a and a D flip-flop with test inputs 18, a second stage with a D flip-flop with test inputs 19 and a reset stage with an AND gate 20.

The phase sensor realized with digital integrated D flip-flop cells works under special conditions. For the reliable switching of a D flip-flop, it must be ensured that the signal at the D input is not subjected to a change in state during the declocking. Otherwise instable switching operations could result, the initial state of the D flip-flop then being undefinable. A metastable state would then arise. However, since the phase sensor serves specifically to detect a change in the data auxiliary clock pulse DHT1, the probability of the occurrence of unstable switching operations is therefore relatively high. This means that the correction request signal K1 can often become unstable. Metastable states can, however, be suppressed by a multistage sampling of the correction request signal K1. This is realized in two stages in the synchronous generation of the correction signal K by means of the D flip-flop with test inputs 18 and 19. Both the genera-

tion of the correction signal K as well as the resetting are synchronous to the data auxiliary clock pulse DHT1.

How this phase sensor works will be explained below also with reference to the pulse diagram in Fig. 6: The setting signal E at input 21 with the logical "L" state sets all D flip-flops 3a, 10a, 18 and 19 to their initial state. The Q outputs of the D flip-flops 18 and 19 as well as the output of the AND gate 20 receives the logical "L" state. Following this, the $\overline{Q}$ outputs of the D flip-flops 3a and 10a assume the logical "H" state and finally the output of the NAND gate 17a assumes the logical "L" state. Via the feedback from the Q output of the D flip-flop 19 to the TE inputs of the D flip-flops 18 and 19, the latter are switched to D mode. This state remains unchanged as long as the sampling values have the logical "L" state. This corresponds to a logical "H" state at the $\overline{Q}$ output of the D flip-flop 3a. If, on the other hand, the sampling value has the logical "H" (t_1) state and accordingly the $\overline{Q}$ output has the logical "L" state, then this means a correction request signal K1. The latter is read into the D flip-flop 18 as a precorrection signal K^* at instant t_2 with the here effective leading edge of the data auxiliary clock pulse DHT1 via the NAND gate 17a. If this reading-in operation was executed in a stable manner, then in the next period of the data auxiliary clock pulse DHT1 a synchronous correction signal K is generated (t_3) by means of the precorrection signal K^* from the D flip-flop 19 at the Q output. Otherwise this does not take place. The correction signal K with the logical state "H" simultaneously switches the D flip-flops 18 and 19 over to the test inputs TI, which were moved to the logical "L" state via the input 22, in order to switch off the correction signal K at instant t_4 in the subsequent period of the data auxiliary clock pulse DHT1. The correction signal K triggers at instant t_3 a switch-over US in the auxiliary clock pulses, the effective edge of the next DHT period being displaced forwards by the switch-over with the phase

spacing of the auxiliary clock pulses at instant t_4 and hence a phase correction being created. During the generation of the correction signal K (between instants t_2 and t_4), the $\overline{Q}$ outputs of the D flip-flops 18 and 19 block a further sampling via the AND gate 20. At instant t_5, the phase sensor can again monitor the phase position of the digital signal DS1 with respect to DHT1 by means of sampling.

On a bipolar digital signal DS2a, DS2b is supplied to the inputs 1 and 8, the correction signal K can be generated both by the correction request signal K1 and from the correction request signal K2.

Fig. 7 shows a two-stage "bisynchronous" phase sensor for a timing recovery device working with positive frequency deviation. Bisynchronous means that the correction signal K for producing a delay equalization for the switch-over is generated synchronously to a second derived data auxiliary clock pulse DHT2, the sample and hold circuit 3a and 10a and the reset stage 26 to 30 fixedly connected thereto continue to run synchronously to the data auxiliary clock pulse DHT1.

The arrangement contains a D flip-flop 3a as the sample and hold circuit and, in the case of a processing of bipolar digital signals, additionally a D flip-flop 10a. The rest of the circuit is a device 6a2 for generating the correction signal K. This device contains a first stage with a NAND gate 17 and a D flip-flop 23, a second stage with a D flip-flop with test inputs 24 and a reset stage with an inverter 27, with NAND gates 26 and 29, with an OR gate 28, with an NOR gate 30 and with a D flip-flop 25. The way this arrangement works is also evident from the pulse diagram in Figure 8.

The setting signal E causes with its logical "L" state the device 6a2 to return to its initial state, in that all D flip-flops 3a, 23, 24 and 25 are reset either directly or via the gates. The binary digital signal DS1 is applied to the digital signal input 1 and to the data auxiliary clock pulse input 2 of the data auxiliary clock pulse DHT1. In the D flip-flop 3a, the data auxi-

liary clock pulse DHT1 is then sampled with the digital signal DS1. If the Q output assumes a logical "L" state during the sampling, then this means a correction request signal K1 (t_1). After the reset via the S input, the Q output switches to a logical "H" state.

If half-waves of a bipolar digital signal DS2a and DS2b are present at the digital signal inputs 1 and 8, then a further correction request signal K2 can be generated by the D flip-flop 10a. If in the first stage one of the two inputs of the NAND gate 17 then assumes a logical "L" state, then the D input of the D flip-flop 23 receives a logical "H" state. If this operation was executed in a stable manner, this state is read in (t_2) with the data auxiliary clock pulse DHT2, which has a fixed phase spacing with respect to the data auxiliary clock pulse DHT1, as a precorrection signal K^*. This precorrection signal K^* can be used favourably for the preparation of the switch-over assuming that a metastable operation in this signal cannot cause an incorrect control. In the subsequent period of the data auxiliary clock pulse DHT2, this logical "H" state is read in further at instant t_3 into the D flip-flop 24 of the second stage and the correction signal K arises there at the Q output thereof. This triggers the switch-over US, the effective edges of both data auxiliary clock pulses DHT1 and DHT2 being displaced backwards with the phase spacing of the auxiliary clock pulses, so that at instant t_4 this logical "H" state is read in further via the data auxiliary clock pulse DHT1 into the D flip-flop 25 of the reset stage and the Q output thereof likewise receives the logical "H" state as a reset signal R^*. After the trailing edge of the data auxiliary clock pulse DHT1 (t_5), the D flip-flop 24 is reset via the gate combination 26, 28 and 29 and the reset input and hence the correction signal K is terminated.

The D flip-flops 3a, 10a and 23 are reset via the correction signal K by the reset signal R and blocked until the Q output of the D flip-flop 25 again assumes a logical "L" state with the data auxiliary

clock pulse DHT1 at instant t_6. At instant t_7, the phase position of the digital signal DS1 is again monitored.

With the introduction of the second data auxiliary clock pulse DHT2, the phase spacing of which to the data auxiliary clock pulse DHT1 can be variably selected for matching the delays, the probability of the occurrence of metastable states at the precorrection signal K^* may in some circumstances increase. As a result of using a D flip-flop 24 with test inputs in the second stage, however, the instance of such states on the correction signal K can be avoided.

Both phase sensors can be realized and integrated HCMOS technology for bit rates $\geq$ 34 Mbit/s.

12 Patent claims
8 Figures

The claims defining the invention are as follows:

1. Method for generating a correction signal in a digital timing recovery device upon reaching a defined phase spacing between a digital signal and a first data auxiliary clock pulse associated therewith, said first data auxiliary clock pulse representing a selection of one clock pulse from a plurality of clock pulses having the same frequency, wherein the plurality of clock pulses have fixed and equal phase relationship with respect to each other, said frequency is somewhat greater or smaller then the bit rate of the digital signal characterized in that the data auxiliary clock pulse is sampled with the leading edge of the pulse of the digital signal until an edge of a selected edge type of the data auxiliary clock pulse is detected by means of a change in state during the sampling, and in that the correction signal is then triggered.

2. Method according to claim 1, characterized in that the sampling is blocked for the duration of the correction signal.

3. Method according to claim 1, characterized in that a symmetrical pulse having a pulse duration equal to half the period of said pulse is selected as the first data auxiliary clock pulse and in that, for the detection, the edge type where the edges have the defined phase spacing of 0.5 UI is selected.

4. Phase sensor for carrying out the method according to any one of the preceding claims, characterized in that a first sample and hold circuit is provided with a first digital signal input and with a first data auxiliary clock pulse input, and in that a device for generating the correction signal is provided following said first sample and hold circuit.

5. Phase sensor according to claim 4, characterized in that, as the first sample and hold circuit, a first D flip-flop is provided, the D input of which is connected to the first data auxiliary clock pulse input and the clock pulse input of which is connected to the first digital signal input.

6. Phase sensor according to claim 4 or 5, characterized in that the first digital signal input serves to receive a binary digit signal.

7. Phase sensor for a timing recovery device according to claim 4 or 5 working with negative frequency deviation, characterized in that in a device for generating the correction signal there is provided,

a first NAND gate, the first input of which is connected to the output of the first sample and hold circuit,

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a first D flip-flop with test inputs, the D input of which D flip-flop is connected to the output of the first NAND gate, the clock pulse input of which D flip-flop is connected to the first data auxiliary clock pulse input, the TI input of which D flip-flop is connected to an input for a logical "L" state, the reset input of which D flip-flop is connected to a setting signal input and the Q output of which D flip-flop is connected to the second input of the first NAND gate,

a second D flip-flop with test inputs, the D input of which D flip-flop is connected to the Q output of the first D flip-flop with test inputs, the clock pulse input of which D flip-flop is connected to the first data auxiliary clock pulse input, the reset input of which D flip-flop is connected to the setting signal input, the TI input of which D flip-flop is connected to the input for a logical "L" state and the Q output of which D flip-flop is connected to a correction signal output as well as to the TE inputs of the first and second D flip-flop with test inputs, and

a first AND gate, the first input of which is connected to the Q output of the second D flip-flop with test inputs, the second input of which is connected to the setting signal input, the third input of which is connected to the third input of the first NAND gate and the output of which is connected to a reset input of the first sample and hold circuit.

8. Phase sensor for a timing recovery device according to claim 4 or 5 working with positive frequency deviation, characterized in that in a device for generating the correction signal there is provided a first NAND gate, the first input of which is connected to the output of the first sample and hold circuit,

a second D flip-flop, the D input of which is connected to the output of the first NAND gate, the clock pulse input of which D flip-flop is connected to an input for a second data auxiliary clock pulse which has a fixed phase spacing with respect to the first data auxiliary clock pulse, and the reset input of which is connected to a set input of the first D flip-flop,

a third D flip-flop with test inputs, the D input of which D flip-flop is connected to the Q output of the second D flip-flop , the clock pulse input of which D flip-flop is connected to the input for the second data auxiliary clock pulse, the Q output of which D flip-flop is connected to the correction signal output,

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and the test input of which is connected to an input for a logical "H" state, a third D flip-flop, the D input of which is connected to the Q output and to the test enable input of the third D flip-flop with test inputs and the reset input of which is connected to the setting signal input, a second NAND gate, the first input of which is connected to the first data auxiliary clock pulse input and the second input of which is connected to the setting signal input,

an inverter, the input of which is connected to the setting signal input,

an OR gate, the first input of which is connected to the output of the inverter and the second input of which is connected to the Q output of the third D flip-flop,

a third NAND gate, the first input of which is connected to the output of the second NAND gate, the second input of which is connected to the output of the OR gate and the output of which is connected to the reset input of the third D flip-flop with test inputs, and

a NOR gate, the first input of which is connected to the Q output of the third D flip-flop, the second input of which NOR gate is connected to the Q output of the third D flip-flop with test inputs, the third input of which NOR gate is connected to the output of the inverter and the output of which is connected to the set input of the first D flip-flop and the the reset input of the second D flip-flop.

9. Phase sensor according to claim 4 or 5, characterized in that a second sample and hold circuit is provided with a second input for the digital signal and a second input for the data auxiliary clock pulse wherein a conductive connection is provided between the first and second inputs for the data auxiliary clock pulse.

10. Phase sensor according to claim 7 and 9, characterized in that, as the second sample and hold circuit, a fourth D flip-flop is provided, the D input of which is connected to the second data auxiliary clock pulse input, the Q output of which D flip-flop is connected to a second input of the first NAND gate, the clock pulse input of which D flip-flop is connected to the second digital signal input and the reset input of which is connected to the output of the AND gate.

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11. Phase sensor according to claims 8 and 9, characterized in that, as the second sample and hold circuit, the fourth D flip-flop is provided, the D input of which is connected to the second data auxiliary clock pulse input, the Q output of which D flip-flop is connected to a second input of the first NAND gate, the clock pulse input of which D flip-flop is connected to the second digital signal input and the set input of which D flip-flop is connected to the output of the NOR gate.

12. Phase sensor according to claim 9, 10 or 11 characterised in that the first digital signal input serves to receive the first half-wave of a bipolar digital signal and the second digital signal input servies to receive the second half-wave of said bipolar digital signal.

DATED this TWENTIETH day of NOVEMBER 1989
Siemens Aktiengesellschaft

Patent Attorneys for the Applicant
SPRUSON & FERGUSON

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FIG 1

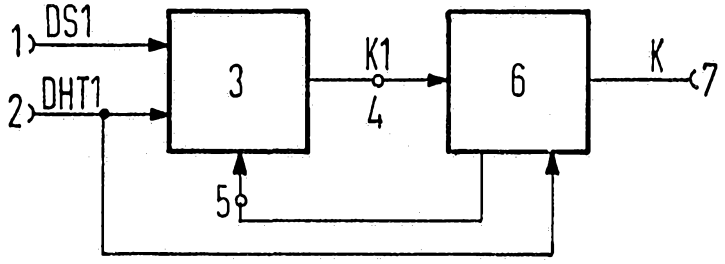


FIG 2

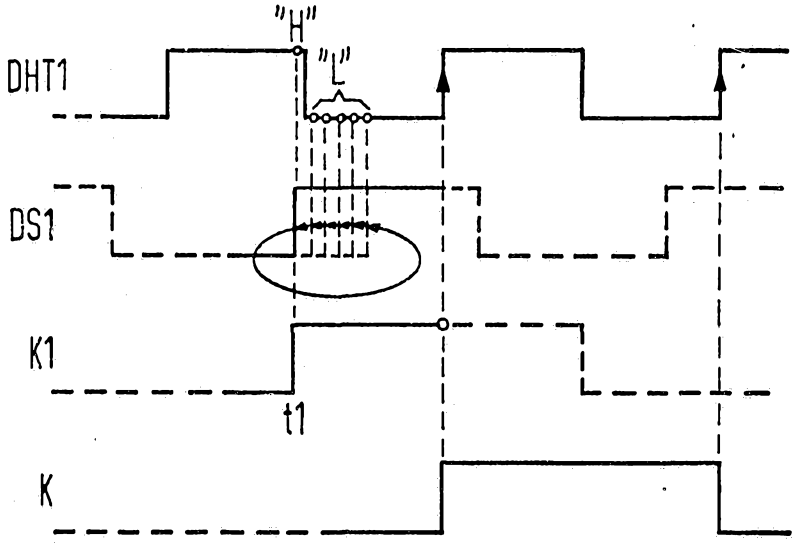


FIG 3

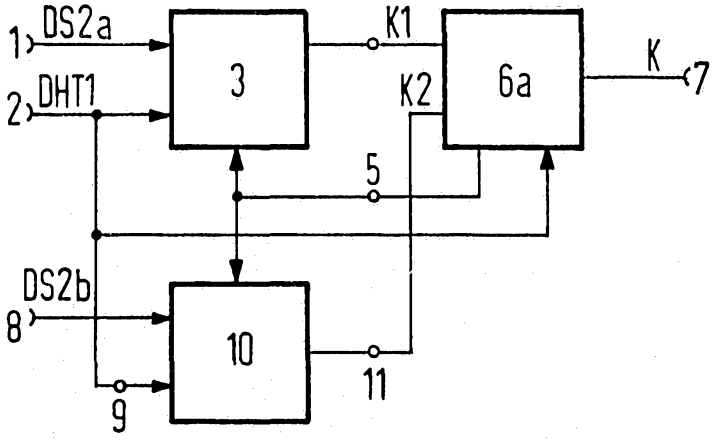
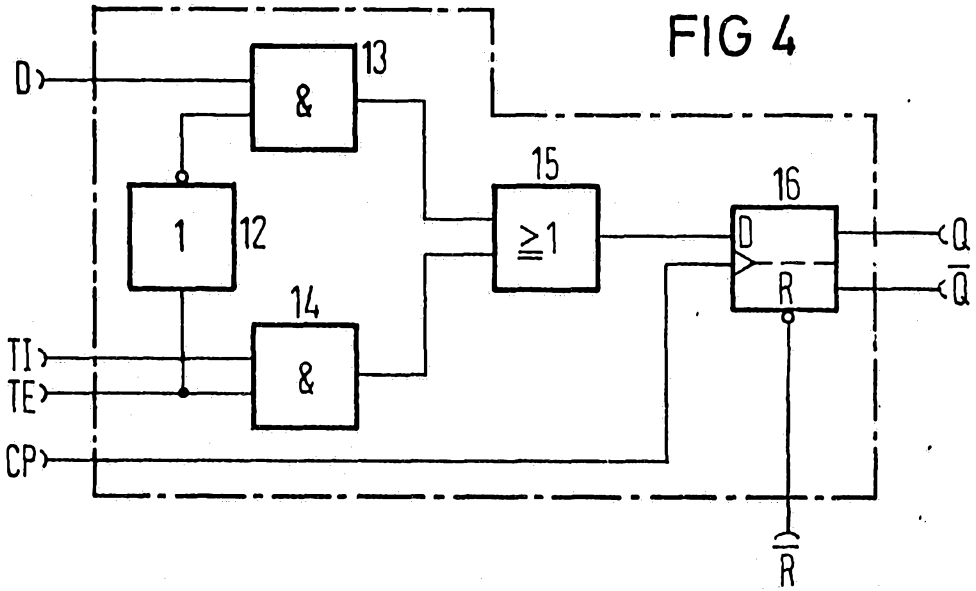


FIG 4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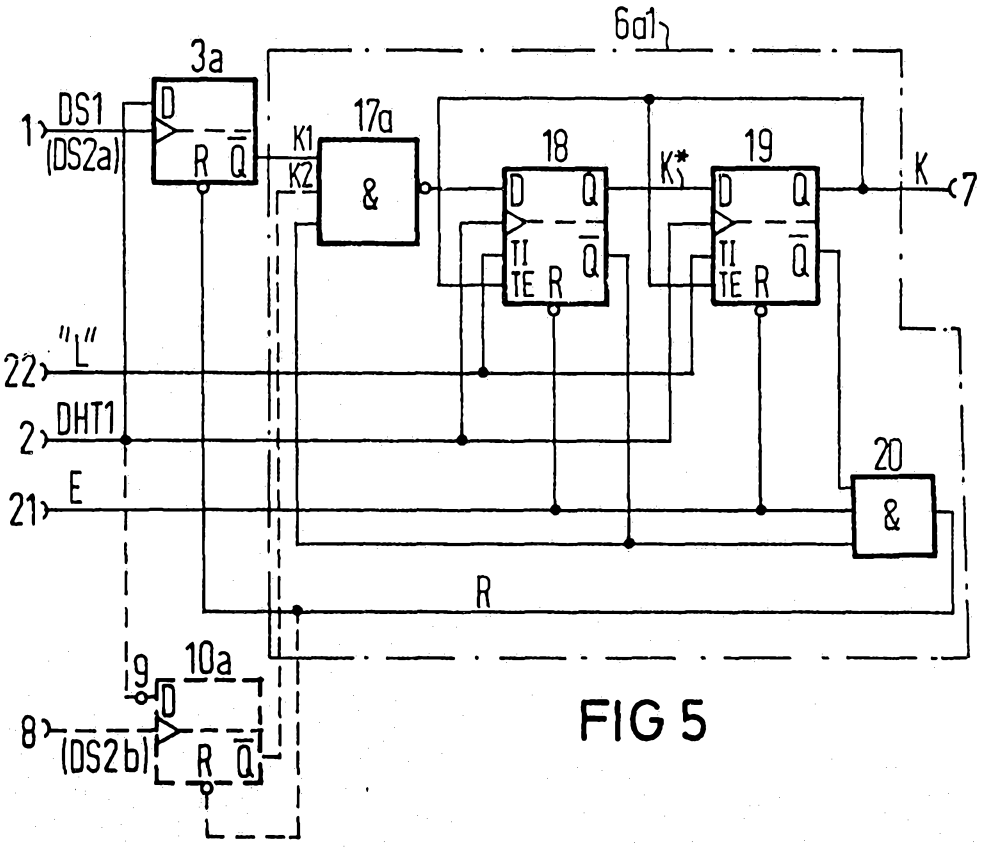
6a1
3a
1
DS1
(DS2a)
D
R
Q̄
K1
K2
17a
&
18
D
Q
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R
Q̄
K*
19
D
Q
TI
TE
R
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K
7
"L"
22
DHT1
2
E
21
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&
R
9
10a
8
(DS2b)
D
R
Q̄

FIG 5

FIG 6

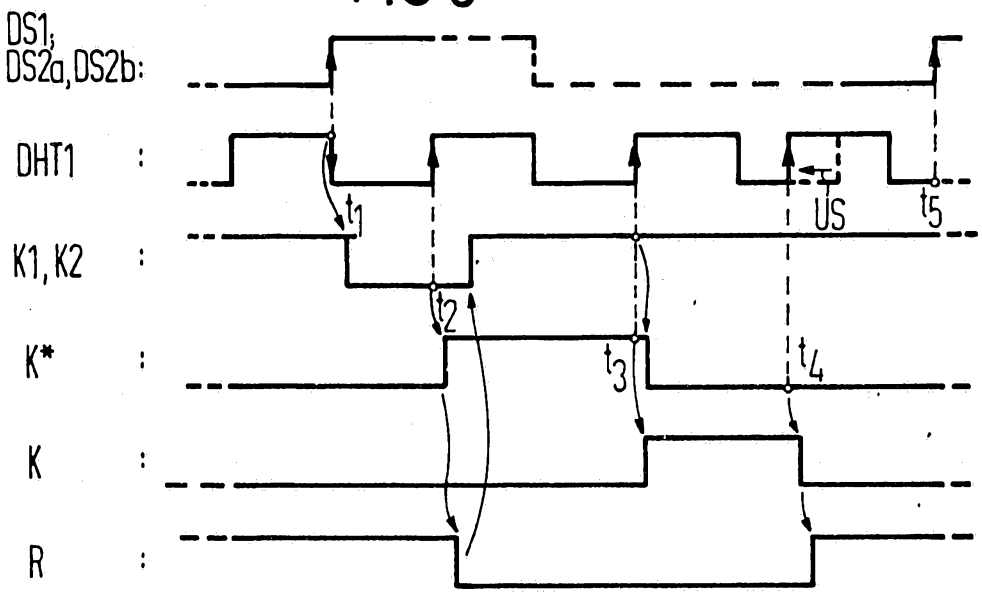
DS1;
DS2a, DS2b:
DHT1 :
K1, K2 :
K* :
K :
R :
t1
t2
t3
t4
t5
US

FIG 7

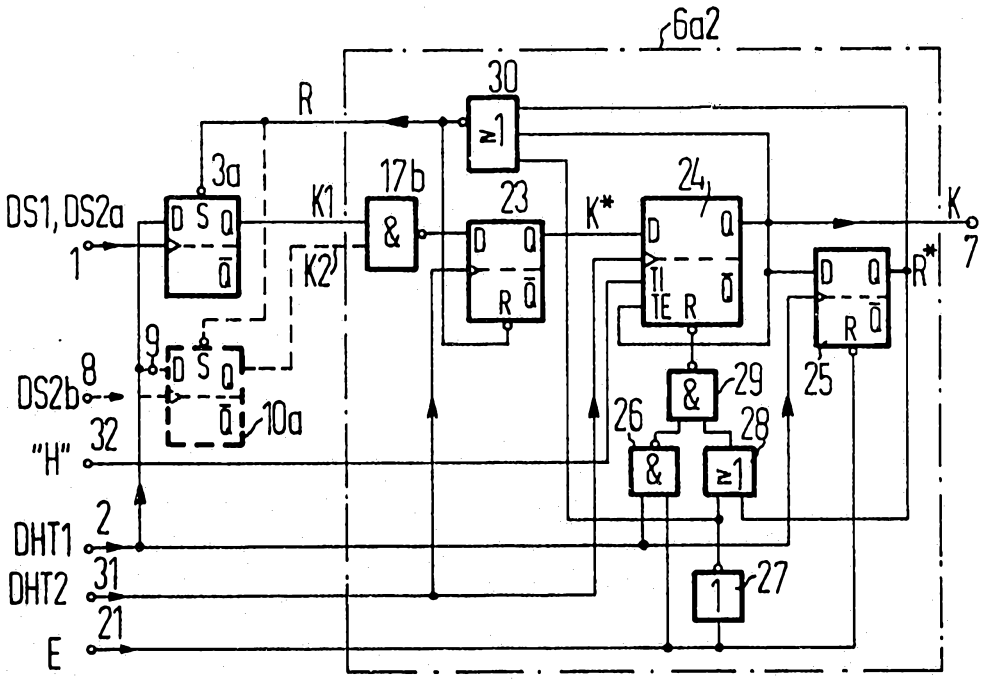
6a2
R
30
≥1
3a
17b
23
24
K1
K*
K
DS1, DS2a
1
K2
7
R*
9
DS2b
8
10a
"H"
32
25
29
26
28
2
DHT1
31
DHT2
21
E
27

FIG 8