

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
25 October 2007 (25.10.2007)

PCT

(10) International Publication Number
WO 2007/120928 A2

(51) International Patent Classification: Not classified

(21) International Application Number:
PCT/US2007/009584

(22) International Filing Date: 18 April 2007 (18.04.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/793,288 18 April 2006 (18.04.2006) US
60/793,276 18 April 2006 (18.04.2006) US
60/793,277 18 April 2006 (18.04.2006) US
60/793,275 18 April 2006 (18.04.2006) US
11/736,561 17 April 2007 (17.04.2007) US

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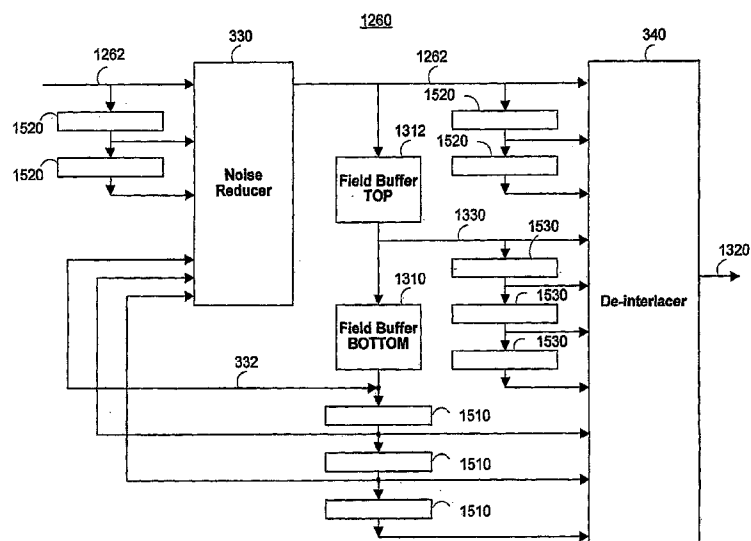
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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO,

[Continued on next page]

(54) Title: SHARED MEMORY MULTI VIDEO CHANNEL DISPLAY APPARATUS AND METHODS



(57) Abstract: A shared memory video processor including signal processing circuitry. The signal processing circuitry may enable a noise reducer and a de-interlacer to share access to field buffers in a memory device to store various field lines. Some of the stored field lines may also be shared within the signal processing circuitry. The sharing of some stored field lines reduces overall memory bandwidth and capacity requirements. The signal processing circuitry may be capable of performing multiple field line processing. A set of field line buffers may be provided to store field lines for multiple field segments and may provide the data to the corresponding inputs of the signal processing circuitry. To further reduce storage, some of the field line buffers may also be shared among the signal processing circuitry.

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RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM,
TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM,
GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL,

Published:

— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

SHARED MEMORY MULTI VIDEO CHANNEL DISPLAY APPARATUS AND
METHODS

Cross Reference to Related Application

[0001] This application claims the benefit of U.S.
5 Provisional Applications Nos. 60/793,288, filed April 18,
2006, 60/793,276, filed April 18, 2006, 60/793,277, filed
April 18, 2006, and 60/793,275, filed April 18, 2006 each
disclosure of which is hereby incorporated by reference
herein in its entirety.

10 Background of the Invention

[0002] Traditionally, multi video channel television
display screens are equipped with dual channel video
processing chips which enable a user to view one or more
channels simultaneously on various portions of the
15 display screen. This form of displaying a picture within
a picture is commonly referred to as picture-in-picture
or PIP. FIG. 1A is an example of displaying two channels
on various portions of the display screen having an
aspect ratio of 4:3. A screen 100A displays a first
20 channel 112 on the majority portion of the screen

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simultaneously with a second channel 122 that is displayed on a substantially smaller portion of the screen. FIG. 1B is an example of a display having a first channel and a second channel with substantially the same aspect ratio on different portions of the screen and will be described in more detail below.

[0003] A typical television system for generating PIP display 100A is shown in FIG. 2. Television display system 200 includes, television broadcast signals 202, a hybrid TV tuner 210, baseband inputs 280, a demodulator 220, an MPEG Codec 230, an off-chip storage 240, an off-chip memory 300, video processor 250, and an external component 270 (e.g., a display). Hybrid TV tuner 210 can tune to one or more television channels provided by television broadcast signals 202. Hybrid TV tuner 210 may provide digital television signals to demodulator 220 and analog video signal components (e.g., Composite Video Baseband Signals (CVBS)) to video processor 250.

Additionally, baseband inputs 280 may receive various television signals (e.g., CVBS, S-Video, Component, etc.) and provide them to video processor 250. Other external digital or analog signals (e.g., DVI or High Definition (HD)) may also be provided to video processor 250.

[0004] The video is demodulated by demodulator 220 and is then decompressed by MPEG Codec 230. Some operations required by MPEG Codec 230 may use off-chip storage 240 to store data. The digital signal(s) are then processed by video processor 250, which can be a dual channel processing chip, in order to generate the proper signals 260 for display on external component 270. Video

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processor 250 may use off-chip memory 300 to perform memory intensive video processing operations such as noise reducing and de-interlacing; 3D YC separation and frame rate conversion (FRC).

5 **[0005]** In these PIP applications, it is generally perceived that first channel 112 is more important than second channel 122. Typical dual channel processing chips that are used to generate PIP place more quality emphasis on the first channel video pipe, which generates
10 the large display of first channel 112. The second channel video pipe, which generates the smaller display of second channel 122 is of lesser quality in order to reduce costs. For example, 3-D video processing operations, such as de-interlacing, noise reduction, and
15 video decoding, may be implemented on the first channel video pipe while implementing only 2-D video processing operations on the second channel video pipe. 3-D video processing operations refer to operations that process video in the spatial and temporal domains, often
20 buffering one or more frames of video used in the processing operations. In contrast, 2-D video processing operations only process video in the spatial domains, operating only on the current frame of video.

[0006] With the advent of wide display screens having
25 an aspect ratio of 16:9, displaying two channels having the same size or an aspect ratio of 4:3 on the same screen has become increasingly higher in demand. This form of application is commonly referred to as picture-and-picture (PAP). In FIG. 1B screen 100B displays a
30 first channel 110 and a second channel 120 having

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substantially the same aspect ratio is displayed on a second portion of the screen. In these applications the first channel should be generated with similar quality as the second channel.

5 **[0007]** An implementation of 3-D video processing on both the first and second video channel pipes is therefore needed to produce two high-quality video images. Performing 3-D video processing to produce the desired display generally requires memory intensive
10 operations that have to be performed within a time frame suitable to display the images without loss in quality or integrity. The memory operations increase proportionally with the number of channels that require 3-D video processing. Typical dual video processing chips lack
15 ability to process two video signals with high-quality and are therefore becoming obsolete with the increase in demand to display two channels having high video quality.
[0008] One reason that typical dual video processing chips lack in the ability to process multiple high-
20 quality video signals, is the large amount of data bandwidth required between the video processor and the off-chip memory. Traditionally, a portion of the video processing chip pipeline includes a noise reducer and de-interlacer each requiring high data bandwidth with the
25 off-chip memory.

[0009] In particular, the noise reducer works primarily by comparing one field to the next field and removing portions of the field that are not the same in each field. For this reason, the noise reducer requires
30 storage of at least two fields for comparison with a

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current field. The de-interlacer reads the two fields that were stored and combines them, thereby reversing the operations of the interlacer.

[0010] FIG. 3 illustrates the off-chip memory access operations of the noise reducer and de-interlacer of a typical video processor. A portion of the video processing pipeline includes a noise reducer 330, a de-interlacer 340, and off-chip memory 300, which contains at least four field buffer sections 310, 311, 312, and 313.

[0011] During a first field interval, noise reducer 330 reads a field buffer section 310 compares it to a video signal 320, produces a new field with reduced noise and writes this field output 322 to two field buffer sections 311 and 312. The contents that were previously stored in field buffer sections 311 and 312 are copied over to field buffer sections 310 and 313, respectively. Thus, at the end of the field interval, field output 322 of noise reducer 330 is stored in field buffer sections 311 and 312 and the fields previously stored in field buffer sections 311 and 312 are now in field buffer sections 310 and 313, respectively.

[0012] During the following field interval, field buffer section 312 containing the field output from noise reducer 330 from the previous field interval is read by de-interlacer 340, field buffer section 313 containing the field output from noise reducer 330 from the field interval previous to this field interval that was stored in field buffer section 312 is read by de-interlacer 340. Field output 322 of noise reducer 330 of the current

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field interval is also read by de-interlacer 340. De-interlacer 340 processes these field segments and combines them to provide a de-interlaced output 342 to the next module in the video pipeline.

5 **[0013]** The exemplary aforementioned video pipeline portions perform these operations for a single channel and its operations would be multiplied for each additional channel. Therefore, since memory access bandwidth increases proportionally with the amount of
10 data that has to be written/read in the same interval, performing noise reduction and de-interlacing on multiple channels would increase the data bandwidth in the same manner. The incredible bandwidth demand of the above video processing operations limit the ability to perform
15 these operations simultaneously.

[0014] Therefore, it would be desirable to have systems and methods for reducing memory access bandwidth in various sections of one or more video pipeline stages of one or more channels in order to produce a display
20 having multiple high-quality video channel streams.

Summary of the Invention

[0015] In accordance with the principles of the present invention systems and methods are provided for reducing memory access bandwidth in various sections of
25 one or more video pipeline stages of one or more channels in order to produce a display having multiple high quality video channel streams.

[0016] Systems and methods are provided for sharing memory in a video processing system. Previously stored
30 contents of a first field buffer may be moved to a second

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field buffer. A first noise reduced live field may be stored in the first field buffer. Previously stored contents of the second field buffer may be provided to a noise reducer and a de-interlacer. The previously stored
5 contents of the first field buffer may be provided to the de-interlacer.

[0017] In accordance with the principles of the present invention, methods and apparatus are provided for reducing memory access bandwidth in various sections of
10 one or more video pipeline stages of one or more channels in order to produce a display having multiple high-quality video channel streams. A dual video processor may receive one or more analog or digital signals which may be in different formats. A dual video decoder (e.g.,
15 NTSC/PAL/SECAM video decoder) capable of decoding two simultaneous video signals in one or more video modes may be provided. In one of the video modes, the dual video decoder may perform time multiplexing to share at least one component such as an analog to digital converter,
20 used in decoding the video signals.

[0018] The outputs of the video decoder, or another set of video signals provided by another component in the system, may be provided to signal processing circuitry (e.g., a noise reducer and/or a de-interlacer). The
25 signal processing circuitry may access a memory device to store various field lines. Some of the stored field lines, that may be needed by the signal processing circuitry, may be shared. The sharing of some stored field lines reduces overall memory bandwidth and capacity
30 requirements. The signal processing circuitry may be

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capable of performing multiple field line processing. A set of field line buffers may be provided to store field lines for multiple field segments and may provide the data to the corresponding inputs of the signal processing circuitry. To further reduce storage, some of the field line buffers may also be shared among the signal processing circuitry.

[0019] The outputs of the video decoder, or another set of video signals provided by another component in the system, may be provided to one or more scalers for producing differently scaled video signals. The scaler may be configured to be placed in various slots before the memory, after the memory, or if no memory access is desired either before or after (i.e., between the memory). If a video signal is to be up-scaled, the scaler may be placed after the memory in order to reduce the amount of data that is stored to the memory. If a video signal is to be downscaled, the scaler may be placed before the memory in order to reduce the amount of data that is stored to the memory. Alternatively, one scaler may be configured to be placed before the memory while another scaler may be configured to be placed after the memory thereby providing two video signals that are scaled differently (i.e., one may be up-scaled while the other may be downscaled) while reducing the amount of memory storage and bandwidth.

[0020] The outputs of the video decoder, or another set of video signals provided by another component in the system, may be provided to one or more frame rate conversion units. A blank time optimizer (BTO) may

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receive data pertaining to a field line of a frame of a video signal at a first clock rate. The BTO may determine the maximum amount of time available before the next field line of the frame is received. Based on this determination the BTO may send or receive the field line of the frame to memory at a second clock rate. The second clock rate used for the memory access may be substantially slower than the first, thereby reducing memory bandwidth and enabling another video signal that may have a shorter amount of available time between field lines to access memory faster. In turn, the BTO essentially distributes memory access from several memory clients (i.e., units requiring memory access) in a way that promotes efficient use of the memory bandwidth.

[0021] The video signal outputs of the BTO or another set of video signals provided by another component in the system, may be provided to an overlay engine for further processing. In the overlay engine, two or more video signals may be overlaid and provided to a color management unit (CMU). The CMU may receive the overlaid video signal and may process the overlaid video signal in portions. Upon receiving an indication that a portion of the overlaid video signal corresponds to a first video signal, the CMU may process the video signal portion using parameters that correspond to the first video signal portion and provide an output. Alternatively, upon receiving an indication that a portion of the overlaid video signal corresponds to a second video signal, the CMU may process the video signal portion using parameters that correspond to the second video

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signal portion and provide an output. A multi-plane (M-plane) overlay circuit in the overlay engine may receive two or more video signals, where one of these signals may be provided by the CMU, and provide an overlaid signal.

5 The video signals may include a priority designator, and the overlay circuitry may then overlay the signals based on the priority designator.

[0022] The output of the overlay engine or another set of video signals provided by another component in the system which may be progressive, may be provided to a primary and/or auxiliary output stage. Alternatively, video signals may bypass the overlay engine and be provided to a primary and/or auxiliary output stage. In the primary and/or auxiliary output stages the video signals may undergo format conversion or processing to meet the requirements of a primary and/or auxiliary device such as, for example a display device and a recording device.

Brief Description of the Drawings

20 [0023] The above and other objects and advantages of the invention will be apparent upon consideration of the following detailed description, taken in conjunction with the accompanying drawings, in which like reference characters refer to like parts throughout, and in which:

25 [0024] FIGS. 1A and 1B is exemplary illustration of two channels being displayed on various portions of the same screen;

[0025] FIG. 2 is an illustration of generating PIP display;

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[0026] FIG. 3 is an illustration of off-chip memory access operations of a noise reducer and a de-interlacer in a typical video processor;

[0027] FIG. 4 is an illustration of a television display system in accordance with principles of the present invention;

[0028] FIG. 5 is a detailed illustration of the functions of an onboard video processing section of a dual video processor in accordance with principles of the present invention;

[0029] FIG. 6 is an illustration of a clock generation system in accordance with principles of the present invention;

[0030] FIGS. 7-9 are illustrations of three modes of generating video signals in accordance with principles of the present invention;

[0031] FIG. 10 is an illustration of an exemplary implementation of using two decoders to generate three video signals in accordance with principles of the present invention;

[0032] FIG. 11 is an exemplary timing diagram for time division multiplexing two portions of two video signals in accordance with principles of the present invention;

[0033] FIG. 12 is a detailed illustration of the functions of the front end video pipeline of the dual video processor in accordance with principles of the present invention;

[0034] FIG. 13 is an illustration of off-chip memory access operations of a noise reducer and a de-interlacer in accordance with principles of the present invention;

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[0035] FIG. 14 is an exemplary illustrative timing diagram of the off-chip memory access operations of a noise reducer and a de-interlacer in accordance with principles of the present invention;

5 [0036] FIG. 15 is an illustration of multiple field line processing in accordance with principles of the present invention;

[0037] FIG. 16 is a detailed illustration of performing frame rate conversion and scaling in accordance with principles of the present invention;

10 [0038] FIG. 17 is an illustration of a scaler positioning module in accordance with principles of the present invention;

[0039] FIG. 18 is an illustrative example of the operation of a BTO multiplexor in accordance with principles of the present invention;

[0040] FIG. 19 is a detailed illustration of the color processing and channel blending (CPCB) video pipeline of the dual video processor in accordance with principles of the present invention;

20 [0041] FIG. 20 is a detailed illustration of the overlay engine in accordance with principles of the present invention;

[0042] FIG. 21 is a detailed illustration of the color management unit in accordance with principles of the present invention; and

25 [0043] FIG. 22 is a detailed illustration of the back end video pipeline of the dual video processor in accordance with principles of the present invention.

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Detailed Description of the Invention

[0044] The invention relates to methods and apparatus for reducing memory access bandwidth and sharing memory and other processing resources in various sections of multiple video pipeline stages of one or more channels in order to produce one or more high-quality output signals.

[0045] FIG. 4 illustrates a television display system in accordance with the principles of the present invention. The television display system depicted in FIG. 4 may include, television broadcast signals 202, a dual tuner 410, MPEG Codec 230, off-chip storage 240, off-chip memory 300, a dual video processor 400, a memory interface 530 and at least one external component 270.

Dual tuner 410 may receive television broadcast signals 202 and produce a first video signal 412 and a second video signal 414. Video signals 412 and 414 may then be provided to a dual decoder 420. Dual decoder 420 is shown to be internal to dual video processor 400, but may alternatively be external to video processor 400.

Dual decoder 420 may perform similar functions as decoder 220 (FIG. 2) on first and second video signals 412 and 414. Dual decoder 420 may include at least a multiplexor 424 and two decoders 422. In alternative arrangements, multiplexor 424 and one or two of decoders 422 may be external to dual decoder 420.

Decoders 422 provide decoded video signal outputs 426 and 428. It should be understood that decoders 422 may be any NTSC/PAL/SECAM decoders different from MPEG decoders. The inputs to decoders 422 may be digital CVBS, S-Video or Component video signals and the output

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of decoders 422 may be digital standard definition such as Y-Cb-Cr data signals. A more detailed discussion of the operation of dual decoder 420 is provided in connection with FIGS. 7, 8, 9, and 10.

5 [0046] Multiplexor 424 may be used to select at least one of two video signals 412 and 414 or any number of input video signals. The at least one selected video signal 425 is then provided to decoder 422. The at least one selected video signal 425 appears in the figure as a
10 single video signal to avoid overcrowding the drawing, however, it should be understood the video signal 425 may represent any number of video signals that may be provided to the inputs of any number of decoders 422. For example, multiplexor 424 may receive 5 input video
15 signals and may provide two of the 5 input video signals to two different decoders 422.

[0047] The particular video signal processing arrangement shown in FIG. 4 may enable the internal dual decoder 420 on dual video processor 400 to be used
20 thereby reducing the cost of using an external decoder which may be required in the time-shifting applications. For example, one of the outputs 426 and 428 of dual decoder 420 may be provided to a 656 encoder 440 to properly encode the video signal to standard format prior
25 to interlacing the video signals. 656 encoder 440 may be used to reduce the data size for processing at a faster clock frequency. For example, in some embodiments, 656 encoder 440 may reduce 16-bits of data, h-sync and v-sync signals to 8-bits for processing at double the frequency.
30 This may be the standard to interface between SD video

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and any NTSC/PAL/SECAM decoders and MPEG encoders. The encoded video signal 413 may then be provided to an external MPEG Codec 230, for example, via a port on the video processor, to generate a time shifted video signal.

5 Another port, flexiport 450 on dual video processor 400 may be used to receive the time shifted video signal from MPEG Codec 230. This may be desirable to reduce the complexity of the video processor by processing portions of digital video signals outside of the video processor.

10 Moreover, time-shifting performed by MPEG Codec 230 may require operations that include compression, decompression and interfacing with non-volatile mass storage devices all of which may be beyond the scope of the video processor.

15 **[0048]** Other video signals such as a cursor, an on-screen display, or various other forms of displays other than broadcast video signals 202 that may be used in at least one external component 270 or otherwise provided to an external component, may also be generated using dual
20 video processor 400. For example, dual video processor 400 may include a graphics port 460 or pattern generator 470 for this purpose.

[0049] The decoded video signals, as well as various other video signals, graphics generator 460, or pattern
25 generator 470, may be provided to selector 480.

Selector 480 selects at least one of these video signals and provides the selected signal to onboard video processing section 490. Video signals 482 and 484 are two illustrative signals that may be provided by selector
30 480 to onboard video processing section 490.

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[0050] Onboard video processing section 490 may perform any suitable video processing functions, such as de-interlacing, scaling, frame rate conversion, and channel blending and color management. Any processing resource in dual video processor 400 may send data to and receive data from off-chip memory 300 (which may be SDRAM, RAMBUS, or any other type of volatile storage) via memory interface 530. Each of these function will be described in more detail in connection with the description of FIG. 5.

[0051] Finally, dual video processor 400 outputs one or more video output signals 492. Video output signals 492 may be provided to one or more external components 270 for display, storage, further processing, or any other suitable use. For example, one video output signal 492 may be a primary output signal that supports high-definition TV (HDTV) resolutions, while a second video output signal 492 may be auxiliary output that supports standard definition TV (SDTV) resolutions. The primary output signal may be used to drive a high-end external component 270, such as a digital TV or a projector at the same time as the auxiliary output is used for a standard definition (DVD) video recorder, a standard-definition TV (SDTV), a standard-definition preview display, or any other suitable video application. In this way, the auxiliary output signal may enable a user to record an HDTV program on any suitable SDTV medium (e.g., a DVD) while allowing the user to simultaneously view the program on an HDTV display.

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[0052] FIG. 5 illustrates the functions of onboard video processing section 490 of dual video processor 400 in greater detail. Onboard video processing section 490 may include an input signal configuration 510, a memory
5 interface 530, a configuration interface 520, a front end pipeline section 540, a frame rate conversion (FRC) and scaling pipeline section 550, a color processing and channel blending pipeline section 560, and a backend pipeline section 570.

10 [0053] Configuration interface 520 may receive control information 522 from an external component such as a processor via, for example an I2C interface.

Configuration interface 522 may be used to configure input signal configuration 510, front end 540, frame rate
15 conversion 550, color processor 560, backend 570, and memory interface 530. Input signal configuration 510 may be coupled to external inputs on dual video processor 400 in order to receive video signals on input 502 (such as HDTV signals, SDTV signals, or any other suitable digital
20 video signals) and selected video signals 482 and 484 (FIG. 4). Input signal configuration 510 may then be configured to provide at least one of the received video signals (e.g., signals 482, 484 and 502) as video source streams 512 to front end 540.

25 [0054] Based on this configuration, various ones of these inputs provided to onboard video processing section 490 may be processed at different times using the onboard video processing pipeline. For example, in one embodiment dual video processor 400 may include eight
30 input ports. Exemplary ports may include two 16-bit HDTV

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signal ports, one 20-bit HDTV signal port, three 8-bit SDTV video signal ports which may be in CCIR656 format, one 24-bit graphics port and one 16-bit external on-screen display port.

5 **[0055]** Front end 540 may be configured to select between at least one video signal streams 512 (i.e., channels) of the available inputs and process the selected video signal stream(s) along one or more video processing pipeline stages. Front end 540 may provide
10 processed video signal stream(s) from one or more pipeline stages to frame rate conversion and scaling pipeline stage 550. In some embodiments, front end 540 may include three video processing pipeline stages and provide three separate outputs to FRC and scaling
15 pipeline stage 550. In FRC and scaling pipeline stage 550 there may be one or more processing channels. For example, a first channel may include a main scaler and frame rate conversion unit, a second channel may include another scaler and frame rate conversion unit,
20 and a third channel may include a lower cost scaler. The scalars may be independent of each other. For example, one scalar may upsize the input image while another may downsize the image. Both scalars may be capable of working with 444 pixels (RGB/YUB 24-bits) or 422 pixels
25 (YC 16-bits).

[0056] Color processing and channel blending pipeline stage 560 may be configured to provide color management functions. These functions may include color re-mapping, brightness, contrast, hue & saturation enhancement, gamma
30 correction and pixel validation. Additionally, color

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processing and channel blending pipeline stage 560 may provide video blending functions, overlaying different channels, or blend or overlay two blended video channels with a third channel.

5 **[0057]** Back end pipeline stage 570 may be configured to perform data formatting, signed/unsigned number conversion, saturation logic, clock delay, or any other suitable final signal operations that may be needed prior to the output of one or more channels from dual video
10 processor 400.

[0058] Each of the various pipeline stage segments may be configured to send data to and receive data from off-chip memory 300 using memory interface 530. Memory interface 530 may include at least a memory controller
15 and a memory interface. The memory controller may be configured to run at a maximum speed supported by the memory. In one embodiment, the data bus might be 32-bits and may operate at a frequency of 200 MHz. This bus may provide a throughput substantially close to 12.8 gigabits
20 per second. Each functional block that uses memory interface 530 (i.e., memory client) may address the memory in a burst mode of operation. Arbitration between various memory clients may be done in a round robin fashion or any other suitable arbitration scheme. A more
25 detailed discussion of the various pipeline segments is provided in connection with the description of FIGS. 12, 19, 20, 21 and 22.

[0059] Various components and pipeline stages in dual video processor 400 may require a different clocking
30 mechanisms or clock frequencies. FIG. 6 illustrates a

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clock generation system 600 that generates a variety of clock signals for this purpose. Clock generation system 600 includes at least a crystal oscillator 610, generic analog phase-locked loop circuitry 620, digital phase
5 locked loop circuitries 640a-n and memory analog phase-locked loop circuitry 630. The output 612 of crystal oscillator 610 may be coupled to generic phase locked loop 620, memory phase-locked loop 630, another component in dual video processor 400, or any suitable component
10 external to the processor as needed.

[0060] Memory analog phase-locked loop circuitry 630 may be used to generate a memory clock signal 632 and additionally other clock signals of different frequencies 636 which may be selected by selector 650 for
15 use as a clock signal 652 to operate a memory device (e.g., 200 MHz DDR memory) or another system component.

[0061] Generic analog phase-locked loop 620 may generate a 200 MHz clock that may be used as a base clock for one or more digital phase-locked loop (PLL)
20 circuitries 640a-n. Digital PLL circuitry 640a-n may be used in open loop mode, where it behaves as a frequency synthesizer (i.e., multiplying the base clock frequency by a rational number). Alternatively, digital PLL circuitry 640a-n may be used in closed loop mode, where
25 it may achieve frequency lock by locking onto a respective input clock signal 642a-n (e.g., a video sync input). The digital PLL has the ability, in closed loop mode, to achieve accurate frequency lock to very slow clock signals. For example, in the realm of video
30 processing the vertical video clock signal (e.g., v-sync)

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may be in the range of 50 to 60 Hz. Various system components may use outputs 644a-n of digital PLL circuitry 640a-n for different operations that may require a variety of open loop or closed loop signals.

5 Each of outputs 640a-n should be understood to be capable of providing clock signals of different frequencies or the same frequencies.

[0062] For example, one component that may use clock signals generated by digital PLL circuitry 640a-n is dual decoder 420 (FIG. 4), the operation of which is described in more detail in connection with FIGS. 7, 8, 9, and 10. Dual decoder 420 may include the decoders 422 (FIG. 4). Decoders 422 may be used in various modes of operation as described in connection with FIGS. 7, 8, and 9.

15 **[0063]** FIGS. 7, 8, and 9 illustrate three exemplary modes of operation using decoders 422 to generate video signals 426 and 428. These three modes of operation may provide for example, composite video signals, s-video signals, and component video signals.

20 **[0064]** A first of these three modes, which may be used to generate composite video signals, is shown in connection with FIG. 7. The first decoder mode may include a DC restore unit 720, an analog to digital converter 730, and decoder 422 each of which may be included in dual decoder 420 (FIG. 4). Video signal 425 (FIG. 4), which may be provided by dual tuner 410 or in an alternative arrangement by multiplexor 424, is provided to DC restore unit 720. DC restore unit 720 may be used when video signal 425, which may be an AC coupled
25 signal, has lost its DC reference and should have it
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periodically reset in order to retain video characteristic information such as brightness. The video signal from DC restore unit 720 is digitized by analog to digital converter 730 and provided to decoder 422.

5 **[0065]** In the first mode, decoder 422 may use the digitized video signal 732 from a single analog to digital converter to generate a composite video signal. Analog to digital converter 730 and decoder 422 may operate by receiving digital clock signals 644a-n
10 (FIG. 6) -- which may be, for example, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, or 30 MHz. Additionally, decoder 422 may control the operation of DC restore unit 720 using an output feedback signal 427. Output feedback signal 427 may be, for example, a 2-bit control signal
15 that instructs DC restore unit 720 to increase or decrease the DC output on the video signal provided to analog to digital converter 730.

20 **[0066]** A second of the three modes, which may be used to generate s-video signals, is shown connection with FIG. 8. The second decoder mode may include all of the elements described in the first mode in addition to a second analog to digital converter 820. Video signal 425 (FIG. 4) may be split into a first portion 812 and a second portion 810. First portion 812 of the signals of
25 video signal 425 (FIG. 4), which may be provided by multiplexor 424, may be provided to DC restore unit 720 and a second portion 810 of the signals of video signal 425 (FIG. 4) may be inputted to second digital to analog converter 820. First portion 812 of video
30 signal 425 from DC restore unit 720 is digitized by

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second analog to digital converter 730 and provided to decoder 422. Additionally, second portion 810 of video signal 425 is also provided to decoder 422 by analog to digital converter 820. S-Video signals require a two
5 wire analog port for connecting to various devices (e.g., VCR, DVD player, etc.).

[0067] In this second mode, decoder 422 may use the digitized video signals 732 and 832 from two analog to digital converters 730 and 820 to generate an s-video
10 signal. Analog to digital converters 730 and 820 and decoder 422 may operate by receiving digital clock signals 644a-n (FIG. 6) -- which may be, for example, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, or 30 MHz. In some embodiments, first portion 812 of the video signal may be
15 the Y-channel of video signal 425 and the second portion 810 of video signal 425 may be the chroma channel of the video signal.

[0068] A third of the three modes, which may be used to generate component video signals, is shown in
20 connection with FIG. 9. The third decoder mode may include all the elements described in the second mode in addition to a second and third DC restore unit, 930 and 920, and a multiplexor 940. Video signal 425 may be split into a first portion 914, a second portion 910, and
25 a third portion 912. First portion 914 of the video signal 425 (FIG. 4) , which may be provided by multiplexor 424, may be provided to DC restore unit 720, second portion 910 of the signals of video signal 425 (FIG. 4) may be provided to DC restore unit 930, and
30 third portion 912 of the signals of video signal 425

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(FIG. 4) may be provided to DC restore unit 920. Component video signals require a three wire analog port for connecting to various devices (e.g., VCR, DVD player, etc.).

5 **[0069]** First portion 914 of video signal 425 from DC restore unit 720 is digitized by analog to digital converter 730 and provided to decoder 422. Second and third portions 910 and 912 of video signals 425 from DC restore units 930 and 920 are selectively digitized
10 (e.g., by being selected using multiplexor 940) by analog to digital converter 820 and provided to decoder 422. Multiplexor 940 may receive control signals 429 from decoder 422 in order to time multiplex second and third portions 910 and 912 of video signal 425 through analog
15 to digital converter 820.

[0070] In the third mode, in some embodiments, decoder 422 may use the digitized video signals 732 and 832 from the two analog to digital converters 730, 820 to generate a component video signal. Analog to digital
20 converters 730 and 820 and decoder 422 may operate by receiving digital clock signals 644a-n (FIG. 6) -- which may be, for example, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, or 30 MHz. Additionally, decoder 422 may control the operation of DC restore units 720, 930, and 920 using an
25 output feedback signal 427. In some embodiments, first, second and third portions 914, 910 and 912 of video signal 425 may be the Y-channel, U-channel and V-channel, respectively, of video signal 425.

[0071] It should be understood that various commonly
30 available types of DC restore units, digital to analog

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converters and video decoders may be used to perform the aforementioned functions and for the sake of brevity, their particular operations are being omitted from this discussion.

5 **[0072]** In one embodiment shown in FIG. 10, all three decoder modes may be implemented using two of decoders 422 and three of analog to digital converters 730 or 820. The arrangement described in FIG. 10 may enable dual decoder 420 (FIG. 4) to provide at least two
10 video signals 426 and 428 (i.e., one video signal from each decoder) substantially simultaneously that may correspond to any two of the three modes.

15 **[0073]** FIG. 10 illustrates an exemplary implementation of using two decoders to generate either two composite video signals, one composite and one s-video signals, one composite and one component video signals, or two s-video signals. The exemplary implementation shown in FIG. 10 includes, a set of multiplexors 1020, 1022, 1023, 1025, 1021, 1024, 1026, 1027, and 1028; three analog to digital
20 converters 730, 820, 1010; four DC restore units 720, 721, 930, 920; a demultiplexor 1040; and two decoders 422a and 422b.

25 **[0074]** The exemplary implementation of FIG. 10, when used to generate two composite video signals, may operate in the following manner. A first video signal 425a may be coupled to the first input of multiplexor 1020 and a second video signal 914 may be coupled to the second
input of multiplexor 1024. The first input of multiplexor 1020 may be selected and output to the fourth
30 input of multiplexor 1021 to be input to DC restore

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unit 720. The second input of multiplexor 1024 may be selected and output to DC restore unit 721. The operations of the remaining portions of the implementation are similar to that which was described in connection with FIG. 7 in which a composite video signal is generated. For example, DC restore units 720 and 721, analog to digital converters 730 and 1010, and decoders 422a and 422b operate in a similar manner to generate the composite video signals as described in FIG. 7.

[0075] The generation of one composite and one s-video signals or one composite and one component video signals using the exemplary implementation shown in FIG. 10 is performed in a similar manner as the generation of two composite video signals described above. For example, first and second video signal portions 812 and 810 of video signal 425 used for generating s-video signals are provided to multiplexors 1022 and 1026. The outputs of multiplexors 1022 and 1026 are provided to multiplexors 1021 and 1027 which select the video signals that are to be processed by analog to digital converters 730 and 820. Similarly, multiplexor 1024 selects which video signals are to be processed by analog to digital converter 1010. A more detailed description of the multiplexor input selections for the various modes of operation are depicted in Table 1 shown below.

[0076] The exemplary implementation shown in FIG. 10 also enables the generation of two s-video signals 426 and 428. To provide this functionality, a first clock signal 644a operating at a first frequency and a first

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phase (e.g., 20 MHz) is provided to analog to digital converter 730 and to decoder 422a. A second clock signal 644b operating at a second frequency that may be 180 degrees out of phase from the first clock signal (e.g., 20 MHz at 180 degree out of phase) may be provided to analog to digital converter 1010 and to decoder 422b. A third clock signal 644c at a third frequency that is substantially double the frequency of the first clock signal and having the same phase as the first clock signal (e.g., 40 MHz) may be provided to analog to digital converter 820. Clock signal 644b is provided to multiplexor 1030 to selectively couple clock signal 644b to multiplexors 1026 and 1027. By coupling the clock signals to the select inputs of multiplexors 1026 and 1027 it is possible to perform time-division multiplexing on video signal inputs 810a-c on analog to digital converter 820. Clock signal 644a is coupled to demultiplexor 1040 to demultiplex the time divided video signal. A more clear description of the time-division multiplexing operations is provided in connection with FIG. 11.

[0077] FIG. 11 illustrates an exemplary timing diagram for time-division multiplexing two second portions 810 of two video signals 425. By time division multiplexing the operations, the need for a fourth analog to digital converter may be obviated thereby reducing the total cost of dual video processor 400. The timing diagram shown in FIG. 11 includes, three clock signals that correspond to the first, second and third clock signals 644a, 644b and 644c respectively, and outputs of three analog to digital

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converters 730, 1010, and 820. As shown in the diagram clock 1 and clock 2 operate at half of the frequency of clock 3 and change with the falling edge of clock 3.

[0078] As shown, between the time period of T1 and T4,

5 a full period of clock 644a (clock 1) completes and the output of analog to digital converter 730 (ADC 1) corresponding to the first portion 812a-c of a first video signal (S0) is available for processing by decoder 422a. On the rising edge of clock 3 at the
10 beginning of time period T2, analog to digital converter 820 (ADC 3) begins processing a second portion 810a-c of a second video signal (S1) and completes processing at the end of time period T3.

[0079] At the beginning of time period T3, analog to
15 digital converter 820 (ADC 2) begins processing a first portion 810a-c of video signal S1 and completes at the end of time period T6. The output of ADC 2 corresponding to the first portion 810a-c of video signal S1 becomes available for processing by decoder 422b at the end of
20 time period T6. On the rising edge of clock 3 at the beginning of time period T4, analog to digital converter 820 (ADC 3) begins processing a second portion 810a-c of video signal S0 and completes processing at the end of time period T5.

25 **[0080]** Thus, at the end of time period T6, two portions of two video signals S0 and S1 have completed processing using only three analog to digital converters.

[0081] On the rising edge of clock 3 between the time
30 periods T5 and T6, demultiplexor 1040 provides the output of second portion 810a-c of video signal S0 from ADC 3 to

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decoder 644a for producing processed video signal 426.

At the same time second portion 812 of video signal S1 is selected for processing by analog to digital

converter 820 (ADC 3) and becomes available at the end of time period T7.

[0082] The foregoing demonstrates one embodiment for producing two s-video signals 426 and 428 using three analog to digital converters 730, 1010, and 820. Table 1 below summarizes the various exemplary select signals that may be provided to the corresponding multiplexors for producing various combinations of composite (cst), component (cmp) and s-video signals (svid).

Video1	Video2	M0_sel	M1_sel	M2_sel	M3_sel	M4_sel	M5_sel	M6_sel	M7_sel
425a (cst)	425e (cst)	0,0	X,X	1,1	X,X	X,X	0,1	X,X	X,X
425a (cst)	910,912,914 (cmp)	0,0	X,X	1,1	X,X	X,X	1,0	X,X	1,429
425b (cst)	812a,810a (svid)	0,1	X,X	1,1	X,X	0,0	0,0	0,0	0,0
812a,810a (svid)	812b,810b (svid)	X,X	0,0	0,0	X,X	0,1	0,0	0,644b	0,0
812a,810a (svid)	812c,810c (svid)	X,X	0,0	0,0	X,X	1,0	0,0	644b,0	0,0
812b,810b (svid)	812c,810c (svid)	X,X	0,1	0,0	X,X	1,0	0,0	644b,1	0,0

Table 1

[0083] Dual decoder 420 may also be configured to handle unstable analog or digital signals which may be received from a video cassette recorder (VCR). Unstable signals may be produced by a VCR due to various modes of operation such as fast forwarding, fast rewinding or pausing modes. Dual decoder 420 may be able to process these types of signals to provide a good quality output signal during such situations.

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[0084] Unstable video signals may be caused by unstable sync signals generated by the VCR. One suitable technique for processing unstable sync signals may be to buffer the unstable video signal. For example a first-in-first-out (FIFO) buffer may be placed near the output of the decoder. First, the decoder output data may be written to the FIFO buffer using unstable sync signals as the reference. The sync signals and the clock may be re-generated or re-created from a logic block within the decoder and may then be used for reading the data from the FIFO buffer when such modes of operation are encountered. Thus, the unstable video signal may be output with a stable sync signal. In all other scenarios or modes of operation, the FIFO buffer may be bypassed and the output may be the same as the FIFO's input.

[0085] Alternatively, implementing FIFO buffers in the off-chip memory may enable the proper processing of unstable sync signals. For example, when an unstable sync signal is detected, the decoder may be placed in 2-D mode thereby using less off-chip memory. A substantial portion of off-chip memory 300, which is normally used for 3-D operations, becomes free and may be used for implementing the aforementioned FIFO buffer (i.e., the equivalent of at least one full data vector is available as free memory space). Moreover, the FIFO buffer inside the off-chip memory may be capable of storing the pixels for a full frame, so even if the write and read rates are not matched, at the output the frames either get repeated or get dropped. The repeating or dropping of a

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particular frame or of fields within a frame may still enable the system to display a reasonably good picture.

[0086] FIG. 12 illustrates in more detail the exemplary functionality of front end 540 within the video pipeline. In particular, channel selector 1212 may be configured to select four channels from multiple video source streams 512. The four channels may be processed along 4 pipelined stages within front end 540. In some embodiments, the four channels may include: a main video channel, a PIP channel, an on-screen display (OSD) channel, and a data instrumentation or testing channel.

[0087] Front end 540 may implement various video processing stages 1220a, 1220b, 1230, and 1240 on any of the channels. In some embodiments, the various channels may share one or more resources from any of the other stages to increase processing power of the various channels. Some examples of functions that may be provided by video processing stages 1220a and 1220b may include noise reduction and de-interlacing which may be used for producing maximum picture quality. The noise reduction and de-interlacing functions may also share off-chip memory 300 and, as such the memory is denoted as shared memory stages 1260 which will be described in more detail in connection with the description of FIGS. 13 and 15. To avoid overcrowding the drawing, shared memory stages 1260 are shown in FIG. 12 as being part of the processing stages corresponding to channel 1. However, it should be understood that one or more shared memory stages 1260 may be part of any of the channel pipelines in front end 540.

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[0088] Noise reduction may remove impulse noise, Gaussian noise (spatial and temporal), and MPEG artifacts such as block noise and mosquito noise. De-interlacing may include generating progressive video from interlaced video by interpolating any missing lines using edge-adaptive interpolation in the presence of motion. Alternatively, de-interlacing functions may use a combination of temporal and spatial interpolation adaptively based on motion. Both the noise reducer and de-interlacer may operate in the 3-D domain and may require storing fields of frames in off-chip memory. Hence, the de-interlacer and noise reducer may act as clients to memory interface 530 which may be used to access off-chip memory. In some embodiments, the noise reducer and de-interlacer may share the off-chip memory to maximize memory space and process data in the most efficient manner -- as shown by the shared memory stages 1260. This process will be described in more detail in connection with the description of FIGS. 13 and 15.

[0089] Any of the three video processing stages 1220a, 1220b, and 1230 may run format conversion to convert a video signal into the desired domain. For example, this type of conversion may be used to change an input video signal stream to YC 4:2:2 format in 601 or 709 color-space.

[0090] Front end 540 may also provide an instrumentation pipeline 1240 to run data instrumentation functions. Instrumentation pipeline 1240 may be used, for example, to find the start and end pixel and line

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positions of an active video or to find the preferred sampling clock phase when there is a controllable phase sampler (ADC) upstream. Performing these operations may help in auto-detecting input channel parameters such as resolution, letter-boxing, and pillar-boxing. Moreover, detecting such channel parameters may aid in using them to control features like scaling and aspect ratio conversion through a micro-controller or any other suitable processing element. Front end 540 may also run sync video signal instrumentation functions on all four channels in order to detect a loss of sync signal, a loss of clock signal, or an out-of-range sync or clock signal. These functions may also be used to drive power management control through a micro-controller or any other suitable processing element.

[0091] At the end of front end 540, a set of FIFO buffers 1250a-c may sample the video stream to provide sampled video signals 1252, 1254, and 1256, which may be used for retiming the selected channels, between front end 540 and frame rate conversion and scaling 550 (FIG. 5) pipeline stages.

[0092] A more detailed description of shared memory stages 1260 is provided in connection with the description of FIGS. 13 and 15. In particular, as illustrated in FIG. 13 the shared memory stages 1260 may include at least the functions of a noise reducer 330 and a de-interlacer 340. Both of these functions are temporal functions that may need frame storage in order to produce a high-quality image. By enabling various memory access blocks (i.e., memory clients) to share off-

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chip memory 300, the size of off-chip memory 300 and bandwidth required for interfacing with off-chip memory 300 may be reduced.

[0093] Noise reducer 330 may operate on two fields of the interlaced input in 3-D mode. The two fields that noise reducer 330 may operate on may include live field 1262 and a field that was two fields prior to live field 1262 (i.e., previous to the previous field 332 or twice delayed noise reduced field 332). De-interlacer 340 may operate on three interlaced fields in 3-D mode. The three fields may include a live field 1262, a previous field 1330 (e.g., once delayed field), and a previous to the previous field 332 (e.g., twice delayed field).

[0094] As shown in FIG. 13 and FIG. 14 the field buffers 1310 and 1312 may be shared by noise reducer 330 and de-interlacer 340. Noise reducer 330 may read from off-chip chip memory 300 a previous to the previous field 332 from field buffer 1310 and process it with live field 1262 to provide noise reduced output 322. Noise reduced output 322 may be written to off-chip memory 300 into field buffer 1312. De-interlacer 340 may read from off-chip chip memory 300 a previous field 1330 from field buffer 1312 and previous to the previous field 332 from field buffer 1310 and process the read fields with either live field 1262 or noise reduced output 322 and provide de-interlaced video 1320 as output.

[0095] For example as illustrated in FIG. 14, live field 1262 (FIELD 1) may be provided to noise reducer 330 for outputting noise processed output 322 during a first

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time period (i.e., T1). After or before noise reducer 330 completes processing FIELD 1 (i.e., during a time period T2), noise reduced output 322 (FIELD 1) may be provided by noise reducer 330 to de-interlacer 340 or alternatively, may bypass noise reducer 330 and be provided directly to de-interlacer 340 via 1262 (e.g., if no noise reduction is required). In either case, during the second time period (i.e., time period T2), noise reduced output 322 (FIELD 1) may be written to field buffer 1312 in off-chip memory 300 by noise reducer 330.

[0096] The output 1330 of field buffer 1312 (FIELD 1) may be read by de-interlacer 340 from off-chip memory 300 during the time period T2, while processing the next live field in the frame (FIELD 2). Field buffer 1312 subsequently provides the noise reduced output (FIELD 1) that was processed previous to the noise processed output 322 (FIELD 2) (i.e., previous to the live field or once delayed noise reduced live field).

[0097] After or before noise reducer 330 completes processing the next field in live field 1262 (FIELD 2) during a third time period (i.e., T3), the previous to the live field 1330 of field buffer 1312 may be written to field buffer 1310. The next noise reduced output 322 (FIELD 2) may be written to field buffer 1312 in place of the noise reduced output (FIELD 1). During time period T3, the contents of field buffer 1312 is noise reduced output (FIELD 2) (i.e., previous live field or once delayed noise reduced live field) and the contents of field buffer 1310 is noise reduced output (FIELD 1)

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(i.e., previous to previous the live field or twice delayed noise reduced live field).

5 **[0098]** During time period T3, noise reducer 330 may operate on live field 1262 (FIELD 3) and the previous to the previous live field 332 (FIELD 1). During the same time period T3, de-interlacer 340 may operate on live field 1262 (FIELD 3) or the noise reduced output (FIELD 3), live field previous to the live field 1330 (FIELD 2), and live field previous to the previous live field 332 (FIELD 2). The sharing of off-chip memory 300 between noise reducer 330 and de-interlacer 340 thereby results in using only 2-field buffer locations whereas illustrated in FIG. 3, four field buffer locations are typically required in off-chip memory 300 for providing similar functionality.

15 **[0099]** By reducing the number of field buffer locations in memory, additional video processing pipelines may be provided with equal processing power and more memory storage and bandwidth, thereby enabling the high-quality video processing of at least two channels. Furthermore, the data transfer bandwidth between dual video processor 400 and off-chip memory 300 may be reduced as only a single write port and two read ports may be used to provide the aforementioned functionality.

20 **[0100]** In some other embodiments, noise reducer 330 and de-interlacer 340 may operate on multiple field lines in each frame simultaneously. As illustrated in FIG. 15, each of these field lines may be stored in live field line buffers 1520, previous live field line buffers 1530, and previous to the previous live field line

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buffers 1510. Line buffers 1510, 1520, and 1530 may be storage locations in dual video processor 400 that may provide high efficiency and speed in storing and accessing data. To further reduce the amount of storage space, line buffers 1510, used by both noise reducer 330 and de-interlacer 340, may be shared among the noise reducer and the de-interlacer modules.

[0101] As illustrated in FIG. 15, as live field 1262 is received by noise reducer 330 and de-interlacer 340, in addition to the operation described in connection with FIGS. 13 and 14 for storing the live field in field buffer 1312, live field 1262 may also be stored in live field line buffers 1520. This enables noise reducer 330 and de-interlacer 340 to access multiple live field lines received at different time intervals simultaneously.

Similarly, the contents stored in field buffer locations 1310 and 1312 may be moved to the corresponding line buffers 1510 and 1530, respectively in turn providing buffering for previous live field (noise reduced output previous to the live field) and previous to the previous live field lines (noise reduced output previous to the previous live field). This enables noise reducer 330 and de-interlacer 340 to access multiple previous live field lines and previous to the previous live field lines simultaneously. As a result of including field line buffers, noise reducer 330 and de-interlacer 340 may operate on multiple field lines simultaneously. Consequently, because the noise reducer 330 and de-interlacer 340 share access to the previous to the previous live field, stored in field

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buffer location 1310, they may also share access to corresponding field line buffers 1510. This in turn may reduce the amount of storage required on or substantially close to dual video processor 400.

5 **[0102]** Although only three line buffers are shown in FIG. 15, it should be understood that any number of field line buffers may be provided. In particular, the number of field line buffers that are provided depend on the amount of storage space available on dual video
10 processor 400 and/or the number of simultaneous field lines that may be needed by noise reducer 330 and de-interlacer 340. However, it should be understood that any number of additional noise reduction units and de-interlacing units may be provided to aid in processing
15 multiple field lines.

[0103] For example, if two noise reducers 330 and two de-interlacers 340 that can each process three live field lines simultaneously are provided, then eight live field line buffers 1520, six previous live field line
20 buffers 1530, and six previous to the previous live field line buffers 1510 may be used to process multiple field lines -- where the outputs of each field line buffer would be coupled to the corresponding inputs of the noise reducers and de-interlacer units. In fact, it has been
25 contemplated that the contents of one or more frames can be stored in the field buffers if the number of required noise reducers and de-interlacers and on-chip space is available.

[0104] FIG. 16 illustrates in more detail frame rate
30 conversion and scaling pipeline 550 (FIG. 5) (FRC

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pipeline). FRC pipeline 550 may include at least scaling and frame rate conversion functionality. In particular, the FRC pipeline 550 may include at least two modules used for scaling that may be placed in two of scaler
5 slots 1630, 1632, 1634, and 1636 -- one scaler for providing scaling on a first channel and one for providing scaling on a second channel. The advantages of this arrangement will become more apparent in the description of FIG. 17. Each of these scaling modules in
10 scaler slots 1630, 1632, 1634, and 1636 may be capable of performing up-scaling or down-scaling in any scaling ratio. The scalers may also include circuitry for performing aspect ratio conversion, horizontal non-linear 3 zone scaling, interlacing and de-interlacing.
15 Scaling in some embodiments may be performed in synchronous mode (i.e., the output is synchronous with the input) or through off-chip memory 300 (i.e., the output may be positioned anywhere with respect to the input).
20 **[0105]** FRC pipeline 550 may also include functionality for frame rate conversion (FRC). At least two of the channels may include frame-rate conversion circuitry. In order to perform FRC, video data should be written to a memory buffer and read from the buffer at the desired
25 output rate. For example, an increase in frame rate results from reading the output buffer faster than the input frame thereby causing a particular frame to be repeated over time. A decrease in frame rate results from reading a frame to be outputted from a buffer at a
30 slower rate than the particular frame is written (i.e.,

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reading a frame slower than the input rate). Frame tearing or video artifacts may result from reading a particular frame during the period in which video data is available (i.e., active video).

5 **[0106]** In particular, in order to avoid video artifacts such as frame tearing appearing within an active video, the repetition or dropping of frames should happen over entire input frames and not in the middle of fields within a frame. In other words, the discontinuity
10 in video should happen only across frame boundaries (i.e., during the vertical or horizontal sync in which no picture data is provided) and not within the region of active video. A tearless control mechanism 1610 may operate to alleviate discontinuities between frames by
15 for example, controlling when a memory interface 530 reads a portion of a frame in memory. FRC may be performed in normal mode or in tearless mode (i.e., using tearless control mechanism 1610)..

20 **[0107]** In addition to the two scalers that are placed in two of scaler slots 1630, 1632, 1634, and 1636 in each of the first and second channels, there may be a further lower end scaler 1640 on a third channel. The lower end scaler 1640 may be a more basic scaler, for example, a scaler that performs only 1:1 or 1:2 up-scaling or any
25 other necessary scaling ratios. Alternatively, one of the scalers in the first and second channels may perform scaling on the third channel. Multiplexors 1620 and 1622 may control which of the at least three channels are directed to which of the available scalers. For example,
30 multiplexor 1620 may select channel 3 for performing a

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first type of scaling operation in a scaler in slot 1630 or 1632 and multiplexor 1622 may select channel 1 for performing a second type of scaling operation in a scaler in slot 1634 or 1636. It should be understood that one
5 channel may also use any number of available scalers.

[0108] FRC pipeline 550 also may include a smooth-movie mode in order to reduce motion jitter. For example, there may be a film-mode detection block in the de-interlacer that detects the mode of an input video
10 signal. If the video input signal is run at a first frequency (e.g., 60 Hz), it may be converted to either a higher frequency (e.g., 72 Hz) or a lower frequency (e.g., 48 Hz). In the case of converting to a higher frequency, a frame-repeat indication signal may be
15 provided from the film-mode detection block to the FRC block. The frame-repeat indication signal may be high during a first set of the frames (e.g., one of the frames) and low during a second set of frames (e.g., four frames) of data that may be generated by the
20 de-interlacer. During the portion of time that the frame-repeat indication signal is high, the FRC may repeat a frame consequently generating the correct sequence of data at the higher frequency. Similarly, in the case of converting to a lower frequency, a frame-drop
25 indication signal may be provided from the film-mode detection block to the FRC block. During the time period that the frame-drop indication signal is high a particular set of frames are dropped out of a sequence consequently generating the correct sequence of data at
30 the lower frequency.

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[0109] Depending on the type of scaling that is desired, as shown in scaler positioning module 1660, a scaler may be configured to be placed in various scaler slots 1630, 1632, 1634, and 1636. Scaler slots 1632 and 1636 are both located after the memory interface, although scaler slot 1632 corresponds to the scaling operation performed on a first channel and scaler slot 1636 corresponds to the scaling operation performed on a second channel. As illustrated, one scaler positioning module 1660 may include a multiplexor 1624 which selects the output that corresponds to a particular scaler configuration, while another scaler positioning module 1660 may not include a multiplexor but instead may have the output of the scaler coupled directly to another video pipeline component. Multiplexor 1624 provides the flexibility of implementing three modes of operation (described in more detail in connection with FIG. 17) using only two scaler slots. For example, if multiplexor 1624 is provided, a scaler positioned in slot 1630 may be coupled to the memory for providing down-scaling or up-scaling and also coupled to multiplexor 1624. If no memory operations are desired, the multiplexor 1624 may select the output of scaler slot 1630. Alternatively, if memory operations are required, scaler in scaler slot 1630 may scale the data and multiplexor 1624 may select the data from another scaler which up-scales or down-scales the data and is placed in scaler slot 1632. The output of multiplexor 1624 may then be provided to another video pipeline component such as a blank time optimizer 1650

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which is described in more detail in connection with the description of FIG. 18.

[0110] As illustrated in FIG. 17, scaler positioning module 1660 may include at least an input FIFO

5 buffer 1760, a connection to memory interface 530, at least one of three scaler positioning slots 1730, 1734, and 1736, a write FIFO buffer 1740, a read FIFO buffer 1750, and an output FIFO buffer 1770. Scaler positioning slots may correspond to the slots described
10 in FIG. 16. For example, scaler positioning slot 1734 may correspond to slots 1630 or 1634, similarly scaler positioning slot 1730 may correspond to slot 1630 - as described above using multiplexor 1624 enables slot 1630 to provide the functionality of scaler positioning
15 slots 1730 and 1734. One or two scalers may be positioned in any one or two of three scaler positioning slots 1730, 1734, or 1736 with respect to memory interface 530. Scaler positioning module 1660 may be part of any channel pipeline in FRC pipeline 550.

20 [0111] When synchronous mode is desired the scaler may be positioned in scaler positioning slot 1730. In this mode, FRC may be absent from the system, obviating the need to access memory by the particular FRC channel pipeline. In this mode, the output v-sync signals may be
25 locked to the input v-sync signals.

[0112] The scaler may alternatively be positioned in scaler positioning slot 1734. It may be desired to position the scaler in slot 1734 when FRC is needed and the input data should be downscaled. Down-scaling the
30 input data before writing to the memory (i.e., because a

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smaller frame size may be desired), consequently reduces the amount of memory storage that may be required. Since less data may be stored to the memory, the output data read rate may be reduced, thereby also reducing the total memory bandwidth that is required (and in turn reducing the cost) and providing a more efficient system.

[0113] In another scenario, the scaler may be positioned in scaler positioning slot 1736. It may be desired to position the scaler in slot 1736 when FRC is needed and the input data should be up-scaled. The data may be provided to the memory at a lower rate than the output data that is read (i.e., the frame size is smaller at the input than at the output). In turn, less data may be written to the memory by storing the smaller frame and later using the scaler at the output to increase the frame size. For example, if on the other hand, the scaler was positioned before the memory in slot 1734 and was used to upscale the input data, a larger frame would be stored to the memory thus requiring more bandwidth. However, in this case by positioning the scaler after the memory, a smaller frame may initially be stored to the memory (thus consuming less bandwidth) and later read back and up-scaled.

[0114] Since there may be two independent scalers in two separate scalar positioning modules 1660, for first and second channels, if there is a memory access requirement on both of these scalar positioning modules 1660, it may be the case that one of them requires high bandwidth and the other may require a low bandwidth memory access. Blank time optimizer (BTO)

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multiplexor 1650 may provide one or more storage buffers (large enough to store one or more field lines) in order to reduce memory bandwidth and enable any number of channels to share the stored field line -- thereby
5 reducing memory storage requirements.

[0115] FIG. 18 is an illustrative example of the operation of BTO multiplexor 1650 (FIG. 16). As shown in FIG. 18, a first channel (Main) occupies a majority portion of screen 1810 and a second channel (PIP)
10 occupies a smaller portion of screen 1810. As a consequence, the PIP channel may have less active data and require less access to memory than the Main channel over the same time interval thereby requiring less bandwidth.

[0116] For example, if one field line in a frame contains 16 pixels, the PIP channel may only occupy 4 pixels of the total field in the frame while the Main channel may occupy the remaining 12 pixels. The amount of time, therefore, that the PIP channel has to access
15 the memory to process 4 pixels is four times longer than that of the Main channel and thereby requires less bandwidth as shown by memory access timeline 1840 (i.e., the PIP has a larger blank time interval). Therefore, in order to reduce the memory bandwidth that is required,
20 the PIP channel may access the memory at a substantially slower rate and enable the Main channel to use the remaining bandwidth.

[0117] BTO multiplexor 1650 may be configured to use various clock rates when accessing memory on different
25 channels. For example, when a slower clock rate may be
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desired on a particular channel, BTO multiplexor 1650 may receive the requested data from the memory accessing block (client) 1820 (i.e., PIP channel) using one clock rate 1844, store the data in a field line storage buffer, and access memory using a second clock rate (which may be slower) 1846. By preventing the client from using a high clock rate to access memory directly and instead using a field line buffer to access memory with a slower clock rate, the bandwidth requirement may be reduced.

[0118] BTO multiplexor 1650 may enable sharing of different channel field line buffers which may further reduce the amount of storage required by off-chip memory 300. This way BTO multiplexor 1650 may use the shared field line buffers to blend or overlay the different channels that share a portion of the display.

[0119] The output of BTO multiplexor 1650 may be provided to color processing and channel blending video pipeline 560 (FIG. 5). FIG. 19 illustrates a more detailed description of the color processing and channel blending (CPCB) video pipeline 560. CPCB video pipeline 560 includes at least a sampler 1910, a visual processing and sampling module 1920, an overlay engine 2000, and auxiliary channel overlay 1962, further primary and auxiliary channel scaling and processing modules 1970 and 1972, a signature accumulator 1990, and a downscaler 1980.

[0120] The functions of CPCB video pipeline 560 may include at least improving video signal characteristics such as image enhancement by luma and chroma edge enhancement, and film grain generation and addition

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through blue noise shaping mask. Additionally, the CPCB video pipeline 560 can blend at least two channels. The output of the blended channels may be selectively blended with a third channel to provide a three channel blended output and a two channel blended output.

[0121] As shown in FIG. 21, CMU 1930, which may be included in the overlay engine 2000 portion of the CPCB video pipeline 560, may improve at least one video signal characteristic. The video signal characteristics may include adaptive contrast enhancement 2120, brightness, contrast, hue and saturation adjustment globally in the image, intelligent remapping of color locally 2130, intelligent saturation control keeping the hue and brightness unchanged, gamma control through a look up table 2150 and 2160, and color space conversion (CSC) 2110 to desired color space.

[0122] The architecture of CMU 1930 enables the CMU to receive video channel signal 1942 in any format and convert the output 1932 to any other format. CSC 2110 in the front of the CMU pipeline may receive video channel signal 1942 and may convert any possible 3-color space into a video color processing space (e.g., converting RGB to YCbCr). Additionally, a CSC at the end of the CMU pipeline may convert from the color processing space into an output 3-color space. A global processing function 2140 may be used to adjust brightness, contrast, hue and/or saturation and may be shared with the output CSC. Since CSC and global processing function 2140 perform matrix multiplication operations, two matrix multipliers may be combined into one. This type of

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sharing may be performed by pre-computing the final coefficients after combining the two matrix multiplication operations.

[0123] CPCB video pipeline 560 may also provide dithering to a particular number of bits as may be required by a display device. An interlacer for the at least one of the channel outputs may also be provided. CPCB video pipeline 560 may also generate control outputs (Hsync, Vsync, Field) for at least one of the channel outputs that may be displayed on a device. Also, CPCB video pipeline 560 may separate brightness, contrast, hue and saturation adjustment globally for at least one of the output channels and provide extra scaling and FRC for at least one of the output channels.

[0124] Referring again to FIGS. 16 and 19, channel outputs 1656, 1652, and 1654 from FRC pipeline 550 are provided to CPCB video pipeline 560. First channel 1656 may be processed along a first path which may use sampler 1910 for up-sampling video signal on first channel 1656 and the output 1912 of sampler 1910 may be provided to both a primary channel overlay 1960 and an auxiliary channel over 1962 to produce a blended image for at least one of the outputs. Second channel 1652 may be processed along a second path that provides visual processing and sampling on module 1920. The output of the visual processing and sampling module 1920 (which may up-sample the video signal) may be input to video overlay 1940 (or overlay engine 2000) for blending or positioning a third channel 1654 (which may also be run through sampler 1910) with the output. The function of

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overlay engine 2000 will be described in more detail in connection with FIG. 20.

[0125] The output 1942 (which may be first video channel signal 1623 overlayed with second video channel signal 1625) of video overlay may be provided through CMU 1930 to primary channel overlay 1960 and may also be provided to a multiplexor 1950. In addition to receiving output 1942 of video overlay, multiplexor 1950 may also receive outputs of visual processing and sampling module 1920 and sampler 1910. Multiplexor 1950 operates to select which of its video signal inputs to provide to auxiliary channel overlay 1962. Alternatively, a multiplexor 1951 may select either the output of multiplexor 1950 or output 1932 of CMU 1930 to provide as video signal output 1934 to auxiliary channel overlay 1962. The arrangement of the processing units before the primary and auxiliary channel overlays enables the same video signal to be provided to the primary as well as the auxiliary channel overlays. After further processing by units 1970 and 1972, the same video signal (VI) may be simultaneously 1) output for display on primary output 1974 as a primary output signal and 2) undergo further down-scaling prior to being output for display or storage on auxiliary output 1976 as auxiliary output signal.

[0126] In order to provide independent control of data selection to both primary output 1974 and auxiliary output 1976, the primary and auxiliary channels may be formed by independently selecting first and second video channel signals 1932 and 1934 from the first and second

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video channel overlay module 1940. Auxiliary channel overlay module 1962 may select the first video channel signal 1652, the second video channel signal 1654, or the overlaid first and second video channel signal 1942.

5 Since CMU 1930 is applied to first video channel signal 1652, second video channel signal 1654 may be selected either before or after CMU 1930 by multiplexor 1951 depending on whether the first and second video channel signals have the same or different
10 color spaces. Additionally, first and second video channel signals 1932 and 1934 may have independent blending with third video channel signal 1656.

[0127] CPCB video pipeline 560 may also provide scaling and FRC for auxiliary output 1976 represented by
15 downscaler 1980. This feature may be necessary in order to provide separate auxiliary output 1976 from primary output 1974. Since the higher frequency clock should be selected as the scaling clock, the CPCB video pipeline 560 may run off the primary output clock because
20 the auxiliary clock frequency may be less than or equal to that of the primary clock. Downscaler 1980 may also have the capability of generating interlaced data, which may undergo FRC and output data formatting to be used as the auxiliary output.

25 [0128] In some scenarios, when the first channel is an SDTV video signal and primary output 1974 should be an HDTV signal while auxiliary output 1976 should be an SDTV video signal, CMU 1930 may convert the first channel SD video signal into HD video and then perform HD color
30 processing. In this case, multiplexor 1950 may select as

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its output video signal 1942 (signal that may not be passed through CMU 1930) thereby providing an HD signal to primary channel overlay module 1960 and the processed SDTV signal to auxiliary channel overlay 1962. Further
5 auxiliary channel scaling and processing module 1972 may perform color control for auxiliary output 1976.

[0129] In some other scenarios, when the first channel is an HDTV video signal and primary output 1974 should be an HDTV signal while auxiliary output 1976 should be an
10 SDTV video signal, CMU 1930 may perform HD processing and multiplexor 1951 may select output of CMU 1932 to provide the HDTV processed signal to auxiliary channel overlay module 1962. Further auxiliary channel scaling and processing module 1972 may perform color control to
15 change the color space into SDTV for auxiliary output 1976.

[0130] In some other scenarios, in which both primary and auxiliary outputs 1974 and 1976 should be SD video signals, further channel scaling and processing
20 modules 1970 and 1972 may perform similar color control functions to place the signals in condition for output to corresponding primary and auxiliary outputs 1974 and 1976.

[0131] It should be understood that if a video channel
25 does not use a particular portion of the pipeline in any of pipeline segments 540, 550, 560, and 570 (FIG. 5) then that portion may be configured to be used by another video channel to enhance video quality. For example, if second video channel 1264 does not use de-interlacer 340
30 in FRC pipeline 550, then first video channel 1262 may be

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configured to use de-interlacer 340 of second video channel pipeline in order to improve its video quality. As described in connection with FIG. 15, an additional noise reducer 330 and an additional de-interlacer 340 may
5 increase the quality of a particular video signal by allowing shared memory pipeline segment 1260 to process additional field lines simultaneously (e.g., 6 simultaneous field line processing).

[0132] Some example output formats that may be
10 provided using CPCB video pipeline 560 include National Television Systems Committee (NTSC) and Phase Alternating Line (PAL) primary and secondary outputs of the same input image, HD and SD (NTSC or PAL) primary and secondary outputs of the same input image, two different
15 outputs in which a first channel image is provided on the primary output and a second channel image is provided on the auxiliary output, overlaid first and second channel video signals on the primary output and one channel video signal (first channel or a second channel) on the
20 auxiliary output, different OSD blending factors (alpha values) on the primary and auxiliary outputs, independent brightness, contrast, hue, and saturation adjustments on the primary and auxiliary outputs, different color spaces for the primary and auxiliary outputs (e.g., Rec. 709 for
25 primary output and Rec. 601 for auxiliary output), and/or sharper/smooth image on an auxiliary outputs through the use of different sets of scaling coefficients on a first channel scaler and a second channel scaler.

[0133] FIG. 20 illustrates in more detail overlay
30 engine 2000 (FIG. 19). Overlay engine 2000 includes at

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least video overlay module 1940, CMU 1930, first and second channel parameters 2020 and 2030, a selector 2010, and a primary M-plane overlay module 2060. It should be understood that primary M-plane overlay 2060 is similar to primary channel overlay 1960 (FIG. 19) but may include additional functionality that may be used to blend or overlay further channel video signals 2040 with third channel input 1912 (FIG. 19).

[0134] Overlay engine 2000 may generate a single video channel stream by placing M available independent video/graphics planes on the final display canvas. In one particular embodiment overlay engine 2000 may generate a single channel stream by placing 6 planes on the final display canvas. Position for each plane on the display screen may be configurable. The priority of each plane may also be configurable. For example, if the position of the planes on the display canvas is overlapped, then priority ranking may be used to resolve which plane is placed on top and which plane may be hidden. The overlay may also be used to assign an optional border for each plane.

[0135] Examples of further video channel signals 2040 and their sources may include a main plane which may be first channel video signal 1652, PIP plane which may be second channel video signal 1654, char OSD plane which may be generated using an on-chip character OSD generator, bit-mapped OSD plane which may be generated using a bit-mapped OSD engine. The OSD images may be stored in a memory where a memory interface may be used to fetch various bit-mapped pre-stored objects in the

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memory and place them on the canvas which may also be stored in the memory. The memory interface may also perform format conversions while fetching the requested object. The bit-mapped OSD engine may read the stored canvas in a raster scan order and send it to the overlay. Additional video channel signals 2040 may include a cursor OSD plane which may be generated by a cursor OSD engine and may use a small on-chip memory to store the bit map of a small object like a cursor, an external OSD plane which is received from an external source. The external OSD engine may send out the raster control signals and the display clock. The external OSD source may use these control signals as a reference and send data in the scan order. This data may be routed to the overlay. If an external OSD plane is enabled, Flexiport may be used to receive the external OSD data.

[0136] Overlay 1940 before CMU 1930 may overlay first video channel stream 1653 and second video channel stream 1655. Overlay 1940 may enable CMU 1930 to perform more efficiently by allowing the CMU 1930 to operate on a single video stream thereby obviating the need to replicate modules within CMU 1930 for multiple video channel streams. Overlay 1940 in addition to providing a single video channel signal 1942 to CMU 1930 may also provide a portion (i.e., pixel-by-pixel) indicator 1944 to CMU 1930 that identifies the video portion as either belonging to the first video channel stream or the second video channel stream.

[0137] Two sets of programmable parameters 2020 and 2030 that correspond to first video channel

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stream 1653 and second video channel stream 1655 may be provided. Selector 2010 may use portion indicator 1944 to select which programmable parameters to provide to CMU 1930. For example, if portion indicator 1944
5 indicates that the portion processed by CMU 1930 belongs to first video channel stream 1653, selector 2010 may provide to CMU 1930 programmable parameters 2020 that correspond to first video channel stream 1653.

[0138] There may be the same number of layers as the
10 number of video planes. Layer 0 may be the bottom most layer and the subsequent layers may have an increasing layer index. The layers may not have dimensional or positional characteristics but instead may provide an order in which they should be stacked. Overlay
15 engine 2000 may mix the layers beginning with layer 0 and moving upwards. Layer 1 may be first blended with layer 0 using a blend factor associated with the video plane put on layer 1. The output of layer 0 and layer 1 blending may then be blended with layer 2. The blend
20 factor that may be used may be the one associated with the plane put on layer 2. The output of the layer 0, layer 1, and layer 2 blending may then be blended with layer 3 and so on until the final layer is mixed. It
25 should be understood that one of ordinary skill may choose to blend the layers in any combination without departing from the teachings of this invention. For example, layer 1 may be blended with layer 3 and then with layer 2.

[0139] It should also be understood that although
30 overlay engine 2000 is described in connection with the

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primary output channel, color processing and channel blending pipeline 560 may be modified to provide an M-plane overlay using overlay engine 2000 on auxiliary output channel.

5 **[0140]** FIG. 22 illustrates in more detail back end pipeline stage 570 of the video pipeline. Back end pipeline stage 570 may include at least a primary output formatter 2280, a signature accumulator 1990, an auxiliary output formatter 2220 and a selector 2230.

10 **[0141]** Back end pipeline stage 570 may perform output formatting for both primary and auxiliary outputs and may generate control outputs (Hsync, Vsync, Field) as the auxiliary output. The back end pipeline stage 570 may facilitate both digital and analog interfaces. Primary
15 output formatter 2280 may receive processed primary video channel signals 1974 and generate a corresponding primary output signal 492a. Auxiliary output formatter 2220 may receive processed auxiliary video channel signals 1976 and generate a corresponding auxiliary output
20 signal 492b. Signature accumulator 1990 may receive auxiliary video channel signals 1976 and accumulate and compare the differences between the accumulated signals to determine the video signal quality of the output video signal and may provide this information to a processor to
25 change system parameters if necessary.

[0142] Auxiliary video channel signals 1976 may also be provided to a CCIR656 encoder (not shown) prior to being formatted for output 492b. The CCIR656 encoder may perform any necessary encoding to place the signal in
30 condition for external storage or some other suitable

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means. Alternatively auxiliary video channel signals 1976 may be provided as output signal 492b without being encoded or formatted by using selector 2230 to select bypass auxiliary video channel signal 2240.

5 **[0143]** An interlacing module (not shown) in back end pipeline stage 570 may also be provided. If an input signal is interlaced, it may first be converted to progressive by de-interlacer 340 (FIG. 13). The de-interlacer may be necessary because all the subsequent
10 modules in the video pipeline stages may work in the progressive domain. The interlacer in back end pipeline stage 570 may be selectively turned on if an interlaced output is desired.

15 **[0144]** The interlacer module may include at least a memory large enough to store at least two lines of pixels but may be modified to store an entire frame if necessary. The progressive input may be written to the memory with the progressive timings. The interlaced timings in lock with the progressive timings may be
20 generated at half the pixel rate. The data may be read from the memory with the interlaced timings. Even field lines may be dropped in odd fields and odd field lines may be dropped in even fields. This in turn may produce an interlaced output that is suitable for use with a
25 given device.

30 **[0145]** Thus it is seen that apparatus and methods for providing multiple high-quality video channel streams using shared storage are provided. A person skilled in the art will appreciate that the present invention can be practiced by other than the described embodiments, which

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are presented for purposes of illustration rather than of limitation, and the present invention is limited only by the claims which follow.

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What is Claimed is:

1. A shared memory video processing system comprising:

a noise reducer;

a de-interlacer; and

5 a memory comprising a first field buffer and a second field buffer, wherein:

said first field buffer is configured to receive an output of said noise reducer;

10 said noise reducer is configured to receive an output of said second field buffer; and

said de-interlacer is configured to receive said output of said noise reducer, said output of said second field buffer, and said output of said first field buffer.

2. The system of claim 1, wherein said noise reducer is configured to receive a live field input signal and output a noise reduced live field.

3. The system of claim 2, wherein said noise reduced live field is stored in said first field buffer and wherein said output of said first field buffer comprises a once delayed noise reduced live field.

4. The system of claim 3, wherein said once delayed noise reduced live field is stored in said second field buffer and wherein said output of said second field buffer comprises a twice delayed noise reduced live
5 field.

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5. The system of claim 1, wherein said noise reducer and said de-interlacer are on a first device and said memory is on a second device.

6. The system of claim 1, wherein said noise reducer and said de-interlacer operate on a video signal using only said first and second field buffers.

7. A method for sharing memory in a video processing system comprising:

storing a first noise reduced live field in a first field buffer;

5 providing previously stored contents of a second field buffer to a noise reducer and a de-interlacer; and

moving previously stored contents of said first field buffer to said second field buffer and
10 providing said previously stored contents of said first field buffer to a de-interlacer.

8. The method of claim 7, wherein said previously stored contents of said first field buffer comprise a second noise reduced live field.

9. The method of claim 8, wherein said previously stored contents of said second field buffer comprise a third noise reduced live field.

10. The method of claim 7 further comprising producing said first noise reduced live field by processing in said noise reducer a first live field and said previously stored contents of said second field
5 buffer.

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11. The method of claim 7 further comprising processing said first noise reduced live field, said previously stored contents of said first field buffer and said previously stored contents of said second field
5 buffer in said de-interlacer to produce a de-interlaced video output.

12. The method of claim 7, wherein said noise reducer and said de-interlacer are on a first device and said first and second field buffers are on a second device.

13. A shared memory video processing system comprising:

a noise reducer that receives a live field, a delayed live field, a first noise reduced live field, and a first delayed noise reduced live field and
5 that provides a second noise reduced live field;

a plurality of field buffers that receive said second noise reduced live field and that provide said first noise reduced live field and a third noise
10 reduced live field;

a plurality of line buffers that receive said live field and said first, second and third noise reduced live fields and that provide said delayed live field, said first delayed noise reduced live field, a
15 second delayed noise reduced live field, and third delayed noise reduced live field; and

a de-interlacer that receives said first noise reduced live field, said first delayed noise reduced live field, said second noise reduced live field,

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20 said second delayed noise reduced live field, said third
noise reduced live field, and said third delayed noise
reduced live field,.

14. The system of claim 13, wherein a first of
said plurality of field buffers stores said second noise
reduced live field and moves previously stored contents
of said first field buffer to a second of said plurality
5 of field buffers.

15. The system of claim 14, wherein said
previously stored contents comprise said third noise
reduced live field.

16. The system of claim 15, wherein said first
noise reduced live field comprises previously stored
contents of said second field buffer.

17. The system of claim 13, wherein said
delayed live field and said first, second and third
delayed noise reduced live fields each correspond
respectively to said live field and said first, second
5 and third noise reduced live fields delayed by at least
one time interval.

18. The system of claim 17, wherein said
delayed live field and said first, second and third
delayed noise reduced live fields are each further
delayed by at least one time interval.

19. The system of claim 18, wherein said noise
reducer, said plurality of field buffers, and said de-
interlacer each receive said further delayed live field

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and said first, second and third delayed noise reduced
5 live fields.

20. The system of claim 13, wherein said noise reducer and said de-interlacer share access to at least one of said plurality of field buffers.

21. The system of claim 13, wherein said noise reducer and said de-interlacer share access to at least one of said plurality of line buffers.

22. A method for processing a plurality of field lines in a shared memory video processing system, the method comprising:

processing a live field, a delayed live
5 field, a first noise reduced live field, and a first delayed noise reduced live field to provide a second noise reduced live field;

buffering said second noise reduced live field to provide a third noise reduced live field;

10 delaying said live field and said first, second and third noise reduced live fields and providing said delayed live field, said first delayed noise reduced live field, a second and third delayed noise reduced live field; and

15 processing said first noise reduced live field, said first delayed noise reduced live field, said second noise reduced live field, said second delayed noise reduced live field, said third noise reduced live field, and said third delayed noise reduced live field,
20 to provide a de-interlaced output.

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23. The method of claim 22, wherein said buffering further comprises storing said second noise reduced live field and moving previously stored contents of a first buffer to a second buffer.

24. The method of claim 23, wherein said previously stored contents comprise said third noise reduced live field.

25. The method of claim 24, wherein said first noise reduced live field comprises previously stored contents of said second buffer.

26. The method of claim 22, wherein said delayed live field and said first, second and third delayed noise reduced live fields each correspond respectively to said live field and said first, second
5 and third noise reduced live fields delayed by at least one time interval.

27. The method of claim 26, wherein said delayed live field and said first, second, and third delayed noise reduced live field are each further delayed by at least one time interval.

28. The method of claim 27 further comprising receiving said further delayed live field and said further delayed first, second, and third noise reduced live fields.

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29. The method of claim 22 further comprising sharing access to at least one of said buffered noise reduced live fields.

30. The method of claim 22 further comprising sharing access to at least one of said delayed noise reduced live fields.

31. A shared memory video processing system that processes at least three sequential video fields comprising a live video field, a once delayed noise reduced video field, and a twice delayed noise reduced video field, the system comprising:

5 a first shared field buffer that stores the twice delayed noise reduced video field;

a noise reducer that receives the live video field and the twice delayed noise reduced video field and provides a noise reduced live video field;

10 a de-interlacer that receives the noise reduced live video field, the once delayed noise reduced video field, and the twice delayed noise reduced video field and provides a noise reduced de-interlaced output

15 video field.

32. The system of claim 31 further comprising:

a second shared field buffer that stores the once delayed noise reduced video field, wherein the twice delayed noise reduced video field is moved from the

5 second shared field buffer into the first shared field buffer in response to receiving the live video field; and

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wherein the noise reduced live video field is stored in the second shared field buffer as the once delayed noise reduced video field.

33. The system of claim 32, wherein a memory device comprises said first and second shared field buffers and wherein said memory device comprises one write port and two read ports.

34. The system of claim 33, wherein said noise reducer is operable to control said write port and a first of said two read ports and said de-interlacer is operable to control a second of said two read ports.

35. A method of operating a shared memory video processing system that processes at least three sequential video fields comprising a live video field, a once delayed noise reduced video field, and a twice delayed noise reduced video field, the method comprising:

5 storing in a first shared field buffer the twice delayed noise reduced video field;

processing the live video field and the twice delayed noise reduced video field to provide a

10 noise reduced live video field; and

processing the noise reduced live video field, the once delayed noise reduced video field, and the twice delayed noise reduced video field from the first shared field buffer to provide a noise reduced de-

15 interlaced output video field.

36. The method of claim 35 further comprising:

receiving the live field;

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moving the twice delayed noise reduced
video field from a second shared field buffer into the
5 first shared field buffer; and
storing the noise reduced live video field
in the second shared field buffer to provide the once
delayed noise reduced video field.

37. The method of claim 36 further comprising
performing a noise reduction and de-interlacing operation
on the twice delayed noise reduced video field.

38. The method of claim 37 further comprising
controlling a write port and one of two read ports of a
memory device comprising said first and second field
buffers and controlling a second one of said two read
5 ports.

39. A shared memory video processing system
comprising:

a memory device;
signal processing circuitry operable to
5 process a plurality of live fields and a plurality of
noise reduced live fields;
delay circuitry operable to delay at least
one of said plurality of live fields and at least one of
said plurality of noise reduced live fields; and
10 wherein said signal processing circuitry
is further operable to process along with said plurality
of live fields and plurality of noise reduced live fields
said at least one delayed live field and said at least
one delayed noise reduced live field.

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40. The system of claim 39, wherein said delay circuitry comprises at least one field line buffer.

41. The system of claim 39, wherein:
said signal processing circuitry is further operable to:

read a once delayed noise reduced
5 live field from a first portion of said memory device;
store a noise reduced live field in
said first portion of said memory device; and
read a twice delayed noise reduced
live field from a second portion of said memory device;
10 and

said delay circuitry is further operable to further delay said once delayed noise reduced live field and said twice delayed noise reduced live field.

42. The system of claim 41, wherein said signal processing circuitry is further operable to perform a noise reduction on said at least one live field, said at least one delayed live field, said twice
5 delayed noise reduced live field and said further delayed twice delayed noise reduced live field.

43. The system of claim 42, wherein said signal processing circuitry is further operable to perform a de-interlacing operation on said at least one noise reduced live field, said once delayed noise reduced
5 live field, said further delayed once delayed noise reduced live field and said further delayed twice delayed noise reduced live field.

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44. The system of claim 43, wherein said noise reduction and said de-interlacing operation share said further delayed twice delayed noise reduced live field provided by a field line buffer.

45. A method of operating a shared memory video processing system, the method comprising:

processing a plurality of live fields and a plurality of noise reduced live fields;

5 delaying at least one of said plurality of live fields and at least one of said plurality of noise reduced live fields; and

 processing along with said plurality of live fields and plurality of noise reduced live fields
10 said at least one delayed live field and said at least one delayed noise reduced live field.

46. The method of claim 45 further comprising:

reading a once delayed noise reduced live field from a first portion of a memory device;

5 storing a noise reduced live field in said first portion of said memory device;

reading a twice delayed noise reduced live field from a second portion of said memory device; and

 further delaying said once delayed noise reduced live field and said twice delayed noise reduced
10 live field.

47. The method of claim 45 further comprising performing a noise reduction on said at least one live field, said at least one delayed live field, said twice

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5 delayed noise reduced live field and said further delayed
twice delayed noise reduced live field.

48. The method of claim 47 further comprising
performing a de-interlacing operation on said at least
one noise reduced live field, said once delayed noise
reduced live field, said further delayed once delayed
5 noise reduced live field, and said further delayed twice
delayed noise reduced live field.

49. The method of claim 48, further comprising
sharing, during said noise reduction and said de-
interlacing operation, said further delayed twice delayed
noise reduced live field.

5 50. An apparatus for sharing memory in a video
processing system comprising:

means for storing a first noise reduced
live field in a first field buffer means;

10 means for providing previously stored
contents of a second field buffer means to a noise
reducer means and a de-interlacer means; and

means for moving previously stored
contents of said first field buffer means to said second
field buffer means and means for providing said
15 previously stored contents of said first field buffer
means to said de-interlacer means.

51. The apparatus of claim 50, wherein said
previously stored contents of said first field buffer
means comprise a second noise reduced live field.

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52. The apparatus of claim 51, wherein said previously stored contents of said second field buffer means comprise a third noise reduced live field.

53. The apparatus of claim 50 wherein said noise reducer means produces said first noise reduced live field by processing a first live field and said previously stored contents of said second field buffer means.

54. The apparatus of claim 50 wherein said de-interlacer means produces a de-interlaced video output by processing said first noise reduced live field, said previously stored contents of said first field buffer means and said previously stored contents of said second field buffer means.

55. The apparatus of claim 50, wherein said noise reducer means and said de-interlacer means are on a first device and said first and second field buffers means are on a second device.

56. An apparatus for processing a plurality of field lines in a shared memory video processing system, the apparatus comprising:

means for processing a live field, a delayed live field, a first noise reduced live field, and a first delayed noise reduced live field to provide a second noise reduced live field;

means for buffering said second noise reduced live field to provide a third noise reduced live field;

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15 means for delaying said live field and
said first, second and third noise reduced live fields
and providing said delayed live field, said first delayed
noise reduced live field, a second and third delayed
noise reduced live field;

20 means for processing said first noise
reduced live field, said first delayed noise reduced live
field, said second noise reduced live field, said second
delayed noise reduced live field, said third noise
reduced live field, and said third delayed noise reduced
25 live field to provide a de-interlaced output.

57. The apparatus of claim 56, wherein said
means for buffering further comprises means for storing
said second noise reduced live field and means for moving
previously stored contents from a first buffer means to a
5 second buffer means.

58. The apparatus of claim 57, wherein said
previously stored contents comprise said third noise
reduced live field.

59. The apparatus of claim 58, wherein said
first noise reduced live field comprises previously
stored contents of said second buffer means.

60. The apparatus of claim 56, wherein said
delayed live field and said first, second and third
delayed noise reduced live fields each correspond
respectively to said live field and said first, second
5 and third noise reduced live fields delayed by at least
one time interval.

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61. The apparatus of claim 60, wherein said delayed live field and said first, second and third delayed noise reduced live fields are each further delayed by at least one time interval.

62. The apparatus of claim 61 further comprising means for receiving said further delayed live field and said further delayed first, second and third noise reduced live fields.

63. The apparatus of claim 56 further comprising means for sharing access to at least one of said plurality of buffered noise reduced live fields.

64. An apparatus for operating a shared memory video processing system that processes at least three sequential video fields comprising a live video field, a once delayed noise reduced video field, and a twice delayed noise reduced video field, the apparatus comprising:

means for storing in a first shared field buffer means the twice delayed noise reduced video field;

means for processing the live video field and the twice delayed noise reduced video field to provide a noise reduced live video field; and

means for processing the noise reduced live video field, the once delayed noise reduced video field, and the twice delayed noise reduced video field to provide a noise reduced de-interlaced output video field.

65. The apparatus of claim 64 further comprising:

- 74 -

means for receiving the live field;
means for moving the twice delayed noise
5 reduced video field from a second shared field buffer
into the first shared field buffer means; and
means for storing the noise reduced live
video field in the second shared field buffer means to
provide the once delayed noise reduced video field.

66. The apparatus of claim 65 further
comprising means for performing a noise reduction and de-
interlacing operation on the twice delayed noise-reduced
live field.

67. The apparatus of claim 65 further
comprising means for controlling a memory device
comprising a write port, two read ports, and said first
and second shared field buffer means.

5 68. An apparatus for operating a shared memory
video processing system, the apparatus comprising:
means for processing a plurality of live
fields and a plurality of noise reduced live fields;
means for delaying at least one of said
10 plurality of live fields and at least one of said
plurality of noise reduced live fields; and
means for processing along with said
plurality of live fields and plurality of noise reduced
live fields said at least one delayed live field and said
15 at least one delayed noise reduced live field.

69. The apparatus of claim 68 further
comprising:

- 75 -

means for reading a once delayed noise
reduced live field from a first portion of a memory

5 device means;

means for storing a noise reduced live
field in said first portion of said memory device means;

means for reading a twice delayed noise
reduced live field from a second portion of said memory

10 device means; and

means for further delaying said once
delayed noise reduced live field and said twice delayed
noise reduced live field.

70. The apparatus of claim 69 further
comprising means for performing a noise reduction on said
at least one live field, said at least one delayed live
field interval, said twice delayed noise reduced live
5 field and said further delayed twice delayed noise
reduced live field.

71. The apparatus of claim 70 further
comprising means for performing a de-interlacing
operation on said at least one noise reduced live field,
said once delayed noise reduced live field, said further
5 delayed once delayed noise reduced live field, and said
further delayed twice delayed noise reduced live field.

72. The apparatus of claim 71, further
comprising means for sharing during said noise reduction
and said de-interlacing operation said further delayed
twice delayed noise reduced live field.

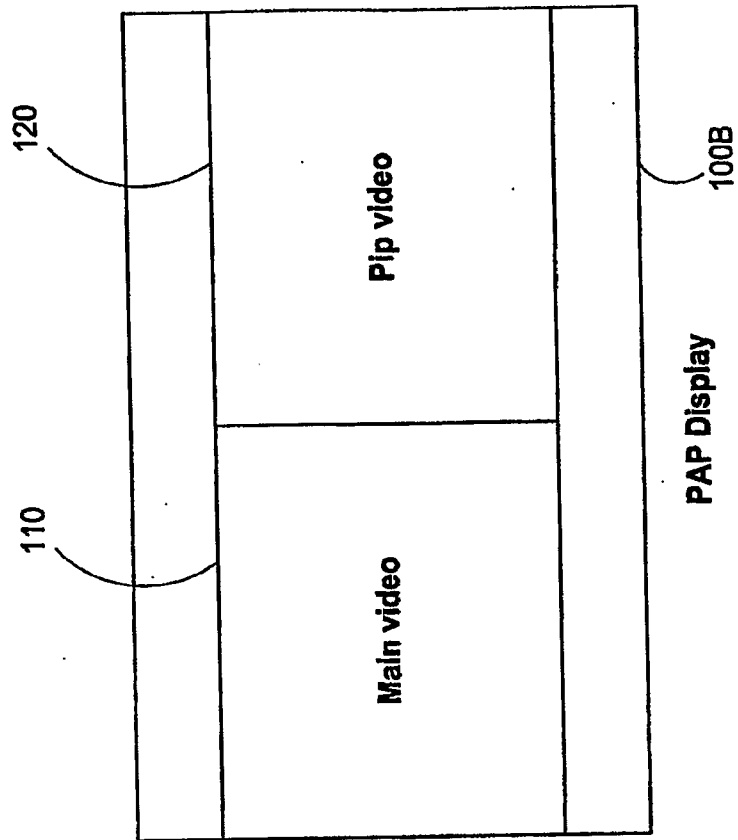


FIG. 1B

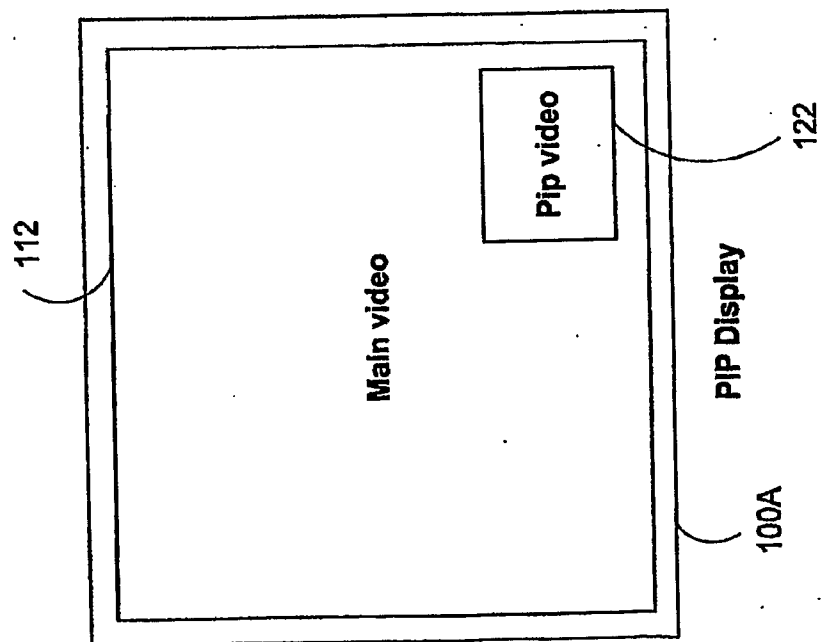


FIG. 1A

FIG. 1

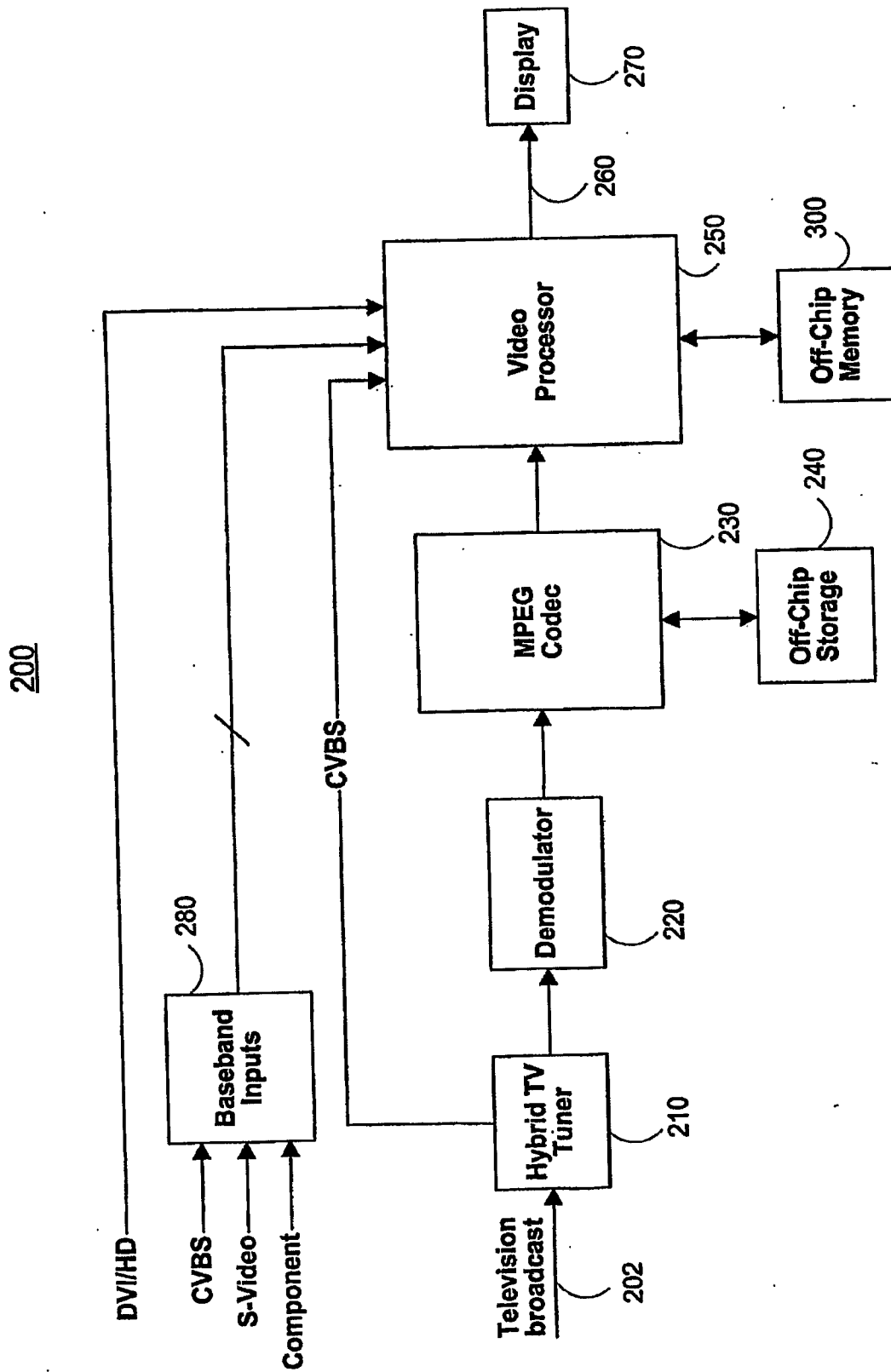


FIG. 2

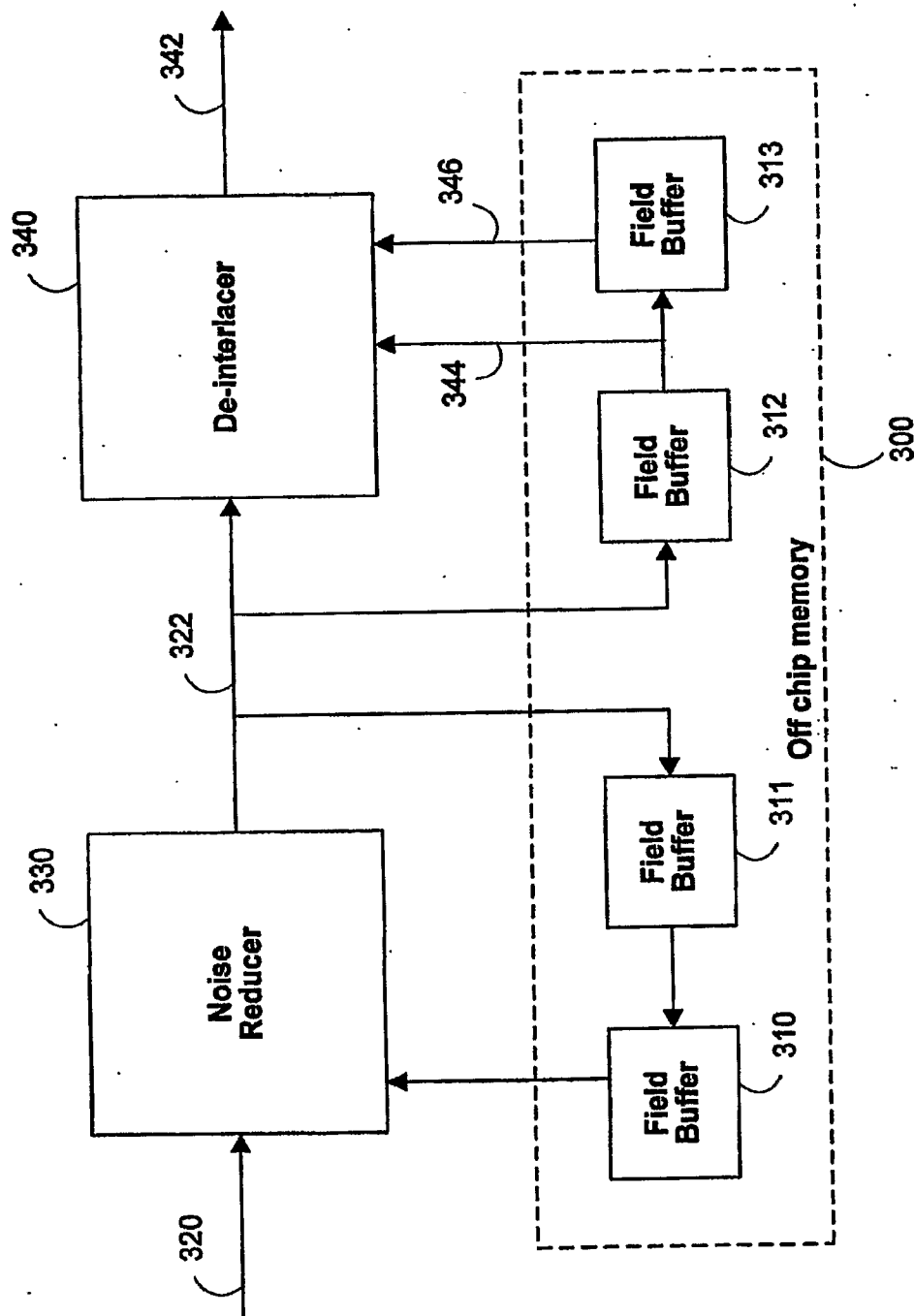


FIG. 3

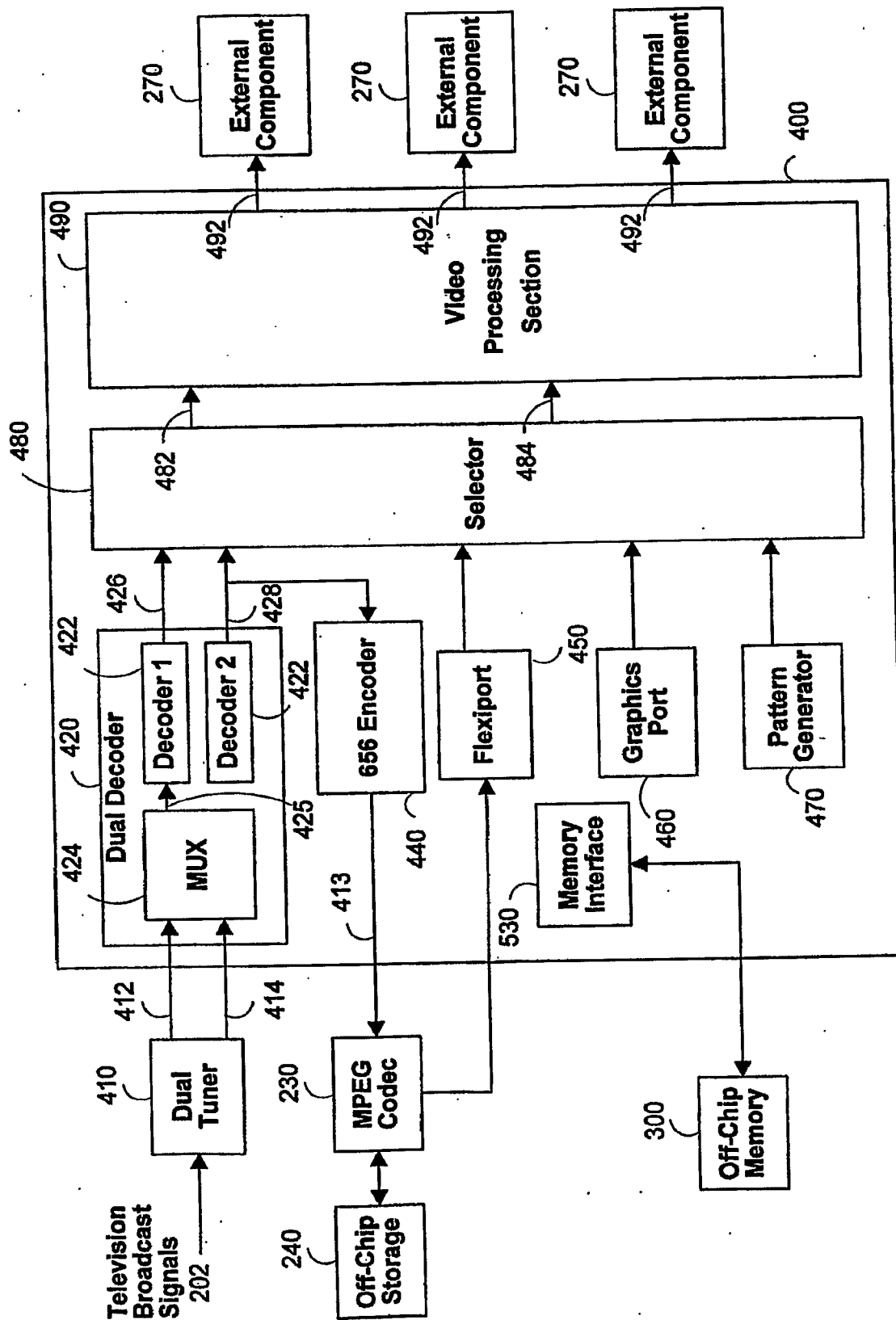


FIG. 4

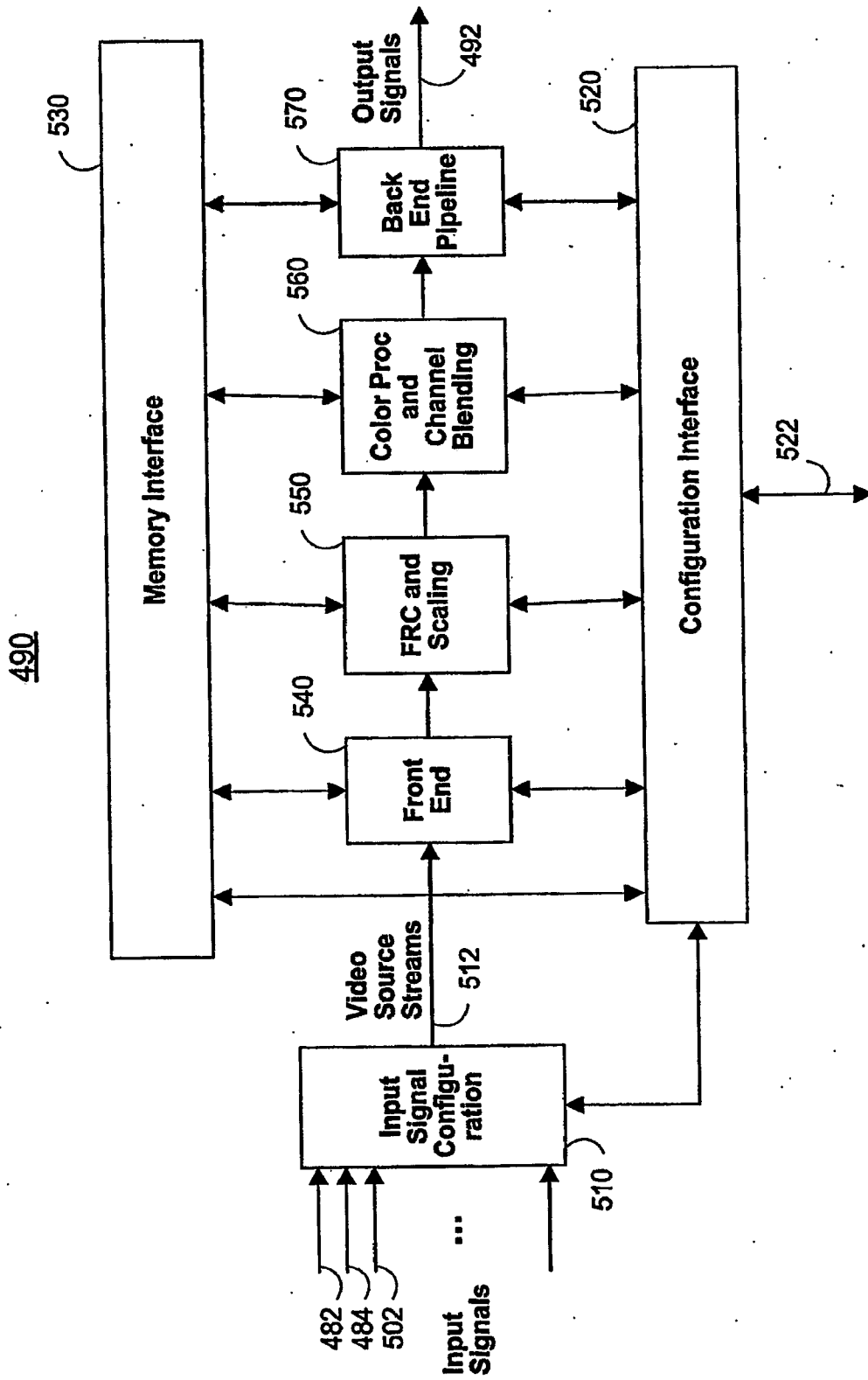


FIG. 5

600

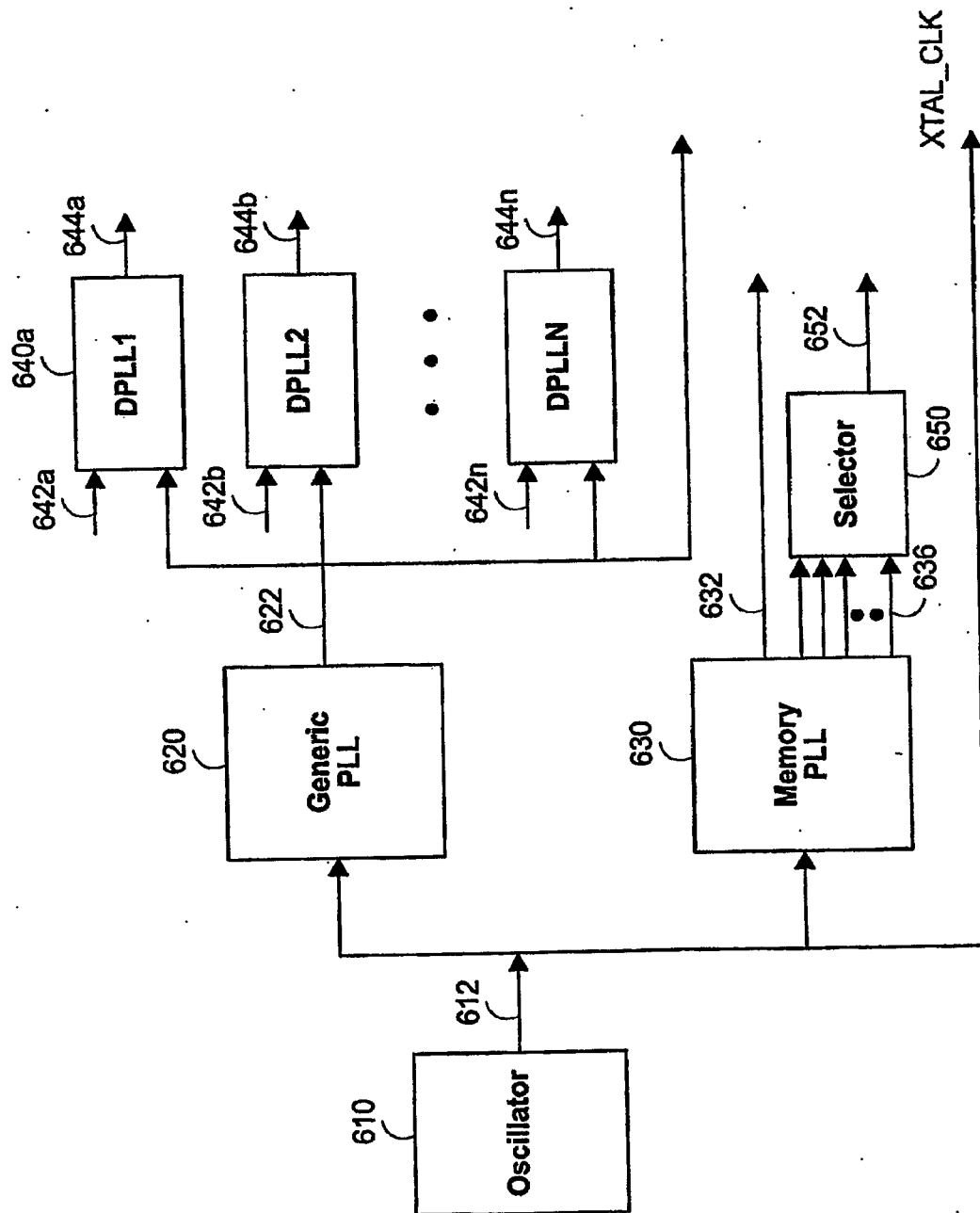
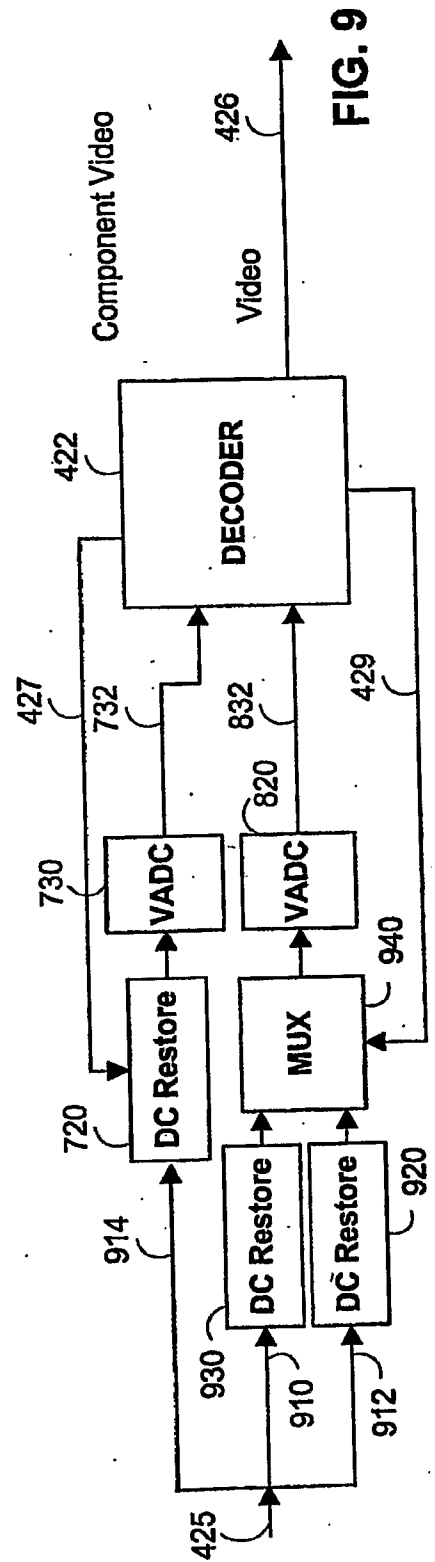
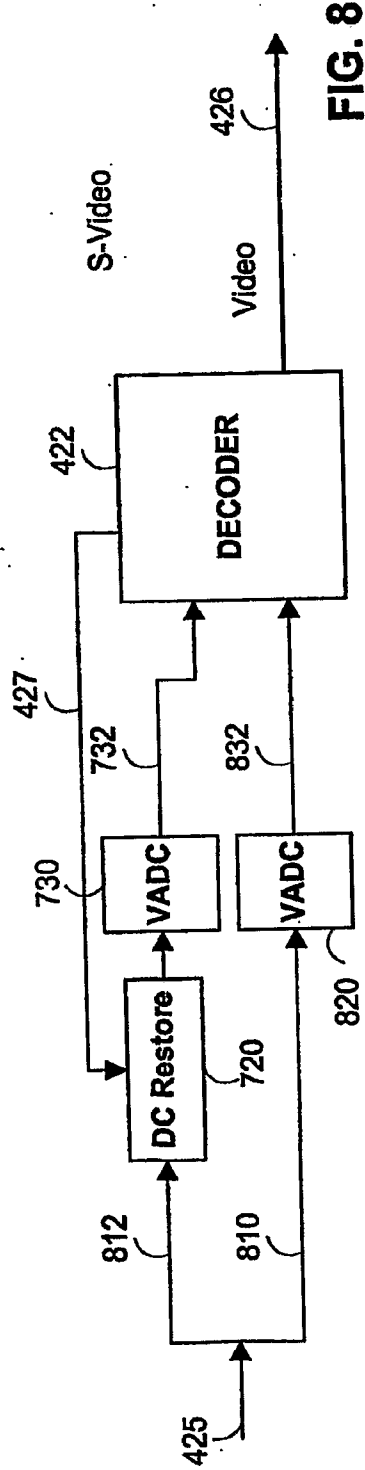
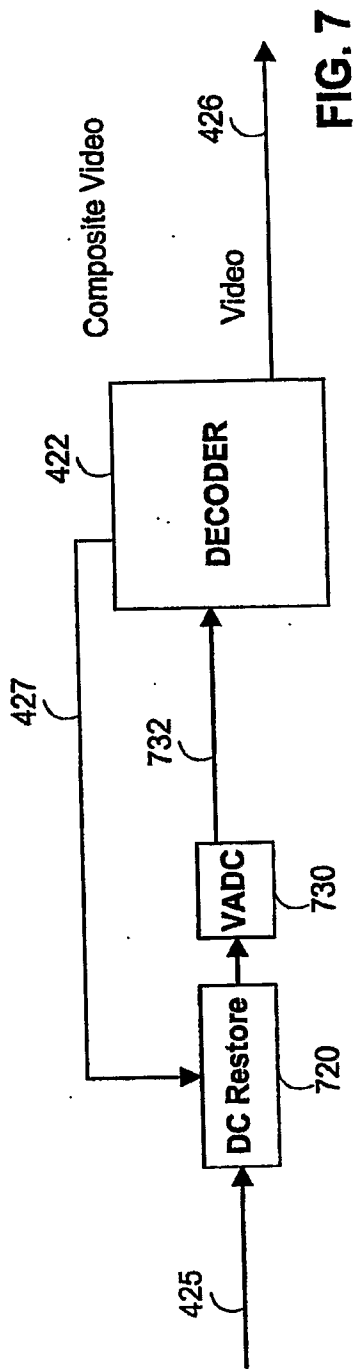


FIG. 6



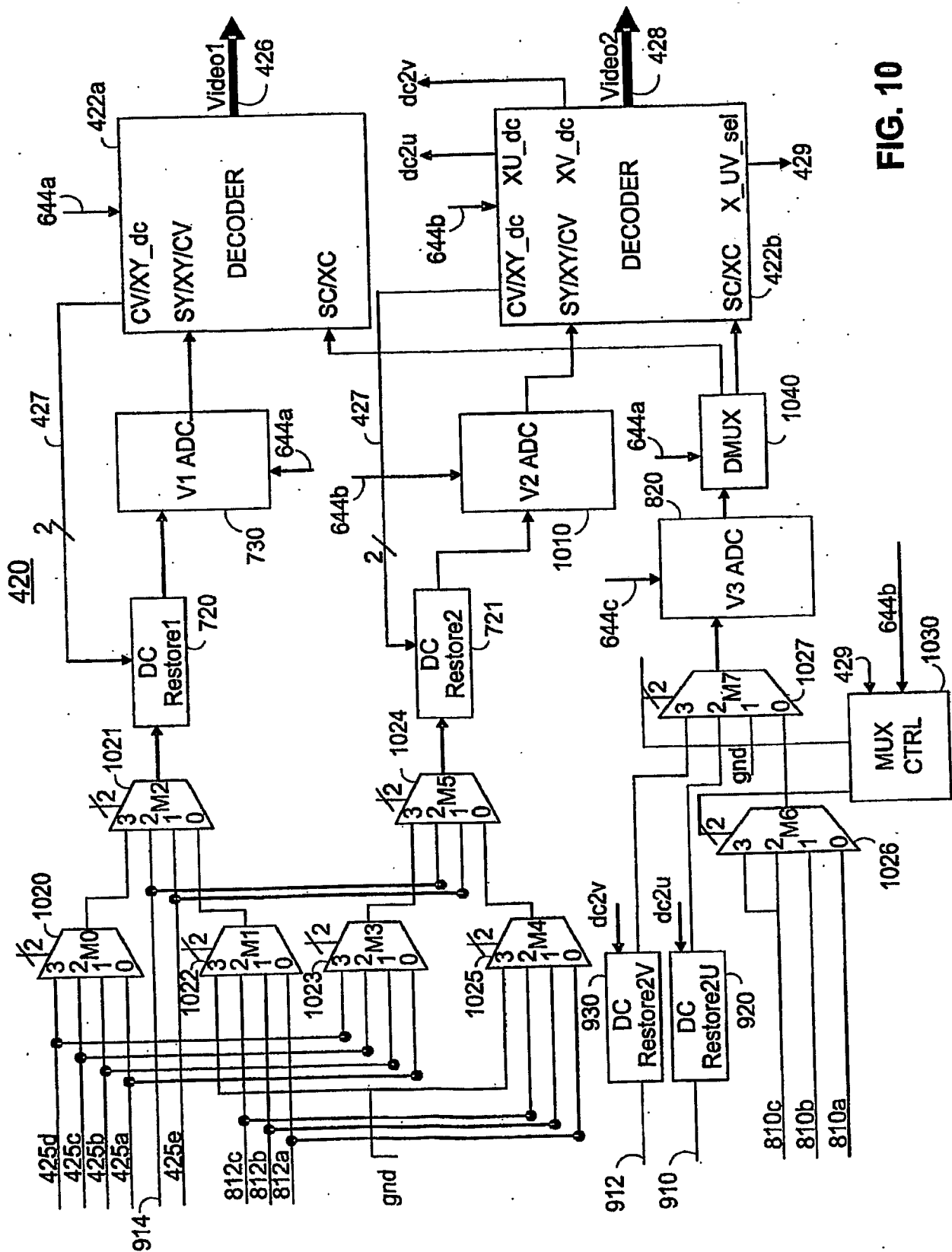


FIG. 10

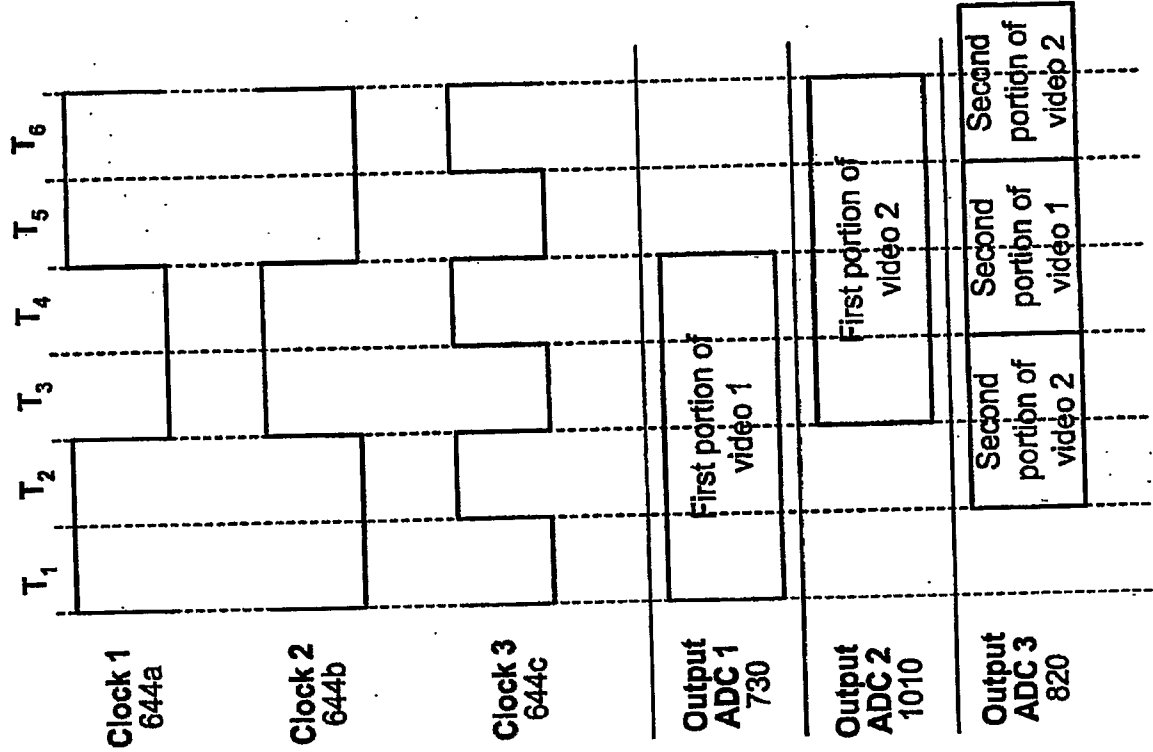


FIG. 11

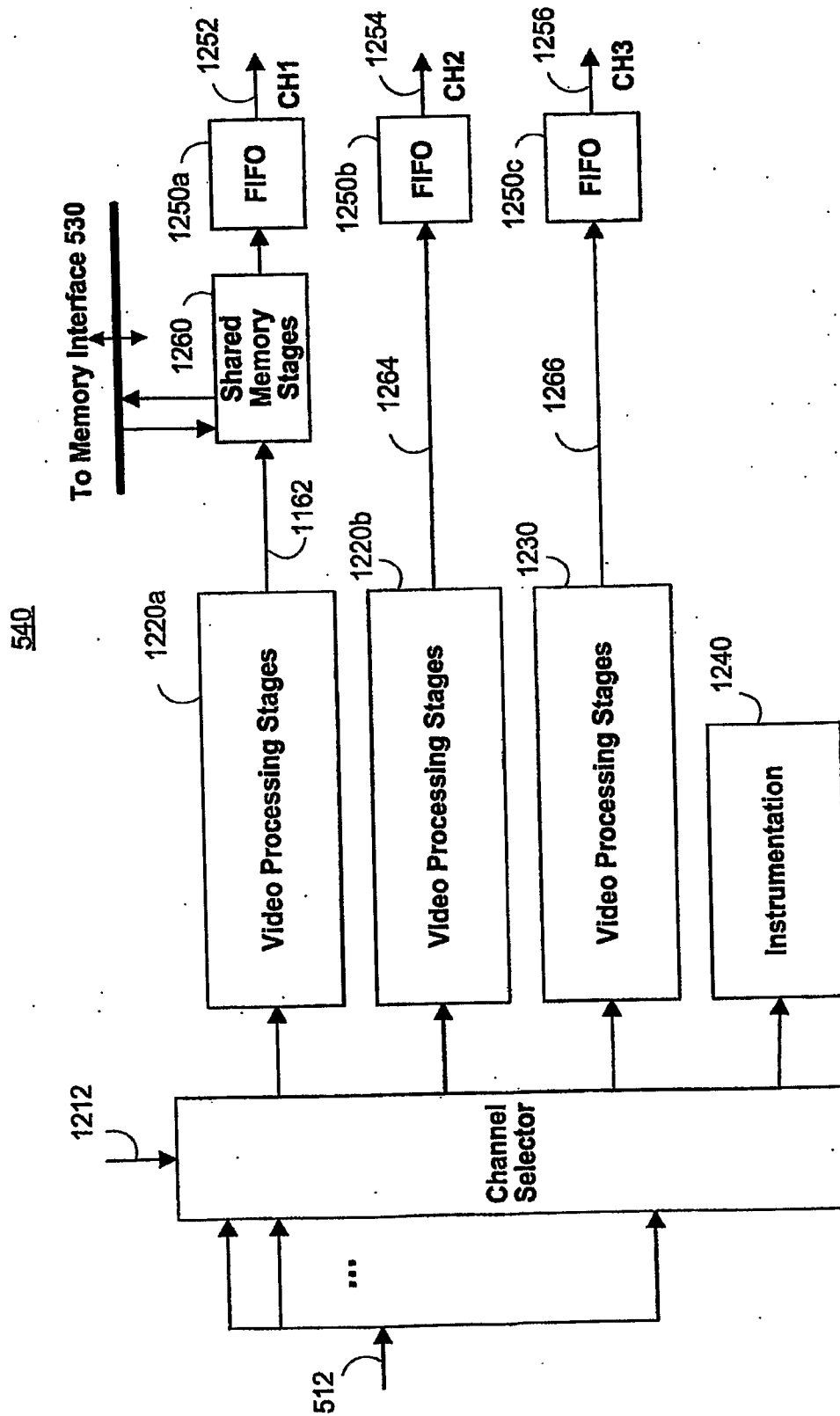


FIG. 12

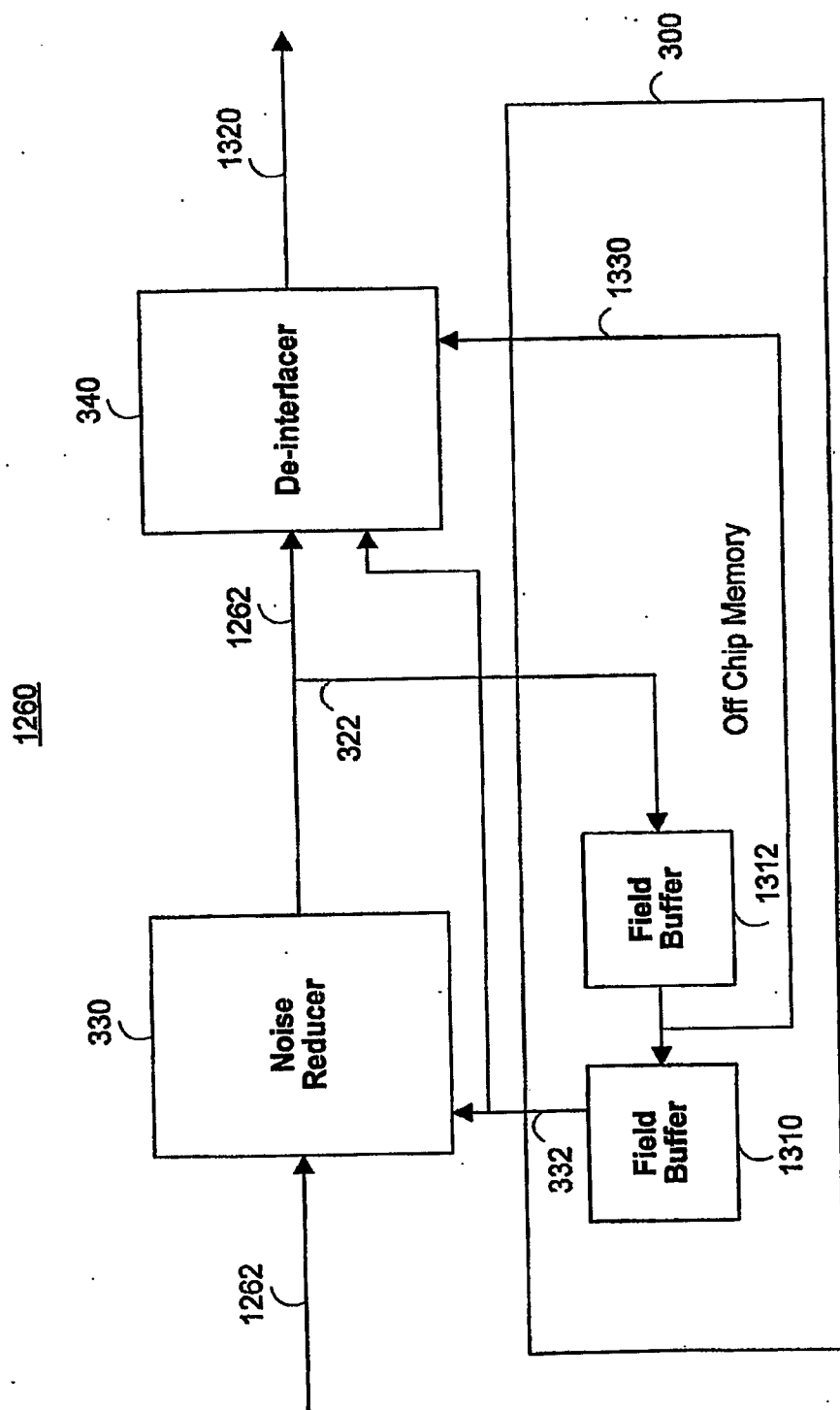


FIG. 13

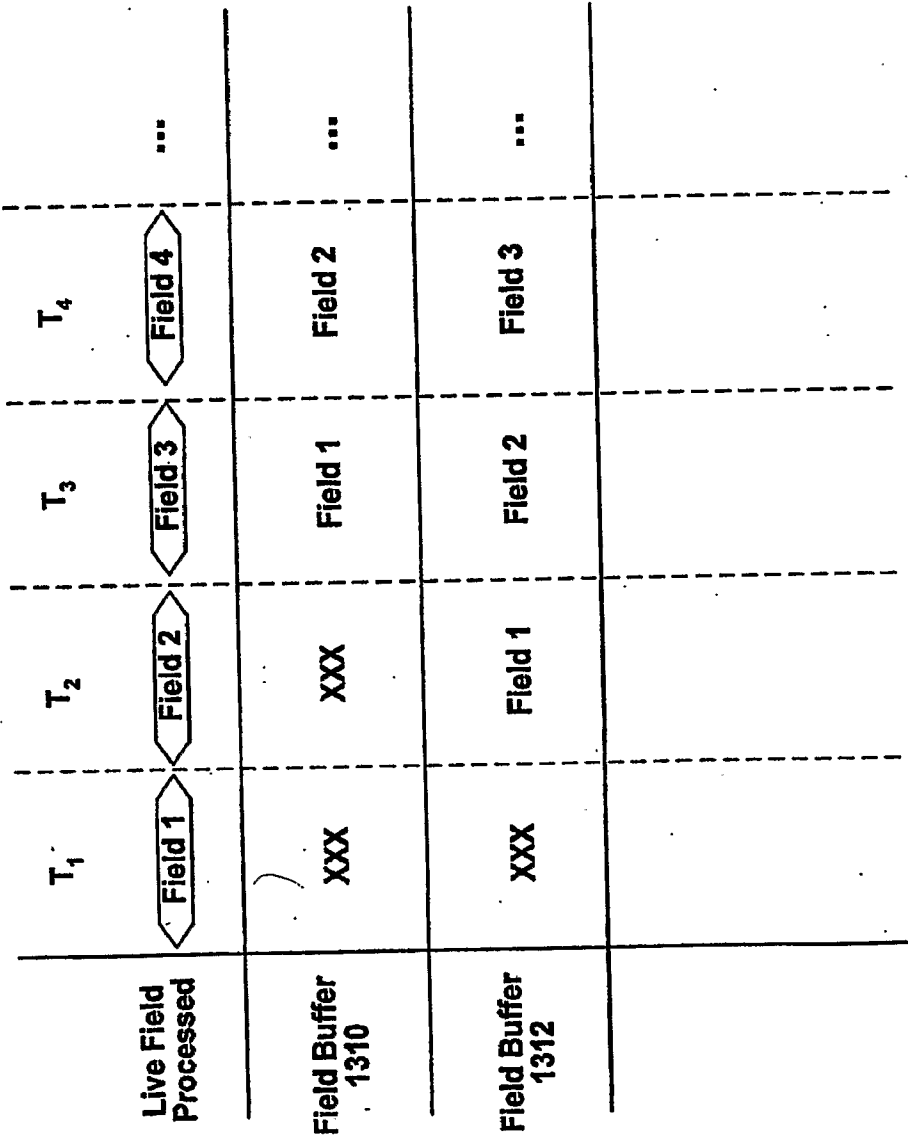


FIG. 14

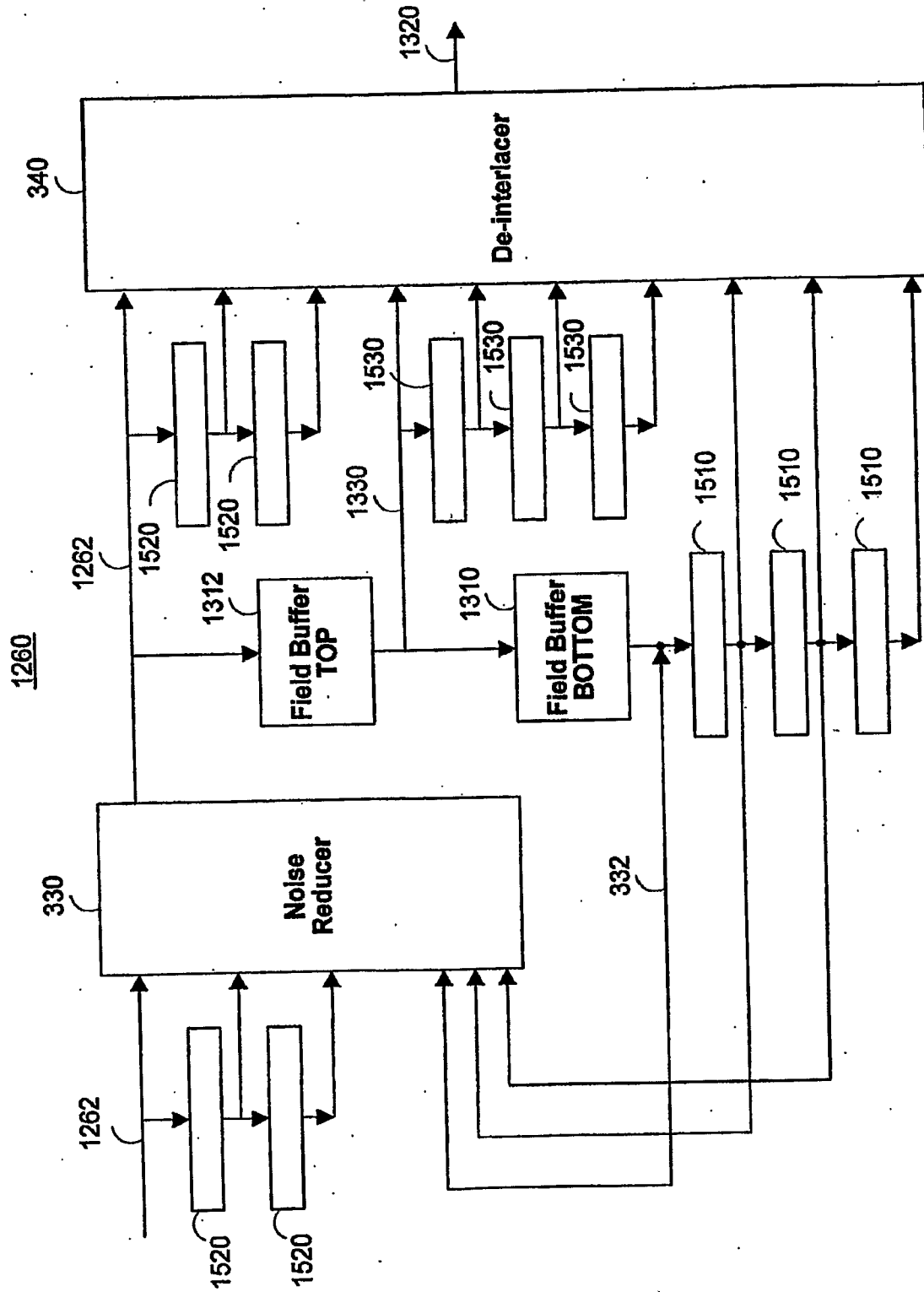


FIG. 15

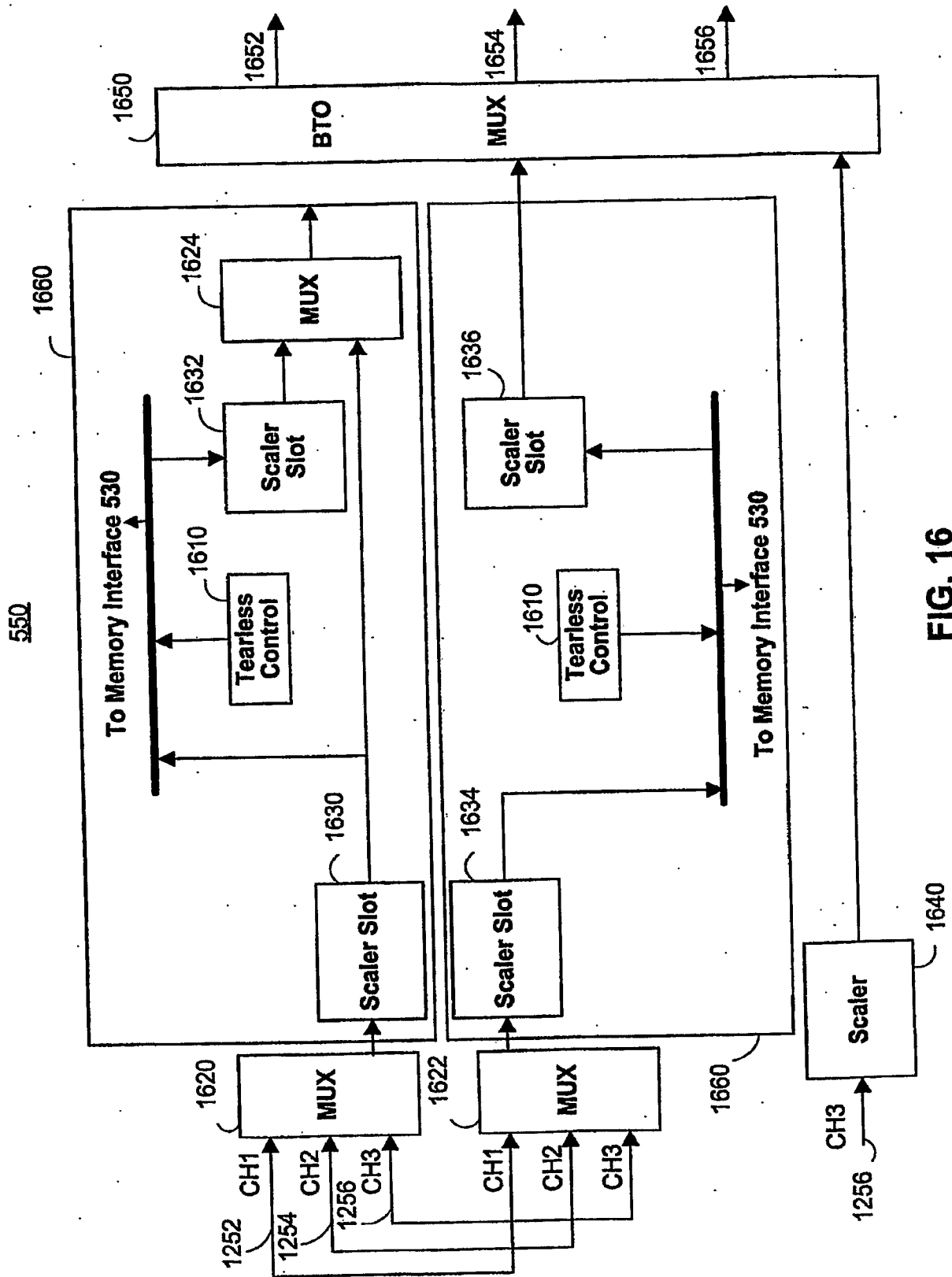


FIG. 16

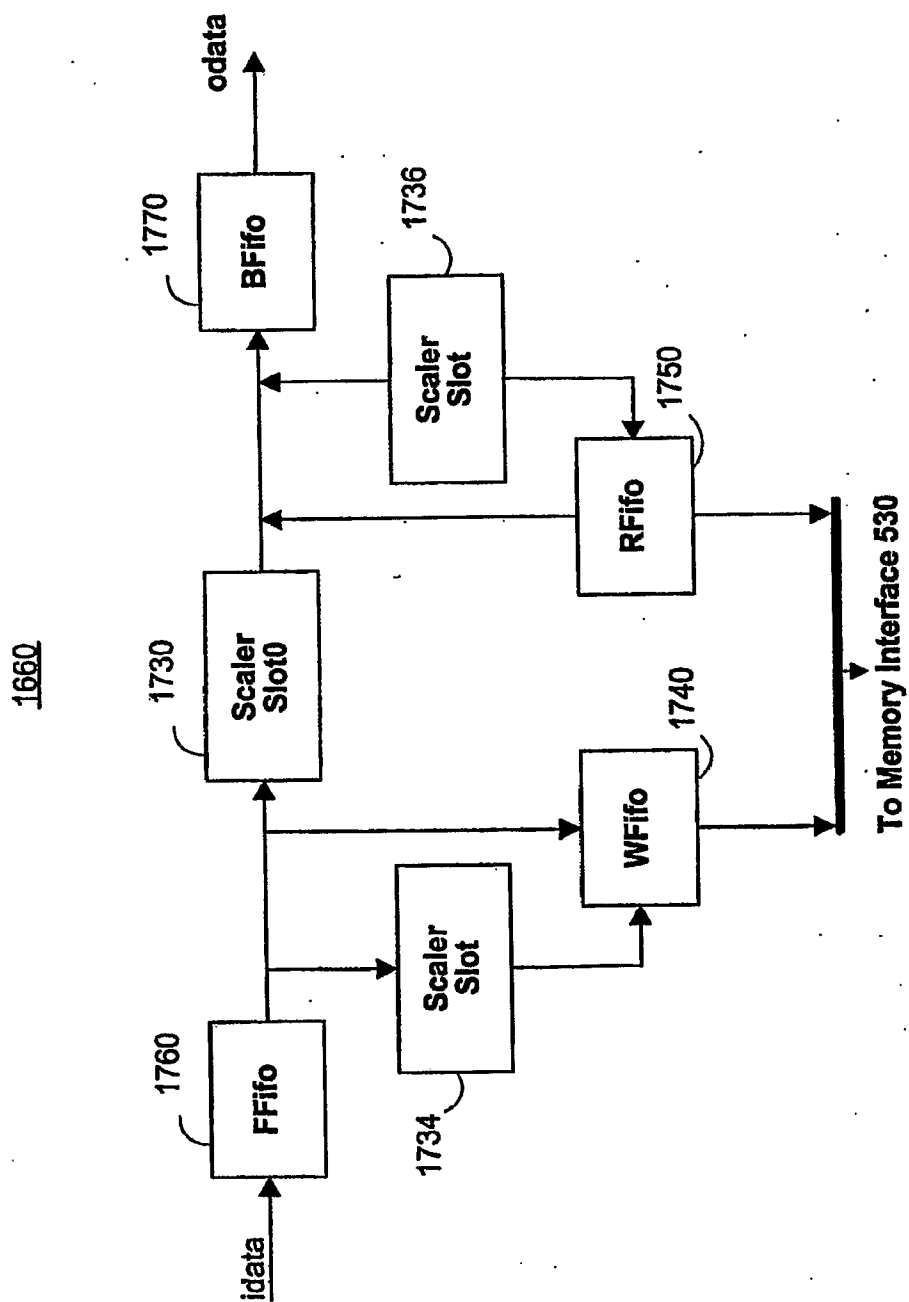


FIG. 17

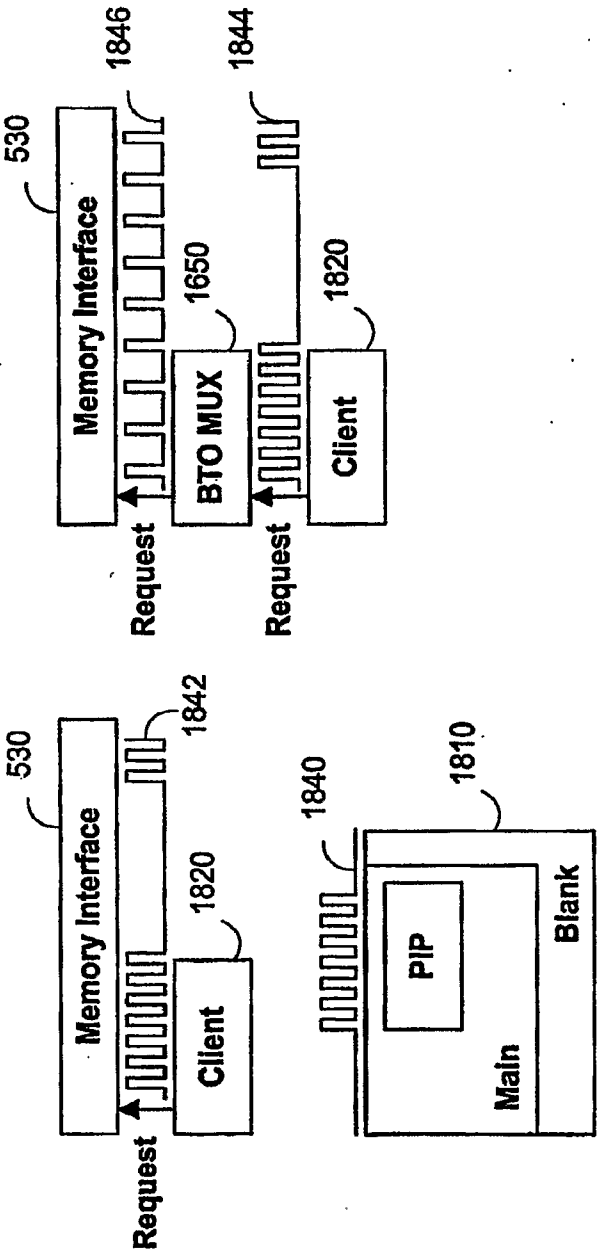
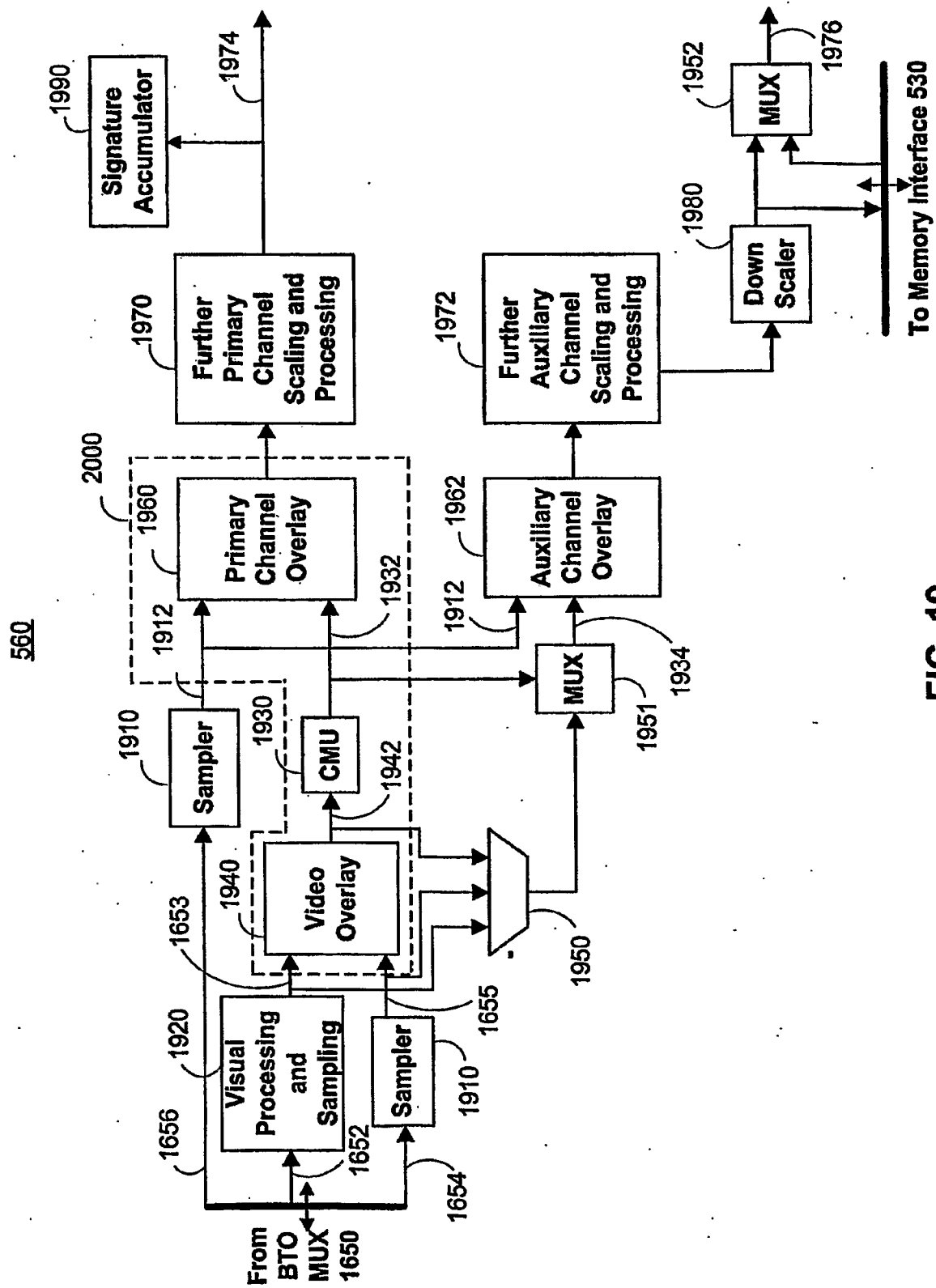


FIG. 18



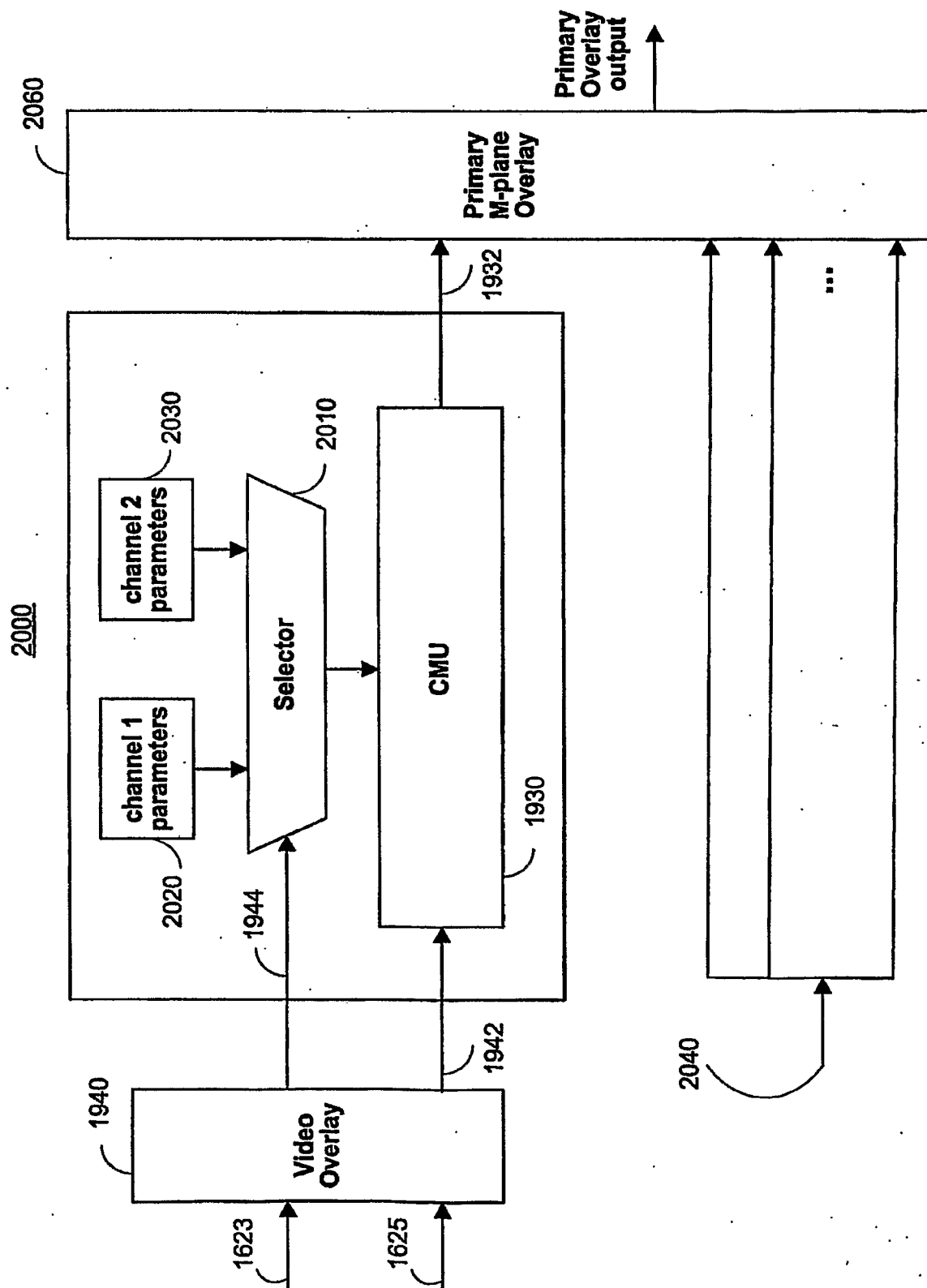


FIG. 20

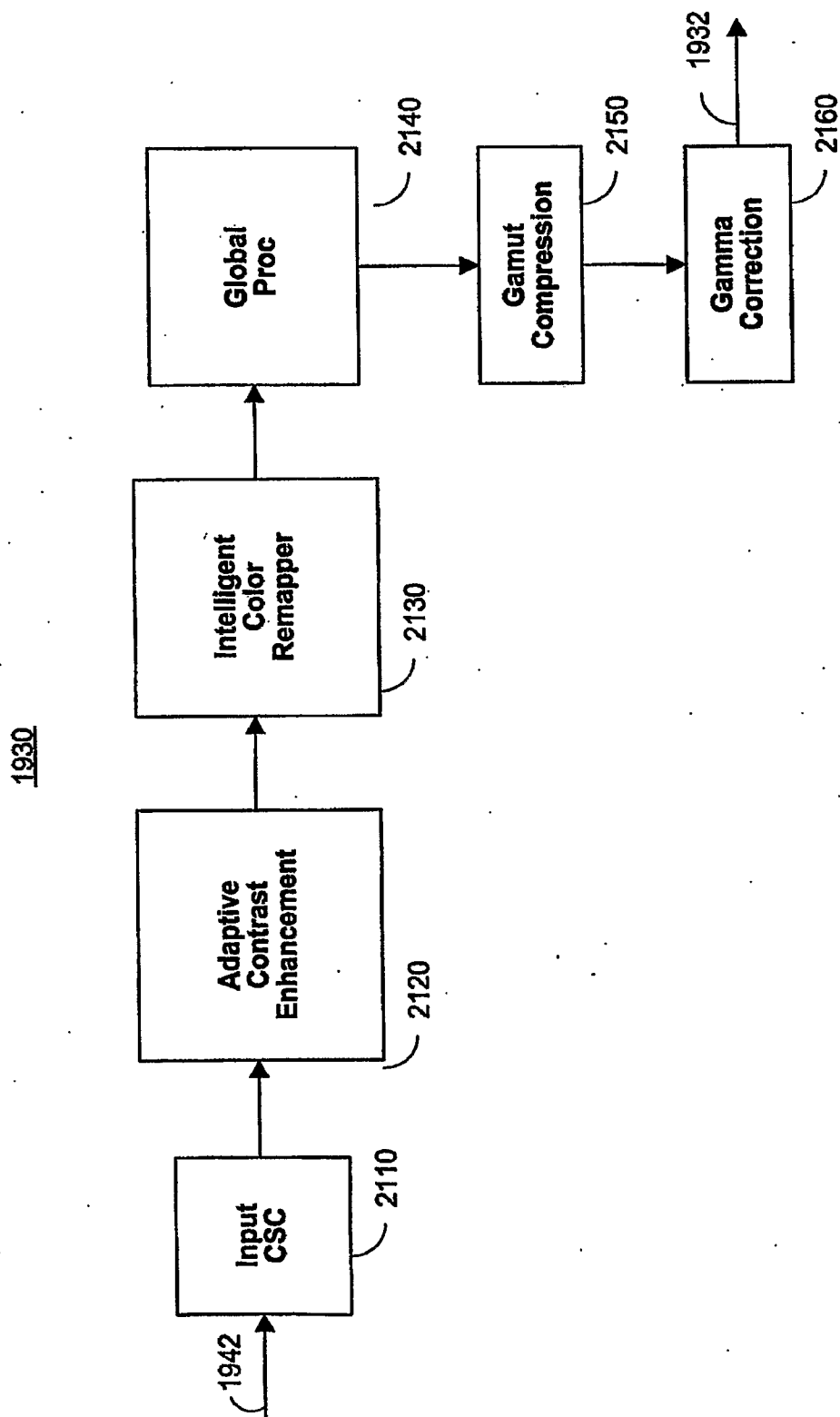


FIG. 21

570

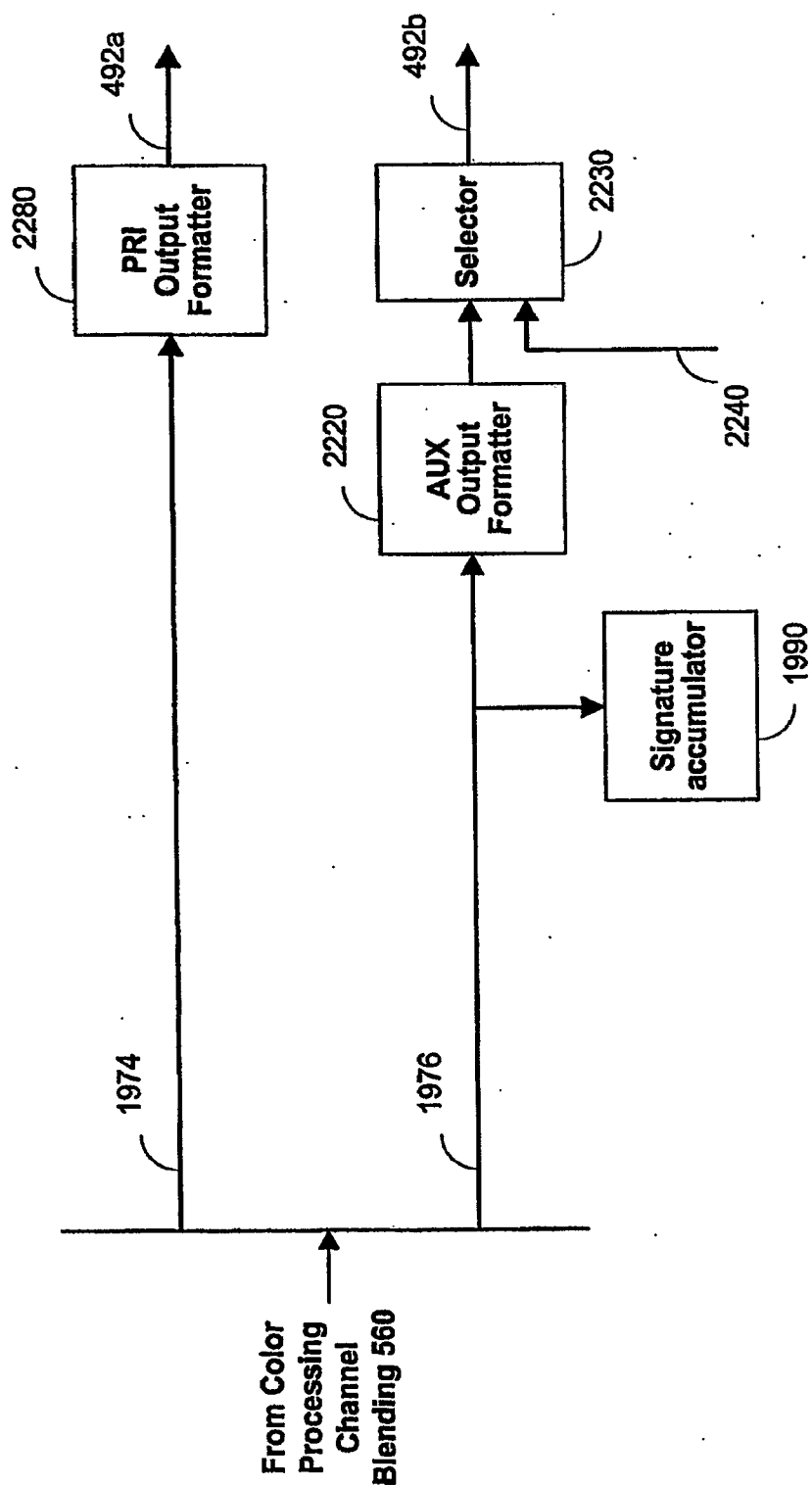


FIG. 22