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— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

[Continued on next page]

(54) **Title**: CONTROLLING CURRENT DURING POWER-UP AND POWER -DOWN SEQUENCES

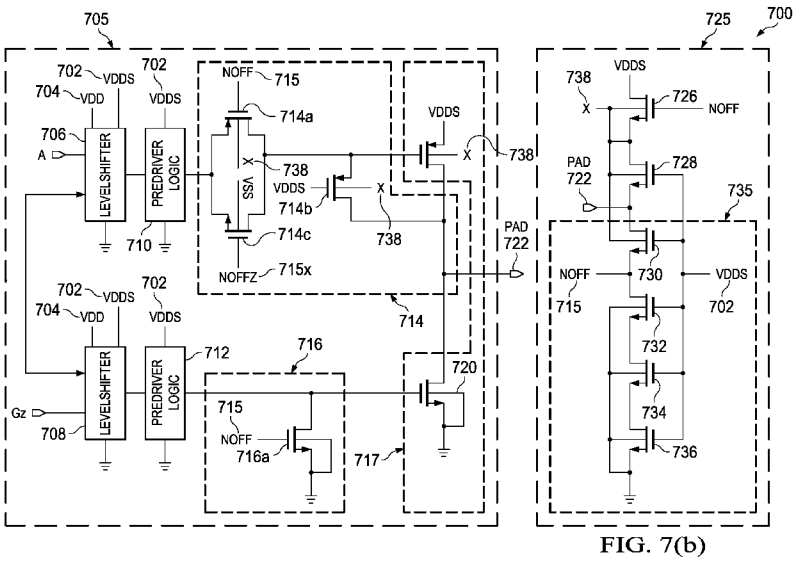

FIG. 7(b)

(57) **Abstract**: In described examples of an input/output (10) circuit (700) powered by an input/output (10) supply voltage (VDDS), a supply detector cell detects a core supply voltage (VDD) and generates a supply detect signal. A driver circuit (705) is connected to a PAD (722) and receives the supply detect signal. A failsafe circuit (725) receives a PAD (722) voltage. The failsafe circuit (725) and the supply detector cell control a leakage current from the PAD (722) based on the IO supply voltage (VDDS) and the PAD (722) voltage.

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CONTROLLING CURRENT DURING POWER-UP AND POWER-DOWN SEQUENCES

[0001] This relates in general to integrated circuits (ICs), and in particular to controlling current during power-up and power-down sequences in integrated circuits.

BACKGROUND

[0002] The ever-increasing complexity and performance requirements of portable media devices call for effective system-level power management in integrated circuits (ICs). Having one or more switchable power-domains in core-logic is a well-known low-power methodology that is employed for ICs in portable media devices. When a supply of a specific power domain is powered down, the outputs of that power-domain serving as inputs to IO (input/output) circuits are no longer valid, and these IO circuits are tri-stated to avoid possible leakage current. An IO circuit drives and receives signals on a PAD to interface with the outside world. If the IO circuit is not properly tri-stated, it results in high leakage currents (conduction currents) from the PAD into the IO circuit. A similar condition results when the IO supply voltage is powered up or down, while the PAD is held at a logical high state. Serial low-power inter-chip media bus (SLIMbus) is a standard interface between baseband or application processors and peripheral components in portable media devices. The SLIMbus is a failsafe interface and specifies that devices have ultra low PAD current (or pin current) while powering up, while powering down, and while having a stable power state in portable media devices.

SUMMARY

[0003] In described examples of an input/output (IO) circuit powered by an input/output (IO) supply voltage, a supply detector cell detects a core supply voltage and generates a supply detect signal. A driver circuit is connected to a PAD and receives the supply detect signal. A failsafe circuit receives a PAD voltage. The failsafe circuit and the supply detector cell control a leakage current from the PAD based on the IO supply voltage and the PAD voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1 is a block diagram of a supply detector cell.

[0005] FIG. 2 is a schematic of a supply detector cell.

[0006] FIG. 3(a) an example graph of operation of the supply detector cell under different operating conditions.

[0007] FIG. 3(b) an example graph of leakage current in the supply detector cell under different operating conditions.

[0008] FIG. 4 is a block diagram of a driver circuit coupled to a PAD.

[0009] FIG. 5 is a schematic of an input/output (IO) circuit.

[0010] FIG. 6(a) is an example graph of the response of a control signal (Noff) to the IO supply voltage.

[0011] FIG. 6(b) is an example graph of the leakage current (conduction current) from the PAD.

[0012] FIG. 7(a) is a block diagram of an input/output (IO) circuit.

[0013] FIG. 7(b) is a schematic of an input/output (IO) circuit.

[0014] FIG. 8(a) is an example graph of the response of a control signal (Noff) to the IO supply voltage.

[0015] FIG. 8(b) is an example graph of the leakage current (conduction current) from the PAD.

[0016] FIG. 9 is a block diagram of a computing device.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0017] FIG. 1 is a block diagram of a supply detector cell 100. The supply detector cell 100 is powered by an input/output (IO) supply voltage (VDDS) 102 and receives a core supply voltage (VDD) 104 as an input signal. A diode connected transistor 106 is powered by the IO supply voltage (VDDS) 102. In at least one example, the diode connected transistor 106 is an NMOS transistor or a PMOS transistor. An input inverter stage 108 is coupled to the diode connected transistor 106. The input inverter stage 108 receives the core supply voltage (VDD) 104. A second inverter stage 110 receives an output of the input inverter stage 108 and is powered by the IO supply voltage (VDDS) 102. A pair of weak keeper transistors 112 is coupled to an output of the second inverter stage 110. The weak keeper transistors 112 are connected in series and powered by the IO supply voltage (VDDS) 102. An output of the pair of weak keeper transistors 112 is provided as input to the second inverter stage 110, which is also the output of the input inverter stage 108. An output inverter stage 114 is coupled to the second inverter stage 110 and generates a supply detect signal 116. The output inverter stage 114 is powered by the IO supply voltage (VDDS) 102.

[0018] The supply detector cell 100 is configured to detect the core supply voltage (VDD) 104 and generate the supply detect signal 116. When the core supply voltage (VDD) 104 is in OFF state,

and IO supply voltage (VDDS) 102 is ramping up, the diode connected transistor 106 is turned ON. Accordingly, the output of the input inverter stage 108 is (IO supply voltage (VDDS)-Vtn). Vtn is a threshold voltage of diode connected transistor 106. The output of the input inverter stage 108 (IO supply voltage (VDDS)-Vtn), which is a weak logic-HIGH, is inverted by the second inverter stage 110. Accordingly, the output of the second inverter stage 110 becomes weak logic-LOW. In response to receiving this weak logic-LOW signal, the pair of weak keeper transistors 112 pull the output of the input inverter stage 108 to an IO supply voltage (VDDS) level from (VDDS -Vtn). This provides for zero static leakage current in the second inverter stage 110, because a logic-HIGH signal is now provided to the second inverter stage 110. This logic-HIGH signal received at the second inverter stage 110 results in a logic-LOW signal at the output of the second inverter stage 110. The logic-LOW signal output of the second inverter stage 110 is provided as input to the output inverter stage 114, which results in a logic-HIGH supply detect signal 116. Accordingly, the output inverter stage 114 buffers the output of the input inverter stage 108.

[0019] FIG. 2 is a schematic of a supply detector cell 200. The supply detector cell 200 is similar in connections and operation to supply detector cell 100. The supply detector cell 200 is powered by an input/output (IO) supply voltage (VDDS) 202 and receives a core supply voltage (VDD) 204. A diode connected NMOS transistor 206 is powered by the IO supply voltage (VDDS) 202. The diode connected NMOS transistor 206 includes a gate terminal 206G and a drain terminal 206D connected to the IO supply voltage (VDDS) 202. In one embodiment, the diode connected NMOS transistor 206 is a PMOS transistor. An input inverter stage 208 is coupled to the diode connected NMOS transistor 206. The input inverter stage 208 includes a PMOS transistor 208a and two NMOS transistors 208b and 208c connected in series. Gate terminals 208aG, 208bG and 208cG of the three transistors 208a, 208b and 208c respectively receive the core supply voltage (VDD) 204. Drain terminals 208aD and 208bD of the respective transistors 208 a and 208b are combined to generate an output of the input inverter stage 208. A second inverter stage 210 receives the output of the input inverter stage 208. The second inverter stage 210 includes a PMOS transistor 210a and an NMOS transistor 210b. A source terminal 210aS of the PMOS transistor 210a receives the IO supply voltage (VDDS) 202. Gate terminals 210aG and 210bG receive the output of the input inverter stage 208. Drain terminals 210aD and 210bD of the transistors 210a and 210b respectively are combined to generate an output of the second inverter stage 210. A pair of weak keeper transistors 212 is coupled to the output of the second inverter stage 210. The weak keeper transistors include a top

PMOS transistor 212a and a bottom PMOS transistor 212b connected in series. Gate terminals 212aG and 212bG of the top PMOS transistor 212a and the bottom PMOS transistor 212b respectively are combined together to receive the output of the second inverter stage 210. A source terminal 212aS of the top PMOS transistor 212a is coupled to the IO supply voltage (VDDS) 202, and a drain terminal 212bD of the bottom PMOS transistor 212b is coupled to the output of the input inverter stage 208, which is also the input to the second inverter stage 210. An output inverter stage 214 is coupled to the second inverter stage 210 and generates a supply detect signal 216. The output inverter stage 214 includes a PMOS transistor 214a and an NMOS transistor 214b. A source terminal 214aS of the PMOS transistor 214a is connected to the IO supply voltage (VDDS) 202. Gate terminals 214aG and 214bG receive the output of the second inverter stage 210. Drain terminals 214aD and 214bD of the transistors 214a and 214b respectively are combined to generate the supply detect signal 216. Source terminals 208cS, 210bS and 214bS of the transistors 208c, 210b and 214b are connected to a ground terminal. Also, the PMOS transistors 208a, 210a and 214a receive the IO supply voltage (VDDS) 202 at a substrate. In one embodiment, an inverter stage in supply detector cell 200 is replaced by any inverter.

[0020] The supply detector cell 200 is configured to detect the core supply voltage (VDD) 204 and generate the supply detect signal 216. When the core supply voltage (VDD) 204 is in OFF state, the NMOS transistors 208b and 208c are in OFF state. When the IO supply voltage (VDDS) 202 starts ramping and becomes more than a threshold voltage (Vtn) of the diode connected NMOS transistor 206, the diode connected NMOS transistor 206 is turned ON. Accordingly, the output of the input inverter stage 208 is (VDDS -Vtn). The voltage of (VDDS - Vtn), which is a weak logic-HIGH, is inverted by the second inverter stage 210 whose output becomes weak logic-LOW. In response to receiving this weak logic-LOW signal, the pair of weak keeper transistors 212 pulls the output of the input inverter stage 208 to an IO supply voltage (VDDS) level from (VDDS-Vtn). This provides for zero static leakage current in the second inverter stage 210, because a logic-HIGH signal is provided to the second inverter stage 210. The logic-HIGH signal received at the second inverter stage 210 results in a logic-LOW signal at an output of the second inverter stage 210. The logic-LOW signal output of the second inverter stage 210 is provided as input to the output inverter stage 214, which results in a logic-HIGH supply detect signal 216. Accordingly, the output inverter stage 214 buffers the output of the input inverter stage 208. The supply detector cell 200 provides a logic-HIGH supply detect signal 216 when the core supply voltage (VDD) 204 is in OFF state. The

logic-HIGH supply detect signal is suitable to tristate associated input/output circuits. Advantageously, when the IO supply voltage (VDDS) 202 ramps up, the supply detect signal 216 also ramps up with IO supply voltage (VDDS) 202. Moreover, the supply detector cell 200 generates zero static current from the IO supply voltage (VDDS) 202 at all values of core supply voltage (VDD) 204.

[0021] In a state when IO supply voltage (VDDS) 202 is stable, and core supply voltage (VDD) ramps up, the NMOS transistors 208b and 208c are turned ON, thereby pulling the output of the input inverter stage 208 to a logic-LOW. The supply detect signal 216 is also pulled to a logic-LOW. In this condition, the PMOS transistor 208a will be in OFF stage if the source-gate voltage (Vsg) of the PMOS transistor 208a is less than a threshold voltage (Vtp) of the PMOS transistor 208a.

$$Vsg = VDDS - Vtn - \text{Core supply voltage} < Vtp \qquad (1)$$

So long as the condition of equation (1) is met across process, voltage and temperature combinations, it results in a zero static current consumption in the supply detector cell 200. Accordingly, the supply detector cell 200 is applicable across multiple IO circuits, operating conditions and different ranges of core supply voltage (VDD) that satisfy (1). This is further shown with reference to FIGS. 3(a) and 3(b).

[0022] FIG. 3(a) is an example graph of the operation of the supply detector. FIG. 3(a) shows the core-supply values at which the supply detect signal switches to logic-HIGH and logic-LOW, when core-supply powers down and powers-up respectively. These core-supply voltage values (Y-axis) are plotted under different operating conditions (X-axis).

[0023] FIG. 3(b) is an example graph of the zero-static current behavior of the supply detector at different states of the core supply voltage (VDD) and IO supply voltage (VDDS). The leakage current through the IO supply voltage (VDDS) is plotted under different operating conditions. The maximum IO supply leakage current is 224nA at core supply voltage (VDD) value of 1.1V, IO supply voltage (VDDS) value of 1.98V, and temperature of 125C.

[0024] FIG. 4 is a block diagram of a driver circuit 400 coupled to a PAD 422. The driver circuit 400 is powered by an IO (input/output) supply voltage (VDDS) 402. The driver circuit 400 includes a pair of level shifter circuits 406 and 408. The level shifter circuit 406 receives an input signal A, and the level shifter circuit 408 receives a tristate signal GZ, as respective inputs. Also, the pair of level shifter circuits 406 and 408 receives the core supply voltage (VDD) 404 and the IO supply voltage (VDDS) 402. Moreover, the driver circuit 400 includes a pair of predriver logic circuits 410

and 412. Each predriver logic circuit is coupled to an output of the level shifter circuit, so the predriver logic circuit 410 is coupled to an output of level shifter circuit 406, and the predriver logic circuit 412 is coupled to an output of level shifter circuit 408. The pair of predriver logic circuits 410 and 412 is powered by IO supply voltage (VDDS) 402. A pair of gating circuits 414 and 416 is coupled to the pair of predriver logic circuits 410 and 412 respectively. The gating circuit 414 is coupled to an output of predriver logic circuit 410, and the gating circuit 416 is coupled to an output of predriver logic circuit 412. The pair of gating circuits 414 and 416 receives a control signal (Noff) 415 from a failsafe circuit (not shown in FIG. 4). The gating circuit 414 also receives the IO supply voltage (VDDS) 402 and a substrate signal (X) 419 from the failsafe circuit. A final driver circuit 417 is coupled to the pair of gating circuits 414 and 416. The final driver circuit 417 includes a final driver PMOS transistor 418 and a final driver NMOS transistor 420. The final driver PMOS transistor 418 is powered by the IO supply voltage (VDDS) 402 and receives a substrate signal (X) 419 from the failsafe circuit (not shown in FIG. 4). The PAD 422 is coupled to the final driver circuit 417. The pair of level shifter circuits 406 and 408, the pair of predriver logic circuits 410 and 412, the gating circuit 416 and the final driver NMOS transistor 420 are also connected to a ground terminal. The operation of the driver circuit 400 is described in connection with FIG. 5.

[0025] FIG. 5 is a schematic of an input/output (IO) circuit 500. The IO circuit 500 includes a driver circuit 505, a PAD 522 and a failsafe circuit 525. The driver circuit 505 is similar in connections and operation to the driver circuit 400. The driver circuit 500 is powered by an IO (input/output) supply 502. The driver circuit 500 includes a pair of level shifter circuits 506 and 508. The level shifter circuit 506 receives an input signal A, and the level shifter circuit 508 receives a tristate signal GZ. Also, the level shifter circuits 506 and 508 receive the core supply voltage (VDD) 504 and the IO supply voltage (VDDS) 502. Moreover, the driver circuit 500 includes a pair of predriver logic circuits 510 and 512. Each predriver logic circuit is coupled to an output of the level shifter circuit, so the predriver logic circuit 510 is coupled to an output of the level shifter circuit 506, and the predriver logic circuit 512 is coupled to an output of the level shifter circuit 508. The pair of predriver logic circuits 510 and 512 is powered by IO supply voltage (VDDS) 502.

[0026] A pair of gating circuits 514 and 516 is coupled to the pair of predriver logic circuits 510 and 512 respectively. The gating circuit 514 is coupled to an output of the predriver logic circuit 510, and the gating circuit 516 is coupled to an output of the predriver logic circuit 512. The gating circuit 514 includes two PMOS transistors 514a and 514b and an NMOS transistor 514c. The

PMOS transistor 514a receives a control signal (Noff) 515 at a gate terminal and a substrate signal (X) 538 at a body terminal from the failsafe circuit 525. The PMOS transistor 514b receives the IO supply voltage (VDDS) 502 at a gate terminal and the substrate signal (X) 538 at a body terminal. The NMOS transistor 514c receives an inverted control signal (Noffz) 515X at a gate terminal. The gating circuit 516 includes an NMOS transistor 516a. The NMOS transistor 516a receives the control signal (Noff) 515 at a gate terminal from the failsafe circuit 525, and its source terminal is connected to ground. A final driver circuit 517 is coupled to the pair of gating circuits 514 and 516. The final driver circuit 517 includes a final driver PMOS transistor 518 and a final driver NMOS transistor 520. The final driver PMOS transistor 518 receives the IO supply voltage (VDDS) 502 at a source terminal and receives the substrate signal (X) 538 at a body terminal. An output of the gating circuit 514 is connected to a gate terminal of the final driver PMOS transistor 518. A gate terminal of the final driver NMOS transistor 520 is connected to an output the gating circuit 516. The source terminal of the final driver NMOS transistor 520 is connected to ground terminal. The PAD 522 is coupled to the final driver circuit 517.

[0027] The failsafe circuit 525 generates the control signal (Noff) 515 and the substrate signal (X) 538. The failsafe circuit 525 includes a first PMOS transistor 526, a second PMOS transistor 528 and an inverting stage 535. A source terminal of the first PMOS transistor 526 is connected to the IO supply voltage (VDDS) 502. A drain terminal of the second PMOS transistor 528 is connected to the PAD 522, and a gate terminal of the second PMOS transistor 528 is connected to the IO supply voltage (VDDS) 502. A source terminal of the second PMOS transistor 528, the drain terminal of the first PMOS transistor 526, body terminal of the first PMOS transistor 526, and the body terminal of second PMOS transistor 528 are combined together to generate the substrate signal (X) 538. The inverting stage 535 of the failsafe circuit 525 includes a third PMOS transistor 530, a first NMOS transistor 532, a second NMOS transistor 534 and a third NMOS transistor 536. The first NMOS transistor 532, the second NMOS transistor 534 and the third NMOS transistor 536 are connected in cascode arrangement. Gate terminals of the third PMOS transistor 530, the first NMOS transistor 532, the second NMOS transistor 534 and the third NMOS transistor 536 are configured to receive the IO supply voltage (VDDS) 502. A source terminal of the third PMOS transistor 530 is connected to the PAD 522. A drain terminal of the first NMOS transistor 532 is connected to a drain terminal of the third PMOS transistor 530 to generate the control signal (Noff) 515. A source terminal of a third NMOS transistor 536 is connected to ground.

[0028] The pair of level shifter circuits 506 and 508 translates a signal from a core supply voltage (VDD) level to an IO supply voltage (VDDS) level, because the IO circuit (the pair of predriver logic circuits 510 and 512, final driver circuit 517 and the failsafe circuit 525) operates with IO supply voltage (VDDS) 502. The pair of predriver logic circuits 510 and 512 implement a logic based on the level-shifted versions of the input signal A and the tristate signal GZ. The final driver PMOS transistor 518 and the final driver NMOS transistor 520 are controlled by output of the pair of predriver logic circuits 510 and 512. The predriver logic circuits 510 and 512 implement the following truth table:

GZ	A	PAD
0	0	0
0	1	1
1	0	High-Impedance
1	1	High-Impedance

where 'High-Impedance' state is achieved when both final driver PMOS transistor 518 and final driver NMOS transistor 520 are in OFF state.

[0029] In one of the operating modes, the PAD 522 is at logic-HIGH, IO supply voltage (VDDS) is powered down, and the final driver PMOS transistor 518 and the final driver NMOS transistor 520 are not turned OFF, which results in leakage currents (conduction currents) from the PAD 522 to either: the IO supply voltage (VDDS) 502 through the final driver PMOS transistor 518; or the ground terminal through the final driver NMOS transistor 520. The failsafe circuit 525 avoids this operating mode by correctly turning OFF the final driver PMOS transistor 518 and final driver NMOS transistor 520. The failsafe circuit 525 generates the control signal (Noff) 515 to turn OFF final driver PMOS transistor 518 and final driver NMOS transistor 520. The failsafe circuit 525 is powered by a PAD voltage and receives the IO supply voltage (VDDS) 502. The PAD voltage is the voltage at the PAD 522. When no IO supply voltage (VDDS) 502 exists, and the PAD voltage is at logic-HIGH, the PMOS transistor 530 turns ON and passes the logic-HIGH voltage on the PAD 522 to the control signal (NOFF) signal 515. Also, the PMOS transistor 528 turns ON and pulls up the substrate signal (X) 538 to logic-HIGH. As the control signal (NOFF) 515 is at logic-HIGH, the PMOS 526 is turned OFF. The logic-HIGH control signal (Noff) 515 turns OFF the final driver NMOS transistor 520 by pulling the gate terminal of the NMOS 520 to ground. The PMOS transistor 514a and the NMOS transistor 514c are also turned OFF by the logic-HIGH control

signal (Noff) 515 and the logic-LOW inverted control signal(NoffZ) 515X respectively, thereby cutting off the output of the predriver logic circuit 510 from the final driver PMOS transistor 518. As the PAD voltage is at logic-HIGH, the gate terminal of the final driver PMOS transistor 518 is pulled up to logic-HIGH by the PMOS 514b, which is turned ON due to IO supply voltage (VDDS) 502 at its gate terminal and PAD voltage at its drain, thereby avoiding any leakage current (conduction current) from the PAD 522 to the IO supply voltage (VDDS) 502 through the final driver PMOS transistor 518. Also, because the substrate signal (X) 538 is pulled to logic-HIGH, it avoids forward-biasing the internal pn-junction of the final driver PMOS 518. The failsafe circuit 525 is effective when the IO supply voltage (VDDS) 502 is below a trip-point voltage. In at least one version, this trip-point voltage is dependent on a threshold voltage of the transistors in the inverting stage 535 in the failsafe circuit 525. For example, the trip-point voltage is selectable by designing the relative widths of the PMOS transistor 530 and the cascoded NMOS transistors 532, 534 and 536 in the failsafe circuit 525. The extent of skewing the ratio of widths of the PMOS transistor 530 and the cascoded NMOS transistors 532, 534 and 536 determines the trip-point voltage during IO supply voltage (VDDS) 502 ramp-up, when NOFF trips from logic-HIGH to logic-LOW. If PAD 522 is at logic-HIGH, and the IO supply voltage (VDDS) 502 is above the trip-point voltage, then the control signal (Noff) 515 is turned OFF, so the final driver PMOS transistor 518 and final driver NMOS transistor 520 are not turned OFF. This causes leakage currents (conduction currents) from the PAD 522 to the IO supply voltage (VDDS) 502 or to the ground terminal. This is further shown with reference to FIG. 6(a) and FIG. 6(b).

[0030] FIG. 6(a) is an example graph of the response of a control signal (Noff) 515 to the IO supply voltage (VDDS) 502. As shown in FIG. 6(a), the control signal (Noff) 515 remains constant when IO supply voltage (VDDS) 502 increases as a ramp function from 0 volt to 1.98 volt. However, when the IO supply voltage (VDDS) 502 exceeds the trip-point voltage, which is 1.25 volt in the example graph, the control signal (Noff) 515 is turned OFF.

[0031] FIG. 6(b) is an example graph of the conduction (leakage) current from the PAD 522 to the IO supply voltage (VDDS) 502 when the IO supply voltage (VDDS) 502 exceeds the trip-point voltage while PAD 522 is at logic-HIGH. The graph shows a huge spike in leakage current (conduction current) (about 20mA) from the pad at the trip-point voltage.

[0032] As shown in FIGS. 7(a) and 7(b), an input/output (IO) circuit 700 includes a driver circuit 705, a PAD 722, a failsafe circuit 725 and a supply detector cell 750. The driver circuit 705 is

similar in connections and operation to driver circuit 500. The failsafe circuit 725 is similar in connections and operation to the failsafe circuit 525. The supply detector cell 750 is similar in connections and operation to the supply detector cell 100.

[0033] The supply detector cell 750 is powered by an input/output (IO) supply 702 and receives a core supply voltage (VDD) 704 as an input signal. A diode connected transistor 756 is powered by the IO supply voltage (VDDS) 702. In at least one example, the diode connected transistor 756 is an NMOS transistor or a PMOS transistor. An input inverter stage 758 is coupled to the diode connected transistor 756. The input inverter stage 758 receives the core supply voltage (VDD) 704. The second inverter stage 760 receives an output of the input inverter stage 758 and is powered by the IO supply voltage (VDDS) 702. A pair of weak keeper transistors 762 is coupled to an output of the second inverter stage 760. The transistors 762 are connected in series and powered by the IO supply voltage (VDDS) 702. An output of the pair of weak keeper transistors 762 is provided as input to the second inverter stage 760, which is also the output of the input inverter stage 758. An output inverter stage 764 is coupled to the second inverter stage 760 and generates a supply detect signal 766. The output inverter stage 764 is powered by the IO supply voltage (VDDS) 702.

[0034] The driver circuit 705 is powered by an IO (input/output) supply 702. The driver circuit 700 includes a pair of level shifter circuits 706 and 708. The level shifter circuit 706 receives an input signal A, and the level shifter circuit 708 receives a tristate signal GZ. The level shifter circuits 706 and 708 receive the supply detect signal 766 from the supply detector cell 750. Also, the level shifter circuits 706 and 708 receive the core supply voltage (VDD) 704 and the IO supply voltage (VDDS) 702. Moreover, the driver circuit 700 includes a pair of predriver logic circuits 710 and 712. Each predriver logic circuit is coupled to an output of the level shifter circuit, so the predriver logic circuit 710 is coupled to an output of the level shifter circuit 706, and the predriver logic circuit 712 is coupled to an output of the level shifter circuit 708. The pair of predriver logic circuits 710 and 712 is powered by IO supply voltage (VDDS) 702.

[0035] A pair of gating circuits 714 and 716 is coupled to the pair of predriver logic circuits 710 and 712 respectively. The gating circuit 714 is coupled to an output of the predriver logic circuit 710, and the gating circuit 716 is coupled to an output of the predriver logic circuit 712. The gating circuit 714 includes two PMOS transistors 714a and 714b and an NMOS transistor 714c. The PMOS transistor 714a receives a control signal (Noff) 715 at a gate terminal and a substrate signal (X) 738 at a body terminal from the failsafe circuit 725. The PMOS transistor 714b receives the IO

supply voltage (VDDS) 702 at a gate terminal and the substrate signal (X) 738 at a body terminal. The NMOS transistor 714c receives an inverted control signal (Noffz) 715X at a gate terminal. The gating circuit 716 includes an NMOS transistor 716a. The NMOS transistor 716a receives the control signal (Noff) 715 at a gate terminal from the failsafe circuit 725, and its source terminal is connected to ground. A final driver circuit 717 is coupled to the pair of gating circuits 714 and 716. The final driver circuit 715 includes a final driver PMOS transistor 718 and a final driver NMOS transistor 720. The final driver PMOS transistor 718 receives the IO supply voltage (VDDS) 702 at a source terminal and receives the substrate signal (X) 738 at a body terminal. An output of the gating circuit 714 is connected to a gate terminal of the final driver PMOS transistor 718. A gate terminal of the final driver NMOS transistor 720 is connected to an output of the gating circuit 716. The source terminal of the final driver NMOS transistor 720 is connected to ground terminal. The PAD 722 is coupled to the final driver circuit 715. The pair of level shifter circuits 706 and 708 and the pair of predriver logic circuits 710 and 712 are also connected to the ground terminal.

[0036] The failsafe circuit 725 generates the control signal (Noff) 715 and the substrate signal (X) 738. The failsafe circuit 725 includes a first PMOS transistor 726, a second PMOS transistor 728 and an inverting stage 735. The source terminal of the first PMOS transistor 726 is configured to receive the IO supply voltage (VDDS) 702. A drain terminal of the second PMOS transistor 728 is connected to the PAD 722, and a gate terminal of the second PMOS transistor 728 is connected to the IO supply voltage (VDDS) 702. A source terminal of the second PMOS transistor 728, the drain terminal of the first PMOS transistor 726, body terminal of the first PMOS transistor 726, and the body terminal of second PMOS transistor 728 are combined together to generate the substrate signal (X) 738. The inverting stage 735 of the failsafe circuit 725 includes a third PMOS transistor 730, a first NMOS transistor 732, a second NMOS transistor 734 and a third NMOS transistor 736. The first NMOS transistor 732, the second NMOS transistor 734 and the third NMOS transistor 736 are connected in cascode arrangement. Gate terminals of the third PMOS transistor 730, the first NMOS transistor 732, the second NMOS transistor 734 and the third NMOS transistor 736 are configured to receive the IO supply voltage (VDDS) 702. A source terminal of the third PMOS transistor 730 is connected to the PAD 722. A drain terminal of the first NMOS transistor 732 is connected to a drain terminal of the third PMOS transistor 730 to generate the control signal (Noff) 715. A source terminal of a third NMOS transistor 736 is connected to ground.

[0037] The supply detector cell 750 is configured to detect the core supply voltage (VDD) 704 and generate the supply detect signal 766. The pair of level shifter circuits 706 and 708 translates a signal from a core supply voltage (VDD) level to an IO supply voltage (VDDS) level, because the IO circuit (the pair of predriver logic circuits 710 and 712, final driver circuit 717 and the failsafe circuit 725) operates with IO supply voltage (VDDS) 702. The supply detect signal 766 is also received as an input to the pair of level-shifter circuits 706 and 708. The pair of predriver logic circuits 710 and 712 implement a logic based on the level-shifted versions of the input signal A and the tristate signal GZ. The input signal A and the tristate signal GZ are modified based on the supply-detect signal 766 received by the pair of level shifters circuits 706 and 708. The final driver PMOS transistor 718 and the final driver NMOS transistor 720 are controlled by output of the pair of predriver logic circuits 710 and 712. If core supply voltage (VDD) is in OFF state, then the supply detect signal 766 is in logic-HIGH state. In this case, outputs of the pair of level shifter circuits 706 and 708 are logic-HIGH, which turns OFF both the final driver PMOS transistor 718 and final driver NMOS transistor 720.

[0038] For the failsafe IO, in one of the operating modes, the PAD 722 is at logic-HIGH, IO supply voltage (VDDS) 702 is powered down, and the final driver PMOS transistor 718 and final driver NMOS transistor 720 are not turned OFF, which results in leakage currents (conduction currents) from the PAD 722 to either: the IO supply voltage (VDDS) 702 through the final driver PMOS transistor 718; or the ground terminal through the final driver NMOS transistor 720. The failsafe circuit 725 avoids this operating mode by correctly turning OFF the final driver PMOS transistor 718 and final driver NMOS transistor 720. The failsafe circuit 725 generates the control signal (Noff) 715 to turn OFF final driver PMOS transistor 718 and final driver NMOS transistor 720. The failsafe circuit 725 receives a PAD voltage and the IO supply voltage (VDDS) 702. The PAD voltage is the voltage at the PAD 722. When no IO supply voltage (VDDS) 702 exists, and the PAD voltage is at logic-HIGH, the PMOS transistor 730 turns ON and passes the logic-HIGH voltage on the PAD 722 to the control signal (Noff) 715. Also, the PMOS 728 turns ON and pulls up the substrate signal (X) 738 to logic-HIGH. As the control signal (NOFF) 715 is at logic-HIGH, the PMOS 526 is turned OFF. The logic-HIGH control signal (Noff) 715 turns OFF the final driver NMOS transistor 720 by pulling the gate terminal of the NMOS 720. The PMOS transistor 714a and the NMOS transistor 714c are also turned OFF by the logic-HIGH control signal (Noff) 715 and the logic-LOW inverted control signal(NoffZ) 715X respectively, thereby cutting off the output of the

predriver logic circuit 710 from the final driver PMOS transistor 718. As the PAD voltage is at logic-HIGH, the gate terminal of the final driver PMOS transistor 718 is pulled up to logic-HIGH by the PMOS 714b, which is turned ON due to IO supply voltage (VDDS) 702 at its gate terminal and PAD voltage at its drain, thereby avoiding any leakage current (conduction current) from the PAD 722 to the IO supply voltage (VDDS) 702 through the final driver PMOS transistor 718. Also, because the substrate signal (X) 738 is pulled to logic-HIGH, it avoids forward-biasing the internal pn-junction of the final driver PMOS 718. The failsafe circuit 725 is effective when the IO supply voltage (VDDS) 702 is below a trip-point voltage. In at least one version, the trip-point voltage is dependent on a threshold voltage of the transistors in the inverting stage 735 in the failsafe circuit 725. For example, the trip-point voltage is selectable by designing the relative widths of the PMOS transistor 730 and the cascoded NMOS transistors 732, 734 and 736 in the failsafe circuit 725. The extent of skewing the ratio of widths of the PMOS transistor 730 and the cascoded NMOS transistors 732, 734 and 736 determines the trip-point voltage during IO supply voltage (VDDS) ramp-up, when NOFF trips from logic-HIGH to logic-LOW. Accordingly, the failsafe circuit 725 controls the leakage current (conduction current) through deactivation of the final driver circuit 715, when the PAD 722 is at logic-HIGH, and the IO supply voltage (VDDS) 704 is below the trip-point voltage. However, if the core supply voltage (VDD) 704 is in OFF state, the PAD 722 is at logic-HIGH, and the IO supply voltage (VDDS) 702 is above the trip-point voltage, then the control signal (Noff) 715 is turned OFF. Accordingly, the final driver PMOS transistor 718 and final driver NMOS transistor 720 would be incorrectly gated, resulting in leakage currents. This state is avoided by the supply detector cell 750.

[0039] When the core supply voltage (VDD) 704 is in OFF state, and IO supply voltage (VDDS) 702 is ramping up, the diode connected transistor 756 is turned ON. Accordingly, the output of the input inverter stage 758 is (VDDS-Vtn). Vtn is a threshold voltage of diode connected transistor 756. The output of the input inverter stage 758 (IO supply voltage (VDDS)-Vtn), which is a weak logic-High, is inverted by the second inverter stage 760. Accordingly, the output of second inverter stage 760 becomes weak logic-LOW. In response to receiving this weak logic-LOW signal, the pair of weak keeper transistors 762 pull the output of the input inverter stage 758 to the IO supply voltage (VDDS) level from (VDDS-Vtn). This provides for zero static leakage current in the second inverter stage 760, because a logic-HIGH signal is provided to the second inverter stage 760. The logic-HIGH signal received at the second inverter stage 760 results in a logic-LOW signal at an

output of the second inverter stage 760. The logic-LOW signal output of the second inverter stage 760 is provided as input to the output inverter stage 764, which results in a logic-HIGH supply detect signal 766. Accordingly, the output inverter stage 764 buffers the output of the input inverter stage 758. A logic-HIGH supply detect signal 766 is provided to the pair of level shifter circuits 706 and 708. The outputs of the pair of level shifter circuits 706 and 708 become logic-HIGH, which drives the outputs of the pair of predriver logic circuits 710 and 712 to logic-HIGH and logic-LOW respectively, thereby turning OFF both the final driver PMOS transistor 718 and final driver NMOS transistor 720 using predriver logic ciruits710 and 712. Accordingly, when core supply voltage (VDD) 704 is in OFF state, the supply detector cell 750 turns OFF or deactivates the final driver circuit 717 when the IO supply voltage (VDDS) 702 is above the trip-point voltage. The IO circuit 700 provides very low leakage current from the PAD 722 when the core supply voltage (VDD) is in OFF state and the IO supply voltage (VDDS) 702 is above the trip-point, even when PAD is at logic-HIGH. This method of choosing the trip-point by skewing relative widths of the PMOS transistor 730 and the NMOS transistors 732, 734, 734 is used in controlling the maximum PAD current/pin-current. During power-down sequencing, when IO supply voltage (VDDS) 702 ramps-down, before the trip-point, the supply detector disables the final driver circuit 717 while core-supply is LOW. Below the trip-point voltage, the failsafe circuit 725 and gating circuits 714 and 716 disable (by tristate) the final driver. The IO circuit 700 provides ultra low PAD current (pin current) during powering up or powering down of a failsafe IO interface (such as the SLIMbus interface), thereby achieving true fail safe compliance.

[0040] FIG. 8(a) is an example graph of the response of a control signal (Noff) 715 to the IO supply voltage (VDDS) 702. As shown in FIG. 8(a), the control signal (Noff) 715 remains constant when IO supply voltage (VDDS) 702 increases as a ramp function from 0 volt to 1.25 volt. However, when the IO supply voltage (VDDS) 702 exceeds the trip-point voltage, which is 1.25 volt in the example graph, the control signal (Noff) 715 is turned OFF.

[0041] FIG. 8(b) is an example graph of the leakage current from the PAD 722 to the IO supply voltage (VDDS) 702 when the IO supply voltage (VDDS) 702 exceeds the trip-point voltage. The graph shows that leakage current from the PAD 722 to IO supply voltage (VDDS) 702 is negligible, because the supply detector cell 750 deactivates the final driver circuit 717 when the PAD voltage is at logic-HIGH while the IO supply voltage (VDDS) is above the trip-point voltage.

[0042] FIG. 9 is a block diagram of a computing device 900. The computing device 900 is (or is an integrated circuit incorporated into) a mobile communication device, such as a mobile phone, a personal digital assistant, a personal computer, or any other type of electronic system.

[0043] In some embodiments, the computing device 900 is one of, but not limited to, a microcontroller, microprocessor or system-on-chip (SoC), which includes a processing unit 912 such as a CPU (central processing unit), a memory unit 914 (such as random access memory (RAM)), and a tester 910. The processing unit 912 can be, for example, a CISC-type (complex instruction set computer) CPU, RISC-type CPU (reduced instruction set computer), or a digital signal processor (DSP). The memory module 914 (which can be memory, such as RAM, flash memory, or disk storage) stores one or more software applications 930 (such as embedded applications) that, when executed by the processing unit 912, perform any suitable function associated with the computing device 900. The tester 910 includes logic that supports testing and debugging of the computing device 900 executing the software application 930. For example, the tester 910 is suitable for emulating a defective or unavailable component(s) of the computing device 900 to allow verification of how the component(s), if actually existing on the computing device 900, would perform in various situations (such as how the component(s) would interact with the software application 930). In this way, the software application 930 can be debugged in an environment that resembles post-production operation.

[0044] The processing unit 912 includes cache-memory and logic, which store and use information frequently accessed from the memory module 914, and which are responsible for operation of the computing device. The computing device 900 includes logic circuits 915 coupled to the processing unit 912 and the memory module 914. An IO circuit 916 is coupled to at least one logic circuit of the logic circuits 915. The IO circuit 916 operates as an interface between the computing device 900 and the external world. The IO circuit 916 is analogous to the IO circuit 700 in connection and operation. The IO circuit 916 has low leakage current from the PAD during power-up sequence, during power-down sequence, and during stable powered up states, because it uses: the failsafe circuitry mechanism when the IO supply voltage (VDDS) is below the trip-point voltage; and the core-supply detection mechanism when the IO supply voltage (VDDS) is above the trip-point voltage.

[0045] In the foregoing discussion, the term "logic-HIGH" refers to a signal that is at logic state "1," and the term "logic-LOW" refers to a signal that is at logic state "0." Also, the terms “OFF

state" or turn "OFF" or turned "OFF" refer to deactivation of a device, a component or a signal. The term turned "ON" refer to activation of a device, a component or a signal.

[0046] Accordingly, in at least one version of an input/output (IO) circuit powered by an input/output (IO) supply voltage, a supply detector cell that detects a core supply voltage. Also, the IO circuit includes a pair of level shifter circuits. Each level shifter circuit receives an output of the supply detector cell and translates the output of supply detector cell from a core supply voltage level to an IO supply voltage level. The IO circuit includes a pair of predriver logic circuits. Each predriver logic circuit is connected to an output of a level shifter circuit. The IO circuit includes a pair of gating circuits and each gating circuit is connected to an output of a predriver logic circuit. The IO circuit includes a failsafe circuit that receives a PAD voltage. The failsafe circuit and the supply detector cell control a leakage current from the PAD based on the IO supply voltage and the PAD voltage.

[0047] Another example embodiment provides a method of controlling current through a PAD. The core supply voltage is detected. A failsafe circuit controls a leakage current from a PAD through deactivation of a final driver circuit when the input/output (IO) supply is below a trip-point voltage, and PAD is at logic-HIGH. A supply detector cell, when core supply voltage is in OFF state, controls the leakage current from the PAD through deactivation of the final driver circuit when the IO supply voltage is above a trip-point voltage, and PAD is at logic-HIGH.

[0048] An example embodiment provides a computing device that includes a processing unit and a memory module coupled to the processing unit. Logic circuits are coupled to the processing unit and the memory module. An input/output (IO) circuit is coupled to at least one logic circuit of the logic circuits. The IO circuit includes a supply detector cell that detects a core supply voltage and generates a supply detect signal. A driver circuit is connected to a PAD and receives the supply detect signal. A failsafe circuit receives a PAD voltage. The failsafe circuit and the supply detector cell control a leakage current from the PAD based on the IO supply voltage and the PAD voltage.

[0049] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. An input/output (IO) circuit powered by an input/output (IO) supply voltage, the IO circuit comprising:

a supply detector cell configured to detect a core supply voltage and generate a supply detect signal;

a driver circuit connected to a PAD and configured to receive the supply detect signal; and

a failsafe circuit configured to receive a PAD voltage, wherein the failsafe circuit and the supply detector cell are configured to control a leakage current from the PAD based on the IO supply voltage and the PAD voltage.

2. The IO circuit of claim 1, wherein the driver circuit includes:

a pair of level shifter circuits, wherein each level shifter circuit is configured to receive the supply detect signal and the core supply voltage and configured to translate the supply detect signal from a core supply voltage level to an IO supply voltage level;

a pair of predriver logic circuits, wherein each predriver logic circuit is connected to an output of a level shifter circuit;

a pair of gating circuits, wherein each gating circuit is connected to an output of a predriver logic circuit; and

a final driver circuit, wherein the failsafe circuit and the pair of predriver logic circuits are configured to drive the pair of gating circuits that deactivates the final driver circuit to control the leakage current from the PAD based on the IO supply voltage and the PAD voltage.

3. The IO circuit of claim 1, wherein the final driver circuit includes a final driver PMOS transistor and a final driver NMOS transistor.

4. The IO circuit of claim 1, wherein the supply detector cell is powered by the IO supply voltage, and the supply detector cell includes:

a diode connected transistor coupled to the IO supply voltage;

an input inverter stage connected to the diode connected transistor and configured to receive the core supply voltage as an input;

a second inverter stage connected to an output of the input inverter stage;

a pair of weak keeper transistors coupled in series, wherein gate terminals of the pair of weak keeper transistors are connected to an output of the second inverter stage, and wherein the pair of

weak keeper transistors is configured to pull the output of the input inverter stage to the IO supply voltage level; and

an output inverter stage coupled to the second inverter stage, wherein the output inverter stage is configured to buffer the output of the input inverter stage and generate a supply detect signal.

5. The IO circuit of claim 4, wherein the diode connected transistor includes one of an NMOS transistor and a PMOS transistor.

6. The IO circuit of claim 4, wherein the diode connected transistor includes a drain terminal and a gate terminal connected to the IO supply voltage.

7. The IO circuit of claim 4, wherein the pair of weak keeper transistors includes a top PMOS transistor and a bottom PMOS transistor connected in series, wherein gate terminals of the top PMOS transistor and the bottom PMOS transistor are configured to receive the output of the second inverter stage, and a source terminal of the top PMOS transistor is connected to the IO supply voltage, and a drain terminal of the bottom PMOS transistor is connected to the output of the input inverter stage.

8. The IO circuit of claim 4, wherein the supply detect signal is configured to change based on the IO supply voltage.

9. The IO circuit of claim 4, wherein the supply detect signal is configured to follow the IO supply voltage when the IO supply voltage is a ramp function, and the core supply voltage is in OFF state.

10. The IO circuit of claim 1, wherein the supply detector cell is configured to control the leakage current from the PAD through deactivation of the final driver circuit when the IO supply voltage is above a trip-point voltage, and the PAD voltage is at logic-HIGH.

11. The IO circuit of claim 1, wherein the failsafe circuit includes:

a first PMOS transistor with a source terminal configured to receive the IO supply voltage;

a second PMOS transistor with a source terminal connected to the PAD, a gate terminal connected to the IO supply voltage, and a drain terminal connected to a drain terminal of the first PMOS transistor to generate a substrate signal, wherein the substrate signal is provided to the final driver PMOS transistor; and

an inverting stage including: a third PMOS transistor with a gate terminal configured to receive the IO supply voltage, and a source terminal connected to the PAD; a first NMOS transistor

with a gate terminal configured to receive the IO supply voltage, and a drain terminal connected to a drain terminal of the third PMOS to generate a control signal, wherein the control signal is provided to the pair of gating circuits; a second NMOS transistor with a gate terminal configured to receive the IO supply voltage; and a third NMOS transistor with a gate terminal configured to receive the IO supply voltage, and a source terminal connected to ground, wherein the first NMOS transistor, the second NMOS transistor and the third NMOS transistor are connected in cascode arrangement.

12. An input/output (IO) circuit powered by an input/output (IO) supply voltage, the IO circuit comprising:

a supply detector cell configured to detect a core supply voltage;

a pair of level shifter circuits, wherein each level shifter circuit is configured to receive an output of the supply detector cell and configured to translate the output of supply detector cell from a core supply voltage level to an IO supply voltage level;

a pair of predriver logic circuits, wherein each predriver logic circuit is connected to an output of a level shifter circuit;

a pair of gating circuits, wherein each gating circuit is connected to an output of a predriver logic circuit; and

a failsafe circuit configured to receive a PAD voltage, wherein the failsafe circuit and the supply detector cell are configured to control a leakage current from the PAD based on the IO supply voltage and the PAD voltage.

13. A method comprising:

detecting a core supply voltage;

configuring a failsafe circuit to control a leakage current from a PAD through deactivation of a final driver circuit when the input/output (IO) supply is below a trip-point voltage, and the PAD is at logic-HIGH; and

configuring a supply detector cell, when core supply voltage is in OFF state, to control the leakage current from the PAD through deactivation of the final driver circuit when the IO supply voltage is above a trip-point voltage, and the PAD is at logic-HIGH.

14. The method of claim 13 further comprising generating in the supply detector cell a supply detect signal that is configured to follow the IO supply voltage when the IO supply voltage is a ramp function and the core supply voltage is in OFF state.

15. The method of claim 13 further comprising generating a zero static current in the supply detector cell at all values of core supply voltage.

16. The method of claim 13 further comprising powering the supply detector cell by the IO supply voltage, wherein the supply detector cell includes: a diode connected transistor coupled to the IO supply voltage; an input inverter stage connected to the diode connected transistor and configured to receive the core supply voltage as an input; a second inverter stage connected to an output of the input inverter stage; a pair of weak keeper transistors coupled in series, wherein gate terminals of the pair of weak keeper transistors are connected to an output of the second inverter stage, and wherein the pair of weak keeper transistors is configured to pull the output of the input inverter stage to the IO supply voltage level; and an output inverter stage coupled to the second inverter stage, wherein the output inverter stage is configured to buffer the output of the input inverter stage and generate a supply detect signal.

17. The method of claim 13, wherein the failsafe circuit includes:

a first PMOS transistor with a source terminal configured to receive the IO supply voltage;

a second PMOS transistor with a source terminal connected to the PAD voltage, a gate terminal connected to the IO supply voltage, and a drain terminal connected to a drain terminal of the first PMOS transistor to generate a substrate signal, wherein the substrate signal is provided to the final driver PMOS transistor; and

an inverting stage, wherein the inverting stage includes: a third PMOS transistor with a gate terminal configured to receive the IO supply voltage, and a source terminal connected to the PAD; a first NMOS transistor with a gate terminal configured to receive the IO supply voltage, and a drain terminal connected to a drain terminal of the third PMOS to generate a control signal, wherein the control signal is provided to the pair of gating circuits; a second NMOS transistor with a gate terminal configured to receive the IO supply voltage; and a third NMOS transistor with a gate terminal configured to receive the IO supply voltage, and a source terminal connected to ground, wherein the first NMOS transistor, the second NMOS transistor and the third NMOS transistor are connected in cascode arrangement.

18. A computing device comprising:

a processing unit;

a memory module coupled to the processing unit;

a plurality of logic circuits coupled to the processing unit and the memory module; and

an input/output (IO) circuit coupled to at least one logic circuit of the plurality of logic circuits, the IO circuit including: a supply detector cell configured to detect a core supply voltage and generate a supply detect signal; a driver circuit connected to a PAD and configured to receive the supply detect signal; and a failsafe circuit configured to receive a PAD voltage, wherein the failsafe circuit and the supply detector cell are configured to control a leakage current from the PAD based on the IO supply voltage and the PAD voltage.

19. The computing device of claim 18, wherein the driver circuit includes:

a pair of level shifter circuits, wherein each level shifter circuit is configured to receive the supply detect signal and the core supply voltage and configured to translate the supply detect signal from a core supply voltage level to an IO supply voltage level;

a pair of predriver logic circuits, wherein each predriver logic circuit is connected to an output of a level shifter circuit;

a pair of gating circuits, wherein each gating circuit is connected to an output of a predriver logic circuit; and

a final driver circuit, wherein the failsafe circuit and the pair of predriver logic circuits are configured to drive the pair of gating circuits that deactivate the final driver circuit to control the leakage current from the PAD based on the IO supply voltage and the PAD voltage.

20. The computing device of claim 18, wherein the supply detector cell is powered by the IO supply voltage, and the supply detector cell includes:

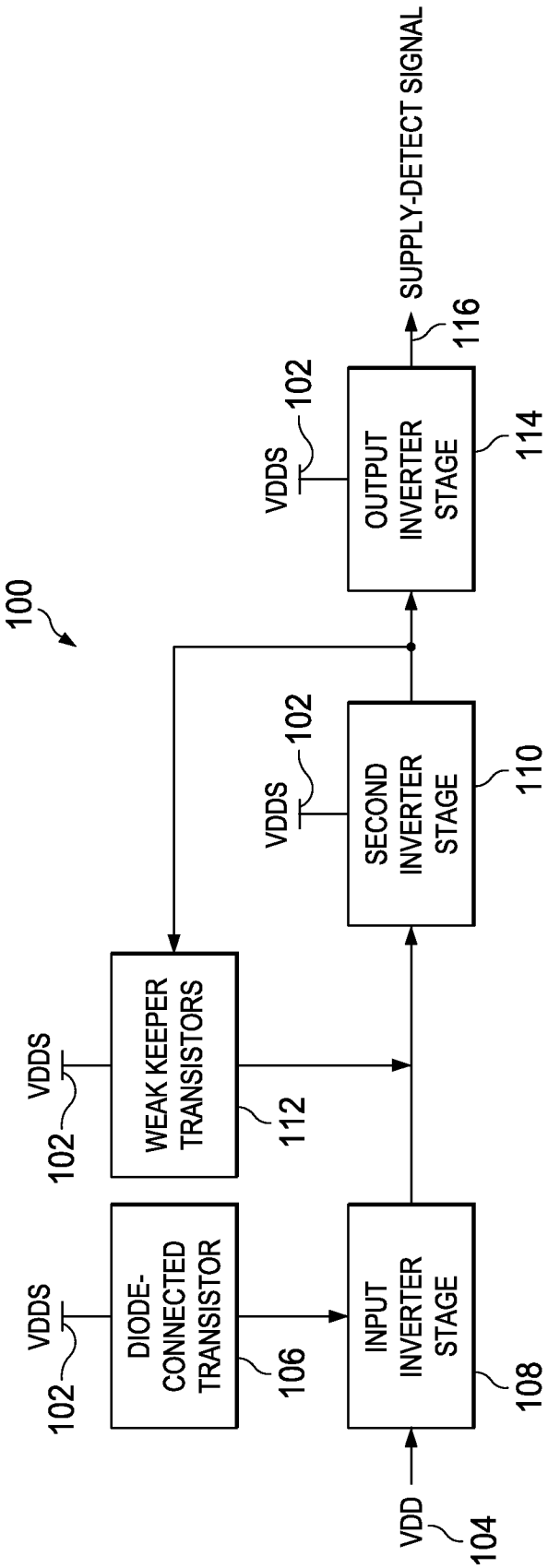
a diode connected transistor coupled to the IO supply voltage;

an input inverter stage connected to the diode connected transistor and configured to receive the core supply voltage;

a second inverter stage connected to an output of the input inverter stage;

a pair of weak keeper transistors coupled in series, wherein gate terminals of the pair of weak keeper transistors are connected to an output of the second inverter stage, and wherein the pair of weak keeper transistors is configured to pull the output of the input inverter stage to the IO supply voltage level; and

an output inverter stage connected to the second inverter stage, wherein the output inverter stage is configured to buffer the output of the input inverter stage and generate a supply detect signal.


100
VDD
104
INPUT INVERTER STAGE
108
DIODE-CONNECTED TRANSISTOR
106
VDDS
102
WEAK KEEPER TRANSISTORS
112
VDDS
102
SECOND INVERTER STAGE
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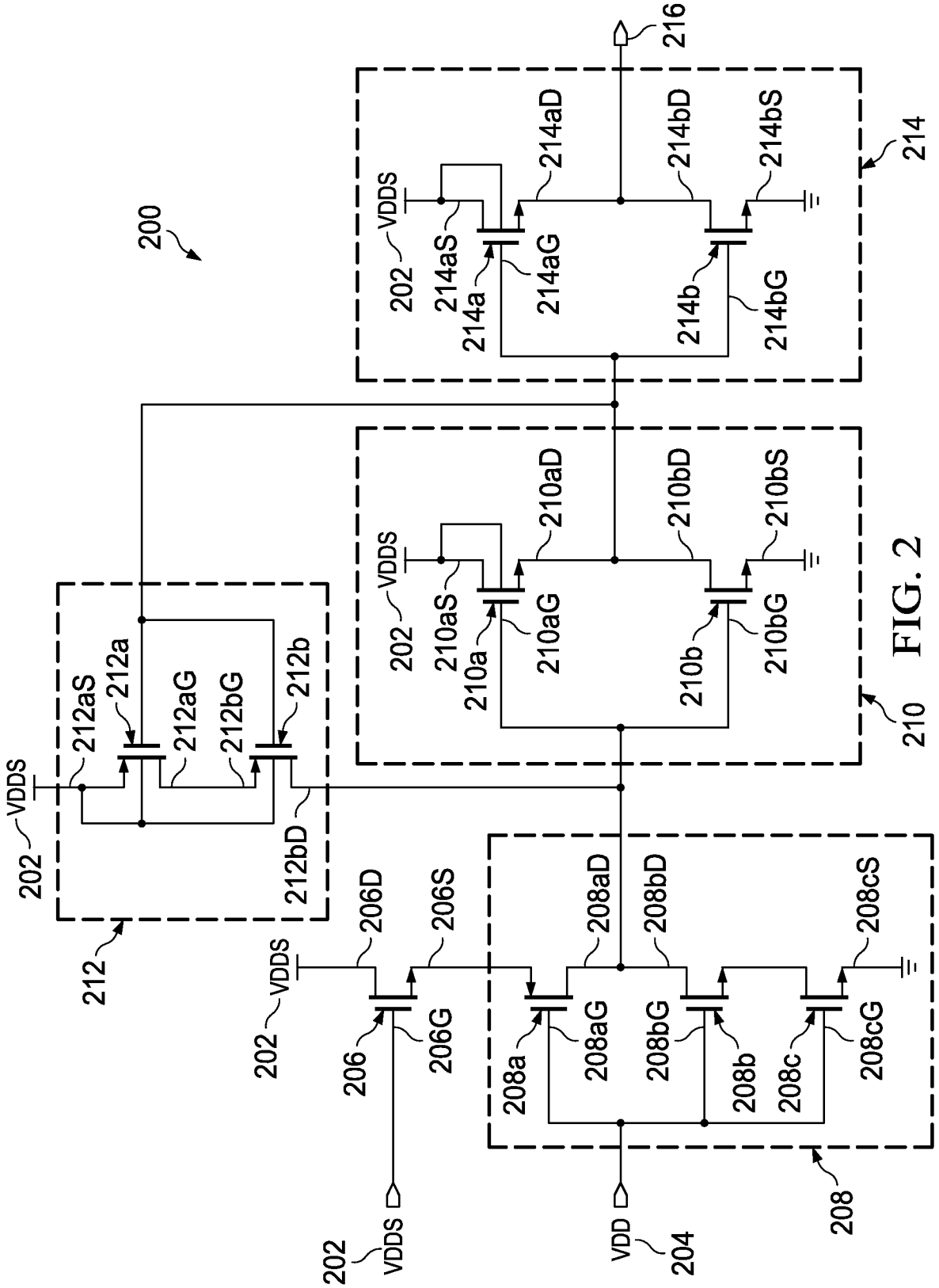
VDDS
102
OUTPUT INVERTER STAGE
114
VDDS
102
SUPPLY-DETECT SIGNAL
116

FIG. 1


200
216
214
214aD
214bD
214bS
VDDS
202
214aS
214a
214aG
214b
214bG
210
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210bS
210aS
210a
210aG
210b
210bG
212
212aS
212a
212aG
212bG
212b
212bD
206D
206S
206
206G
208
208aD
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208bG
208b
208c
208cG
VDD
204

FIG. 2

FIG. 3(a)

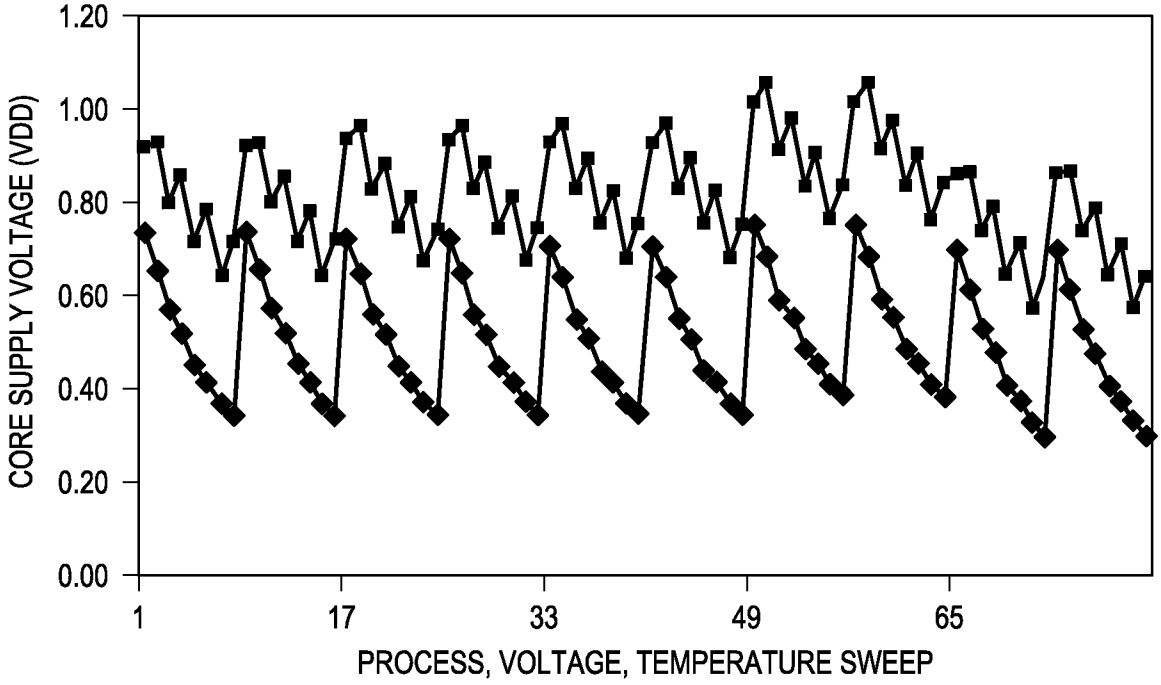
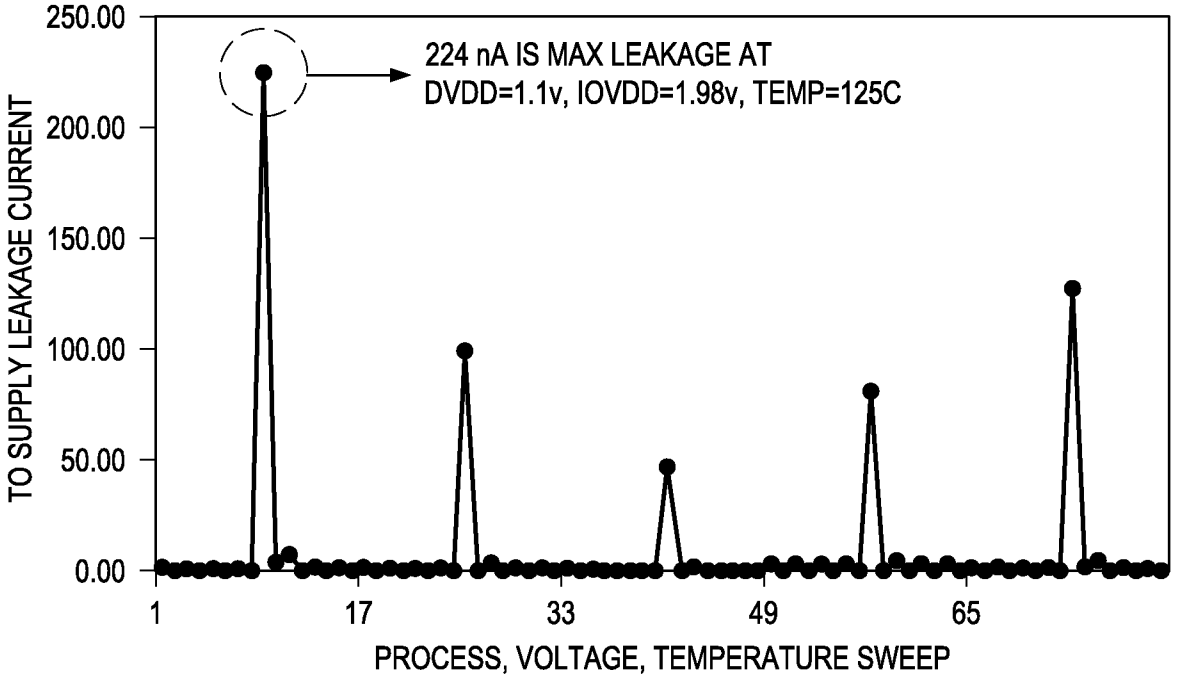

1.20
1.00
0.80
0.60
0.40
0.20
0.00
CORE SUPPLY VOLTAGE (VDD)
1
17
33
49
65
PROCESS, VOLTAGE, TEMPERATURE SWEEP

FIG. 3(b)


250.00
200.00
150.00
100.00
50.00
0.00
TO SUPPLY LEAKAGE CURRENT
224 nA IS MAX LEAKAGE AT
DVDD=1.1v, IOVDD=1.98v, TEMP=125C
1
17
33
49
65
PROCESS, VOLTAGE, TEMPERATURE SWEEP

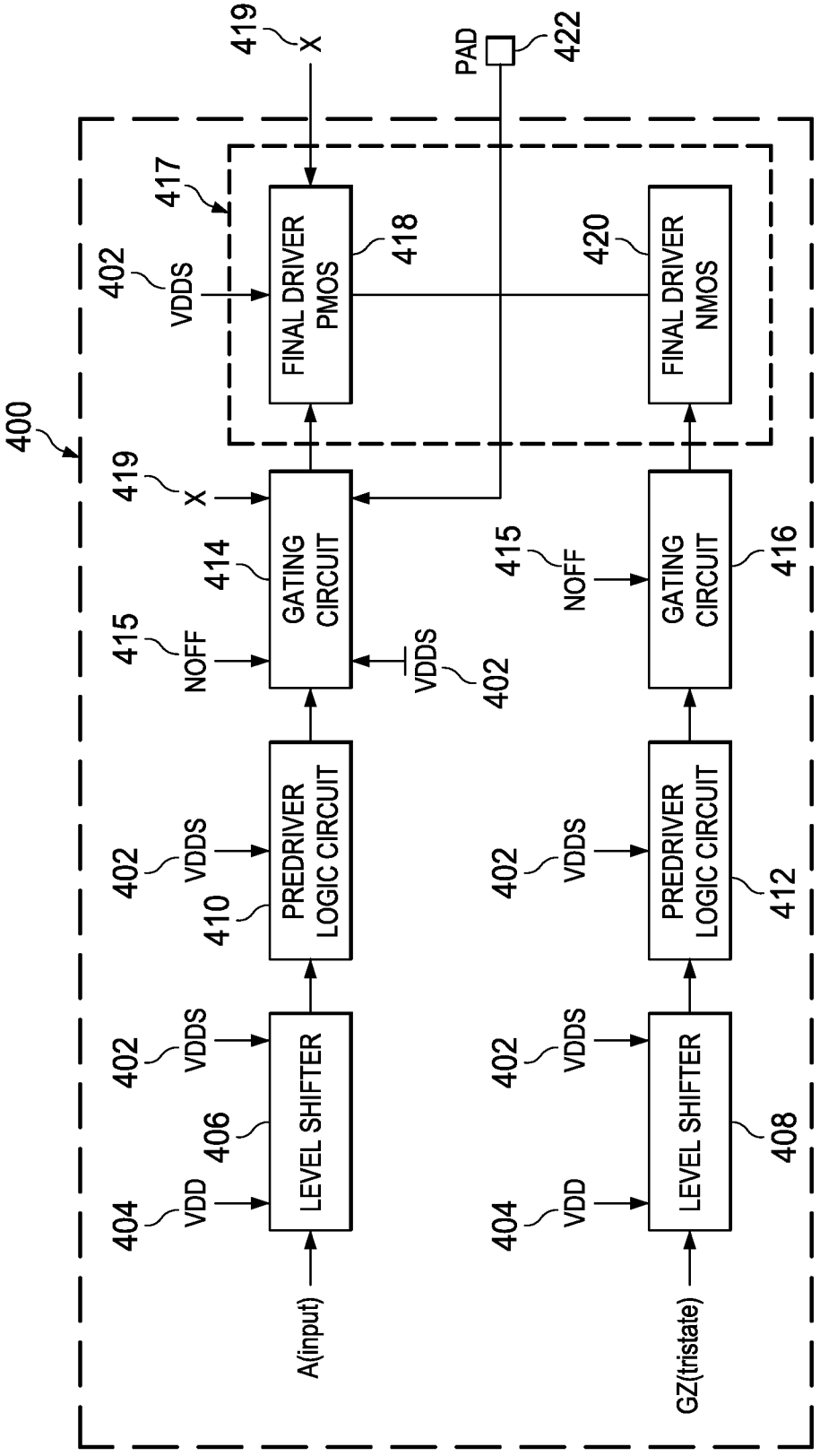

400
419
X
PAD
422
417
402
VDDS
FINAL DRIVER PMOS
418
420
FINAL DRIVER NMOS
419
X
414
GATING CIRCUIT
415
NOFF
VDDS
402
415
NOFF
GATING CIRCUIT
416
402
VDDS
410
PREDRIVER LOGIC CIRCUIT
402
VDDS
PREDRIVER LOGIC CIRCUIT
412
402
VDDS
406
LEVEL SHIFTER
402
VDDS
LEVEL SHIFTER
408
404
VDD
404
VDD
A(input)
GZ(tristate)

FIG. 4

FIG. 5

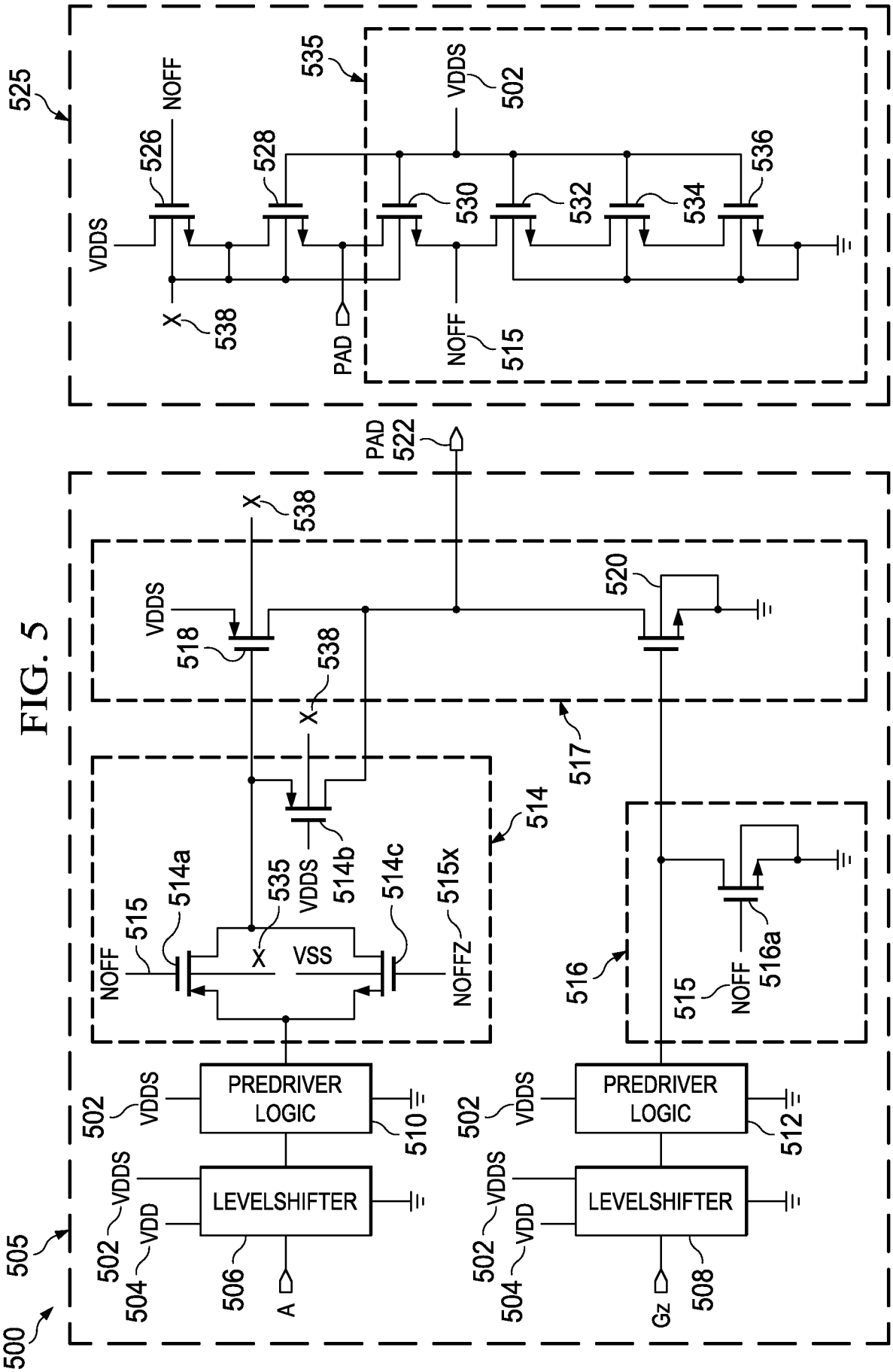

525
535
VDDS
502
NOFF
526
528
530
532
534
536
VDDS
X
538
PAD
NOFF
515
PAD
522
X
538
520
VDDS
518
538
X
517
514
514a
535
VDDS
514b
514c
515x
515
NOFF
X
VSS
NOFFZ
516
515
NOFF
516a
502
VDDS
PREDRIVER LOGIC
510
502
VDDS
PREDRIVER LOGIC
512
VDDS
LEVELSHIFTER
502
VDD
504
506
A
VDDS
LEVELSHIFTER
502
VDD
504
Gz
508
505
500

FIG. 6(a)

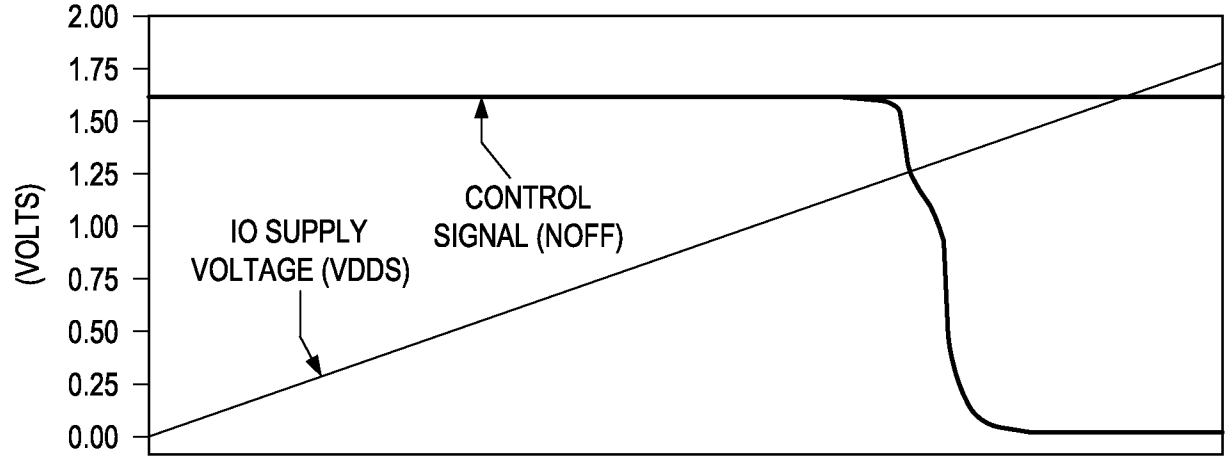


FIG. 6(b)

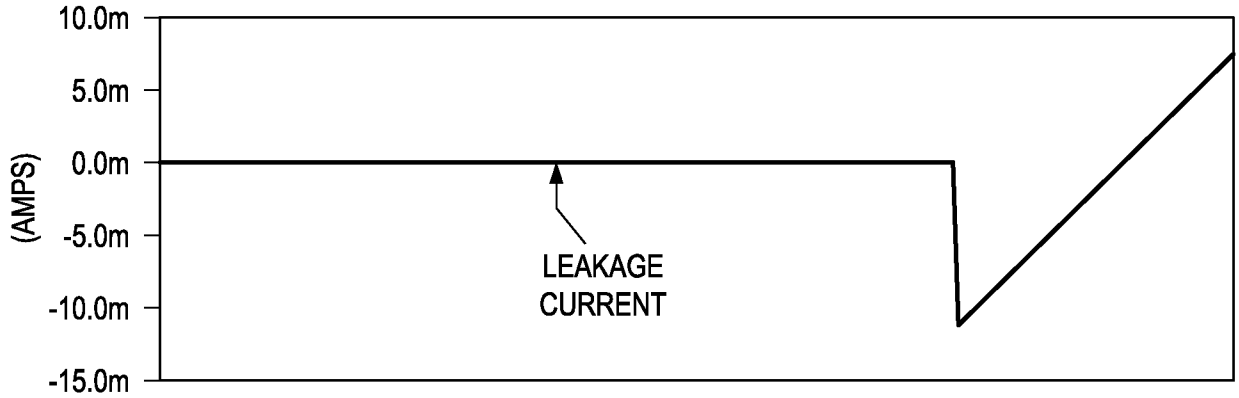
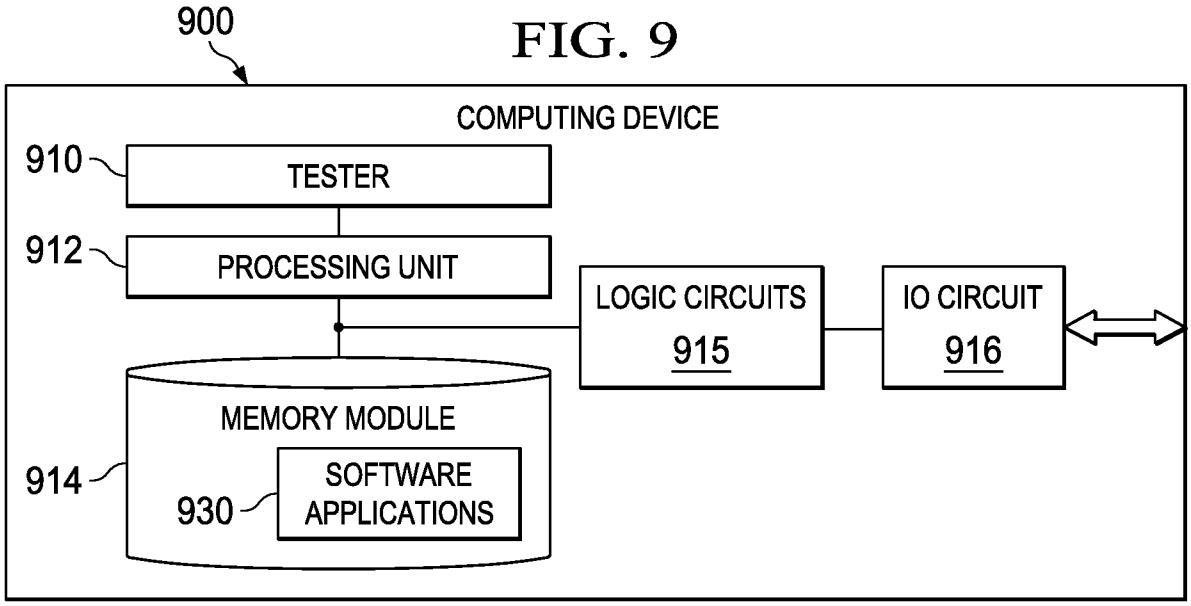


FIG. 9



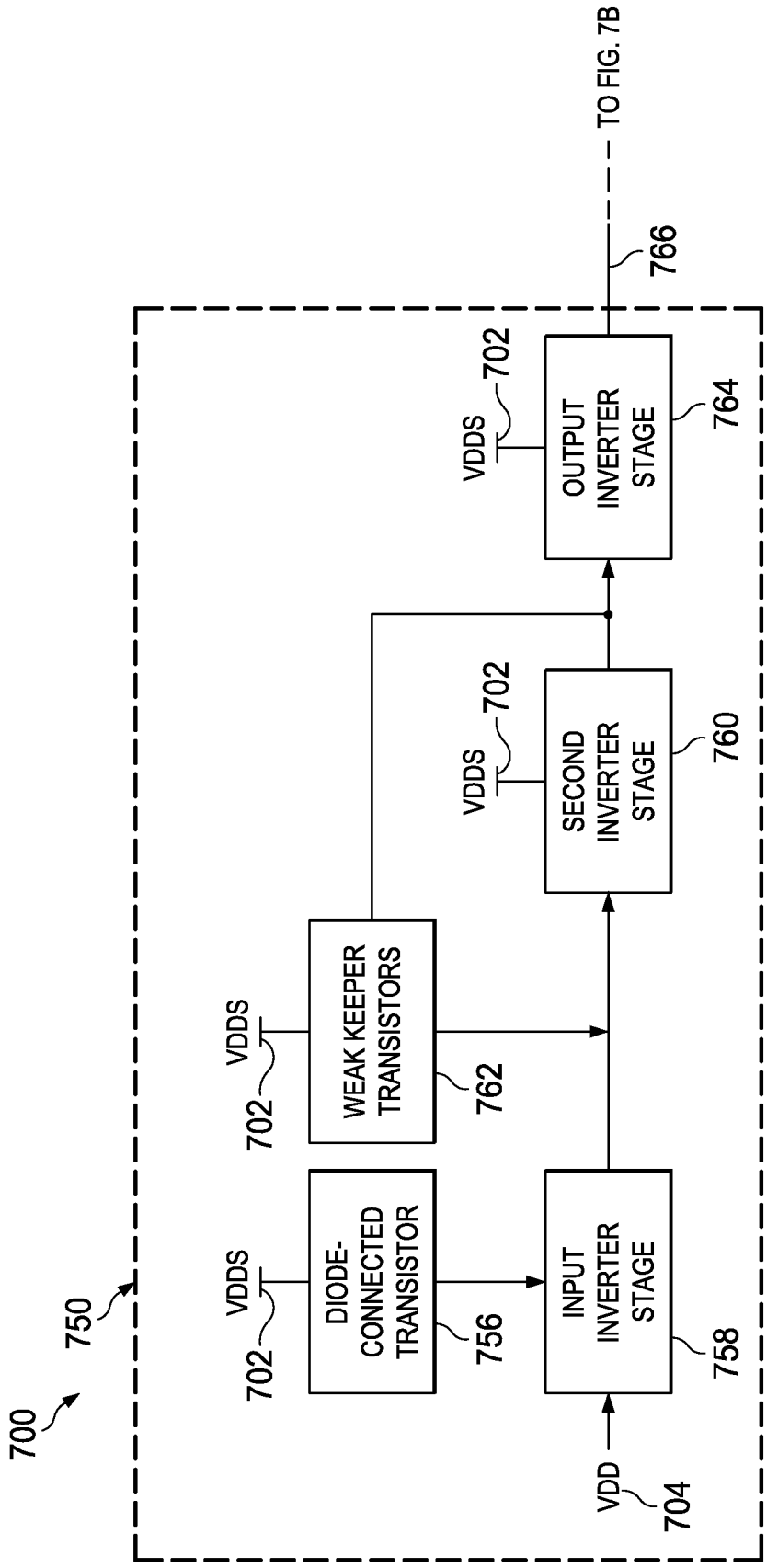

700
750
VDDS
702
DIODE-CONNECTED TRANSISTOR
756
VDDS
702
WEAK KEEPER TRANSISTORS
762
INPUT INVERTER STAGE
758
VDD
704
VDDS
702
SECOND INVERTER STAGE
760
VDDS
702
OUTPUT INVERTER STAGE
764
766
TO FIG. 7B

FIG. 7(a)

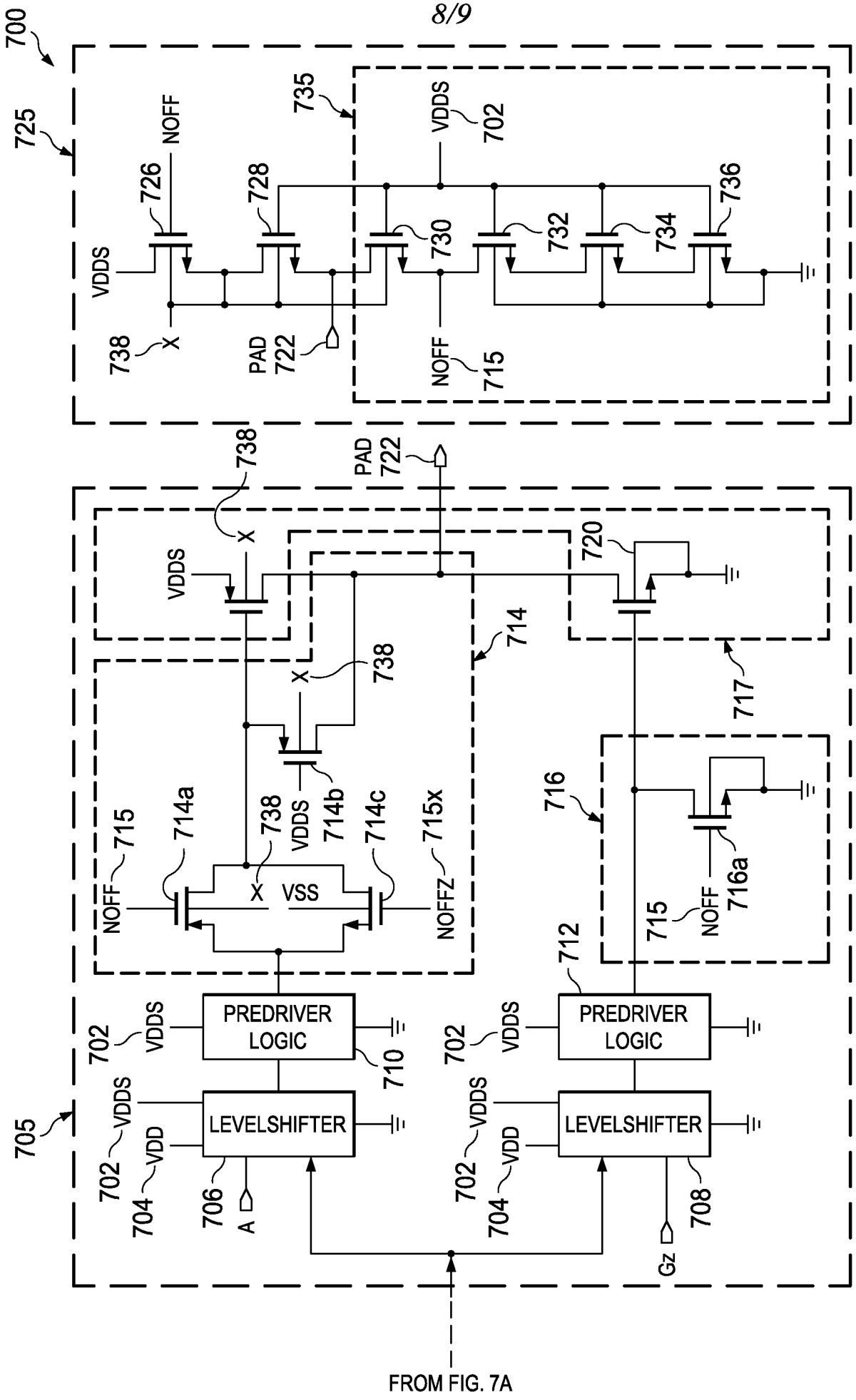

700
725
735
VDDS
702
NOFF
726
728
730
732
734
736
VDDS
738
X
PAD
722
NOFF
715
PAD
722
738
X
VDDS
720
714
738
X
717
716
714a
738
VDDS
714b
714c
715x
715
NOFF
X
VSS
NOFFZ
716a
715
NOFF
712
PREDRIVER LOGIC
PREDRIVER LOGIC
702
VDDS
710
LEVELSHIFTER
LEVELSHIFTER
705
VDD
704
706
A
708
Gz
FROM FIG. 7A

FIG. 7(b)

FIG. 8(a)

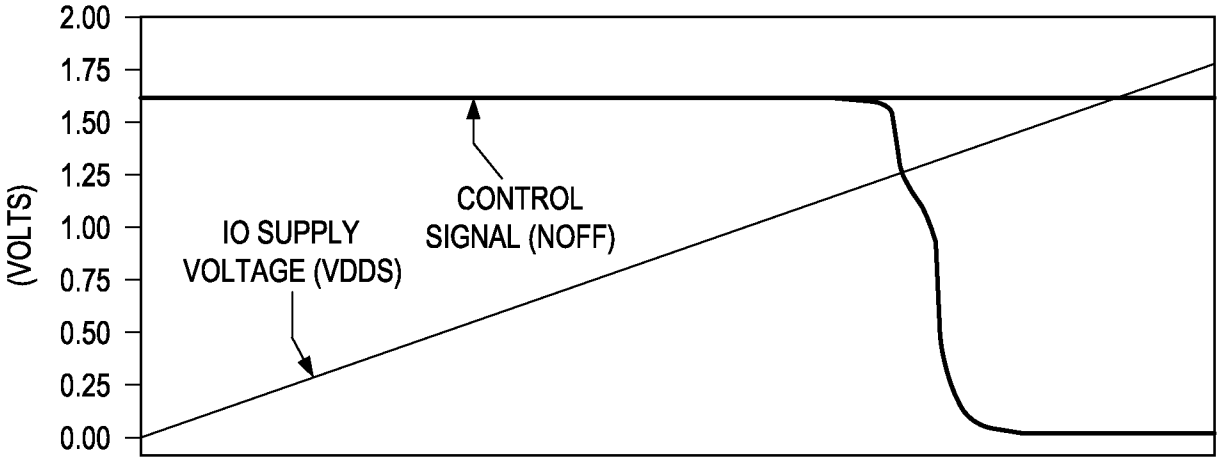
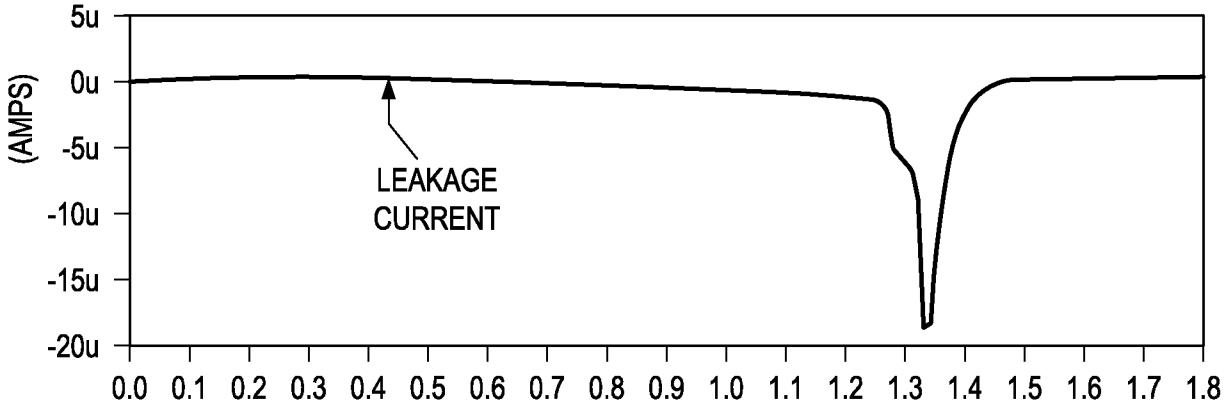

2.00
1.75
1.50
1.25
1.00
0.75
0.50
0.25
0.00
(VOLTS)
IO SUPPLY
VOLTAGE (VDDS)
CONTROL
SIGNAL (NOFF)

FIG. 8(b)


5u
0u
-5u
-10u
-15u
-20u
(AMPS)
LEAKAGE
CURRENT
0.0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0 1.1 1.2 1.3 1.4 1.5 1.6 1.7 1.8

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2014/058011

A. CLASSIFICATION OF SUBJECT MATTER

H03K 17/56 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03K 17/00, 17/08, 17/51, 17/56, G06F 17/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2010/271069 A1 (SAMSUNG ELECTRONICS CO., LTD) 28.10.2010	1-20
A	US 2001/047506 A1 (TEXAS INSTRUMENTS INCORPORATED) 29.11.2001	1-20
A	RU 2308146 C2 (OOO "UNIK AI SIZ") 10.10.2007	1-20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 December 2014 (17.12.2014)	15 January 2015 (15.01.2015)
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	Authorized officer C. Chernyakova Telephone No. (499) 240-25-91