(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
26 October 2012 (26.10.2012)

WIPO | PCT

(10) International Publication Number
WO 2012/145473 A1

(51) International Patent Classification:
*H01L 21/3065* (2006.01)

(21) International Application Number:
PCT/US2012/034192

(22) International Filing Date:
19 April 2012 (19.04.2012)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/477,646 21 April 2011 (21.04.2011) US

(71) Applicant *(for all designated States except US)*: **LINDE AKTIENGESELLSCHAFT** [DE/DE]; Klosterhofstr. 1, 80331 Munich (DE).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **CIGAL, Jean-charles** [FR/DE]; Nordstrasse 7, 01099 Dresden (DE). **STOCKMAN, Paul, Alan** [US/US]; 3 Fellen Place, Hillsborough, NJ 08844 (US). **HOGLE, Richard, A.** [US/US]; 4654 Merrick Court, Oceanside, CA 92056 (US).

(74) Agent: **HEY, David, A.**; Linde LLC, 575 Mountain Ave., Murray Hill, NJ 07974 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Published**:

— *with international search report (Art. 21(3))*

(54) **Title**: DRY FLUORINE TEXTURING OF CRYSTALLINE SILICON SURFACES FOR ENHANCED PHOTOVOLTAIC PRODUCTION EFFICIENCY

(57) **Abstract**: Improved techniques for etching and texturing of silicon surfaces for use in solar cells or photovoltaic devices. Dry fluorine gas etching and texturing of crystalline silicon wafers is carried out to improve the efficiency of solar cells and photovoltaic devices produced from the treated wafers.

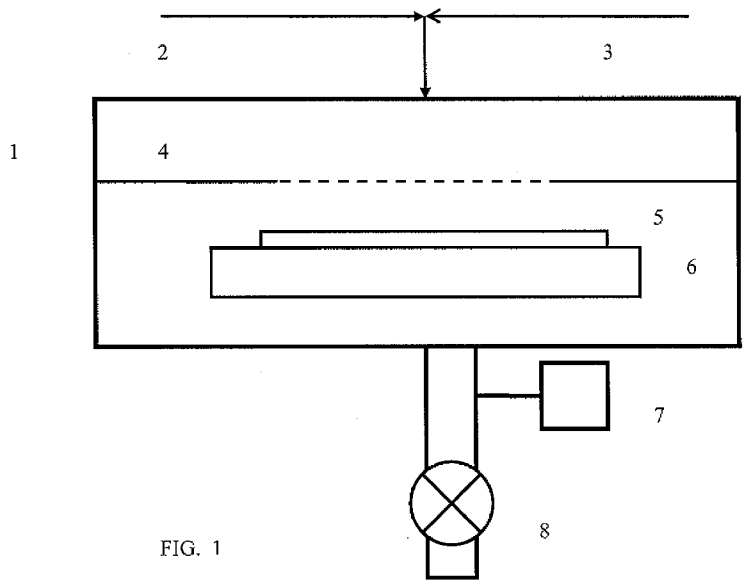


FIG. 1

WO 2012/145473 A1

# DRY FLUORINE TEXTURING OF CRYSTALLINE SILICON SURFACES FOR ENHANCED PHOTOVOLTAIC PRODUCTION EFFICIENCY

## FIELD OF THE INVENTION

**(001)** The present invention relates to texturing of silicon surfaces for use in solar cells or photovoltaic devices, and particularly to the use of fluorine dry gas etching of the silicon surfaces.

## BACKGROUND OF THE INVENTION

**(002)** Most photovoltaic solar cells are thin silicon wafers that can be used to convert sunlight into electricity and serve as an energy source for a wide variety of uses. For example, small area solar cells can be used to power calculators, cell phones and other small electronic devices. Larger arrays can be used for supplementing or fulfilling the electrical needs of individual residences, lights, pumping, cooling, heating, etc.

**(003)** In order to improve the efficiency of solar cells while maintaining cost effectiveness of production, it is necessary to make improvements to the processing of the silicon surfaces. In particular, silicon wafers used for solar cell fabrication are generally sliced from a boule of silicon formed by the Czochralski method or multi-crystalline ingots. The slicing process results in roughness and surface defects on the silicon surface caused by the slicing or sawing equipment. These areas of roughness and damage must be removed in order to form an abrupt, defect free p-n junction and contact wires needed for the final solar cell. The process of removing the roughness, wet chemical and surface damage is typically carried out by an aggressive anisotropic etch known as "saw damage removal".

**(004)** The saw damage removal process is generally needed to optimize the surface micro-geometry to produce the minimum surface reflectance and thereby enhance the photovoltaic efficiency of the solar cell. The saw damage removal process has been accomplished in a number of different ways. For example, wet etching of the silicon surface can be done, using a number of different wet chemicals. However, wet chemical etching has the disadvantages of supply chain issues for the chemicals, as well as chemical abatement requirements. Wet chemical etching is effective for texturing all types of crystal orientations, e.g. single crystalline and poly-silicon surfaces, but requires collection of wafers from conveyors coming from a dry process, placing them in racks, soaking the racks, and drying the wafers fully. Then the wafers must be unloaded from the racks to proceed with dry processing. Cost effective thin Si wafers are very susceptible to breakage in this series of handling steps. The downstream dry processing is very sensitive to water so the drying must be very effective. Using no aqueous baths would improve the yield of the down stream processes.

**(005)** Another method of saw damage removal is reactive ion etching that utilizes chemically reactive plasma generated under low pressure by an electromagnetic field wherein high energy ions react with the silicon surface to remove the damage. Reactive ion etching has the advantages that there is limited plasma induced damage and it is also a dry process. However, reactive ion etching has the disadvantages that it is slow with a tendency for poor uniformity. Where texture is formed, there is often an adjacent region where the wafer is polished by the action of the plasma. In some cases, the non-reflective region can be polished away by the plasma reacting with the freshly formed surface.

**(006)** Another saw damage removal method is dielectric barrier discharge. In this method a plasma of a reactive gas is formed which can be used to interact and etch the silicon surface to remove damage. This method can be used effectively for large area processing and for faster processing time. However, this method also has the disadvantage that it has equal chances of creating or removing surface texturing

(darkening). This creates an intrinsic uniformity problem. Since the electrical field is created across the dielectric wafer, there is higher potential for plasma induced damage. Electrical arcing can further damage the wafer surface.

**(007)** There remains a need in the art for improvements to the efficiency of solar cells and to methods of performing saw damage removal and texturing of silicon surfaces.

## SUMMARY OF THE PRESENT INVENTION

**(008)** The present invention provides improved techniques for texturing of silicon surfaces for use in solar cells or photovoltaic devices. The present invention particularly utilizes fluorine dry gas etching of the silicon surfaces to improve the efficiency of solar cells produced.

## BRIEF DESCRIPTION OF THE DRAWINGS

**(009)** Figure 1 is a diagram showing the process and apparatus for fluorine treatment of a silicon surface according to a first embodiment of the present invention.

**(010)** Figure 2 is a diagram showing the process and apparatus for fluorine treatment of a silicon surface according to a second embodiment of the present invention.

**(011)** Figure 3 is a diagram showing the process and apparatus for fluorine treatment of a silicon surface according to a third embodiment of the present invention.

**(012)** Figure 4 is a diagram showing the process and apparatus for fluorine treatment of a silicon surface according to a fourth embodiment of the present invention.

**(013)** Figure 5 is a diagram showing the process and apparatus for fluorine treatment of a silicon surface according to a fifth embodiment of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

**(014)** The present invention provides for etching of crystalline silicon surfaces using fluorine dry gas. Direct fluorine radical or fluorine molecules may be used on commercially available platforms to improve solar cell efficiencies. The present invention is particularly advantageous for use on poly-silicon surfaces, but provides good results for mono-silicon surfaces also.

**(015)** Several different embodiments of the present invention will be described with reference to the drawing figures in more detail below.

**(016)** Figure 1is a diagram showing the process and apparatus for fluorine treatment of a silicon surface according to a first embodiment of the present invention. In this embodiment, a vacuum chamber 1, holds a heater 6, with a silicon wafer 5, placed on the top surface of the heater 6. The heater 6, is brought to operating temperature, from 450°C and 550°C and then an inert gas 2, such as argon is introduced to the chamber 1, through a gas distributor 4. The inert gas 2, flow rate is 2 to 5 slpm, with chamber 1, pressure being controlled to a constant pressure of 10 to 50 torr as measured by a pressure transducer 7, using a control valve 8, for a vacuum pump (not shown). Upon achieving stable pressure and temperature at the desired values, fluorine gas 3, is introduced through the gas distributor 4, at a set flow rate of 3 to 4 slpm. The fluorine gas 3, may be either fluorine radicals or molecular F2 gas. The fluorine gas 3, is introduced for a time period of 30 seconds to 90 seconds.

**(017)** As a result of the process of the present invention set forth above, 7 to 20 microns of silicon is removed from the surface of the silicon wafer 5, leaving a dark texture on the

surface. This dark texture is more effective at absorbing light than the textures left behind when using wet chemical dips. By removing 7 to 20 microns of the silicon wafer 5, surface, saw damage and contaminants are also removed, potentially eliminating the need for the wet chemical polishing step normally needed to remove the saw damage. Therefore, the dry fluorine gas process of the present invention can be advantageously used in place of the chemical polish step, the chemical texture step or both.

**(018)** Figure 2 is a diagram showing the process and apparatus for fluorine treatment of a silicon surface according to a first embodiment of the present invention. This embodiment is operationally similar to that shown in Figure 1. In particular, a vacuum chamber 21, holds a heater 26, which is brought to operating temperature, from 450°C and 550°C. Inert gas 22, such as argon is introduced to the chamber 21, through a gas distributor 24, at a of 2 to 5 slpm, with pressure in chamber 21, being controlled to a constant pressure of 10 to 50 torr as measured by a pressure transducer 27, using a control valve 28, for a vacuum pump (not shown). The difference in Figure 2 is that the wafer 25 is mounted, for example by clamps, to the underside of the heater 26. Upon reaching stable pressure and temperature at the desired values, fluorine gas 23, is introduced through the gas distributor 24, at a set flow rate of 3 to 4 slpm. The fluorine gas 23, may be either fluorine radicals or molecular F2 gas. The fluorine gas 23, is introduced for a time period of 30 seconds to 90 seconds.

**(019)** Not all chemical contaminants from the silicon wafer sawing process are volatilized by fluorine. For example, elements like iron are reactive with fluorine but form an involatile compound so may be left on the wafer surface when the wafer is placed on top of the heater as shown in Figure 1. By mounting the wafer 25, below the heater 26, as shown in Figure 2, such contaminants can fall away from the wafer 25, when the 7 to 20 microns of silicon are removed using the fluorine gas 23. Once again, the present invention results in a dark texture on the surface that is very effective at

absorbing light. The present invention can be advantageously used in place of the chemical polish step, the chemical texture step or both.

**(020)** Figure 3 is a diagram showing the process and apparatus for fluorine treatment of a silicon surface according to a third embodiment of the present invention. In this embodiment, a conveyor type wafer handling system 31, is used. The inert gas 32, and fluorine gas 33, inlet are situated on the side of the system 31, with the pressure transducer 37, and vacuum valve 38, located on the opposite side. The system 31, can operate in much the same manner as the system described with respect to Figures 1 and 2. In Figure 3, the wafer 35, is situated below the heated carrier 36, although the wafer 35, could alternatively be situated above the heated carrier 36. This configuration of the present invention allows the wafer 25, to be conveyed on the heated carrier 35, perpendicular to the gas flow. The results of this embodiment of the present invention are again a dark texture on the silicon wafer 25, surface that is very effective at absorbing light.

**(021)** Figure 4 is a diagram showing the process and apparatus for fluorine treatment of a silicon surface according to a fourth embodiment of the present invention. In this embodiment of the present invention, rather than using a heater or hot plate as described with respect to Figures 1-3, heating of the wafer 45 is provided by a heat lamp array 49A, or alternatively a pair of heat lamp arrays 49A and 49B. The heat lamp arrays 49A (and 49B) are isolated from the chamber 41, by a sealed window 44A (and 44B), that may be composed of sapphire or quartz as long as conditions are very dry. The lamps can be controlled by an infra-red sensor 46, that receives input from the surface of the wafer 45, and is used to monitor and adjust temperature.

**(022)** As noted, a single heat lamp array 49A, may be used below the wafer 45. Alternatively, the single heat lamp array 49B, may be used above the wafer 45, or as also noted, both heat lamp arrays 49A and 49B can be used. In this embodiment, the inert gas

42, and the fluorine gas 43, can be flowing continuously. While the gas flow is continuous, the texturing/etching time is controlled by the duration of the heating applied by the heat lamp arrays 49A or 49B. Inert gas 22, such as argon flows through the chamber 41, at a flow rate of 2 to 5 slpm, preferably about 2 slpm, while the fluorine gas, either fluorine radicals or F2, flows at a rate of 3 to 4 slpm, preferable about 4 slpm. The chamber 41, pressure is controlled between 10 and 50 torr, preferably at 10 torr, as measured by the pressure transducer 47, and using the control valve 48, for a vacuum pump (not shown).

**(023)** Once the desired pressure and flow rates are set, the heat lamp array 49A (and 49B or both) are turned on so that the wafer reaches greater than 500°C within a few second. The infra-red sensor 46, senses the wafer 45 temperature, and controls the heat lamp array 49A (and 49b or both) so that the wafer 45 temperature is held between 500°C and 550°C for 30 to 90 seconds. One advantage of this embodiment of the present invention is that both surfaces of the wafer 45 can be etched or textured. The resulting surface of the wafer 41, has a dark texture that is very effective at absorbing light.

**(024)** Figure 5 is a diagram showing the process and apparatus for fluorine treatment of a silicon surface according to a fifth embodiment of the present invention. In this embodiment of the present invention, heating of the wafer 55 is again done by a heat lamp array 59A (or alternatively a heat lamp array 59B, or both heat lamp arrays 59A and 59B). The heat lamp arrays 59A (and 59B) are isolated from the chamber 51, by a sealed window 54A (and 54B), that may be composed of sapphire or quartz as long as conditions are very dry. The lamps can be controlled by an infra-red sensor 56, that receives input from the surface of the wafer 55, and is used to monitor and adjust temperature.

**(025)** In this embodiment, the chamber 51 runs at atmospheric pressure, with the process gases, i.e. inert gas 52, and fluorine gas 53, being held in the chamber by a dry

curtain of gas flow 60A and 60B, such as N2 at the wafer inlet and outlet of the chamber 51. The inert gas 52, such as argon, N2 or clean dry air, and the fluorine gas 53, such as F2, flows are maintained at a constant rate and are drawn into a vent duct controlled by a damper 58, leading to an abatement device 61, provided with a small negative pressure, generated for example by a fan 62. In this embodiment, continuous feed of wafers 55, can be carried out.

**(026)** As the process runs, the pressure increases. As the pressure increases, to as much as about 700 torr, the rate of texturing or etching also increases. Therefore, even if the fluorine gas becomes diluted by the inert gas or N2 curtain gas, at this higher pressure, the desired reaction should take no more than 30 to 90 seconds. In operation, the texturing/etching is controlled by the heat provided by the heat lamp array 59A (or 59B or both) as sensed and controlled by the infra-red sensor 56. The heat lamp array 59A (or 59B or both) flash until the infra-red sensor 56 reads a wafer 55, temperature corresponding to optimum texturing/etching, i.e. 250°C to 550°C. This could be a Rapid Flash procedure like Rapid Thermal Processing (RTP) as currently used in the semiconductor industry. In such a procedure, it is possible to remove the saw damage from the wafer 55 in a few seconds in a flash chamber.

**(027)** Experimental results using methods and apparatus according to the present invention are set forth below but are not intended to limit applicability or scope of the present invention.

**(028)** In a first experiment, as-cut wafers were processed according to the present invention, using a hot plate temperature of 550°C, chamber pressure of 10 torr, argon (inert gas) flow of 2 slpm and F2 gas flow of 4 slpm. For F2 flow duration of 30 seconds, 7 microns of material was removed. For F2 flow duration of 60 seconds, 10 microns of material was removed. For F2 flow duration of 90 seconds, 15 microns of material was removed.

**(029)** In a second experiment, a 5 inch as-cut wafer was processed using 2 slpm argon, 3 slpm F2, pressure of 10 torr and temperature of 520°C, for 30 seconds. An Al2O3 bar was placed on the wafer to mask a portion of the wafer surface from the etching gas. Following the etch, the depth of the etch around the Al2O3 bar was measured and 7 microns of silicon had been removed. In further tests, with different etch durations, over 15 microns of silicon have been removed.

**(030)** The dry fluorine processing of wafers for use in solar cells and photovoltaic devices in accordance with the present invention provides many advantages over the prior art methods of wafer etching and texturing. For example, wafers do not need to be picked up and placed in racks then unloaded back on the dry process conveyors. If the presence of aqueous solutions or any water can be eliminated, wafer damage due to handling and reduced yield in the dry processes due to residual water can be greatly reduced. Further, wet chemical abatement systems are not needed. The present invention improves the absorption qualities of the processed wafers and therefore efficiency of solar cells and photovoltaic devices formed from such wafers. The dry etching/texturing processes of the present invention may be able to replace both saw damage removal and texturing processes necessary in the prior art and therefore significantly reduce processing time and operation expense.

**(031)** It is anticipated that other embodiments and variations of the present invention will become readily apparent to the skilled artisan in the light of the foregoing description, and it is intended that such embodiments and variations likewise be included within the scope of the invention as set out in the appended claims.

# CLAIMS

What is claimed:

1. A method of etching a silicon wafer comprising:

mounting the silicon wafer in an etching chamber;

establishing operating temperature and pressure in the chamber with a heater and inert gas;

introducing fluorine gas to the chamber to etch the silicon wafer.

2. The method of claim 1 wherein the silicon wafer is a poly-silicon wafer.

3. The method of claim 1 wherein the silicon wafer is a mono-silicon wafer.

4. The method of claim 1 wherein the operating temperature is from silicon wafer is from 450°C to 550°C, the inert gas is argon and the operating pressure is 10 torr to 50 torr.

5. The method of claim 1 wherein the fluorine gas is either fluorine radicals or molecular F2 gas.

6. The method of claim 1 wherein the fluorine gas is introduced for a period of 30 second to 90 seconds resulting in a removal of 7 microns to 20 microns of silicon from the surface of the silicon wafer.

7. The method of claim 1 wherein the heater is a hot plate and the silicon wafer is mounted above the hot plate.

8. The method of claim 1 wherein the heater is a hot plate and the silicon wafer is mounted below the hot plate.

9. The method of claim 1 wherein the chamber is part of a conveyor wafer handling system.

10. The method of claim 1 wherein etching the surface of the silicon wafer removes saw damage.

11. The method of claim 1 wherein the heater is heat lamp array.

12. The method of claim 11 wherein the heat lamp array is controlled by an infra-red sensor to accurately control the temperature within the chamber.

13. The method of claim 1 wherein etching the silicon wafer provides texture to the surface of the silicon wafer.

14. An apparatus for etching a silicon wafer, comprising:
an etching chamber;
a heater associated with the chamber;
a source of inert gas communicating with the interior of the chamber;
a source of fluorine communicating with the interior or the chamber.

15. The apparatus of claim 14 wherein the silicon wafer is a poly-silicon wafer.

16. The apparatus of claim 14 wherein the silicon wafer is a mono-silicon wafer.

17. The apparatus of claim 14 wherein the inert gas is argon.

18. The apparatus of claim 14 wherein the fluorine gas is either fluorine radicals or molecular F2 gas.

19. The apparatus of claim 14 wherein the heater is a hot plate and the hot plate includes means on its upper surface to mount the silicon wafer.

20. The apparatus of claim 14 wherein the heater is a hot plate and the hot plate includes means on its lower surface to mount the silicon wafer.

21. The apparatus of claim 14 wherein the chamber is part of a conveyor wafer handling system.

22. The apparatus of claim 14 wherein the heater is heat lamp array inside or outside the chamber.

23. The apparatus of claim 22 wherein the heat lamp array is controlled by an infra-red sensor.

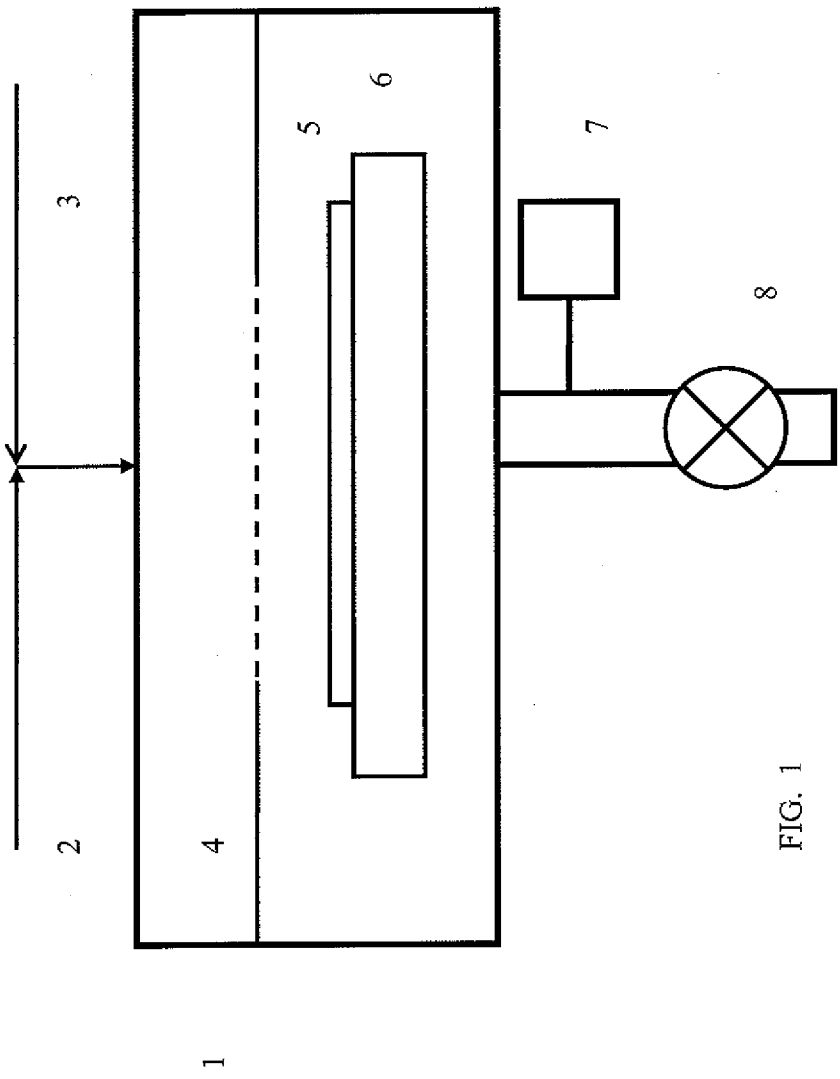


FIG. 1

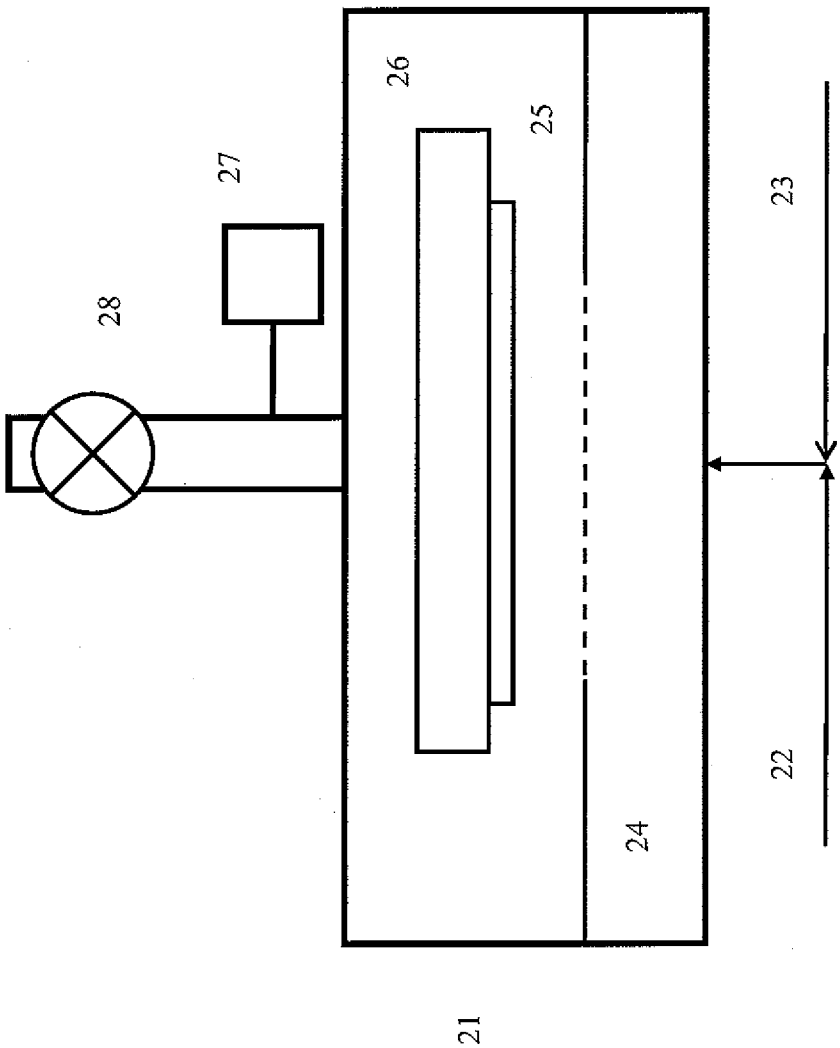


FIG. 2

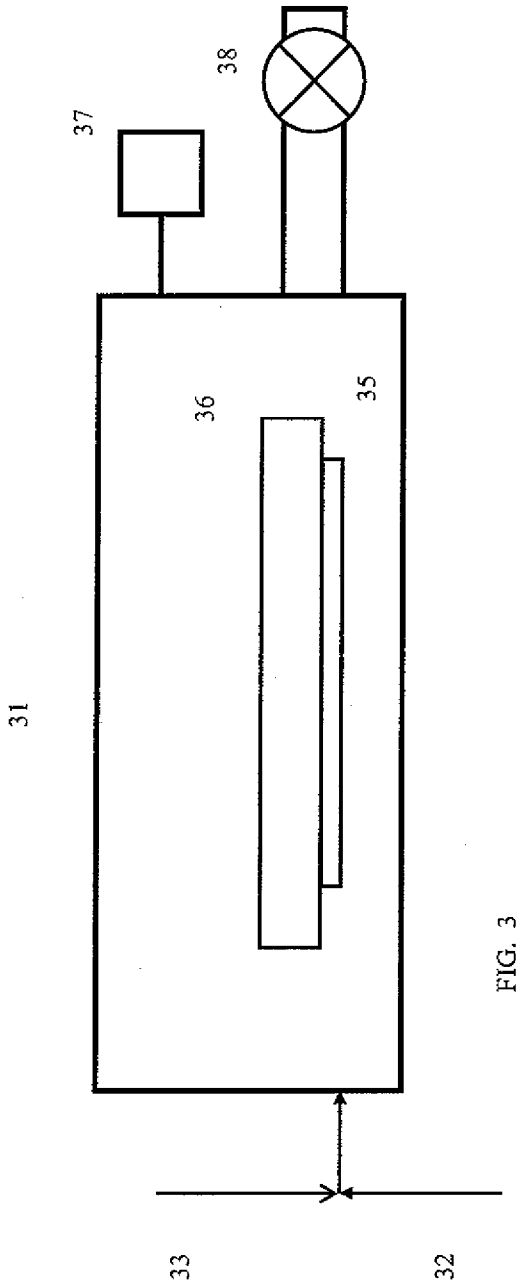


FIG. 3

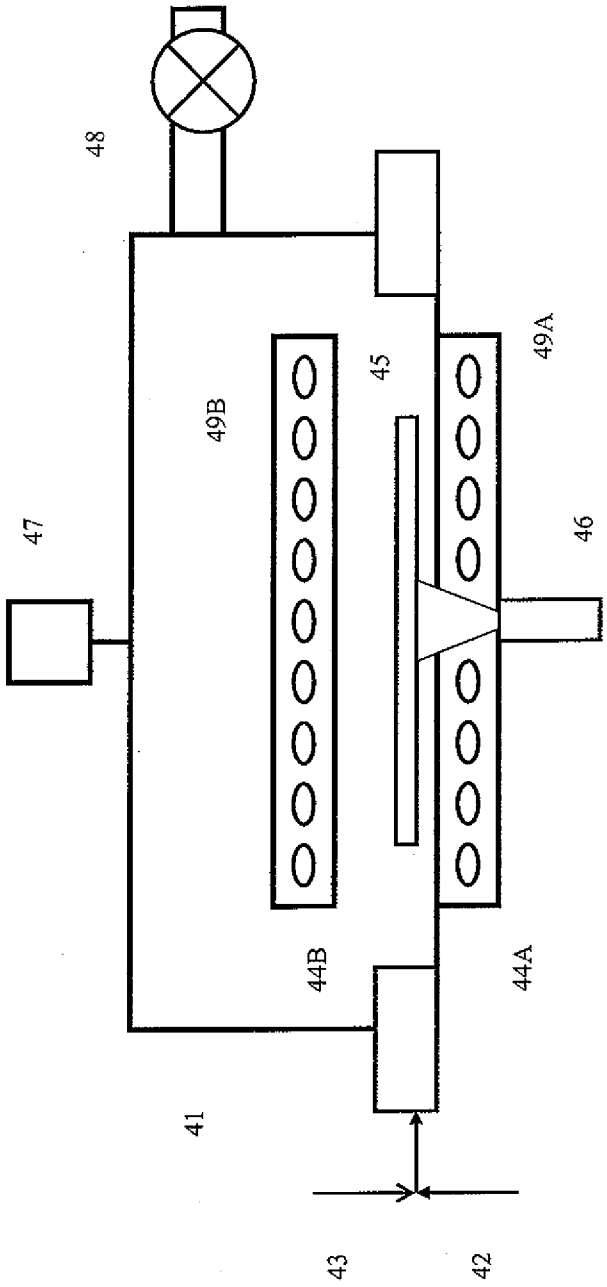


FIG. 4

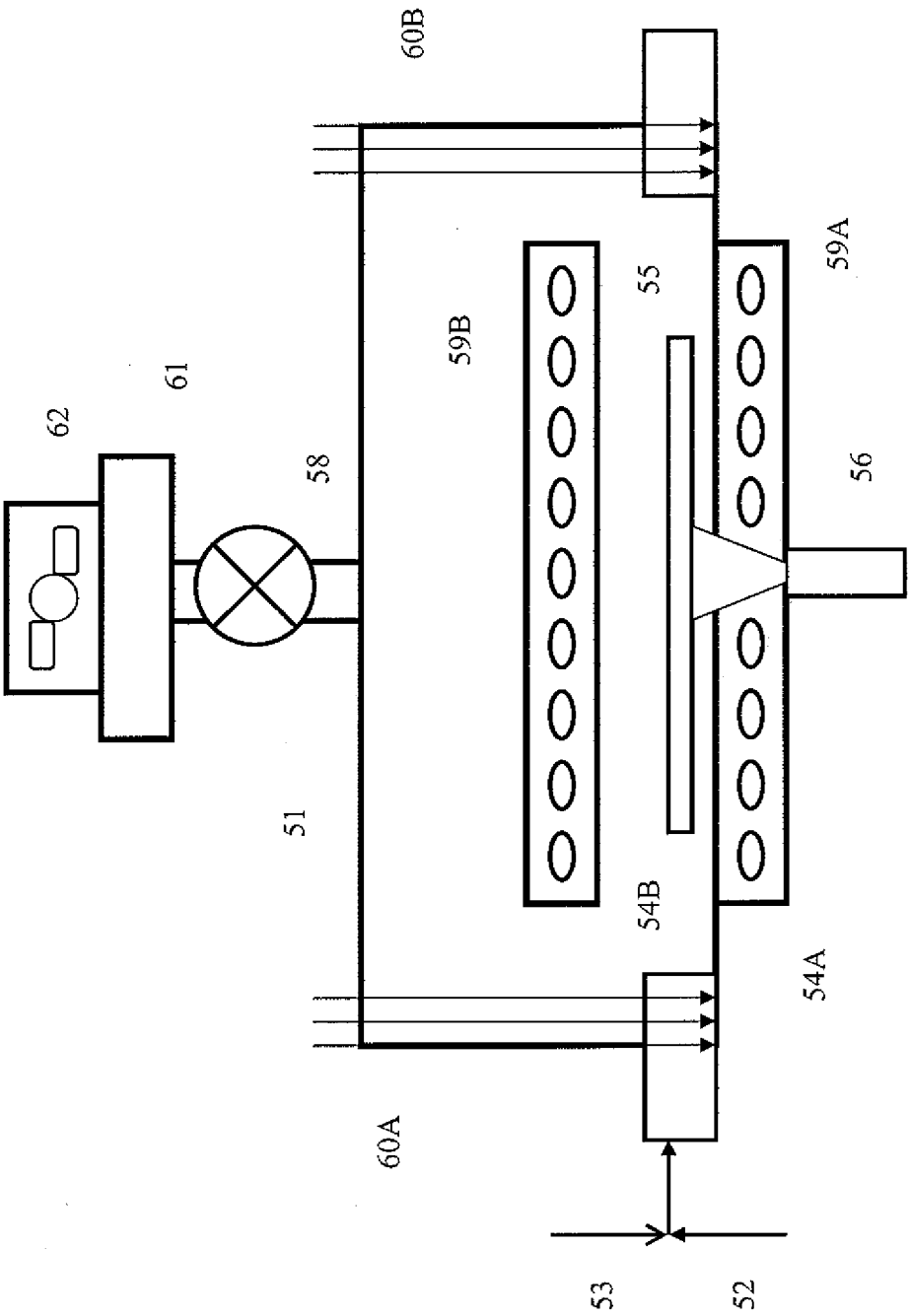


FIG. 5

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 12/34192

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 21/3065, 29/34 (2012.01)
USPC - 257/618; 257/E21.218
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 257/618; 257/E21.218

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 257/E29.108; 438/719

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Electronic Database Searched: PUBWEST (PGPB,USPT,USOC,EPAB,JPAB), GOOGLE. Search Terms Used Infrared, infra-red, etch$ near5 silicon, Polysilicon, poly silicon, wafer, etching chamber, fluorine gas, hot plate, lamp

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| Y | US 2009/0065776 A1 (Scher, et al.) 12 Mar 2009 (12.03.2009)<br>paragraphs [0045], [0053]-[0061], [0087] | 1-23 |
| Y | US 2011/0065276 A1 (Ganguly, et al.) 17 Mar 2011 (127.03.2011)<br>Figure 21, paragraphs [0034], [0106], [0154]-[0155], [0184], [0223], [0237]-[0246] | 1-23 |
| Y | US 6,867,146 B2 (Arita et al.) 15 March 2005 (15.03.2005)<br>especially abstract; summary. figure 1 | 1-23 |
| Y | US 5,536,364 A (Yoshida et al.) 16 July 1996 (16.07.996)<br>especially figure 1; abstract; col 1, ln 65 to col 2, 49 | 1-23 |

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 05 July 2012 (05.07.2012) | 17 JUL 2012 |
| Name and mailing address of the ISA/US<br>Mail Stop PCT, Attn: ISA/US, Commissioner for Patents<br>P.O. Box 1450, Alexandria, Virginia 22313-1450<br>Facsimile No. 571-273-3201 | Authorized officer:<br>Lee W. Young<br>PCT Helpdesk: 571-272-4300<br>PCT OSP: 571-272-7774 |

Form PCT/ISA/210 (second sheet) (July 2009)