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(54) CHIP-SCALE PACKAGES

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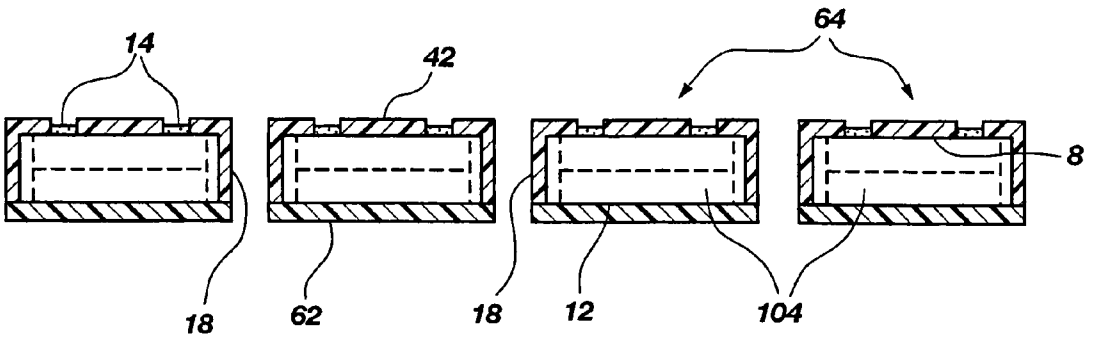
(52) **U.S. Cl.** **257/632**

(57) **ABSTRACT**

Improved chip-scale packages wherein semiconductor die side surfaces are free of the material defects associated with prior art chip-scale package formation. In one embodiment, chip-scale package includes a semiconductor die includes an active surface, an opposing passive surface, and a plurality of etched side surfaces extending from the active surface to the passive surface. A first protective coating may extend over the active surface of the semiconductor die and a second protective coating may extend over the passive surface of the semiconductor die wherein one of the first protective coating and the second protective coating extends over the plurality of etched side surfaces of the semiconductor die.



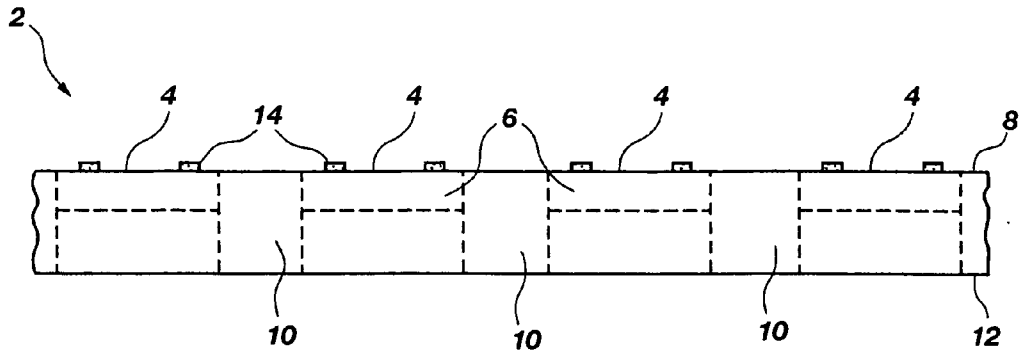


FIG. 1

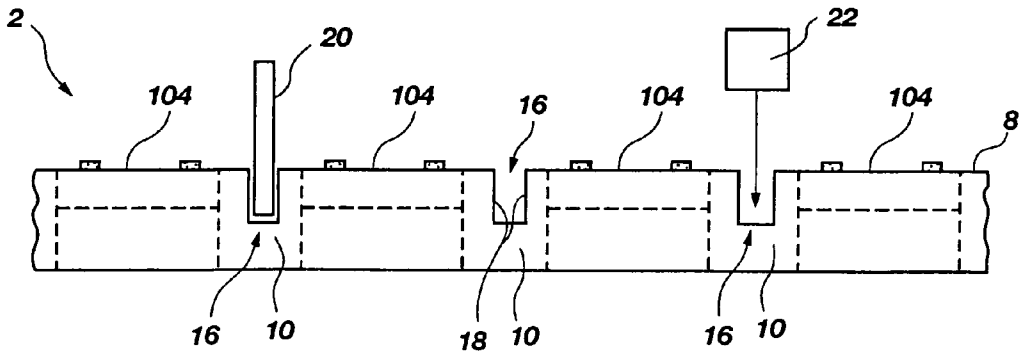


FIG. 2

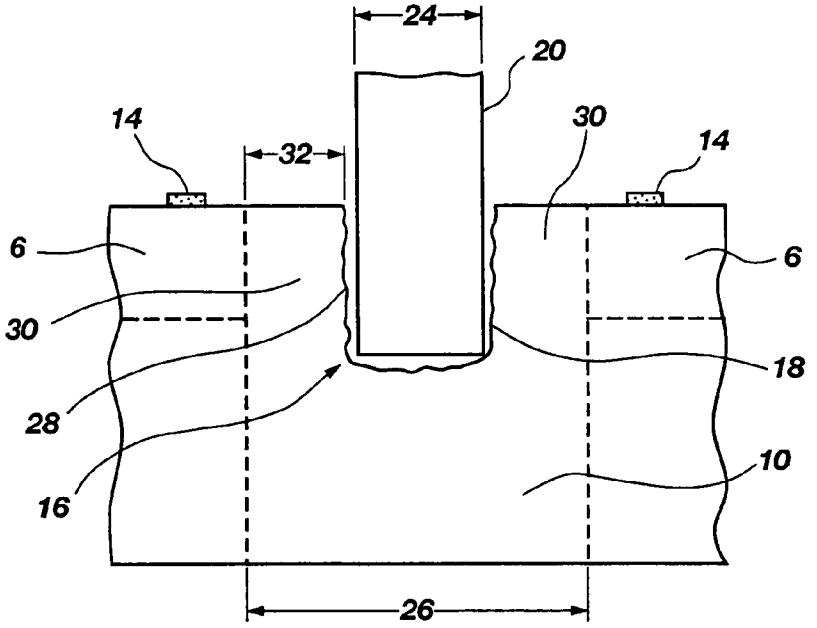

24
20
14
32
30
14
6
6
30
18
28
10
16
26

FIG. 3A

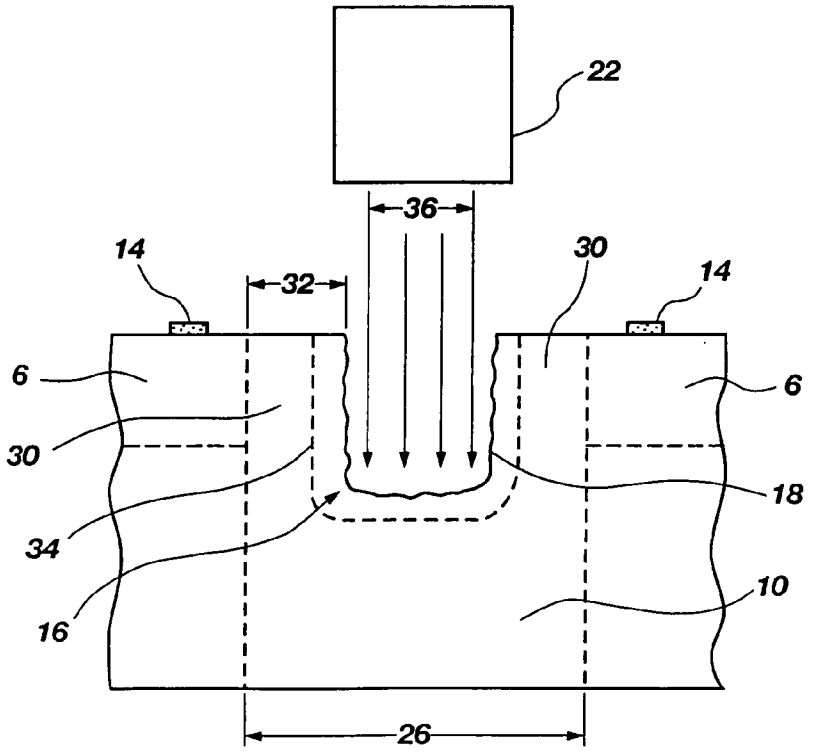

22
36
14
32
30
14
6
6
30
18
34
10
16
26

FIG. 3B

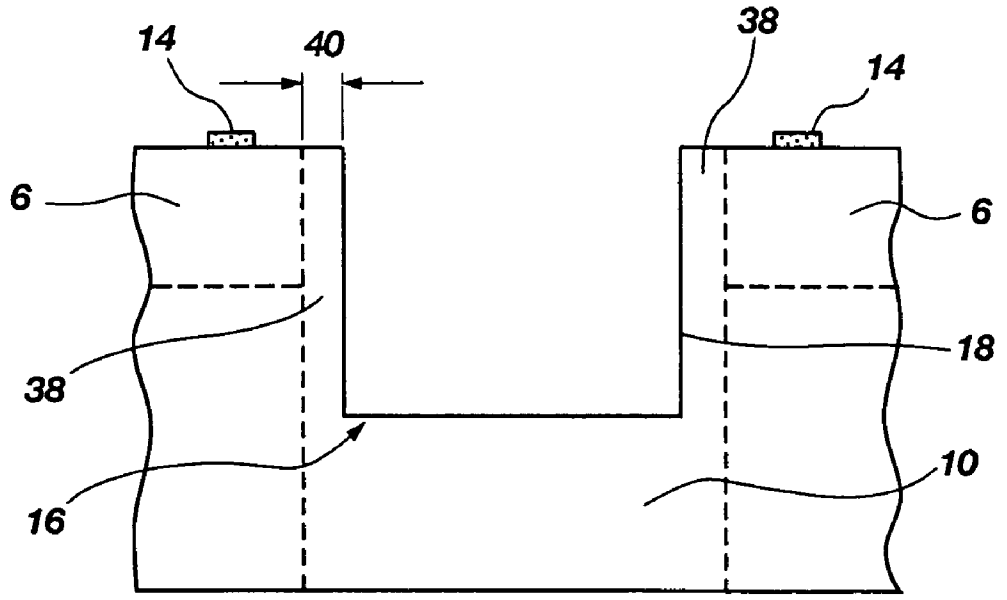


FIG. 4

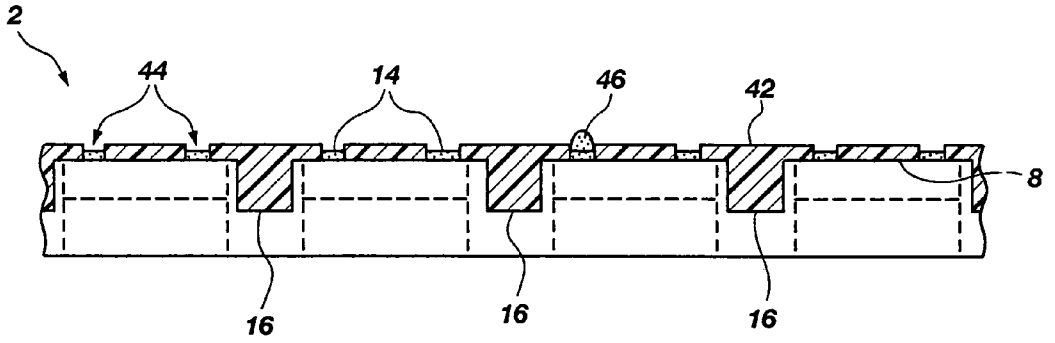


FIG. 5

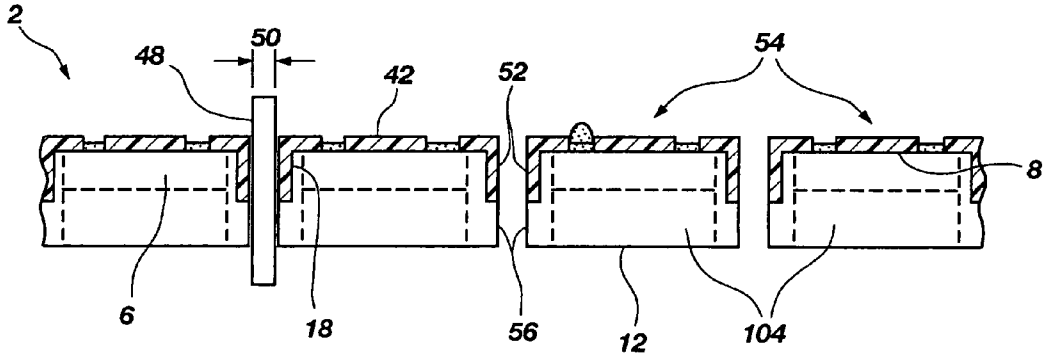


FIG. 6

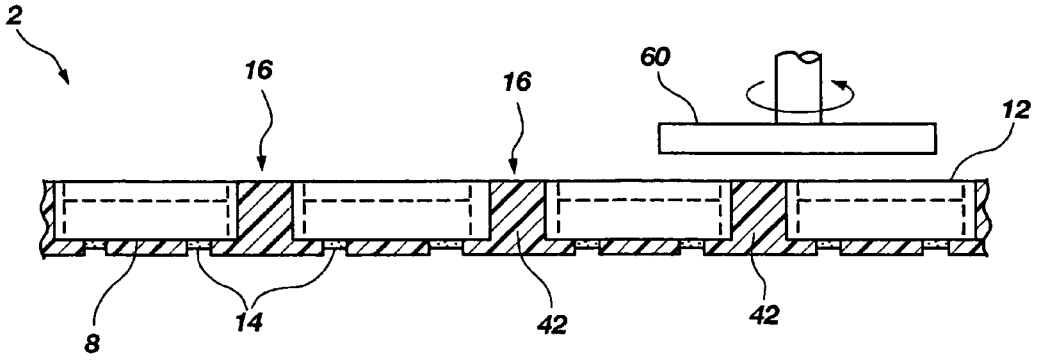


FIG. 7

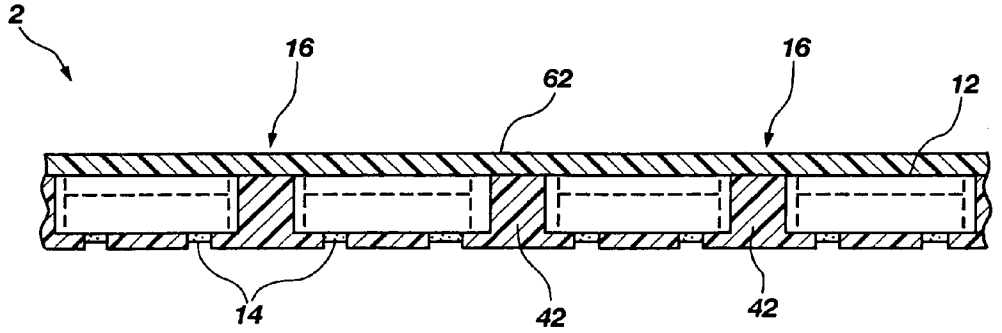


FIG. 8

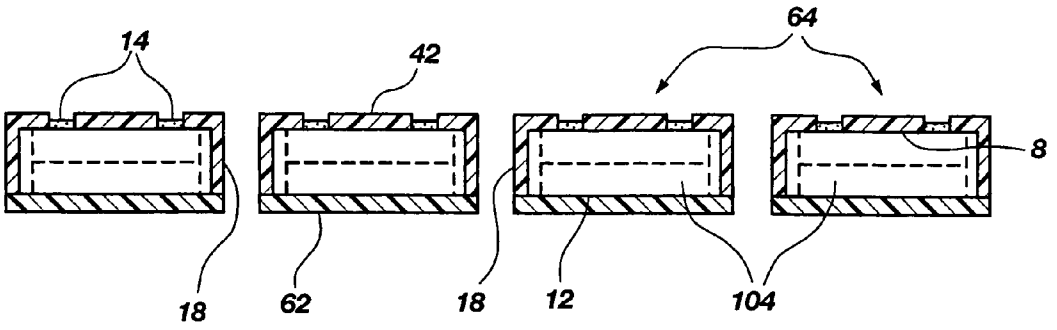


FIG. 9

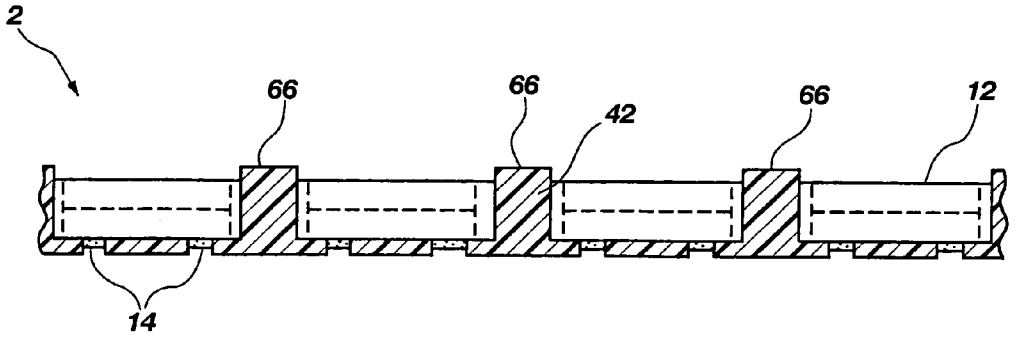


FIG. 10

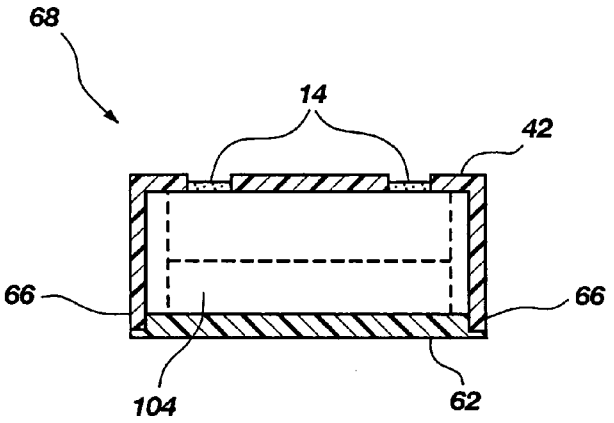


FIG. 11

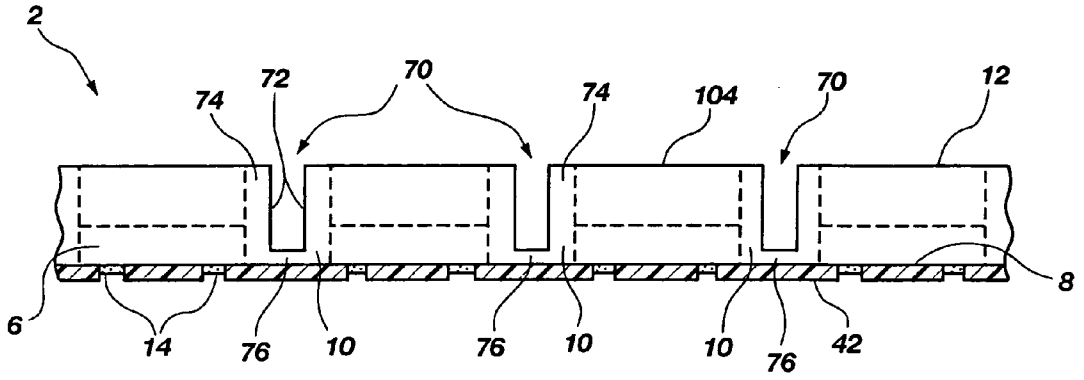


FIG. 12

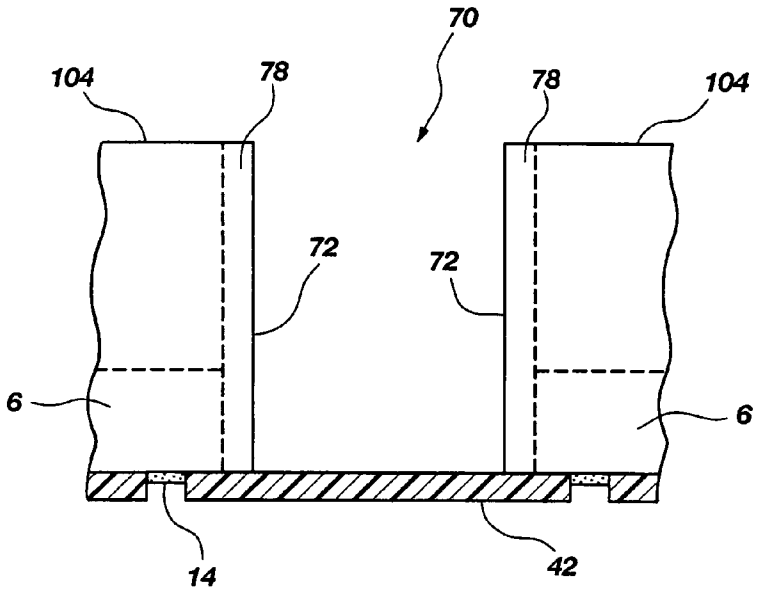


FIG. 13

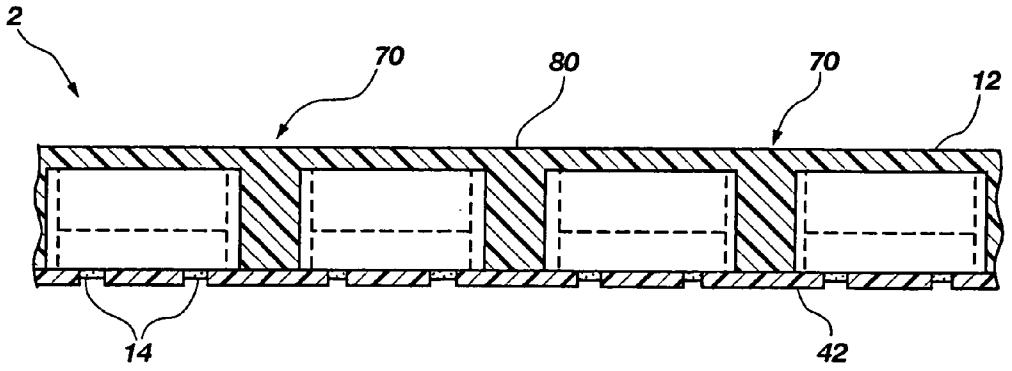


FIG. 14

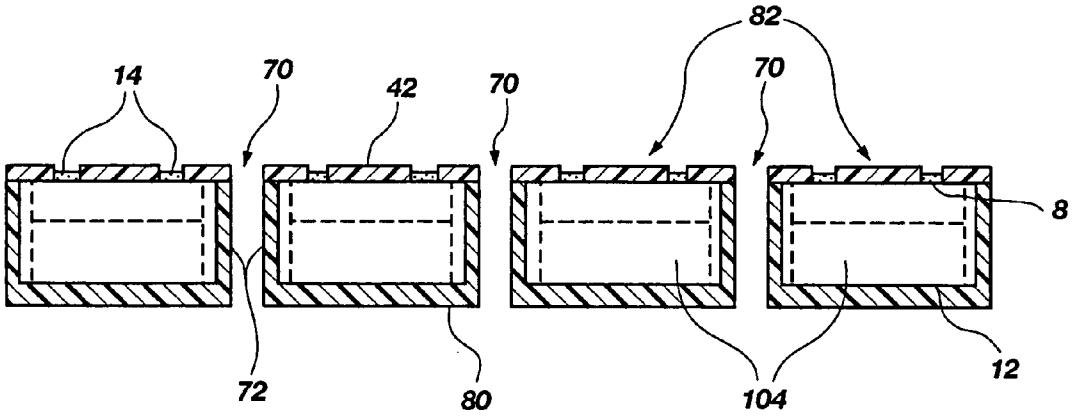


FIG. 15

CHIP-SCALE PACKAGES

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a divisional of application Ser. No. 10/690,417, filed Oct. 20, 2003, pending.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to packaging of semiconductor dice. More particularly, the present invention relates to improved processes for separating and coating semiconductor dice at the wafer level to form individual chip-scale packages.

[0004] 2. State of the Art

[0005] A solid-state electronic device in the form of a semiconductor die or chip is typically manufactured of materials such as silicon, germanium, gallium arsenide or indium phosphide. Circuitry is formed on an active surface of the semiconductor die and may include further circuit levels within the die itself. Bond pads are also formed on the active surface to provide electrical contacts for the semiconductor die circuitry. Due to the materials used and the intricate nature of construction, a semiconductor die is highly susceptible to physical damage or contamination from environmental conditions such as moisture.

[0006] Conventionally, a semiconductor die has been protected by mounting it within a plastic, metal or ceramic package that prevents physical contact with the die and provides hermetic sealing. The package also includes conductive leads for attaching the die bond pads to outside electrical connections. The materials required for this packaging approach increase cost, while resulting in a larger device size that takes up valuable real estate when mounted to a carrier substrate. The added lead structure may also influence processing speed, and further presents opportunities for moisture incursion at interfaces between the conductive leads and other packaging materials.

[0007] Some efforts to reduce the size and cost of these electronic devices have resulted in doing away entirely with the above-described packaging materials. Instead, the semiconductor die is protected by forming what is commonly referred to as a chip-scale package (CSP). In a typical example of this packaging method, a protective coating is added to surfaces of the semiconductor die itself, and conductive bumps are formed over the die bond pads using a variety of known techniques such as screen printing or by ball bumping with wire-bonding equipment. The bumps may then be electrically connected to circuitry on a carrier substrate by tape automated bonding (TAB), or may be directly attached thereto by mounting the semiconductor die in a flip-chip fashion on the carrier substrate. Alternatively, the conductive bumps may be omitted, and the CSP may be attached to a carrier substrate using conventional wire bonds.

[0008] Materials used for formation of the protective coating on the surfaces of the semiconductor die may include, for example, silicon nitride (SiN), silicon dioxide (SiO_2), or other materials like epoxy or polymers. In the prior art, these coatings would be deposited on the active and passive surfaces of a wafer containing an array of semiconductor die locations, and the wafer would subsequently be singulated to provide individual semiconductor dice. A resulting semiconductor die using this method suffers from the fact that its sides, and specifically the sides of its active surface, are left exposed after the wafer singulation. The possibility remains, therefore, that moisture may enter the sides of the die and damage nearby circuitry.

[0009] In order to rectify these shortcomings, various attempts have been made to add additional protective coatings to the sides of a semiconductor die. One approach to coating side surfaces has been to first form cuts or channels in the active surface of a wafer to at least partially expose the sides of each semiconductor die, and then deposit the protective coating onto the wafer. In this manner, the protective coating material enters the channels surrounding each die, and subsequent singulation of the wafer along the channels provides semiconductor dice having active surface and partial side surface coatings. Examples of such a process are disclosed in U.S. Pat. No. 5,742,094 to Ting, U.S. Pat. No. 5,933,713 to Farnworth and U.S. Pat. No. 5,956,605 to Akram et al. While these methods provide at least partial side surface protective coatings, they may require additional processing of the semiconductor dice on an individual basis to completely coat the sides or back of the semiconductor dice.

[0010] Another problem with these methods is that formation of the channels in the active surface of the wafer is typically accomplished using processes that may cause damage to the semiconductor material on the side surfaces of a completed semiconductor die. The channels may be formed, for instance, by cutting with a dicing saw or a laser. When the channels are cut using a dicing saw, diamond particles in the saw may leave nicks and scratches in the cutting surface. Similarly, when the channels are formed by laser cutting, heat from the laser energy may negatively affect the semiconductor material along the channel surfaces, leaving what is sometimes referred to as a heat-affected zone (HAZ). These material defects may result in crack propagation from stress concentrations that will damage the active circuitry adjacent to the channels, or may degrade the semiconductor material to a point where it exhibits current leakages or other undesirable electrical properties. This problem is further aggravated by the fact that the area available for cutting between adjacent semiconductor dice in a wafer, sometimes referred to as a street, is constantly being decreased to save space. For example, while wafers have previously typically been formed with 150-micron street widths, the current manufacturing technology involves forming narrower streets on the order of 100 microns. The reduction in width means that any material defects in the surfaces of channels will be closer to the active circuitry of a semiconductor die and will, therefore, be more likely to cause damage.

[0011] In view of the above, it would be desirable to have an improved method for separating and coating the surfaces of semiconductor dice at the wafer level.

BRIEF SUMMARY OF THE INVENTION

[0012] The present invention, in several embodiments, relates to improved chip-scale packages formed by methods that enable applications of protective coatings to multiple

surfaces of semiconductor dice while remaining in a wafer level array. The methods also provide semiconductor die side surfaces that are free of the material defects associated with prior art chip-scale package formation.

[0013] In a first embodiment according to the present invention, channels are formed in the active surface of a wafer to expose side surfaces of an array of semiconductor dice contained in the wafer. The channels are initially formed along streets between adjacent semiconductor die locations by cutting with a dicing saw or a laser to a depth extending below the active circuitry of the wafer. The surfaces of the channels are then etched to remove defects in the semiconductor material resulting from cutting with the dicing saw or laser. Once the channels are completed, a protective coating is deposited on the active surface of the wafer to seal the active surface and at least a portion of the side surfaces of each semiconductor die. Finally, the wafer is singulated along the channels to provide a plurality of individual chip-scale packages having protective coatings covering the semiconductor die active surface and at least a portion of the side surfaces.

[0014] In a variation of the above embodiment, after depositing the protective coating on the active surface of the wafer, material is removed from the back surface of the wafer by a backgrinding or other planarization process to a depth that exposes the channels. A second protective coating is deposited on the back surface of the wafer, and the wafer is singulated along the channels to provide chip-scale packages having protective coatings covering the semiconductor die active surface, all of the side surfaces and the semiconductor die back surface.

[0015] In a further variations after exposing the channels by backgrinding or planarization, the back surface of the wafer is etched to a depth such that a portion of protective coating material in the channels protrudes from the back surface of the wafer. When the second protective coating is deposited the protruding coating material assists in anchoring the second protective coating in place.

[0016] In a second embodiment according to the present invention, the protective coating is deposited on the active surface of the wafer without forming channels in the active surface. Instead, channels are formed in the back surface of the wafer after depositing the protective coating on the active surface of the wafer. As with the first embodiment, the channels are initially formed along streets between adjacent semiconductor die locations by cutting with a dicing saw or a laser. The surfaces of the channels are then etched to remove defects in the semiconductor material resulting from cutting with the dicing saw or laser and to expose the protective coating formed on the wafer active surface through the channels. Once the channels are completed, a second protective coating is deposited onto the back surface of the wafer and over the protective coating in the channels, and the wafer is singulated along the channels to provide chip-scale packages having protective coatings covering the semiconductor die active surface, all of the side surfaces and the semiconductor die back surface.

[0017] Other and further features and advantages of the present invention will be apparent from the following descriptions of the various embodiments when read in conjunction with the accompanying drawings. It will be understood by one of ordinary skill in the art that the following embodiments are provided for illustrative and exemplary purposes only, and that numerous combinations of the elements of the various embodiments of the present invention are

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0018] In the drawings, which illustrate what is currently considered to be the best mode for carrying out the invention:

[0019] **FIG. 1** is a side view of a semiconductor wafer containing an array of die locations;

[0020] **FIG. 2** is a side view of the wafer in **FIG. 1** with channels cut in the active surface of the wafer between adjacent semiconductor die locations;

[0021] **FIG. 3A** is an enlarged view of a channel cut with a dicing saw;

[0022] **FIG. 3B** is an enlarged view of a channel cut with a laser beam;

[0023] **FIG. 4** is an enlarged view of a channel after it has been etched to remove cutting defects;

[0024] **FIG. 5** is a side view of the wafer in **FIG. 1** with a protective coating formed on the active surface of the wafer;

[0025] **FIG. 6** is a side view of the wafer in **FIG. 5** separated into individual chip-scale packages;

[0026] **FIG. 7** is a side view of the wafer in **FIG. 5** wherein semiconductor material is removed from the passive surface of the wafer by backgrinding;

[0027] **FIG. 8** is a side view of the wafer in **FIG. 7** with a protective coating formed on the passive surface of the wafer;

[0028] **FIG. 9** is a side view of the wafer in **FIG. 8** separated into individual chip-scale packages;

[0029] **FIG. 10** is a side view of the wafer in **FIG. 5**, wherein frame elements of the protective coating project from the passive surface of the wafer;

[0030] **FIG. 11** is a side view of a chip-scale package;

[0031] **FIG. 12** is a side view of the wafer in **FIG. 1** with channels cut in the passive surface of the wafer between adjacent semiconductor die locations;

[0032] **FIG. 13** is an enlarged view of a channel after it has been etched to remove cutting defects;

[0033] **FIG. 14** is a side view of the wafer in **FIG. 12** with a protective coating formed on the passive surface of the wafer; and

[0034] **FIG. 15** is a side view of the wafer in **FIG. 14** separated into individual chip-scale packages.

DETAILED DESCRIPTION OF THE INVENTION

[0035] The following embodiments of the present invention are provided as examples to assist in a thorough understanding of the present invention. It should be apparent, however, that various additions, modifications and com-

binations of the embodiments are within the scope of the present invention. In the accompanying drawings, various aspects of the present invention are illustrated to more clearly show the chip-scale packaging structures and methods for their formation. Common elements of the illustrated embodiments are designated with like reference numerals. The drawings are not meant to be illustrative of actual views of any particular portion of a chip-scale packaging structure, but are merely idealized schematic representations which are employed to more clearly and fully depict the invention in connection with the following description.

[0036] Illustrated in drawing **FIG. 1** is a semiconductor wafer **2** containing an array of semiconductor die locations **4** formed thereon using known fabrication techniques. Typically, the array of semiconductor die locations **4** is created as circuit layers **6** on and/or extending into one side of wafer **2**, forming an active surface **8** of the wafer **2**. **FIG. 1** shows that adjacent semiconductor die locations **4** are separated by streets **10** of semiconductor material providing areas for subsequently separating or "singulating" semiconductor die locations **4** into individual or discrete semiconductor dice **104** (**FIG. 2**), as will be described in further detail below. The opposite or back side of wafer **2** remains free of circuitry leaving a passive surface **12** comprised of the semiconductor material of wafer **2**. In this manner, many semiconductor devices may be formed and processed from wafer **2** at the same time.

[0037] Bond pads **14** are also formed on active surface **8** to provide external electrical contacts for the circuitry of each semiconductor die location **4**. As described above, bond pads **14** may be electrically connected to higher-level circuitry on a carrier substrate using various techniques, including flip-chip mounting, TAB, or conventional wire bonding. While not depicted in **FIG. 1**, bond pads **14** may include one or more layers of metallic material comprising an under-bump metallization (UBM). UBM is known in the art and is used to improve adhesion of tin/lead solder material of conductive bumps formed on bond pads **14** for flip-chip or TAB connection. Furthermore, although not depicted in **FIG. 1**, a known bond pad rerouting structure, often referred to as a redistribution layer (RDL), may be formed on active surface **8** to relocate connection points for the bond pads **14**. This may be required when bond pads **14** are not configured in a suitable pattern for attachment to a given carrier substrate or are too closely spaced, or pitched, to allow formation of conductive bumps. Accordingly, as used herein, the term "bond pads" encompasses bond pads formed directly on active surface **8** of wafer **2**, as well as exposed UBM or RDL surfaces which are configured for use as the external connection points of semiconductor die locations **4**.

[0038] Turning to **FIG. 2**, in a first embodiment of the present invention, channels **16** are formed in active surface **8** of wafer **2** to partially expose side surfaces **18** of semiconductor dice **104**. Channels **16** are initially formed along streets **10** between adjacent semiconductor die locations **4** (**FIG. 1**) by cutting with a dicing saw **20** or a laser beam **22** to a depth extending below circuit layers **6**.

[0039] **FIG. 3A** shows an enlarged view of a channel **16** cut with dicing-saw **20**. When separating semiconductor die locations **4** into individual semiconductor dice **104**, it is necessary to cut channel **16** with a dicing saw **20** having a width **24** that is smaller than the width **26** of streets **10**. As a result, a layer of semiconductor material remains uncut along the sides of channel **16** so circuit layers **6** are not exposed through side surfaces **18**, which may otherwise increase the possibility of circuit damage during cutting or later processing operations. Furthermore, diamond particles in dicing saw **20** may leave scratches **28** in the side surfaces **18** of semiconductor dice **104**. Scratches **28** introduce undesirable stress concentrations in side surfaces **18** that promote crack propagation in the semiconductor material. As previously discussed with respect to the present invention, scratches **28** are subsequently removed by an etching process. Therefore, dicing saw **20** is selected to have a width **24** wherein the combined saw-cutting and etching processes leave a sufficiently wide layer of undamaged semiconductor material between circuit layers **6** and side surfaces **18**. When cutting a wafer **2** having narrow street widths on the order of 100 microns, for example, the width **24** of dicing saw **20** may be about 40 microns. This leaves an initial layer of semiconductor material **30** on each side of channel **16** having a width **32** of about 30 microns between a periphery of circuit layers **6** and a side surface **18**.

[0040] **FIG. 3B** shows an enlarged view of a channel **16** cut with laser beam **22**. When channel **16** is cut in this manner, heat from laser beam **22** may negatively affect the semiconductor material along side surfaces **18**, leaving a heat-affected zone (HAZ) **34**. As with the above-described sawing process of the present invention, HAZ **34** is subsequently removed by an etching process. Therefore, laser beam **22** is selected to have a cutting width **36** wherein the combined laser-cutting and etching processes leave a layer of semiconductor material between circuit layers **6** and side surfaces **18**. When cutting street widths on the order of 100 microns, for example, the cutting width **36** of laser beam **22** may be about 25 microns. This leaves an initial layer of semiconductor material **30** on both sides of channel **16** having a width **32** of close to 40 microns between circuit layers **6** and side surfaces **18**. The specific widths described for dicing saw **20** and laser beam **22** are only exemplary, and may be provided with other widths depending on the amount of semiconductor material **30** that must be left on the sides of channel **16** to enable removal of material defects by subsequent etching.

[0041] **FIG. 4** shows that side surfaces **18** are etched back to remove the cutting defects while leaving a smooth, undamaged layer of semiconductor material **38** in place adjacent to circuit layers **6**. For the 100-micron streets described above, the remaining smooth layer of semiconductor material **38** may have a width **40**, for example, of about 5 microns between circuit layers **6** and side surfaces **18**. Any known process for etching semiconductor material may be used, such as by applying an anisotropic wet etch solution of aqueous tetramethylammonium hydroxide (TMAH) or potassium hydroxide (KOH) to side surfaces **18**. When etching narrow street widths of about 100 microns, it is currently preferable to use such an anisotropic etching process, which selectively etches specific crystallographic orientations, to prevent etching past the desired remaining layer of semiconductor material adjacent to circuit layers **6**.

[0042] After channels **16** have been cut and etched, **FIG. 5** shows that a protective coating **42** is formed on wafer **2** to cover active surface **8** and fill channels **16**. Protective coating **42** may comprise a liquid polymer sealant material

that is sprayed, spin coated or otherwise dispensed onto wafer **2** and then hardened by thermal or ambient temperature curing. One liquid polymer sealant material suitable for protective coating **42** is commercially available from 3D Systems, Inc. of Valencia, Calif., under the product name Acura SI **40**. **FIG. 5** shows that protective coating **42** is formed with apertures **44** exposing bond pads **14** in order to allow subsequent electrical connection. In order to form apertures **44**, the entire active surface **8** of wafer **2** may be covered, with apertures **44** being formed by subsequent removal of portions of protective coating **42**, such as by masking and etching protective coating **42**.

[**0043**] It is also possible that protective coating **42** may be formed on wafer **2** using a known stereolithographic process. In stereolithography, protective coating **42** may be formed by curing superimposed layers of a photocurable liquid polymer over active surface **8** by exposure to a source of electromagnetic radiation. Under this process, the photopolymer over bond pads **14** may be left uncured, thereby forming apertures **44** in protective coating **42**. Examples of stereolithographic processes suitable for forming protective coating **42** are described in U.S. Pat. No. 6,432,752 to Farnworth and U.S. Pat. No. 6,326,698 to Akram, the disclosures of which are incorporated herein by reference.

[**0044**] As previously discussed, conductive bumps **46** may sometimes be formed on bond pads **14** when electrical connection is accomplished by a flip-chip or TAB-type connection. **FIG. 5** shows such a conductive bump **46** formed on a bond pad **14** for purposes of illustration. While the present invention has been described in terms of forming protective coating **42** on wafer **2** prior to the addition of conductive bumps **46**, it is also possible that protective coating **42** may be formed with conductive bumps **46** already in place. Stereolithographic formation of protective coating **42** would be especially suitable for this alternative, because any liquid photopolymer on or over conductive bumps **46** could be left uncured to leave them exposed. Of course, protective coating **42** may, as where bond pads **14** are to be exposed, also be a conventional polymer sealant applied by a dispensing process, with portions of protective coating **42** being subsequently removed to expose conductive bumps **46**.

[**0045**] **FIG. 6** shows that once protective coating **42** is formed on active surface **8**, wafer **2** is cut along channels **16** to completely separate individual semiconductor dice **104**. Cutting may be accomplished with a dicing saw **48** having a width **50** that is narrower than channels **16**. With a wafer **2** having the above-described 100-micron streets, for example, dicing saw **48** may be about 40 microns wide. Side surfaces **18** are thus left covered with a layer **52** of protective coating **42** that is approximately equal to the amount of semiconductor material removed by the etching process. The present embodiment results in chip-scale packages **54**, each comprised of an individual semiconductor die **104** with protective coating **42** covering active surface **8** and side surfaces **18**. The remaining side surfaces **56** and passive surface **12** of a semiconductor die **104**, which are remote from circuit layers **6**, may be left exposed.

[**0046**] In some instances, however, it may be necessary or desirable to completely seal semiconductor dice **104**, such as when intended for use in extreme environments or when circuit layers **6** are highly sensitive to moisture. In a variation of the above-described embodiment, wafer **2** may be further processed prior to singulation in order to completely seal the individual semiconductor dice **104**.

[**0047**] Turning to **FIG. 7**, in this alternative, after protective coating **42** is formed on active surface **8**, wafer **2** is subjected to a backgrinding or other planarization process prior to being completely separated. This removes excess semiconductor material from passive surface **12** of wafer **2** to reduce the thickness of wafer **2** to a desired overall thickness. Several types of processes are available to perform the thinning of the wafer **2**. Either a mechanical grinding process or an abrasive planarization process such as chemical-mechanical planarization (CMP) may be used to remove material from passive surface **12** of wafer **2**. For example, in **FIG. 7**, a grinding wheel **60** may be applied to passive or backside surface **12** of wafer **2** to abrade material therefrom. Alternatively, passive surface **12** of wafer **2** may be chemically etched to remove material. The particular mechanism for thinning wafer **2** is considered to be a matter of convenience to those of ordinary skill in the semiconductor process manufacturing area. As seen in **FIG. 7**, semiconductor material is removed from passive surface **12** to a depth sufficient to expose protective coating **42** contained in channels **16**.

[**0048**] In **FIG. 8**, a second protective coating **62** is formed over passive surface **12**. Protective coating **62** may be formed of the same polymer material and by one of the same deposition or stereolithography processes as described above with respect to protective coating **42**. Wafer **2** is then cut along channels **16** to completely separate individual semiconductor dice **104**. **FIG. 9** shows that this variation of the first embodiment results in chip-scale packages **64**, each comprised of an individual semiconductor die **104** with protective coating **42** covering active surface **8** and side surfaces **18**, and second protective coating **62** covering passive surface **12** of each individual semiconductor die **104**. In other words, individual semiconductor dice **104** are substantially completely sealed from the outside environment.

[**0049**] **FIG. 10** shows a further variation of the first embodiment of the present invention. After exposing channels **16** by backgrinding or planarization, passive surface **12** of wafer **2** is etched to a depth such that a portion of protective coating **42** protrudes from passive surface **12** to form frame elements **66**. Any known process for etching semiconductor material may be used, as long as it selectively etches the semiconductor material of wafer **2** and leaves protective coating **42** in place, such as by using a TMAH etching solution with an additional constituent which reduces or eliminates etching of protective coating **42**. Second protective coating **62** is then formed as in **FIG. 8**, and wafer **2** is cut along channels **16** to completely separate individual semiconductor dice **104**. **FIG. 11** shows that this further variation to the first embodiment provides a chip-scale package **68** wherein frame elements **66** assist in anchoring second protective coating **62** in place, thereby improving the sealing of semiconductor dice **104**.

[**0050**] With either of the above-described variations to the first embodiment of the present invention, it is noted that exposing protective coating **42** within channels **16** through passive surface **12** also provides a mechanism for back side alignment of wafer **2** in subsequent processing. Convention-

ally, back side alignment of a wafer has been difficult because the pattern of semiconductor dice **104** along streets **10** is not visible on passive surface **12**. By exposing protective coating **42** through passive surface **12** in the present invention, the locations of semiconductor dice **104** may be easily viewed for alignment, such by an automated vision system having cameras that enable precision alignment using pattern recognition.

[**0051**] In a second embodiment according to the present invention shown in **FIG. 12**, protective coating **42** is deposited on active surface **8** of wafer **2** without prior formation of channels **16** in active surface **8**. Instead, channels **70** are formed in the passive surface **12** of wafer **2** after depositing protective coating **42** on active surface **8**. As with the first embodiment, channels **70** are initially formed along streets **10** between adjacent semiconductor die locations **4** (**FIG. 1**) by cutting with a dicing saw **20** or laser beam **22** to expose side surfaces **72** of semiconductor dice **104**. **FIG. 12** shows that channels **70** are similarly cut to a width such that an initial layer of semiconductor material **74** is left on both sides of channels **70**. In the second embodiment, channels **70** are cut to extend almost completely through wafer **2**, leaving only a small base portion **76** of wafer semiconductor material connecting adjacent semiconductor dice **104**.

[**0052**] Once the saw-cutting or laser-cutting process is complete, an etching process is carried out to remove the cutting-induced material defects in side surfaces **72** such as the scratches **28** or HAZ **34** described with respect to the first embodiment. As in the first embodiment, **FIG. 13** shows that side surfaces **72** are etched to a point leaving a smooth layer of semiconductor material **78** in place adjacent to circuit layers **6**. **FIG. 13** shows that the base portion **76** of semiconductor material is etched through to completely separate semiconductor dice **104** and expose protective coating **42** within channel **70**.

[**0053**] In the second embodiment of the present invention, a backgrinding or planarization process may also be carried out on passive surface **12** of wafer **2**. While removing semiconductor material from passive surface **12** is not required to expose protective coating **42** as in the first embodiment, it may be desirable for other reasons. Reducing the thickness of wafer **2**, for example, minimizes the final die size and reduces the time and expense associated with cutting wafer **2** during subsequent singulation into individual chip-scale packages. Furthermore, backgrinding or planarization may remove undesirable contaminants which may have been introduced into passive surface **12** of the wafer **2** during fabrication. With the second embodiment, removal of semiconductor material from passive surface **12** by a backgrinding or planarization process may be carried out prior to cutting channels **70**. Alternatively, the etching process itself can be carried out in such a way that the etching solution is applied to remove material from passive surface **12** at the same time side surfaces **72** and base portion **76** are etched within channels **70**.

[**0054**] **FIG. 14** shows that after channels **70** are cut and etched, and any desired removal of semiconductor material from passive surface **12** has been carried out, a second protective coating **80** is formed on wafer **2** to cover passive surface **12** and fill channels **70**. Once again, second protective coating **80** may be formed of the same polymer material and by the same deposition or stereolithography processes as described above with respect to protective coating **42**. Wafer **2** is then cut along channels **70** for separation into individual chip-scale packages **82**, as seen in **FIG. 15**. **FIG. 15** shows that the second embodiment chip-scale packages **82** are each comprised of an individual semiconductor die **104** with protective coating **42** covering active surface **8**, and second protective coating **80** covering side surfaces **72** and passive surface **12**.

[**0055**] All of the above-illustrated embodiments and variations thereof of the present invention provide chip-scale packaging for semiconductor dice with simplified and reduced sealing processes carried out at the wafer level. Furthermore, the side surfaces of the separated semiconductor dice include a substantially smooth layer of semiconductor material that is substantially free of the defects associated with prior art processes. Although the present invention has been depicted and described with respect to the illustrated embodiments, various additions, deletions and modifications are contemplated within its scope. The scope of the invention is, therefore, indicated by the appended claims rather than the foregoing description. Further, all changes which may fall within the meaning and range of equivalency of the claims and elements and features thereof are to be embraced within their scope.

What is claimed is:

1. A chip-scale package, comprising:

a semiconductor die having an active surface, an opposing passive surface, and a plurality of etched side surfaces extending from the active surface to the passive surface;

a first protective coating extending over the active surface of the semiconductor die; and

a second protective coating extending over the passive surface of the semiconductor die wherein one of the first protective coating and the second protective coating extends over the plurality of etched side surfaces of the semiconductor die.

2. The chip-scale package of claim 1, wherein the first protective coating extends over the plurality of etched side surfaces of the semiconductor die.

3. The chip-scale package of claim 2, wherein a portion of the first protective coating protrudes beyond the passive surface of the semiconductor die and a portion of the second protective coating is adhered to a side of the portion of the first protective coating protruding beyond the passive surface of the semiconductor die.

4. The chip-scale package of claim 1, wherein the second protective coating extends over the plurality of etched side surfaces of the semiconductor die.

5. The chip-scale package of claim 1, wherein at least one of the first protective coating and the second protective coating comprises a polymer sealant material.

6. The chip-scale package of claim 5, wherein the polymer sealant material comprises a photocurable polymer sealant material.

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