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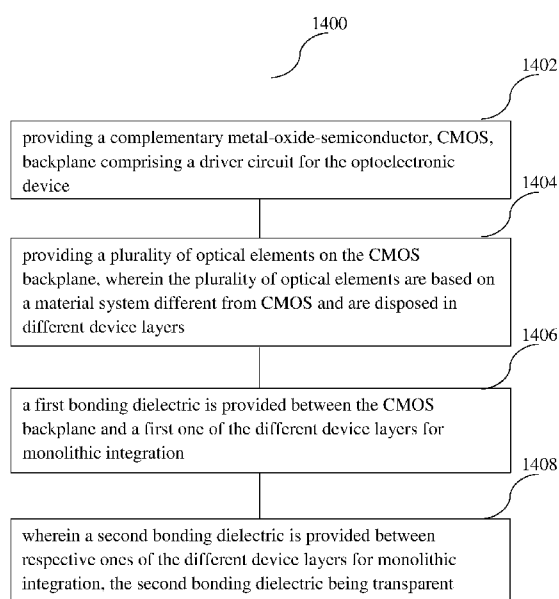


Figure 14

(57) Abstract: An integrated structure for an optoelectronic device and a method of fabricating an integrated structure for an optoelectronic device. The method comprises the steps of providing a complementary metal-oxide-semiconductor, CMOS, backplane comprising a driver circuit for the optoelectronic device; and providing a plurality of optical elements on the CMOS backplane, wherein the plurality of optical elements are based on a material system different from CMOS and are disposed in different device layers; wherein a first bonding dielectric is provided between the CMOS backplane and a first one of the different device layers for monolithic integration; and wherein a second bonding dielectric is provided between respective ones of the different device layers for monolithic integration, the second bonding dielectric being transparent.

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INTEGRATED STRUCTURE FOR AN OPTOELECTRONIC DEVICE AND METHOD OF FABRICATING THE SAME

FIELD OF INVENTION

5 The present invention relates broadly to an integrated structure for an optoelectronic device and to a method of fabricating an integrated structure for an optoelectronic device, in particular to a device architecture for monolithic full-color active-matrix micro-LED micro display with a CMOS backplane and the wafer-level manufacturing method to fabricate the same.

10 BACKGROUND

Any mention and/or discussion of prior art throughout the specification should not be considered, in any way, as an admission that this prior art is well known or forms part of common general knowledge in the field.

15 The conventional micro-display technologies, including liquid-crystal display, LCD, liquid crystal on silicon, LCOS, and active matrix organic light emitting diode, AMOLED, are generally not bright enough for today's augmented reality, AR, and head-up display, HUD, to see the images on a bright, sunlit day, nor efficient or compact enough to be used in wearable devices. Semiconductor-based micro-LED micro-display, on the other hand, naturally excels in brightness, contrast, speed, efficiency, reliability and compactness, which is highly attractive
20 nowadays for wearable electronics and automotive devices. Other technologies such as digital light processing, DLP, can be bright, but the form factor and power efficiency are not ideal for wearable device.

Recently, there have been substantial interests in inorganic micro-LED micro display with pitch size $<10\mu\text{m}$ for near-eye and automotive applications like AR, HUD, etc. Compared with the
25 conventional micro-display technologies (DLP, LCOS, organic light emitting diode, OLED, and LCD), micro-LED micro-display naturally excels in brightness, speed, efficiency, reliability and compactness, which is highly attractive for wearable electronics and automotive devices.

Although micro-LED micro displays are based on well-known and accepted core technologies
30 (III-V semiconductor and complementary metal-oxide-semiconductor, CMOS, technologies), the manufacturing has been challenging. At larger pitch size $>50\mu\text{m}$, R, G, B integration can be achieved through "pick and place" approach, i.e. individual micro-LEDs from separate epitaxial wafers (e.g. R, G, B) are transferred to the backplane in a massively parallel manner. However, when the pixel size shrinks to $<20\mu\text{m}$, such mass-transfer approaches become
35 impractical. Instead, the entire micro-display has to be manufactured at waferscale as a monolithic structure for low-cost high-volume production. However, the complex hybrid

integration involving nitride-based blue and green LEDs, arsenide-based red LEDs and the silicon-based CMOS poses significant manufacturing challenges.

Most of the prior attempts to resolve the monolithic R, G, B integration challenges involve innovations on the light emitting material, but face various practical limitations. For example, 5 glo leads the gallium nitride nano-wire micro- LED technology for full-color micro-displays. However, as they are limited by the small filling ratio of the emissive nano-wire tips (i.e. the actual volume of nano-wire material that emits light is only a small fraction of the total chip size), its brightness is grossly insufficient for state-of-the-art AR applications, which require up to 10^6 nits [1]. Ostendo attempts to integrate 3D heterogeneous electroluminescent LED 10 layers for the different RGB colors, but experiences fabrication difficulties in achieving independent control of R, G, B emission [2]. It is also worthwhile to note that both technologies try to obtain red emission on the gallium nitride material platform, which generally has low-efficiency and has ultra-wide spectrum leading to poor color rendering. Many others are working on color conversion technology, i.e. selectively patterning the color-conversion 15 quantum dots or quantum wells over the monochromatic blue/violet micro-LED arrays to down-convert the color to green and red [3]. However, the large thickness requirements for complete color conversion and the sidewall light leakage are common concerns with this approach, especially when the micro-LED shrinks to $<5\mu\text{m}$. Quantum dots also face thermal reliability and photochemical stability issues, which are usually infeasible for on-chip 20 integration. Thus, to date, how to get color on micro- LED micro-display remains an unresolved issue, especially when mass-manufacturability comes into the discussion.

Other than the technologies described above, which are all generally impractical for mass manufacturing, there is another competing technology, namely monolithic hybrid integration technology, showing decent manufacturability for single-color micro-LED arrays but 25 possessing significant challenges for RGB integration [4]. It utilizes wafer-level metal bonding technique to integrate R, G, B epitaxial, epi, on the integrated circuit, IC, wafer and uses standard semiconductor processing to pattern the micro-LEDs after each bonding. The R, G, B micro-LED arrays are interlaced and stacked, with each micro- LED individually connected to the driver circuit in the CMOS backplane. This technology faces a series of drawbacks, e.g. 30 yield loss due to the high-temperature high-pressure metal bonding process, the metal contamination during the pixel isolation, process compatibility with the bonding material, metal choices for balancing bonding quality and optical reflectance. Also, transferring the process to existing manufacturing infrastructure is difficult due to the involvement of CMOS-non-compatible metal in the bonding layer.

35 Embodiments of the present invention seek to address at least one of the above problems.

SUMMARY

In accordance with a first aspect of the present invention, there is provided an integrated structure for an optoelectronic device, the integrated structure comprising:

a complementary metal-oxide-semiconductor, CMOS, backplane comprising a driver circuit for the optoelectronic device;

a plurality of optical elements on the CMOS backplane, wherein the plurality of optical elements are based on a material system different from CMOS and are disposed in different device layers;

a first bonding dielectric provided between the CMOS backplane and a first one of the different device layers for monolithic integration; and

a second bonding dielectric provided between respective ones of the different device layers for monolithic integration, the second bonding dielectric being transparent.

10 In accordance with a first aspect of the present invention, there is provided a method of fabricating an integrated structure for an optoelectronic device, the method comprising the steps of:

providing a complementary metal-oxide-semiconductor, CMOS, backplane comprising a driver circuit for the optoelectronic device; and

15 providing a plurality of optical elements on the CMOS backplane, wherein the plurality of optical elements are based on a material system different from CMOS and are disposed in different device layers;

wherein a first bonding dielectric is provided between the CMOS backplane and a first one of the different device layers for monolithic integration; and

20 wherein a second bonding dielectric is provided between respective ones of the different device layers for monolithic integration, the second bonding dielectric being transparent.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will be better understood and readily apparent to one of ordinary skill in the art from the following written description, by way of example only, and in conjunction with the drawings, in which:

Fig. 1 shows a cross-sectional schematic drawing illustrating an integrated structure for an optoelectronic device in the form of a pixel structure for active-matrix micro-LED micro display with vertically stacked R, G, B micro-LEDs integrated through transparent dielectric bonding medium, according to an example embodiment.

Fig. 2 shows a cross-sectional schematic drawing illustrating different configurations to establish the electric interconnection in a pixel structure according to different embodiments.

Fig. 3 shows cross-sectional schematic drawings illustrating different structures for micro-LED for use in example embodiments.

Fig. 4 shows a cross-sectional schematic drawing illustrating an integrated structure for an optoelectronic device in the form of a pixel structure with R, G, B micro-LEDs interlaced horizontally, according to an example embodiment.

5 Fig. 5 shows a cross-sectional schematic drawing illustrating an integrated structure for an optoelectronic device in the form of a pixel structure for active-matrix micro-LED micro display with vertically stacked R, G, B micro-LEDs integrated through transparent dielectric bonding medium, according to an example embodiment.

10 Fig. 6 shows a cross-sectional schematic drawing illustrating different configurations to establish the electric interconnection in a pixel structure, according to different example embodiments.

Fig. 7 shows a cross-sectional schematic drawing illustrating an integrated structure for an optoelectronic device in the form of a pixel structure with R, G, B micro-LEDs interlaced horizontally, according to an example embodiment.

15 Fig. 8(a) shows a cross-sectional schematic drawing illustrating an integrated structure for an optoelectronic device in the form of a full-color micro-LED array with stacked R, G, B micro-LED layers integrated on CMOS backplane, according to an example embodiment.

Fig. 8(b) shows a cross-sectional schematic drawing illustrating an integrated structure for an optoelectronic device in the form of a full-color micro-LED array with stacked R, G, B micro-LED layers integrated on CMOS backplane, according to an example embodiment.

20 Fig. 9 shows a cross-sectional schematic drawing illustrating an integrated structuring within a single RGB pixel, including micro-lens, optical isolation trench, redundant tungsten plug, micro-structure patterned over the LED bottom, the current spreading metal pad on n-contact layer, according to example embodiments.

25 Fig. 10 shows cross-sectional schematic drawings illustrating processing steps in a fabrication method according to an example embodiment.

Fig. 11 shows cross-sectional schematic drawings illustrating processing steps in a fabrication method according to an example embodiment.

Fig. 12 shows cross-sectional schematic drawings illustrating processing steps in a fabrication method according to an example embodiment.

30 Fig. 13 shows cross-sectional schematic drawings illustrating processing steps in a fabrication method according to an example embodiment.

Fig. 14 shows a flowchart illustrating a method of fabricating an integrated structure for an optoelectronic device, according to an example embodiment.

DETAILED DESCRIPTION

Embodiments of the present invention provide a new device architecture and the mass-manufacturable approach to realize monolithic full-color micro-LED micro display without color conversion. The device according to an example embodiment features an array of R, G, B micro- LED pixels integrated on a silicon-based active-matrix display backplane, with each constituent micro-LED individually connected to and controlled by a pixel driver circuit in the backplane. Each pixel consists of vertically stacked native R, G, B micro-LEDs with the red LED at the bottom and the blue LED at the top. The R, G, B micro- LEDs are bonded through transparent dielectric medium, typically SiO₂, together with a long-pass reflector (e.g. distributed Bragg reflector, DBR,). The reflector is designed to transmit the long-wavelength light from the micro-LEDs below and reflect the short-wavelength light from the micro-LEDs above. Such vertical structure effectively addresses the resolution reduction issue commonly encountered in any monolithic RGB integration scheme, meanwhile optimizes the color rendering and color mixing with the micro-LED technology. The manufacturing method according to example embodiments is a CMOS compatible wafer-level process, based on multiple-transfers of epitaxial layers through dielectric wafer bonding process. For each color integration, the continuous epitaxial thin film is firstly bonded to the IC wafer via transparent dielectric medium, subsequently, micro-LEDs and the associated electrical connections are patterned using standard semiconductor processing. The detailed process flow according to example embodiments is designed to be CMOS compatible and readily transferred to the existing foundries for mass production.

The manufacturing approach according to example embodiments can overcome all the limitations with the prior-arts. First of all, an 8-inch, CMOS-compatible, wafer-level process can be provided according to an example embodiment, which promises low-cost large-scale mass production. Secondly, the process according to an example embodiment relies on highly established semiconductor processing and commercially available LED epitaxial wafers, which makes the process readily transferrable to the existing foundries. Thirdly, no precise bonding alignment is required, thus display resolution as high as 10000ppi is practically achievable according to an example embodiment.

In terms of device architecture, embodiments of the present invention can provide significant advantages. It is known that the emission efficiency of micro-LED reduces as the size shrinks due to the increased sidewall nonradiative recombination. Such reduction becomes exponential, particularly as the size <10 μ m. To accommodate R, G, B micro-LEDs in a same chip without compromising the display resolution, the current practice is to reduce the micro-LED size and arrange them in an interlaced manner. By doing that, one has to bear the consequence of significant reduction in brightness. The device structure according to example embodiments can effectively eliminate this issue. Meanwhile, the device structure according to example embodiments can also provide the optimal color mixing and reduces challenges for the integrated micro-optics design.

Other than the visible LED, invisible LED or other light-emitting devices, such as lasers, as well as light-detection devices are also applicable according to different example embodiments, without losing the generality.

Fig.1 shows a cross-sectional schematic drawing illustrating a pixel structure 100 according to an example embodiment, for active-matrix micro-LED micro display with vertically stacked R, G, B micro-LEDs 101-103 integrated through transparent dielectric bonding medium 111-113. The respective bottom n-contacts 121-123 of the micro-LED 101-103 is individually connected to the driver circuit (not shown) in the display backplane 124 and the respective top p-contacts 131-133 of the micro-LEDs 101-103 of the same color are connected to a common electrode (not shown). The common electrodes from different device layers can be interconnected.

The interconnect metal pad e.g. 141, which may be made from e.g. Al, Cu, etc., on the display backplane 124 can advantageously serve as an optical reflector. Respective interconnections 141-143 to the pixel driver circuits for the micro-LEDs 101-103 are provided in the display backplane 124.

The bottom contacts 121-123 advantageously function as reflectors, which are transparent to the light emitted from the micro-LED below it. The bottom contacts 121-123 can comprise doped epi and conductive material that forms ohmic contact with the epi. The bottom contact 121-123 functioning as optical reflectors preferably exhibit high optical reflectivity to the light emitted from the LEDs above, and high transmittance to the light emitted from the LEDs below it.

The transparent bonding dielectric medium 111-113 may comprise, for example, SiO₂, SiN, benzocyclobutene (BCB), etc. Dielectric insulating fillings 151-153, for example SiO₂, spin on glass, BCB, etc., are provided for each micro-LED 101-103.

In the micro-LEDs 101-103, respective epi 161-163 of different band gap energy are used, each consisting of doped epi at top and bottom portion and light emitting epi, e.g. quantum well, in between. The epi 163 in the top micro-LED 103 has the largest band gap energy and the epi 161 at the bottom micro-LED 101 has the smallest band gap energy. The respective bottom portions of the epi 161-163 devices are individually connected to the pixel driver in the backplane 124, via vertical interconnects e.g. 164, for example in the form of Tungsten plugs, interconnect metal pads e.g. 166, for example made from Al, Cu, etc., and electrical interconnections e.g. 168 that form ohmic contact with the micro-LED bottom contacts e.g. 123. The interconnection e.g. 168 comprise conductive material that establish vertical/horizontal connection (e.g. metal, tungsten, transparent conducting oxide), passivation, adhesion layers etc.

The respective top contacts 131-133 of the micro-LEDs 101-103 in the same layer of the micro-LED micro display are electrically connected to a common electrode (not shown) via electrical interconnections e.g. 170 that form ohmic contact with the micro-LED top contacts e.g. 133.

The interconnects e.g. 170 comprise conductive material that establish vertical/horizontal connection (e.g. metal, tungsten, transparent conducting oxide), passivation, adhesion etc.

Fig. 2 shows a cross-sectional schematic drawing illustrating different configurations to establish the electric interconnection in pixel structure 100, indicated as numeral 200 in Fig. 2, according to example embodiments, including transparent bonding dielectric e.g. 201 for monolithic integration. Also, transparent filling e.g. 203 is used again in the device layers.

It is noted that the different configurations for the electrical interconnection according to example embodiments as illustrated in Fig. 2 are generally applicable to any of the device layers in the pixel structure 200. They can be utilized in combination, and do not have to be identical among different device layers. These configurations are also applicable to other pixel structures described herein according to other embodiments of the present invention.

In a first configuration according to an example embodiments, a transparent conducting oxide 202 forms ohmic contact with the micro-LED epi 204. A passivation layer 205 is provided for electrical isolation from the bottom contact 207. Metal pad/line/nets 206, 208 serve as the current spreading structure that connects to the common electrode (not shown). The transparent conducting oxide 202 is connected to metal pad 206 which in turn is connected to the metal line/net 208 through a tungsten plug 210 in this example embodiment.

In another configuration according to an example embodiment, transparent conducting oxide 212 forms ohmic contact with the micro-LED epi 214. Metal pad/line/nets 216 in contact with the transparent conducting oxide 212 establish electrical connection with the common electrode (not shown).

In another configuration according to an example embodiment, metal pad 218 touches part of the micro-LED epi 220 top surface to establish ohmic contact with epi 220 and for electrical connection with the common electrode (not shown).

For the bottom contact interconnection according to an example embodiment for the epi 214, metal pad/line 222 is used to establish direct interconnection. It is noted that insulation and adhesion structures are not shown in Fig. 2, but their use is understood by a person skilled in the art.

In another configuration for the bottom contact interconnection according to an example embodiment for the epi 220, a tungsten plug 224 is used to make contact to a metal pad 226 on the bottom contact 228. In Fig. 2, this configuration is also used for the bottom contact interconnection for the epi 204.

Fig. 3 shows cross-sectional schematic drawings illustrating details of different structures for the micro-LEDs in the structure 100, 200 according to example embodiments.

The different structures for the micro-LEDs according to example embodiments as illustrated in Fig. 3 are generally applicable to any device layer in the structure 100, 200. They can be utilized in combination, and do not have to be identical among different device layers. These

configurations are also applicable to other pixel structures described herein according to other embodiments of the present invention.

In one configuration according to an example embodiment, the bottom contact 300 of the micro-LED 302 comprises a non-epi layer 304, which is conductive and forms ohmic contact with the doped epi 306. The non-epi layer 304 preferably exhibits high-reflectivity to the light emitted from the micro-LED 302. The micro-LED epi 308 in this configuration comprises light emitting epi layers 310 sandwiched between doped epi layers 306, 312, as is understood by a person skilled in the art.

In one configuration according to another example embodiment, the bottom contact 300 of the micro-LED 302 comprises a non-epi layer 314, which can, for example, comprise DBR, transparent conducting oxide, metal etc., or a combination. Non-epi layer 314 can be conductive for current spreading, or non-conductive. The non-epi layer 314 preferably exhibits high reflectivity for the light emitted from the micro-LED 302. The micro-LED epi 308 in this configuration comprises light emitting epi layers 316 sandwiched between doped epi layers 318, 320, as is understood by a person skilled in the art.

Fig. 4 shows a cross-sectional schematic drawing illustrating a pixel structure 400 according to another example embodiment with R, G, B micro-LEDs 401-403 interlaced horizontally. In this example embodiment, the interconnection metal e.g. 404 for the micro-LED e.g. 401 from the lower device level functions as bottom reflector for the micro-LEDs e.g. 402 in the upper device level. Again, transparent bonding dielectric e.g. 407, made from, for example, SiO₂, SiN, BCB, etc., are used for integrating the vertically stacking the micro-LEDs 401-403 in this example embodiment. Also, transparent filling e.g. 409 is used again in the device layers.

More specifically, in this example embodiment the interconnection metal e.g. 404 can function as a non-transparent bottom reflector for the micro-LEDs e.g. 402, with the micro-LEDs 401-403 placed interlaced horizontally. When the micro-LEDs 401-403 are horizontally interlaced, and the micro-LED bottom contact e.g. 406 is transparent, the interconnection metal e.g. 404 from the lower device layer can be used as bottom reflector for the upper device layer, as mentioned above. The separation between interconnection metal e.g. 404 and micro-LED epi e.g. 408 can preferably be engineered to achieve optimal reflection condition according to an example embodiment, i.e. can be provided as an optical detected resonance, ODR, structure. In an example embodiment, the 3D arrangement of micro-LEDs and interconnects is preferably optimized to maximize the filling ratio and current loading capability. When R,G, B micro-LEDs 401-403 are horizontally interlaced, the color sequence from top layer to the bottom layer does not have to be B, G, R as described above for the pixel structure 100, 200.

It is noted that the horizontally interlaced configuration and the overlapped configuration (compare Figs. 1 and 2) can be implemented simultaneously within the same micro-LED micro display in different example embodiments.

In the pixel structure 400, the bottom contact e.g. 410 can still be implemented to function as a reflector. For example, a non-epi layer (compare Fig. 3) such as DBR, microstructure can still be implemented to further enhance the bottom reflection and light extraction. Transparent current spreading layer(s) (compare Fig. 2) can optionally be included. For the common electrode (not shown) interconnection metal pad/line/net e.g. 412 are provided in an example embodiment to connect the top-contacts of micro-LEDs e.g. 403 in the same device layer to a common electrode (not shown). The common electrodes from different device layers can be interconnected.

Fig. 5 shows a cross-sectional schematic drawing illustrating a pixel structure 500 for active-matrix micro-LED micro display with vertically stacked R, G, B micro-LEDs integrated through transparent dielectric bonding medium, according to an example embodiment. The top p-contact e.g. 502 of each micro-LED e.g. 504 is individually connected to the driver circuit (not shown) in the display backplane 506. The bottom n-contact e.g. 508 of each micro-LED e.g. 504 of the same color are continuous, with opening window(s) e.g. 510 for the p-contact interconnection(s) e.g. 512. Also, transparent filling e.g. 513 is used again in the device layers.

In this example embodiment, the micro-LED epi e.g. 514 on top has larger bandgap energy than the micro-LED epi e.g. 516 below.

Again, transparent bonding dielectric e.g. 518, made from, for example, SiO₂, SiN, BCB, etc., are used for integrating the vertically stacking the micro-LEDs 504, 520, 522 in this example embodiment.

In this embodiment, the bottom n-contact e.g. 508 is implemented as a common electrode layer, which is electrically conductive and optically transparent to the light emitted from the micro-LED e.g. 516 below it. The n-contact e.g. 508 can comprise part of doped portions of the micro-LED epi e.g. 514, and conductive material that forms ohmic contact with the micro-LED epi e.g. 514, and functions as an optical reflector that preferably exhibits high optical reflectivity to the light emitted from the LEDs e.g. 504 above, and high transmittance to the light emitted from the LEDs e.g. 520 below it. In this embodiment, the n-contact e.g. 508 is electrically continuous.

For the bottom micro-LED 522 layer, non-transparent metal can be implemented as the ohmic n-contact 524 functioning as optical reflector.

Optical isolation trenches can be incorporated in the contacts e.g. 508, 524 layers to prevent optical crosstalk between pixels. Metal pads, lines, or nets can be patterned in direct contact with the top of the n-contacts e.g. 508, 524 layers to enhance the current spreading.

The p-contacts e.g. 502 provide the electrical interconnection with appropriate composition, including ohmic contact, vertical interconnects e.g. 512, horizontal interconnects, passivation, adhesion etc. The conductive part of the p-contact e.g. 502 can comprise one or more electrically conducting materials, e.g. metal or transparent conducting material etc..

Fig. 6 shows a cross-sectional schematic drawing illustrating different configurations to establish the electric interconnection in pixel structure 500, indicated as numeral 600 in Fig. 6, according to example embodiments, including transparent bonding dielectric e.g. 601 for monolithic integration. Also, transparent filling e.g. 603 is used again in the device layers.

5 It is noted that the different configurations for the electrical interconnection as illustrated in Fig. 6 are generally applicable to any of the device layers in the pixel structure 600. They can be utilized in combination, and do not have to be identical among different device layers. These configurations are also applicable to other pixel structures described herein according to other embodiments of the present invention.

10 In one configuration according to an example embodiment, metal or transparent conducting oxide interconnect 602 is used to directly connect the micro-LED 604 top contact and the driver circuit (not shown) in the display backplane 606.

In one configuration according to another example embodiment, transparent conducting oxide 608 is used to form ohmic contact with the micro-LED epi 610. Metal pad 612 in contact with
15 the transparent conduction oxide 608 establishes electrical connection with the tungsten plug 614.

In one configuration according to another example embodiment, metal pad 616 touches part of the micro-LED epi 618 top surface and forms ohmic contact with the micro-LED epi 618. The metal pad 616 is connected with the tungsten plug 620 that is used for vertical interconnection.

20 Fig. 7 shows a cross-sectional schematic drawing illustrating a pixel structure 700 with R, G, B micro-LEDs interlaced horizontally, according to an example embodiment. In this embodiment, the interconnection metal pad e.g. 702 functions as bottom reflector for the micro-LEDs e.g. 704 in the layer above. Again, transparent bonding dielectric e.g. 703 is used for monolithic integration. Also, transparent filling e.g. 707 is used again in the device layers.

25 More specifically, when the micro-LEDs 704-706 are horizontally interlaced, the interconnection metal pad e.g. 702 from the lower device layer can be utilized as bottom reflector of the micro-LED e.g. 704 at upper device layer. The separation between the metal pad e.g. 702 and the micro-LED epi e.g. 708 can preferably be engineered to achieve optimal reflection condition, i.e. providing an ODR structure. In an example embodiment, the 3D
30 arrangement of micro-LEDs and interconnects is optimized to maximize the filling ratio and current loading capability. When R, G, B micro-LEDs are horizontally interlaced, the color sequence from top layer to the bottom layer does not have to be B, G, R.

It is noted that horizontally interlaced micro-LEDs and overlapped micro-LEDs (compare Figs. 5 and 6) can be implemented simultaneously within the same micro-LED micro display. It is
35 noted that when R,G, B micro-LEDs 704-706 are horizontally interlaced in this example embodiment, the color sequence from top layer to the bottom layer does not have to be B, G, R.

In the pixel structure 700, the bottom contact e.g. 710 can still be implemented to function as a reflector. For example, a non-epi layer (compare Fig. 3) such as DBR, micro-structure can still be implemented to further enhance the bottom reflection and light extraction in an example embodiment. Transparent current spreading layer(s) (compare Fig. 6) are preferably used.

5 Fig. 8a) shows a cross-sectional schematic drawing illustrating a full-color micro-LED array 800 with stacked R, G, B micro-LED 801-803 layers integrated on CMOS backplane 804, according to an example embodiment. Each micro-LED 801-803 is individually connected to a pixel driver circuit (not shown) in the CMOS backplane 804 and shares a common bias with micro-LEDs within the same device layer. In different embodiments of a full-color micro LED
10 array, an interlaced pixel structure according to example embodiments described above can be used. It is noted that the bonding dielectric used for the integration of the device layers according to example embodiments are not explicitly shown in Fig. 8. Instead, the bonding dielectric is “merged” with the transparent filling e.g. 806 in Fig. 8a). Top contacts e.g. 808 of micro-LEDs e.g. 803 of the same device layer are connected to a common electrode, indicated
15 as line 810 in Fig. 8a). The corresponding bias voltages V_{bias1} V_{bias2} V_{bias3} can be the same or different, depending on the CMOS driver circuit design, as is understood by a person skilled in the art.

Fig. 8b) shows a cross-sectional schematic drawing illustrating a full-color micro-LED array 850 with stacked R, G, B micro-LED 851-853 layers integrated on CMOS backplane 854, according to an example embodiment. Each micro-LED 851-853 is individually connected to a pixel driver circuit (not shown) in the CMOS backplane 854 and shares a common bias with micro-LEDs within the same device layer. In different embodiments of a full-color micro LED
20 array, an interlaced pixel structure according to example embodiments described above can be used. It is noted that the bonding dielectric used for the integration of the device layers according to example embodiments are not explicitly shown in Fig. 8.b). Instead, the bonding dielectric is “merged” with the transparent filling e.g. 856 in Fig. 8b).

Bottom contacts e.g. 858 of micro-LEDs e.g. 851 of the same device layer are connected to a common electrode, indicated as line 860 in Fig. 8b). The corresponding bias voltages V_{bias1} V_{bias2} V_{bias3} can be the same or different, depending on the CMOS driver circuit design, as is
30 understood by a person skilled in the art.

Fig. 9 shows a cross-sectional schematic drawing illustrating an integrated structuring within a single RGB pixel 900, including micro-lens 902, optical isolation trench 904, redundant tungsten plug e.g. 906, back reflector e.g. 908 with micro-structure pattern on the micro-LED e.g. 910 bottom, and current spreading metal pad e.g. 912 on n-contact e.g. 914 layer, according
35 to an example embodiment. In various embodiments, integrated pixel structure does not necessarily include all, but can be any combination of those features, depending e.g. on the fabrication complexity and device performance required.

It is noted that the bonding dielectric used for the integration of the device layers according to example embodiments are not explicitly shown in Fig. 9. Instead, the bonding dielectric is
40 “merged” with the transparent filling e.g. 915 in Fig. 9.

Spacer 916 can be provided to adjust the separation between microlens 902 and the LEDs e.g. 910 transparent ohmic contact (e.g. ITO), the transparent back reflector e.g. 908 (e.g. DBR) with micro-structure pattern. The redundant tungsten plug e.g. 906 can be provided for light blocking to prevent inter-pixel crosstalk. Metal pad e.g. 912, for example Al, in direct contact with the n-contact e.g. 914 can be provided to improve the current spreading. Optical isolation trench e.g. 904 etching through the common n-contact e.g. 914 layer. The trench e.g. 904 features segments without forming closed loop to ensure electrical continuity among all the micro-LEDs in each device layer. It is noted that a current spreading, ohmic contact, back reflector layer 908 with micro-pattern for the bottom device layer can comprise a non-transparent metal. An optical isolation trench 918 etched through the epi 920 in the bottom device layer can be provided, stopped at the bottom current spreading ohmic contact, back reflector layer 921.

IC electrode pad 924 of the CMOS backplane 922, can serve as optical reflector for the bottom micro-LED 926 if the current spreading, ohmic contact, back reflector layer 921 is transparent.

Fig. 10 shows cross-sectional schematic drawings illustrating a fabrication process according to an example embodiment for fabricating the pixel structure 100, 200 as an example, noting that the same procedure can be employed for realizing pixel structures 400, 500, 600, 700, 900. Similarly, the same procedure can be employed for realizing the full-color micro-LED array 800, 850.

On a substrate 1000, which can be the as-grown epi substrate or a handle wafer, the epitaxial material 1002 with light emitting layers (e.g. quantum well) incorporated and doped contact layer at top and bottom of the light emitting layers is provided. Contact and reflector layer 1004 is also provided, which can comprise of part of doped epi, conductive material that forms ohmic contact with the epi, optical reflector with desired reflection and transmission characteristics, and micro-structures (periodic, such as Bragg grating structures or photonic crystal structures, or non-periodic).

A pixel set 1006 with independent driver circuit for R, G, B is provided in a CMOS driver circuit wafer 1008, with electrical pads e.g. 1010 provided for interconnection.

Dielectric wafer bonding with a transparent bonding dielectric 1011 is used between the substrate 1000 (face down) and the CMOS driver circuit wafer 1008 (face up), followed by substrate 1000 removal, yielding the structure 1012.

With reference to Fig. 11, dry etching is used to pixelate micro-LEDs e.g. 1014, followed by establishing ohmic contact to the micro-LED e.g. 1014 epi 1016, including establishing electrical connection e.g. 1018 between the micro-LED e.g. 1014 and the driver circuit in the CMOS driver circuit wafer 1008, and simultaneously forming vertical interconnects e.g. 1020 (for example tungsten plug) for the micro-LEDs (not shown) in the next device layer(s) to be integrated. Also, transparent filling e.g. 1021 is provided in the device layers.

With reference to Fig. 12, the second epi-layer 1022 and contact and reflector layer 1024 is integrated through dielectric wafer bonding using a transparent bonding dielectric 1025, correspondingly to the dielectric wafer bonding between CMOS driver circuit wafer 1008 and substrate 1000 with reference to Fig. 10, including substrate removal. Next the micro-LEDs e.g. 1026 of second device layer are patterned and associated electrical connection and ohmic contacts are formed, correspondingly to what has been described above with reference to Fig. 11 for the first device layer.

With reference to Fig. 13, the third epi-layer 1028 and contact and reflector layer 1030 is integrated through dielectric wafer bonding using a transparent bonding dielectric 1031, again correspondingly to the dielectric wafer bonding between CMOS driver circuit wafer 1008 and substrate 1000 with reference to Fig. 10, including substrate removal. Next the micro-LEDs e.g. 1032 of third device layer are patterned and associated electrical connection and ohmic contacts are formed, correspondingly to what has been described above with reference to Fig. 11 for the first device layer.

In one embodiment, an integrated structure for an optoelectronic device is provided, the integrated structure comprising a complementary metal-oxide-semiconductor, CMOS, backplane comprising a driver circuit for the optoelectronic device; a plurality of optical elements on the CMOS backplane, wherein the plurality of optical elements are based on a material system different from CMOS and are disposed in different device layers; a first bonding dielectric provided between the CMOS backplane and a first one of the different device layers for monolithic integration; and a second bonding dielectric provided between respective ones of the different device layers for monolithic integration, the second bonding dielectric being transparent.

The second bonding dielectric may be the same as the first bonding dielectric.

Each device layer may comprise a reflector disposed below a first optical element in said each device layer, wherein the reflector is configured to be reflective at a first operating wavelength range of a first optical element. The reflector may be configured to be transmissive at a second operating wavelength range of a second optical element in a lower device layer. The reflector may comprise a distributed Bragg reflector, DBR. At least a portion of an electrical interconnection metal in each device layer may function as the reflector.

Respective top contacts of the optical elements in the same device layer may be connected to a common top electrode, and respective bottom contacts of the optical elements in the same device layer are individually connected to the driver circuit.

Respective bottom contacts of the optical elements in the same device layer may be connected to a common electrode, and respective top contacts of the optical elements in the same device layer are individually connected to the driver circuit. The integrated structure may comprise micro-trenches patterned between optical elements in the same device layer through the common bottom electrode to achieve optical isolation between the optical elements in the same device layer without breaking the electrical continuity of the common bottom electrode. The

integrated structure may comprise metal pads, lines or net patterned on the common bottom electrode with direct electrical contact to enhance current spreading.

The integrated structure may comprise micro-structures patterned on respective bottom layers of the optical elements to enhance a light extraction from the optical elements.

- 5 The integrated structure may comprise a photonic crystal structure patterned on respective bottom layers of the optical elements to increase an emission directionality of light from the optical elements.

At least some of the optical elements in different device layer may be horizontally interlaced.

At least some of the optical elements in different device layer may at least partially overlap.

- 10 The optical devices may comprise at least partially overlapping RGB micro-light emitting diodes, micro-LEDs, in a pixel arrangement for enhancing color mixing.

The integrated structure may further comprise electrical interconnections including one or more of a group consisting of chemical mechanical planarization based contact, tungsten plug, and metal pad.

- 15 The integrated structure may further comprise at least one micro-lens to assist light collimation.

The integrated structure may comprise one or more redundant tungsten plugs to prevent crosstalk between adjacent optical elements.

- Fig. 14 shows a flowchart 1400 illustrating a method of fabricating an integrated structure for an optoelectronic device, according to an example embodiment. At step 1402, a complementary metal-oxide-semiconductor, CMOS, backplane comprising a driver circuit for the optoelectronic device is provided. At step 1404, a plurality of optical elements are provided on the CMOS backplane, wherein the plurality of optical elements are based on a material system different from CMOS and are disposed in different device layer. At step 1406, a first bonding dielectric is provided between the CMOS backplane and a first one of the different device layers for monolithic integration. At step 1408, a second bonding dielectric is provided between respective ones of the different device layers for monolithic integration, the second bonding dielectric being transparent.

The second bonding dielectric may be the same as the first bonding dielectric.

- 30 The method may comprise providing, in each device layer, a reflector disposed below a first optical element in said each device layer, wherein the reflector is configured to be reflective at a first operating wavelength range of a first optical element. The reflector may be configured to be transmissive at a second operating wavelength range of a second optical element in a lower device layer. The reflector may comprise a distributed Bragg reflector, DBR.

- 35 The method may comprise providing, in each device layer, an electrical interconnection metal, wherein at least a portion of an electrical interconnection metal functions as the reflector.

The method may comprise connecting respective top contacts of the optical elements in the same device layer to a common top electrode, and connecting respective bottom contacts of the optical elements in the same device layer individually to the driver circuit.

5 The method may comprise connecting respective bottom contacts of the optical elements in the same device layer to a common electrode, and connecting respective top contacts of the optical elements in the same device layer individually to the driver circuit. The method may comprise patterning micro-trenches between optical elements in the same device layer through the common bottom electrode to achieve optical isolation between the optical elements in the same device layer without breaking the electrical continuity of the common bottom electrode. The
10 method may comprise patterning metal pads, lines or net on the common bottom electrode with direct electrical contact to enhance current spreading.

The method may comprise patterning micro-structures on respective bottom layers of the optical elements to enhance a light extraction from the optical elements.

15 The method may comprise patterning a photonic crystal structure on respective bottom layers of the optical elements to increase an emission directionality of light from the optical elements.

The method may comprise horizontally interlacing at least some of the optical elements in different device layer.

20 The method may comprise at least partially overlapping at least some of the optical elements in different device layer. The method may comprise at least partially overlapping RGB micro-light emitting diodes, micro-LEDs, in a pixel arrangement for enhancing color mixing.

The method may further comprise providing electrical interconnections including one or more of a group consisting of chemical mechanical planarization based contact, tungsten plug, and metal pad.

25 The method may further comprise providing at least one micro-lens to assist light collimation.
The method may comprise providing one or more redundant tungsten plugs to prevent crosstalk between adjacent optical elements.

Industrial Applications

30 The monolithic full-color active matrix micro-LED micro-display according to example embodiments is particularly interesting for, but not limited to, AR, HUD applications which require compact, efficient, high-resolution (>1000ppi) and high-brightness (>500,000 nits) full-color micro-display. It can also be used in mobile or wearable video projector with extensive application examples.

35 The above description of illustrated embodiments of the systems and methods is not intended to be exhaustive or to limit the systems and methods to the precise forms disclosed. While specific embodiments of, and examples for, the systems components and methods are described herein for illustrative purposes, various equivalent modifications are possible within the scope

of the systems, components and methods, as those skilled in the relevant art will recognize. The teachings of the systems and methods provided herein can be applied to other processing systems and methods, not only for the systems and methods described above.

For example, the device architecture and fabrication approach according to example
 5 embodiments can be implemented to any other apparatus, including any other semiconductor apparatus, that requires hybrid integration of optoelectronic device of different material systems on the CMOS wafer, for example, stacking R, G, B vertical cavity surface emitting laser, VCSEL, to give a white laser or integrating visible and infra-red, IR, LEDs for video projection and 3D scanning. Also, other than light-emitting devices, embodiments of the
 10 present invention can also be implemented to light detection systems such as focal plane array or hybrid integration of display and sensor.

The elements and acts of the various embodiments described above can be combined to provide further embodiments. These and other changes can be made to the systems and methods in light of the above detailed description.

15 In general, in the following claims, the terms used should not be construed to limit the systems and methods to the specific embodiments disclosed in the specification and the claims, but should be construed to include all processing systems that operate under the claims. Accordingly, the systems and methods are not limited by the disclosure, but instead the scope of the systems and methods is to be determined entirely by the claims.

20 Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense as opposed to an exclusive or exhaustive sense; that is to say, in a sense of "including, but not limited to." Words using the singular or plural number also include the plural or singular number respectively. Additionally, the words "herein," "hereunder," "above," "below," and
 25 words of similar import refer to this application as a whole and not to any particular portions of this application. When the word "or" is used in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list and any combination of the items in the list.

References

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- [3] H.-V. Han et al. "Resonant-enhanced full-color emission of quantum-dot-based micro LED
 35 display technology" Optics Express 23, 32504 (2015)
- [4] Chong et al. "Making Semiconductor devices by stacking strata of micro LEDs", International Publication Number WO 2018/175338 (2018)

CLAIMS

1. An integrated structure for an optoelectronic device, the integrated structure comprising:

a complementary metal-oxide-semiconductor, CMOS, backplane comprising a driver circuit
5 for the optoelectronic device;

a plurality of optical elements on the CMOS backplane, wherein the plurality of optical elements are based on a material system different from CMOS and are disposed in different device layers;

a first bonding dielectric provided between the CMOS backplane and a first one of the different
10 device layers for monolithic integration; and

a second bonding dielectric provided between respective ones of the different device layers for monolithic integration, the second bonding dielectric being transparent.

2. The integrated structure of claim 1, wherein the second bonding dielectric is the same as the first bonding dielectric.

3. The integrated structure claims 1 or 2, wherein each device layer comprises a reflector disposed below a first optical element in said each device layer, wherein the reflector is configured to be reflective at a first operating wavelength range of a first optical element.
15

4. The integrated structure of claim 3, wherein the reflector is configured to be transmissive at a second operating wavelength range of a second optical element in a lower
20 device layer.

5. The integrated structure of claims 3 or 4, wherein the reflector comprises a distributed Bragg reflector, DBR.

6. The integrated structure of any one of claims 3 to 5, wherein at least a portion of an electrical interconnection metal in each device layer functions as the reflector.

7. The integrated structure of any one of claims 1 to 6, wherein respective top contacts of the optical elements in the same device layer are connected to a common top electrode, and respective bottom contacts of the optical elements in the same device layer are individually connected to the driver circuit.
25

8. The integrated structure of any one of claims 1 to 6, wherein respective bottom contacts of the optical elements in the same device layer are connected to a common electrode, and respective top contacts of the optical elements in the same device layer are individually connected to the driver circuit.
30

9. The integrated structure of claim 8, comprising micro-trenches patterned between optical elements in the same device layer through the common bottom electrode to achieve

optical isolation between the optical elements in the same device layer without breaking the electrical continuity of the common bottom electrode.

10. The integrated structure of claims 8 or 9, comprising metal pads, lines or net patterned on the common bottom electrode with direct electrical contact to enhance current spreading.
- 5 11. The integrated structure of any one of claims 7 to 10, comprising micro-structures patterned on respective bottom layers of the optical elements to enhance a light extraction from the optical elements.
- 10 12. The integrated structure of any one of claims 7 to 11, comprising a photonic crystal structure patterned on respective bottom layers of the optical elements to increase an emission directionality of light from the optical elements.
13. The integrated structure of any one of claims 1 to 12, wherein at least some of the optical elements in different device layer are horizontally interlaced.
14. The integrated structure of any one of claims 1 to 13, wherein at least some of the optical elements in different device layer at least partially overlap.
- 15 15. The integrated structure of claim 14, wherein the optical devices comprise at least partially overlapping RGB micro-light emitting diodes, micro-LEDs, in a pixel arrangement for enhancing color mixing.
- 20 16. The integrated structure of any one of the preceding claims, further comprising electrical interconnections including one or more of a group consisting of chemical mechanical planarization based contact, tungsten plug, and metal pad.
17. The integrated structure of any one of the preceding claims, further comprising at least one micro-lens to assist light collimation.
18. The integrated structure of any one of the preceding claims, comprising one or more redundant tungsten plugs to prevent crosstalk between adjacent optical elements.
- 25 19. A method of fabricating an integrated structure for an optoelectronic device, the method comprising the steps of:

providing a complementary metal-oxide-semiconductor, CMOS, backplane comprising a driver circuit for the optoelectronic device; and

providing a plurality of optical elements on the CMOS backplane, wherein the plurality of

30 optical elements are based on a material system different from CMOS and are disposed in different device layers;

wherein a first bonding dielectric is provided between the CMOS backplane and a first one of the different device layers for monolithic integration; and

wherein a second bonding dielectric is provided between respective ones of the different device layers for monolithic integration, the second bonding dielectric being transparent.

20. The method of claim 19, wherein the second bonding dielectric is the same as the first bonding dielectric.

5 21. The method of claims 19 or 20, comprising providing, in each device layer, a reflector disposed below a first optical element in said each device layer, wherein the reflector is configured to be reflective at a first operating wavelength range of a first optical element.

22. The method of claim 21, wherein the reflector is configured to be transmissive at a second operating wavelength range of a second optical element in a lower device layer.

10 23. The method of claims 21 or 22, wherein the reflector comprises a distributed Bragg reflector, DBR.

24. The method of any one of claims 21 to 23, comprising providing, in each device layer, an electrical interconnection metal, wherein at least a portion of an electrical interconnection metal functions as the reflector.

15 25. The method of any one of claims 19 to 24, comprising connecting respective top contacts of the optical elements in the same device layer to a common top electrode, and connecting respective bottom contacts of the optical elements in the same device layer individually to the driver circuit.

20 26. The method of any one of claims 19 to 24, comprising connecting respective bottom contacts of the optical elements in the same device layer to a common electrode, and connecting respective top contacts of the optical elements in the same device layer individually to the driver circuit.

25 27. The method of claim 26, comprising patterning micro-trenches between optical elements in the same device layer through the common bottom electrode to achieve optical isolation between the optical elements in the same device layer without breaking the electrical continuity of the common bottom electrode.

28. The method of claims 26 or 27, comprising patterning metal pads, lines or net on the common bottom electrode with direct electrical contact to enhance current spreading.

30 29. The method of any one of claims 25 to 28, comprising patterning micro-structures on respective bottom layers of the optical elements to enhance a light extraction from the optical elements.

30. The method of any one of claims 25 to 29, comprising patterning a photonic crystal structure on respective bottom layers of the optical elements to increase an emission directionality of light from the optical elements.

31. The method of any one of claims 19 to 30, comprising horizontally interlacing at least some of the optical elements in different device layer.
32. The method of any one of claims 19 to 31, comprising at least partially overlapping at least some of the optical elements in different device layer.
- 5 33. The method of claim 32, comprising at least partially overlapping RGB micro-light emitting diodes, micro-LEDs, in a pixel arrangement for enhancing color mixing.
34. The method of any one of claims 19 to 33, further comprising providing electrical interconnections including one or more of a group consisting of chemical mechanical planarization based contact, tungsten plug, and metal pad.
- 10 35. The method of any one of claims 19 to 34, further comprising providing at least one micro-lens to assist light collimation.
36. The method of any one of the preceding claims, comprising providing one or more redundant tungsten plugs to prevent crosstalk between adjacent optical elements.

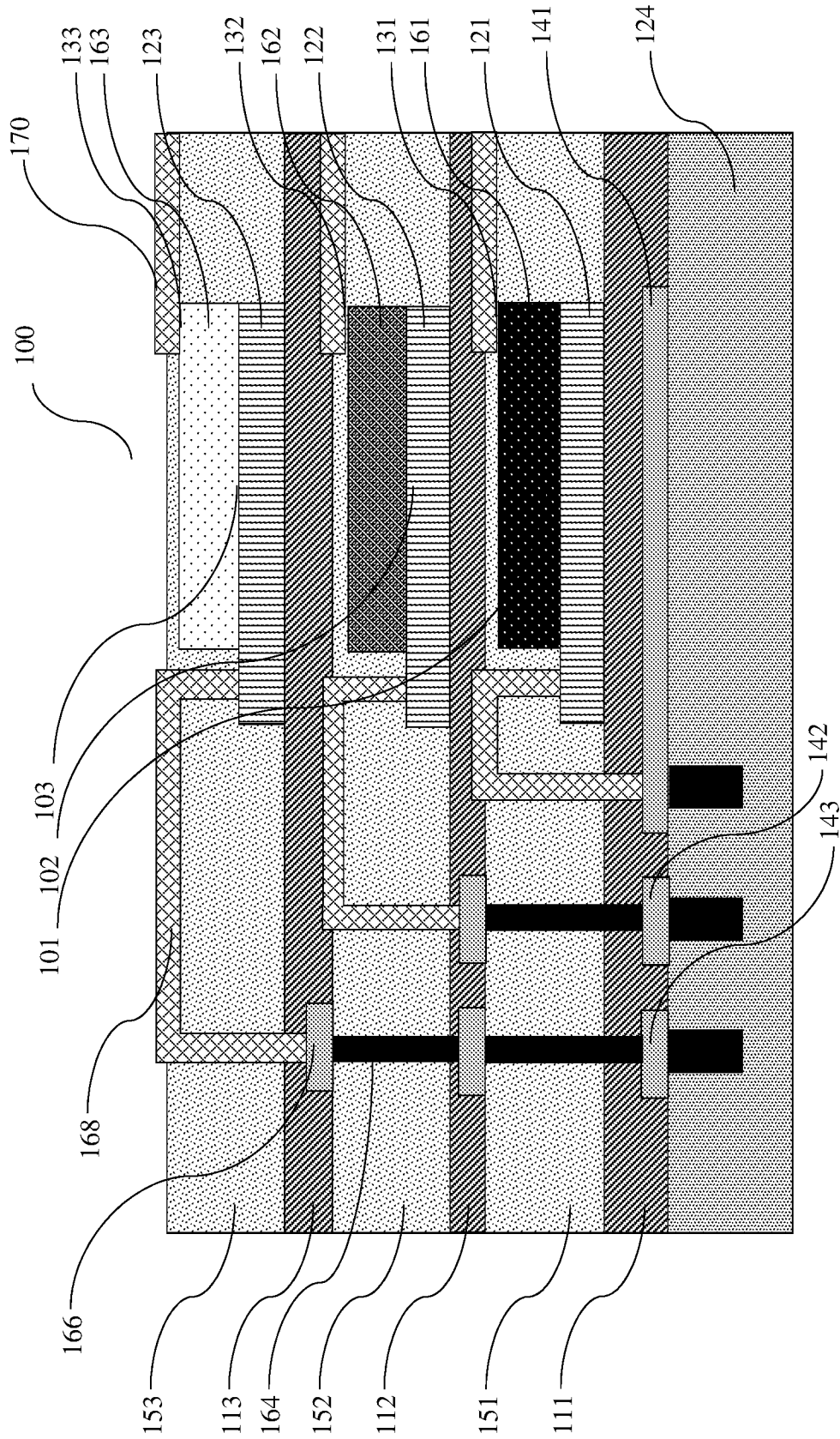


Figure 1

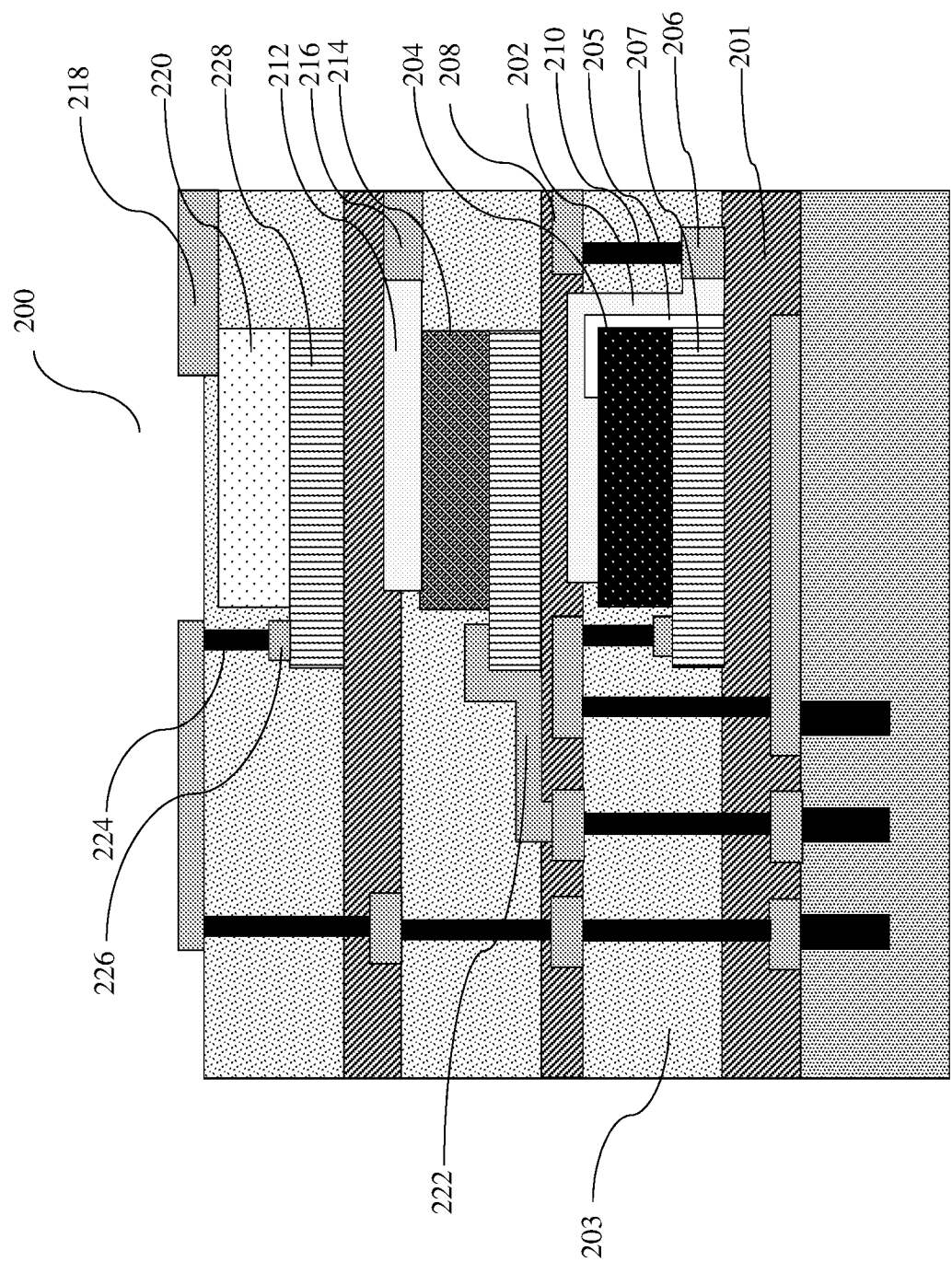


Figure 2

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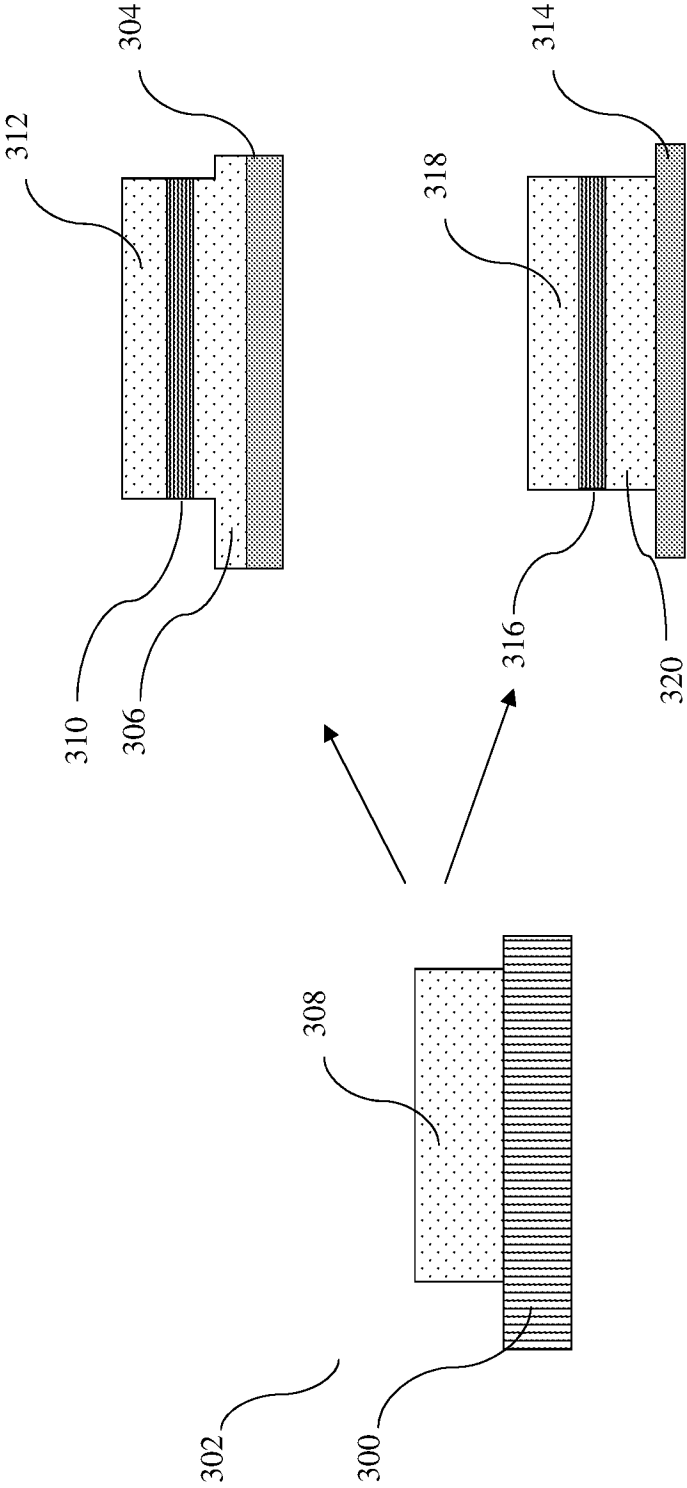


Figure 3

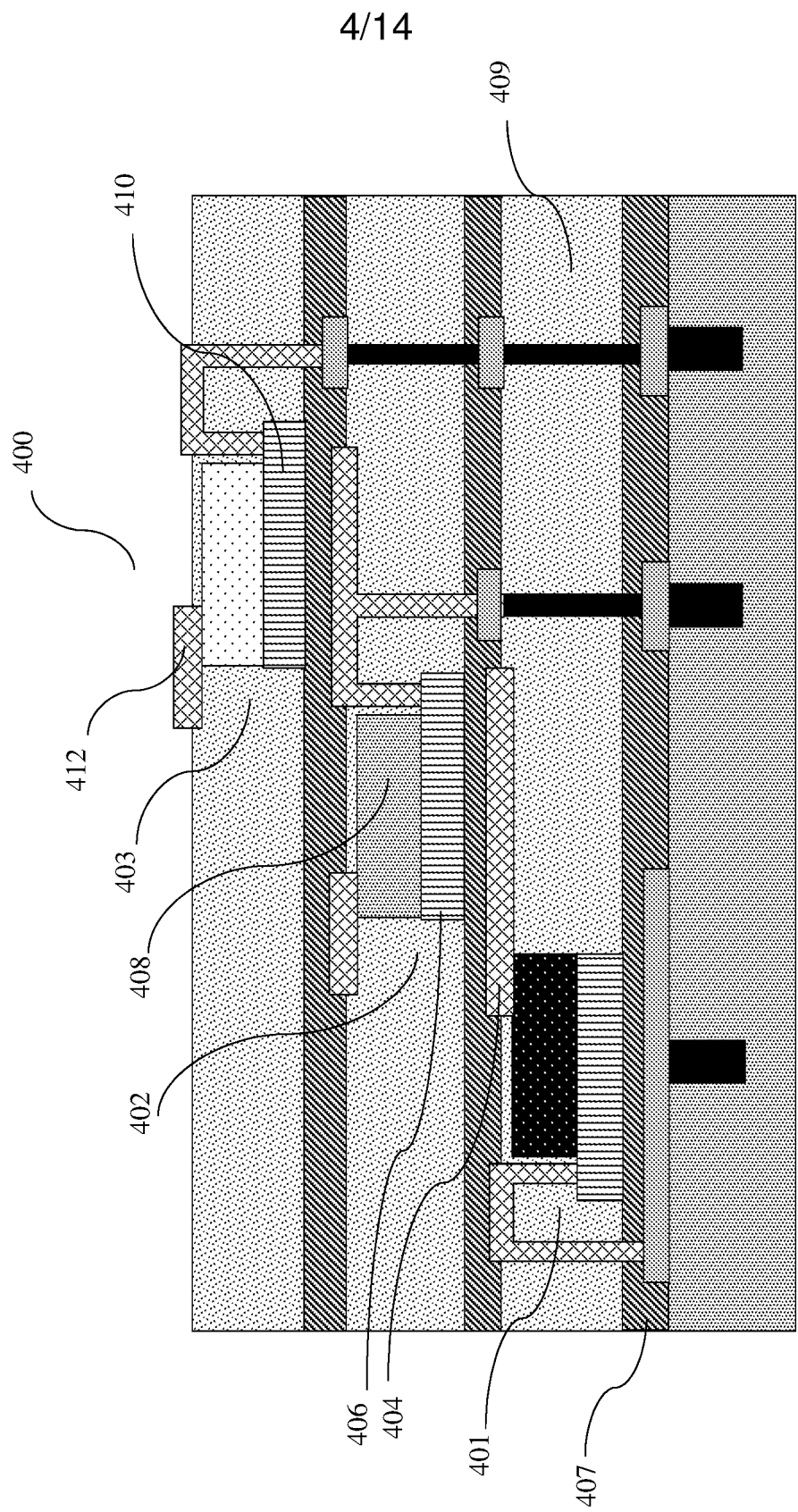


Figure 4

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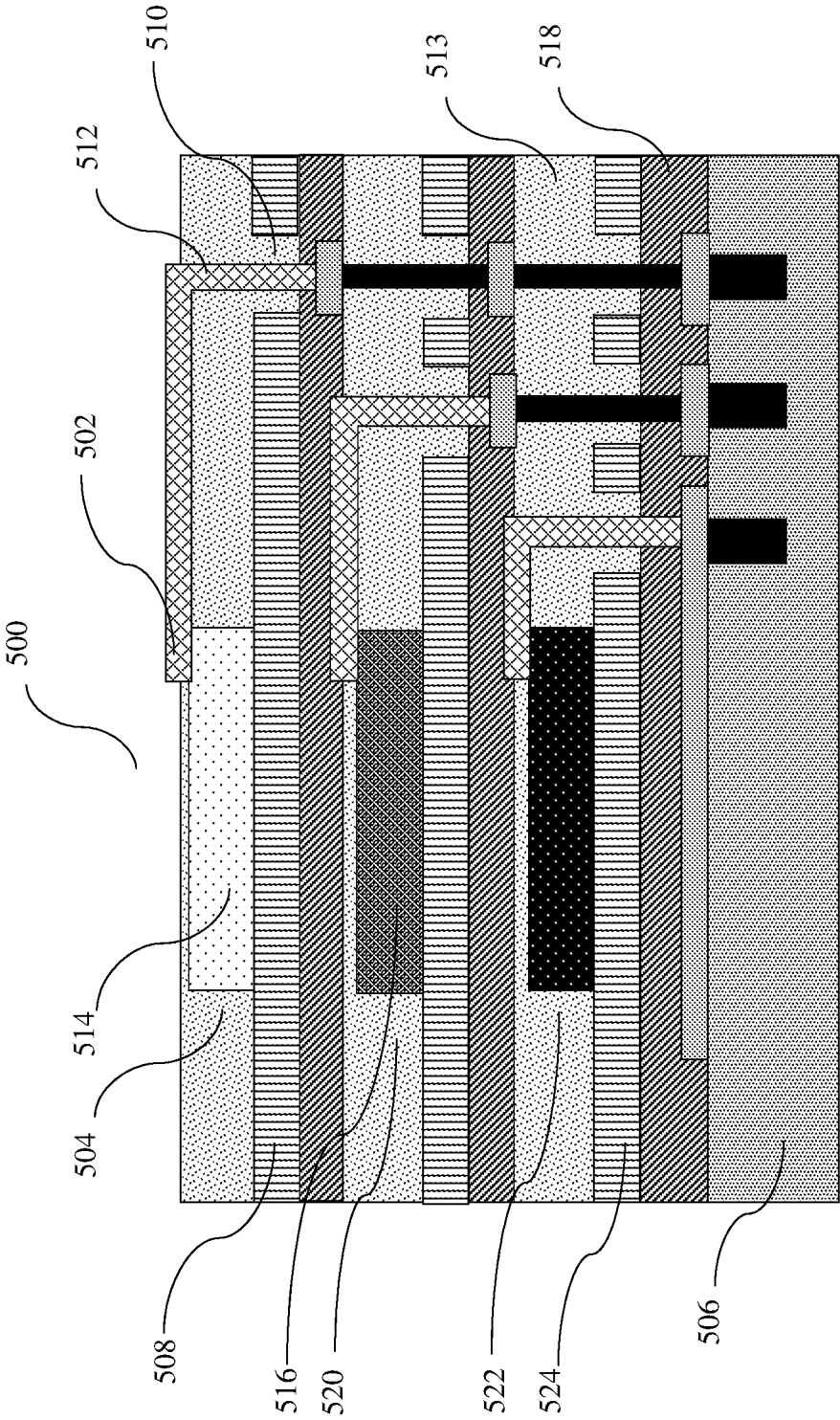


Figure 5

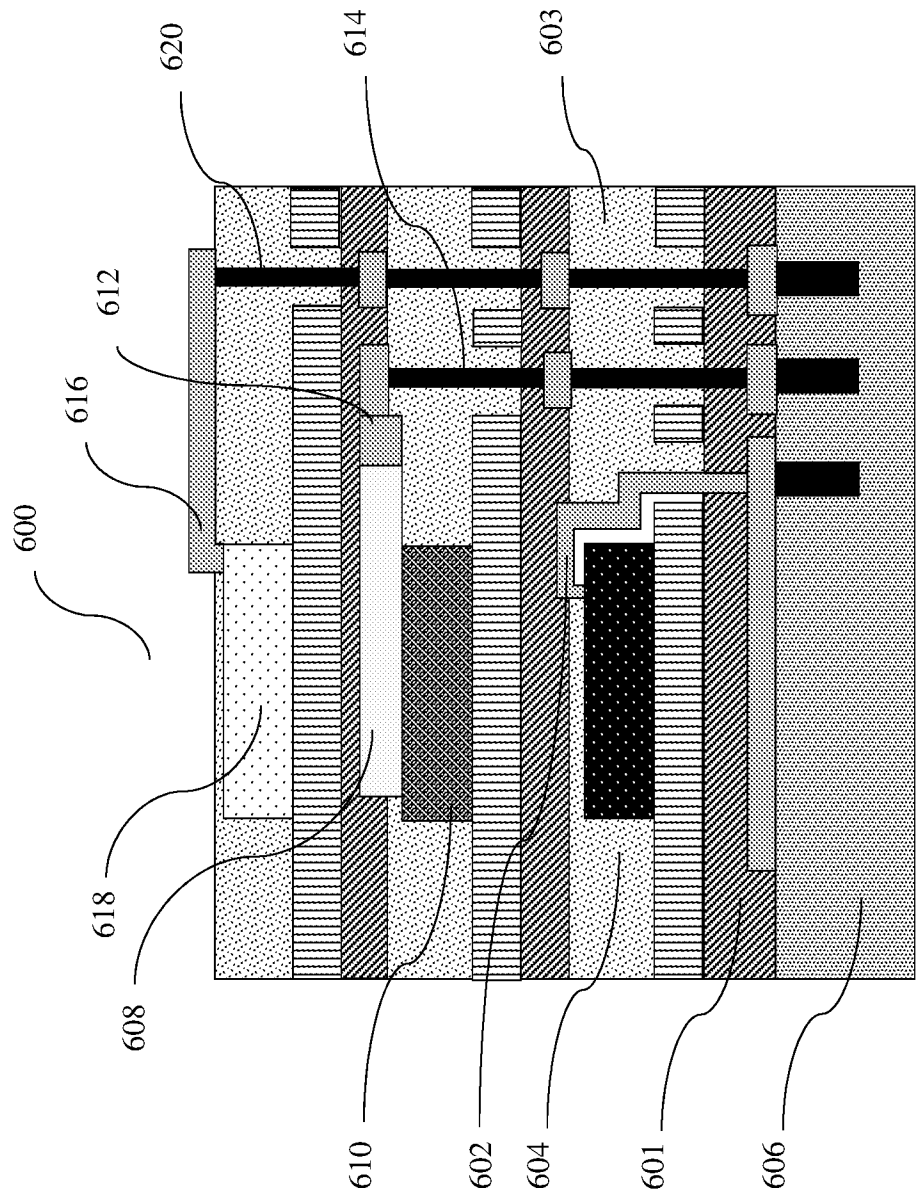


Figure 6

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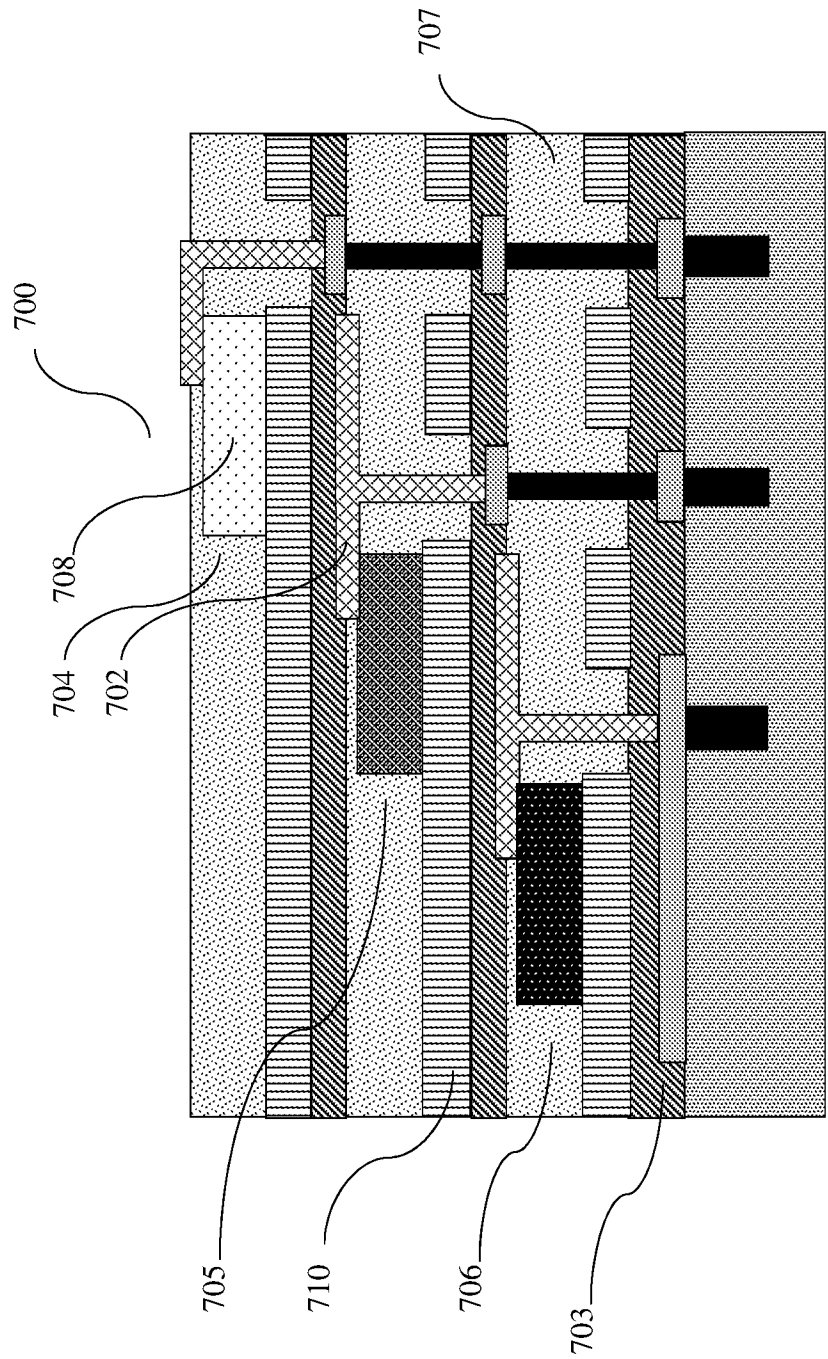


Figure 7

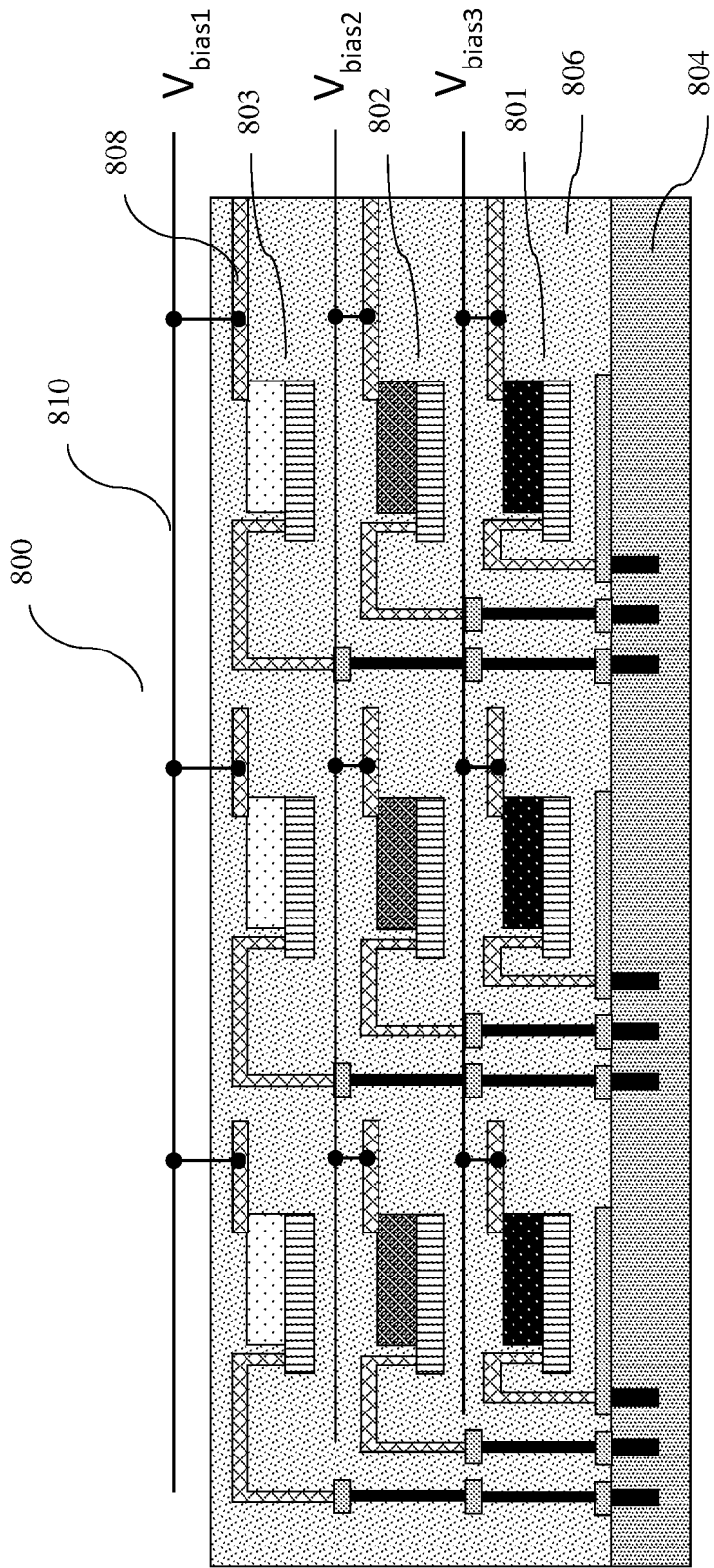


Figure 8(a)

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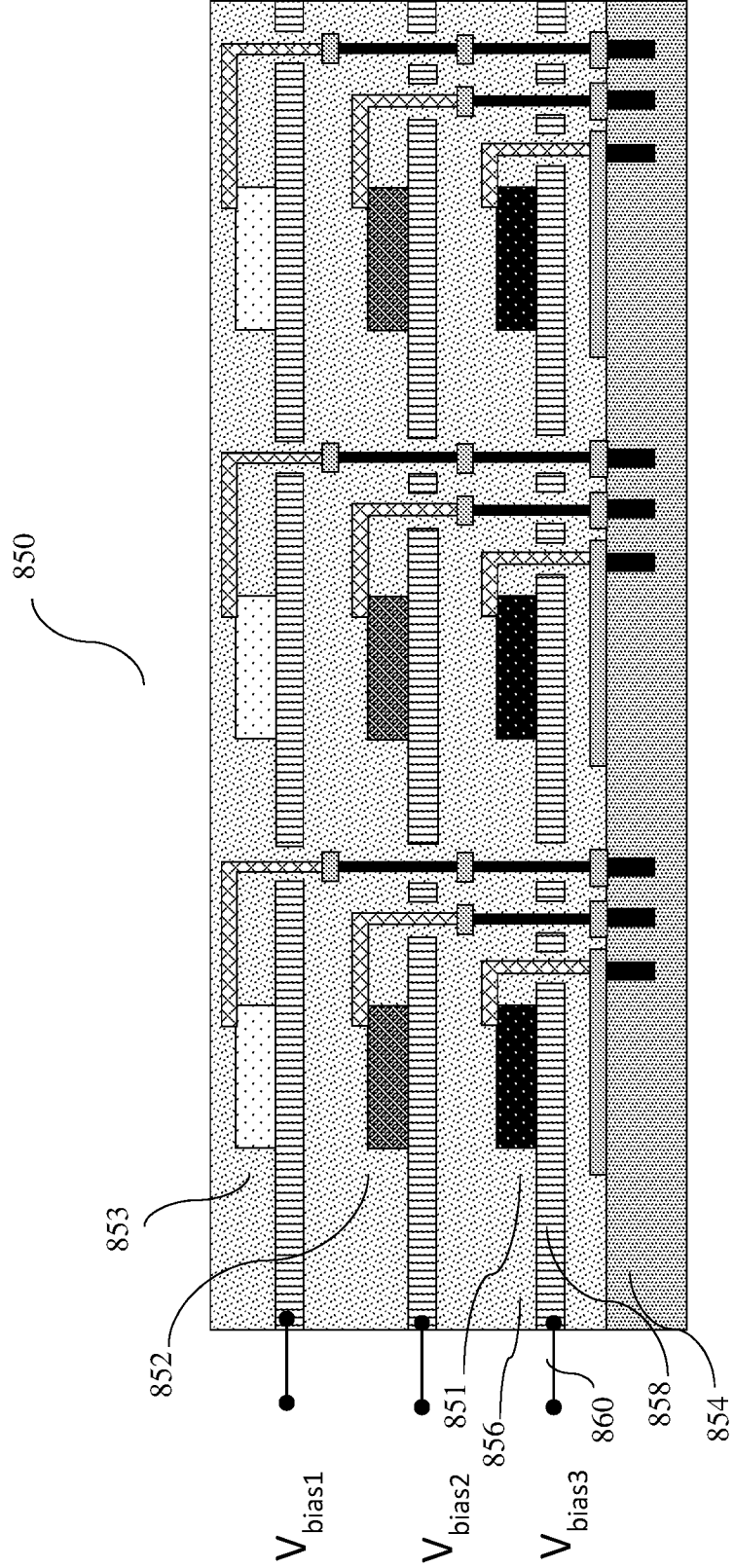


Figure 8(b)

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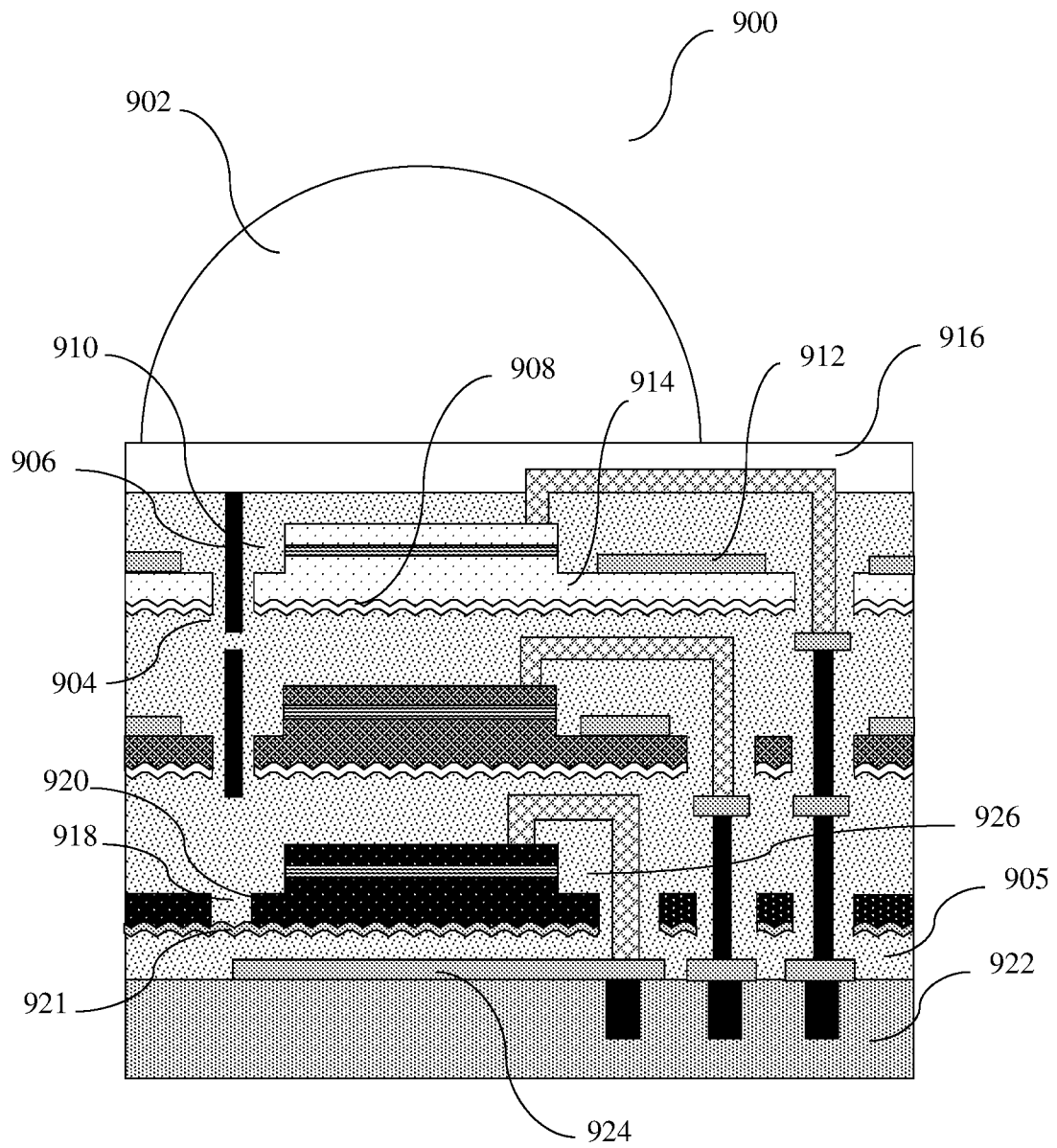


Figure 9

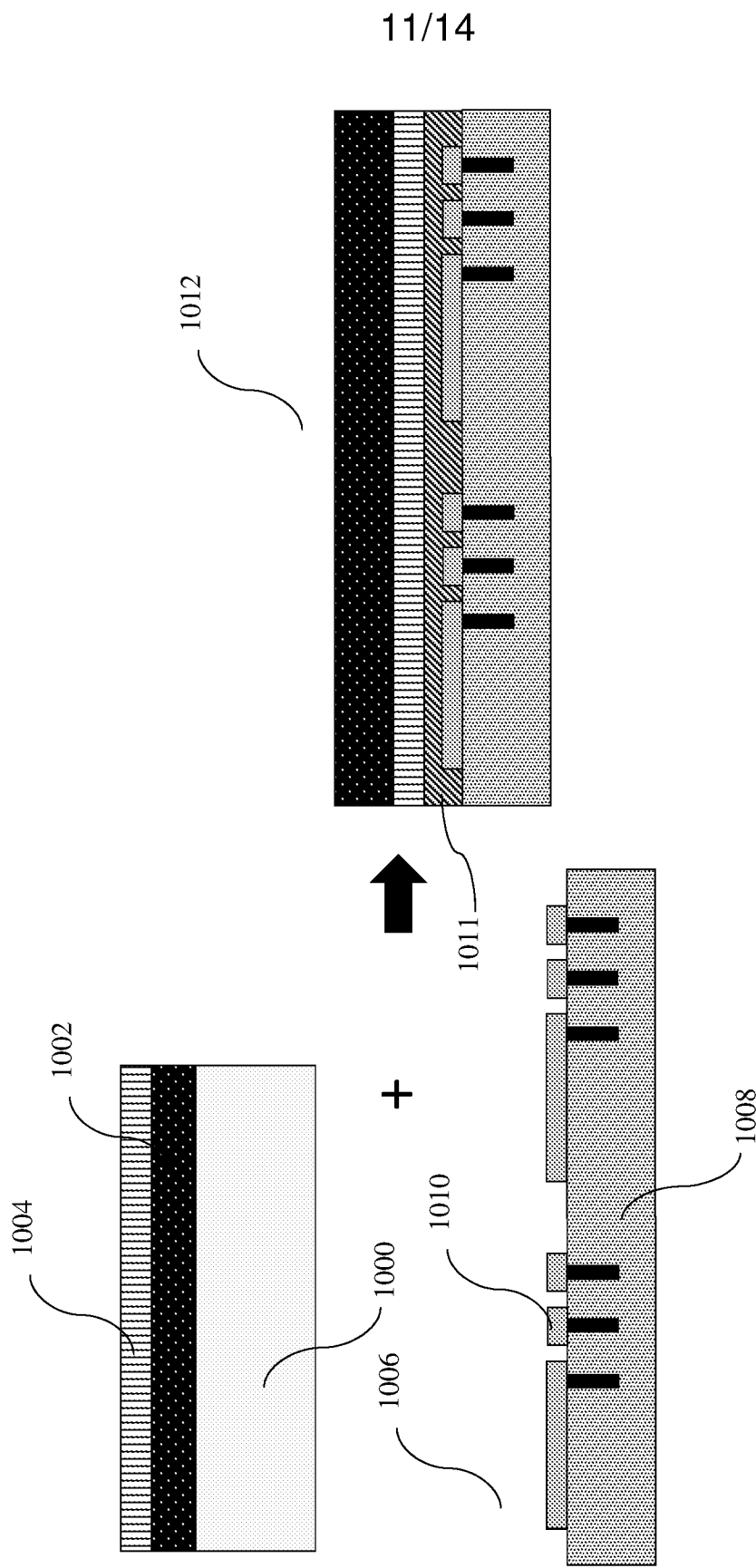


Figure 10

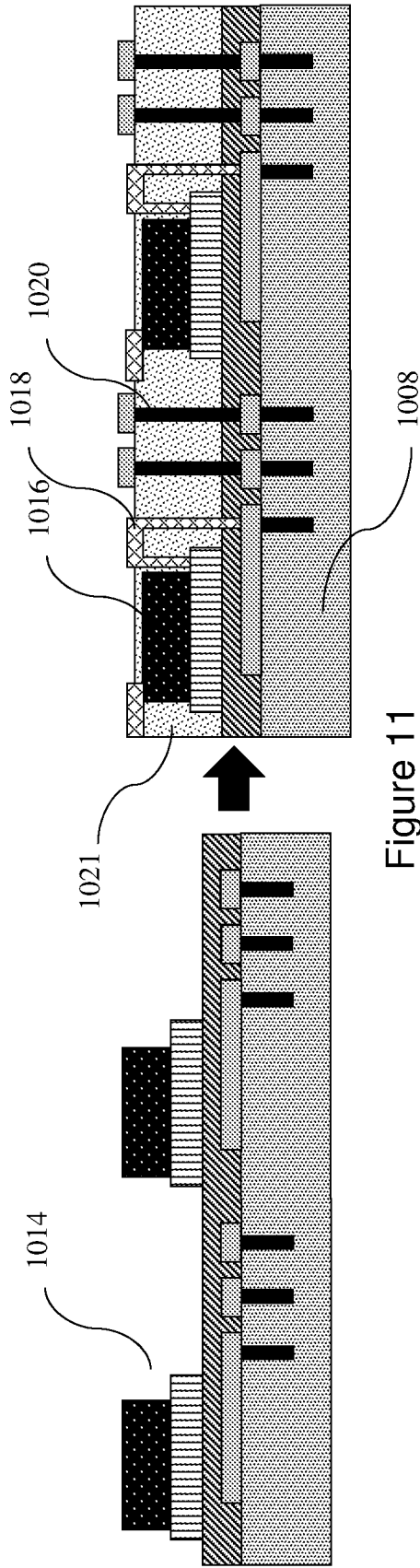


Figure 11

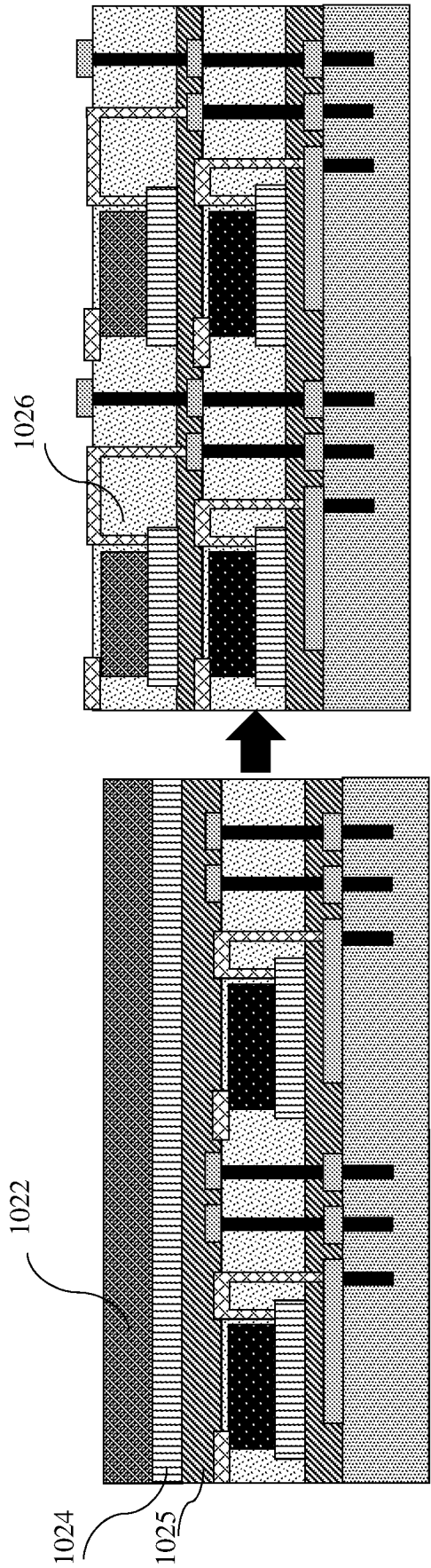


Figure 12

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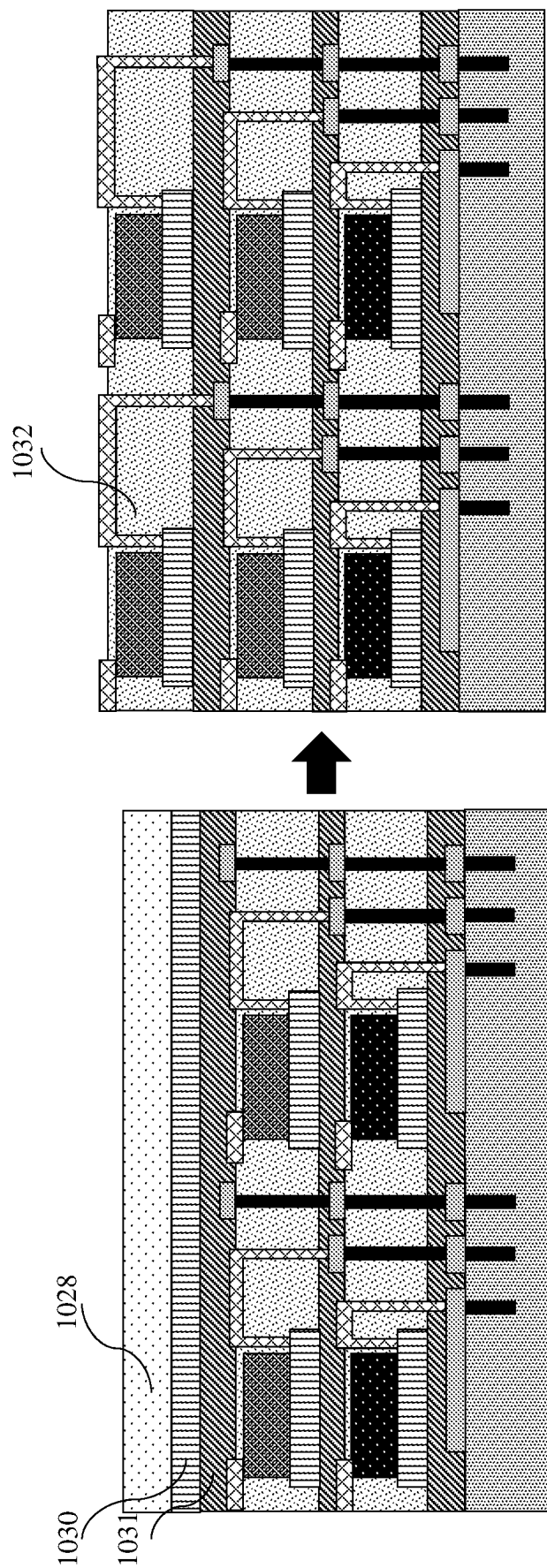


Figure 13

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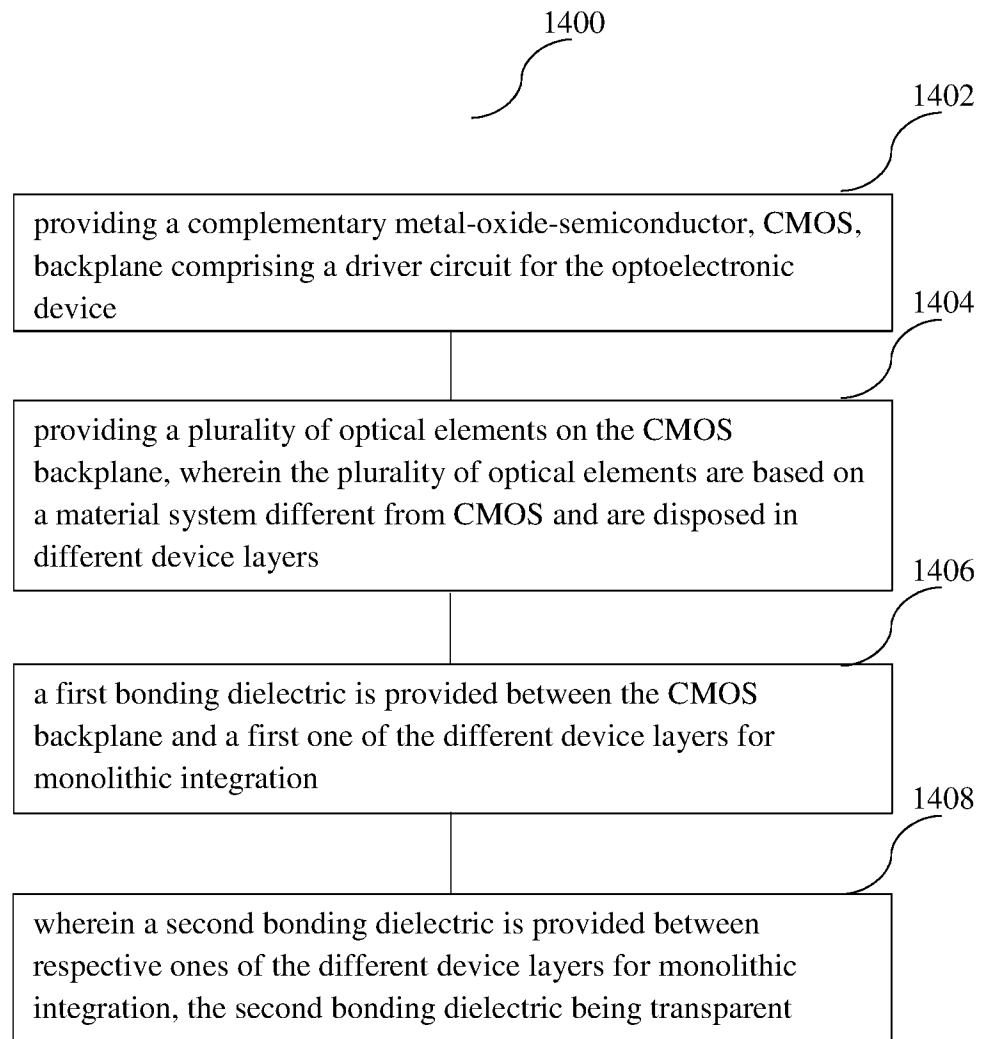


Figure 14

INTERNATIONAL SEARCH REPORT

International application No.

PCT/SG2020/050357

A. CLASSIFICATION OF SUBJECT MATTER

See Supplemental Box

According to International Patent Classification (IPC)

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 25/00; H01L 27/00; H01L 33/00; G09F 9/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

FAMPAT: dielectric bonding, driver circuit, cmos backplane, epitaxial, LEDs, stack, 介电质, 结合, 粘, 驱动, 电路, 外延, 二极管, 堆, 叠 and related search keywords.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2019/0189681 A1 (CHAE J. H. ET AL.) 20 June 2019 Paragraphs [0141]-[0296], [0570]-[0572]; figures 1-34, 81	1-36
X	JP 2015-095517 A (JAPAN BROADCASTING CORP.) 18 May 2015 Paragraphs [0028]-[0069]; figures 1-4 of the machine translation	1, 2, 9, 13, 14, 18-20, 27, 31, 32, 36
X	US 2004/0036074 A1 (KONDO T.) 26 February 2004 Paragraphs [0080]-[0120]; figure 1	1, 2, 13, 14, 19, 20, 31, 32
A	WO 2018/175338 A1 (HONG KONG BEIDA JADE BIRD DISPLAY LIMITED) 27 September 2018 Entire document	
A	WO 2018/132070 A1 (MASSACHUSETTS INSTITUTE OF TECHNOLOGY ET AL.) 19 July 2018 Entire document	

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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Date of the actual completion of the international search

21/09/2020

(day/month/year)

Date of mailing of the international search report

23/09/2020

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/SG2020/050357

Note: This Annex lists known patent family members relating to the patent documents cited in this International Search Report. This Authority is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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INTERNATIONAL SEARCH REPORT

International application No.

PCT/SG2020/050357

Supplemental Box (Classification of Subject Matter)

Int. Cl.

H01L 25/16 (2006.01)

H01L 27/15 (2006.01)

H01L 33/62 (2010.01)

G09F 9/33 (2006.01)

H01L 27/146 (2006.01)