



(51) International Patent Classification:

G11C 13/00 (2006.01) H01L 45/00 (2006.01)
H01L 27/24 (2006.01)

(21) International Application Number:

PCT/US2016/040203

(22) International Filing Date:

29 June 2016 (29.06.2016)

(25) Filing Language:

English

(26) Publication Language:

English

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,

(54) Title: RRAM DEVICES WITH AMORPHOUS BOTTOM BALLAST LAYER

120

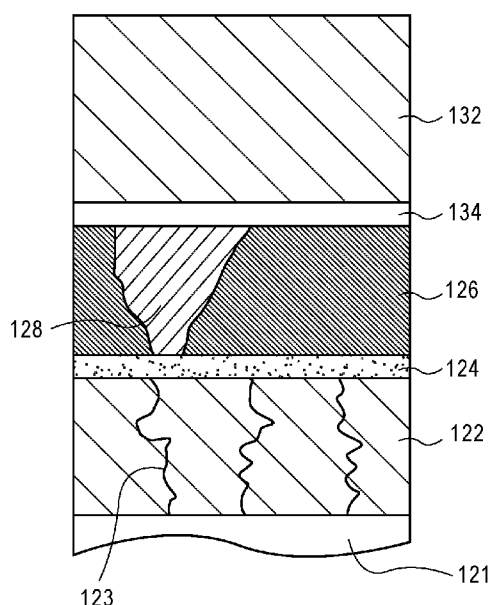


FIG. 1B

(57) Abstract: Approaches for fabricating RRAM stacks with an amorphous bottom ballast layer, and the resulting structures and devices, are described. In an example, a resistive random access memory (RRAM) device includes a conductive interconnect disposed in an inter-layer dielectric (ILD) layer disposed above a substrate. An RRAM element is disposed on the conductive interconnect. The RRAM element includes a first electrode layer disposed on the uppermost surface of the conductive interconnect. An amorphous ballast layer is disposed on the first electrode layer. A resistance switching layer is disposed on the amorphous ballast layer. The amorphous ballast layer is separate and distinct from the first electrode layer and from the resistance switching layer. A second electrode layer is disposed above the resistance switching layer.

TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

RRAM DEVICES WITH AMORPHOUS BOTTOM BALLAST LAYER**TECHNICAL FIELD**

Embodiments of the invention are in the field of integrated circuit fabrication and, in particular, approaches for fabricating resistive random access memory (RRAM) stacks with an amorphous bottom ballast layer, and the resulting structures and devices.

BACKGROUND

For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips. For example, shrinking transistor size allows for the incorporation of an increased number of memory devices on a chip, lending to the fabrication of products with increased capacity. The drive for ever-more capacity, however, is not without issue. The necessity to optimize the performance of each device becomes increasingly significant.

Embedded SRAM and DRAM have problems with non-volatility and soft error rates, while embedded FLASH memories require additional masking layers or processing steps during manufacture, require high-voltage for programming, and have issues with endurance and reliability. Nonvolatile memory based on resistance change is known as RRAM or ReRAM. Although commonly anticipated as a replacement technology for flash memory, the cost benefit and performance benefit of RRAM have not been obvious enough to most companies to proceed with the replacement. Also, for low voltage non-volatile embedded applications, operating voltages less than 1V and compatible with CMOS logic processes may be desirable but challenging to achieve.

Thus, significant improvements are still needed in the area of nonvolatile memory device manufacture and operation. In particular, significant improvements are still needed in the area of non-volatile memory arrays and their integration with logic processors.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A illustrates a cross-sectional view of an RRAM element having unintentional oxide growth on a bottom electrode.

Figure 1B illustrates a cross-sectional view of an RRAM element having an amorphous bottom ballast layer, in accordance with an embodiment of the present invention.

Figure 2 illustrates cross-sectional views of various operations in a method of fabricating an RRAM element having an amorphous bottom ballast layer, in accordance with an embodiment of the present invention.

Figure 3A illustrates a cross-sectional view of two RRAM devices, each including an amorphous bottom ballast layer, in accordance with an embodiment of the present invention.

Figure 3B illustrates a plan view of a pair of RRAM elements integrated with a common line electrode, each RRAM element including an amorphous bottom ballast layer, in accordance with an embodiment of the present invention.

Figure 3C illustrates a plan view of a pair of RRAM elements integrated with discrete via electrodes, each RRAM element including an amorphous bottom ballast layer, in accordance with an embodiment of the present invention.

Figure 4 illustrates a cross-sectional view of an RRAM device fabricated using a damascene process and including an amorphous bottom ballast layer, in accordance with an embodiment of the present invention.

Figure 5 illustrates a cross-sectional view of an RRAM element coupled to a drain side of a transistor selector and having an amorphous bottom ballast layer, in accordance with an embodiment of the present invention.

Figure 6A illustrates schematic views of several options for positioning an RRAM element in an integrated circuit, the RRAM element including an amorphous bottom ballast layer, in accordance with an embodiment of the present invention.

Figure 6B illustrates a cross-sectional view of a logic region together with an RRAM memory array integrated on a common substrate, in accordance with an embodiment of the present invention.

Figures 7A and 7B illustrate a schematic and corresponding I-V plot, respectively, demonstrating concepts involved with filament formation in an RRAM element having an amorphous bottom ballast layer, in accordance with an embodiment of the present invention.

Figure 8 illustrates an operational schematic representing a changing of states for an anionic-based metal-conductive oxide-metal RRAM memory element having an amorphous bottom ballast layer, in accordance with an embodiment of the present invention.

Figure 9 illustrates a schematic representation of resistance change in a conductive oxide layer induced by changing the concentration of oxygen vacancies in the conductive oxide layer, in accordance with an embodiment of the present invention.

Figure 10 illustrates an operational schematic representing a changing of states for a cationic-based metal-conductive oxide-metal RRAM memory element having an amorphous bottom ballast layer, in accordance with an embodiment of the present invention.

Figure 11 illustrates a schematic representation of resistance change in a cationic-based conductive oxide layer induced by changing the concentration of cation vacancies in the conductive oxide layer, in accordance with an embodiment of the present invention.

Figure 12 illustrates a schematic of a memory bit cell which includes a metal-conductive oxide-metal RRAM memory element having an amorphous bottom ballast layer, in accordance with an embodiment of the present invention.

Figure 13 illustrates a block diagram of an electronic system, in accordance with an embodiment of the present invention.

Figure 14 illustrates a computing device in accordance with one embodiment of the invention.

Figure 15 illustrates an interposer that includes one or more embodiments of the invention.

DESCRIPTION OF THE EMBODIMENTS

Approaches for fabricating RRAM stacks with an amorphous bottom ballast layer, and the resulting structures and devices, are described. In the following description, numerous specific details are set forth, such as specific RRAM material regimes and structure architectures, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known features, such as operations associated with embedded memory, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be appreciated that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

Certain terminology may also be used in the following description for the purpose of reference only, and thus are not intended to be limiting. For example, terms such as “upper”, “lower”, “above”, “below,” “bottom,” and “top” refer to directions in the drawings to which reference is made. Terms such as “front”, “back”, “rear”, and “side” describe the orientation and/or location of portions of the component within a consistent but arbitrary frame of reference which is made clear by reference to the text and the associated drawings describing the component under discussion. Such terminology may include the words specifically mentioned above, derivatives thereof, and words of similar import.

One or more embodiments are directed to resistive random access memory (RRAM) material stacks with a ballast layer. Particular embodiments are directed to the implementation of an amorphous bottom ballast layer, such as in the form of an RRAM stack or device including

an engineered TiON-based layer as a built-in ballast amorphous Electrode. One or more embodiments of the present invention are directed to methods for integrating RRAM memory arrays into a logic processor. Particular embodiments may be suitable for fabricating embedded non-volatile memory (e-NVM). Approaches described herein may provide a fabrication pathway for high performance RRAM cells and increase the potential of using scaled RRAM cells for future e-NVM needs, such as for integration in system on chip (SoC) products.

One or more embodiments are directed to designing a resistive RAM (RRAM) memory thin film stack to improve the switching properties and reliability of a memory based on the RRAM memory thin film stack. In particular, in an embodiment, by inserting an amorphous oxide layer that also functions as an internal ballast resistor in series with the RRAM oxide helps with both minimizing the impact of parasitics and reducing the effects of grain boundaries of the electrode. In an embodiment, switching memory performance is improved for both filamentary as well as interfacial RRAM based devices. In an embodiment, a separate thin amorphous oxide layer is integrated in series with an RRAM oxide layer. The separate thin amorphous oxide layer acts as an intrinsic internal ballast resistance, as well as prevents the impact of the weak spots from electrode grain boundaries. In an embodiment, a composition of a TiON-based material layer is engineered to control its resistivity (e.g., within the range of interest for ballast resistor materials) as well as to maintain its amorphous nature even following backend thermal budget processing. As such, the TiON-based material layer may be engineered for an RRAM stack as a built-in ballast amorphous electrode.

To provide additional context, since RRAM oxides are scaling to increasingly thinner dimensions and can be integrated at larger cell size, they may ultimately exhibit appreciable intrinsic capacitance. Such intrinsic capacitance can then generate high spike currents during a resistive switching action that may degrade the memory performance. In order to avoid this phenomena, in accordance with an embodiment of the present invention, a ballast resistor is engineered on a bottom side of an RRAM oxide.

To provide illustrative context, Figure 1A illustrates a cross-sectional view of an RRAM element having unintentional oxide growth on a bottom electrode. Referring to Figure 1A, an RRAM element material stack 100 includes a bottom electrode 102 disposed above a substrate 101. A resistance switching layer 104 is disposed above the bottom electrode 102. A top electrode 108 is disposed on the resistance switching layer 104. A filament 110 may be included in the resistance switching layer 104, in the case of filament-based RRAM. To provide context, for one or more embodiments of the present invention, the bottom electrode 102 is composed of a material having grain boundaries 112 therein. Some of the grain boundaries 112 may be exposed at an uppermost surface of the bottom electrode 102. Furthermore, an unintentional

oxide layer 114 may form at the uppermost surface of the bottom electrode 102, at locations of the exposed grain boundaries 112, as is depicted in Figure 1A. The unintentional oxide layer 114 may be segmented, i.e., non-continuous, as defects resulting from the grain boundaries 112 may be propagated through the unintentional oxide layer 114. Accordingly, such an unintentional oxide layer 114 may not uniform due to columnar nature of the bottom electrode 102.

It is to be appreciated that issues with an RRAM element material stack such as RRAM element material stack 100 may include high parasitics. Issues with an RRAM element material stack such as RRAM element material stack 100 may also include detrimental effects of the grain boundaries 112 of the bottom electrode 102.

An oxide (or other) RRAM-based memory stack may be fabricated to include an amorphous bottom ballast layer to accommodate underlying grain boundaries and, possibly, reduce variability. As an exemplary implementation, Figure 1B illustrates a cross-sectional view of an RRAM element having an amorphous bottom ballast layer, in accordance with an embodiment of the present invention.

Referring to Figure 1B, a resistive random access memory (RRAM) element 120 includes a first electrode layer 122 disposed above a substrate 121. A resistance switching layer 126 is disposed above the first electrode layer 122. A second electrode layer 132 is disposed above the resistance switching layer 126. An amorphous ballast layer 124 is disposed directly between and in contact with the first electrode layer 122 and the resistance switching layer 126. The amorphous ballast layer 124 is separate and distinct from the first electrode layer 122 and the resistance switching layer 126. In one embodiment, the amorphous ballast layer 124 is separate and distinct from the first electrode layer 122 and the resistance switching layer 126 in that a first seam exists between the amorphous ballast layer 124 and the first electrode layer 122 and a second seam exists between the amorphous ballast layer 124 and the resistance switching layer 126. In another embodiment, the amorphous ballast layer 124 is separate and distinct from the first electrode layer 122 and the resistance switching layer 126 in that the composition of the amorphous ballast layer 124 is different from the first electrode layer 122 and different from the resistance switching layer 126. Referring again to Figure 1B, a second electrode layer 132 is disposed above the resistance switching layer 126.

Referring again to Figure 1B, the first electrode layer 122 includes a plurality of crystal grain boundaries 123 therein. At least some of the grain boundaries 123 are exposed at an uppermost surface of the first electrode layer 122, as is depicted in Figure 1B. In an embodiment, the amorphous ballast layer 124 is a continuous layer in direct contact with exposed ones of the plurality of crystal grain boundaries 123. As such, since the amorphous ballast layer 124 is not broken into contiguous segments (as was the case for the unintentional oxide layer 114

of Figure 1A), defects stemming from the exposed ones of the plurality of crystal grain boundaries 123 are not propagated into the amorphous ballast layer 124 and, hence, are not propagated into the resistance switching layer 126. By hindering or altogether eliminating such defects from impacting the resistance switching layer 126, device performance may be stabilized across an array of devices.

In an embodiment, an amorphous ballast layer is referred to as “ballast” since the layer provides stability to the RRAM element, e.g., stability in resistive behavior of the RRAM element. In one such embodiment, a ballast resistor is integrated on a bottom side of the RRAM oxide material. In an embodiment, an amorphous ballast layer is referred to as “amorphous” since it lacks a crystalline structure.

In an embodiment, the amorphous ballast layer 124 is composed of an oxynitride derivative of a transition metal species. In one such embodiment, the oxynitride derivative of the transition metal species is a TiO_xN_y -based oxynitride derivative, where both x and y are greater than 0. In one such embodiment, a TiON material is alloyed with Si or Al, and the TiO_xN_y -based oxynitride derivative is or includes TiSiON or TiAlON , respectively. In a specific embodiment, a TiON material is alloyed with Si and Al, and the TiO_xN_y -based oxynitride derivative is or includes TiSiAlON . In an embodiment, the amorphous ballast layer 124 has a thickness approximately in the range of 1-2 nanometers. In an embodiment, a TiON-based material is engineered in composition and thickness to provide a built-in ballast as well as an amorphous structure.

In an embodiment, a filament 128 is included in the resistance switching layer 126 to provide filament-based RRAM, as is described in greater detail below in association with Figures 7A and 7B. In other embodiment, however, a filament is not included and surface or interface-based RRAM is fabricated. As such, embodiments described herein are applicable to both filamentary and interfacial RRAM implementations.

Referring again to Figure 1B, and as used throughout the present disclosure, exemplary material combinations for the first electrode layer 122, the resistance switching layer 126, and the second electrode layer 132 are described below in association with Figures 7A and 8-11. In one embodiment, the resistance switching layer 126 is an oxide-based material layer including a dielectric oxide material (e.g., such as a layer of HfO_2 , as is described in association with Figures 7A and 7B) or a conductive oxide material (e.g., as described below in association with Figures 8 and 9).

In accordance with an embodiment of the present invention, the second electrode layer 132 is disposed directly on the resistance switching layer 126. However, in other embodiments, as is depicted in Figure 1B, an oxygen exchange layer (OEL) 134 is included on or above the

resistance switching layer 126. In one such embodiment, the second electrode layer 132 is disposed on the OEL 134 which in turn is disposed on the resistance switching layer 126.

As described above, an OEL 134 may be included in stack 120. To provide context, a typical resistive random access (RRAM) memory stack includes a first metal electrode, a stoichiometric metal oxide switching layer disposed on the first metal electrode, and a second metal electrode disposed on the metal oxide switching layer. However, an oxygen exchange layer (OEL) may be disposed on the metal oxide switching layer to facilitate resistive switching.

In a metal oxide based filamentary RRAM system, in particular, a conductive filament is formed during an initial soft dielectric breakdown process. This process, known as “forming,” involves application of a high voltage typically in the range of 1.5 to 3V between the two metal electrodes sandwiching the metal oxide switching layer, as is described in greater detail below in association with Figures 7A and 7B. In a metal oxide filamentary system, the conductive filament is made-up of oxygen vacancies which migrate in response to the electric field created during the forming process. In a fully stoichiometric metal oxide film sandwiched between two metal electrodes, such oxygen vacancies are created during an annealing process at temperatures above, e.g., 350 degrees Celsius. However, when an oxygen exchange layer is disposed above the metal oxide switching layer, it can serve as a more effective oxygen scavenging layer by taking oxygen from the metal oxide switching layer as a result of its oxygen affinity. An oxygen exchange layer typically is composed of metals which are identical to the metal film in the metal oxide layer or metals with higher oxygen affinity compared to the metal oxide switching layer. In the normal course of an RRAM device operation, an OEL may be implemented to serve as a reservoir for oxygen vacancies, helping to create and dissolve the conductive filament by acting as a source and a sink.

Referring again to Figure 1B, advantages of implementing a material stack such as RRAM element 120 for RRAM device fabrication may include one or more of (1) implementation of a bottom side ballast may control any cell capacitance induced parasitic peak currents, (2) implementations may improve variability even for highly scaled RRAM (e.g., with large area), (3) such a stack may be compatible with an NMOS transistor (when ballast is on the bottom), (4) such a stack may be compatible with a PMOS transistor (when ballast is on the top), (5) such a built-in ballast can significantly reduce switching variability (i.e., control of parasitics), and/or (6) the amorphous structure (a) avoids local non-uniformity in the cell (also expect to reduce variability), and/or (b) provides good thermal stability.

In another aspect, material stack 120 may be fabricated in a series of deposition operations. As an example, Figure 2 illustrates cross-sectional views of various operations in a

method of fabricating an RRAM element having an amorphous bottom ballast layer, in accordance with an embodiment of the present invention.

Referring to part (a) of Figure 2, a method of fabricating a resistive random access memory (RRAM) device includes forming a first electrode layer 122 above a substrate 121. In an embodiment, the first electrode layer 122 is formed using a physical vapor deposition (PVD) process. In an embodiment, grain boundaries 123 form within the first electrode layer 122 during or following deposition of the material of the first electrode layer 122, as is depicted in part (a) of Figure 2.

Referring to part (b) of Figure 2, an amorphous ballast layer 124 is formed on the first electrode layer 122. In an embodiment, the amorphous ballast layer 124 is formed using a deposition process such as, but not limited to, a chemical vapor deposition (CVD) process or an atomic layer deposition (ALD) process.

In an embodiment, the amorphous ballast layer 124 does not take on or propagate defects originating from grain boundaries 123. In particular, propagation of potential defects is blocked from affecting a subsequently formed resistance switching layer. Furthermore, by forming an “intentional” amorphous ballast layer 124, formation of an unwanted and uncontrolled oxide layer which is otherwise fragmented and introduces large variability is effectively blocked and, possibly, altogether eliminated. In an embodiment, the amorphous structure or nature of the amorphous ballast layer 124 avoids or prevents local non-uniformity in the cell. In an embodiment, the amorphous structure or nature of the amorphous ballast layer 124 provides good thermal stability. In an embodiment, the term “bottom” ballast layer refers to a ballast layer associated with an electrode formed first, onto which the amorphous ballast layer 124 is subsequently formed, as is described in association with Figure 2.

Referring to part (c) of Figure 2, a resistance switching layer 126 is formed on the amorphous ballast layer 124. In an embodiment, the resistance switching layer 126 is formed using a deposition process such as, but not limited to, a chemical vapor deposition (CVD) process, an atomic layer deposition (ALD) process, or a physical vapor deposition (PVD) process.

Referring to part (d) of Figure 2, optionally, an oxygen exchange layer 132 is formed on the resistance switching layer 126. In an embodiment, the oxygen exchange layer 132 is formed using a deposition process such as, but not limited to, a chemical vapor deposition (CVD) process, an atomic layer deposition (ALD) process, or a physical vapor deposition (PVD) process.

Referring to part (e) of Figure 2, a second electrode layer 132 is formed on the resistance switching layer 126 or (if present, as is depicted), on the oxygen exchange layer 132. In an

embodiment, the second electrode layer 132 is formed using a deposition process such as, but not limited to, a chemical vapor deposition (CVD) process, an atomic layer deposition (ALD) process, or a physical vapor deposition (PVD) process. It is to be appreciated that the second electrode layer 132 may be referred to as a “top” electrode since it is formed after the switching layer of the device is formed. Such a “top” electrode may itself have grain boundaries, but such grain boundaries may not impact the quality of the switching layer since the second electrode layer 132 is formed afterwards.

It is to be appreciated that the RRAM element 120 may be fabricated on a conductive interconnect formed in an inter-layer dielectric (ILD) layer. It is also to be appreciated that the stack of materials described in Figure 2 may ultimately be etched to provide a patterned material stack for RRAM element 120. As a possible example of both such scenarios, Figure 3A illustrates a cross-sectional view of two RRAM devices, each including an amorphous bottom ballast layer, in accordance with an embodiment of the present invention.

Referring to Figure 3A, each of the resistive random access memory (RRAM) devices includes a conductive interconnect 306 disposed in an inter-layer dielectric (ILD) layer 304 disposed above a substrate 302. The ILD layer 306 has an uppermost surface substantially coplanar with an uppermost surface of the conductive interconnect 306. An RRAM element 120 is disposed on the conductive interconnect 306. Each RRAM element 120 includes the material layers described in association with Figure 1B, as is depicted in Figure 3A.

In an embodiment, the conductive interconnect 306 includes a conductive line portion 308 and an underlying via portion 310, as is depicted in Figure 3A. In another embodiment, the conductive interconnect is a conductive via. In one embodiment, the conductive interconnect includes a conductive fill material 314 surrounded by a barrier layer 312, which may include an upper barrier layer 316, as is depicted in Figure 3A. In a specific such embodiment, the conductive fill material 314 but not the barrier layer 312 is recessed to form an opening in which the upper barrier layer 316 is then formed. In an embodiment, although depicted using different shading, the upper barrier layer 316 is composed of substantially the same material as the barrier layer 312. In one such embodiment, the material includes tantalum nitride.

Referring again to Figure 3A, in an embodiment, the materials of the memory (RRAM) elements are patterned following a deposition process such as described in association with Figure 2. In one such embodiment, the material layers are patterned using a subtractive etching process. As depicted in Figure 3A, a dielectric sidewall spacer 340 is laterally adjacent to and in contact with sidewalls of the patterned material layers of stacks 120. In one such embodiment, the dielectric sidewall spacer 340 formation includes conformal deposition of a dielectric material, such as a silicon nitride layer, and subsequent anisotropic etching to form the dielectric

sidewall spacer 340. Thus, in one embodiment, the a dielectric sidewall spacer 340 is formed laterally adjacent to and in contact with sidewalls of the first electrode layer 122 (having grain boundaries 123 therein), the amorphous ballast layer 124, the resistance switching layer 126, the optional oxygen exchange layer 134 (if present), and the second electrode layer 132.

5 Referring again to Figure 3A, and as used throughout the present disclosure, in an embodiment, one or more interlayer dielectrics (ILDs), such as ILD layer 304, are included in an RRAM device structure. Such ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as low-k dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide (SiO₂),
10 carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant. In cases where a stack of ILD layers is implemented, etch stop materials may be included as intervening dielectric layers between the ILD layers. Such etch stop layers
15 may be composed of dielectric materials different from the interlayer dielectric material. In some embodiments, an etch stop layer includes a layer of a nitride of silicon (e.g., silicon nitride) or a layer of an oxide of silicon, or both, or a combination thereof. Other suitable materials may include carbon-based materials, such as silicon carbide. Alternatively, other etch stop layers known in the art may be used depending upon the particular implementation. The etch stop
20 layers may be formed by CVD, PVD, or by other deposition methods.

Referring again to Figure 3A, and as used throughout the present disclosure, in an embodiment, the metal lines (such as 308) and vias (such as 310) are composed of one or more metal or other conductive structures. A common example is the use of copper lines and structures that may or may not include barrier layers (such as Ta or TaN layers) between the
25 copper and surrounding ILD material. As used herein, the term metal includes alloys, stacks, and other combinations of multiple metals. For example, the metal interconnect lines may include barrier layers, stacks of different metals or alloys, etc. The interconnect lines are also sometimes referred to in the arts as traces, wires, lines, metal, or simply interconnect.

Referring again to Figure 3A, and as used throughout the present disclosure, in an
30 embodiment, substrate 302 is a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide,
35 gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group

III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present invention.

It is to be appreciated that the layers and materials described in association with Figures 1B or 3A and as used throughout the present disclosure, are typically formed on or above an underlying semiconductor substrate or structure, such as underlying device layer(s) of an integrated circuit. In an embodiment, an underlying semiconductor substrate 121 or 302 represents a general workpiece object used to manufacture integrated circuits. The semiconductor substrate often includes a wafer or other piece of silicon or another semiconductor material. Suitable semiconductor substrates include, but are not limited to, single crystal silicon, polycrystalline silicon and silicon on insulator (SOI), as well as similar substrates formed of other semiconductor materials. The semiconductor substrate, depending on the stage of manufacture, often includes transistors, integrated circuitry, and the like. The substrate may also include semiconductor materials, metals, dielectrics, dopants, and other materials commonly found in semiconductor substrates. In one embodiment, the illustrated structure depicted in Figure 1B or 3A is fabricated on underlying transistor or other semiconductor device layer(s) formed in or above the substrate 121 or 302. In another embodiment, the illustrated structures depicted in Figure 1B or 3A are fabricated on underlying lower level interconnect layers formed above the substrate 121 or 302, respectively.

In an aspect, RRAM elements 120 may be formed on a common conductive line. As an example, Figure 3B illustrates a plan view of a pair of RRAM elements integrated with a common line electrode, each RRAM element including an amorphous bottom ballast layer, in accordance with an embodiment of the present invention.

Referring to Figure 3B, a conductive interconnect 350 housed in an ILD layer 304 includes two RRAM stacks 120 thereon (e.g., stacks including layers described in association with Figures 1B or 3A). Each RRAM stack 120 is disposed on a portion of an upper barrier layer 316 or a conductive fill material 314 of the conductive interconnect. The conductive interconnect in this example is a conductive line coupled to a first and second RRAM stacks 120.

In another aspect, adjacent RRAM elements 120 may be formed on respective conductive vias. As an example, Figure 3C illustrates a plan view of a pair of RRAM elements integrated with discrete via electrodes, each RRAM element including an amorphous bottom ballast layer, in accordance with an embodiment of the present invention.

Referring to Figure 3C, a pair of conductive vias 360 housed in an ILD layer 304 each has a respective RRAM stack 120 thereon (e.g., stacks including layers described in association with

Figures 1B or 3A). Each via is discrete and includes an exposed upper barrier layer 316 or conductive fill material 314, on which a corresponding RRAM stack 120 is disposed.

The above described RRAM material stacks including a bottom ballast layer may be fabricated through subtractive patterning of the layers of the RRAM stack 120 materials, as is depicted in the examples above. In another aspect, however, the layers of an RRAM element may be fabricated in a damascene-like fabrication scheme. As an example, Figure 4 illustrates a cross-sectional view of an RRAM device fabricated using a damascene process and including an amorphous bottom ballast layer, in accordance with an embodiment of the present invention.

Referring to Figure 4, a resistive random access memory (RRAM) device includes a conductive interconnect 306 (e.g., one such interconnect described in association with Figure 3A) disposed in a first inter-layer dielectric (ILD) layer 304 disposed above a substrate 302. A second ILD layer 404 is disposed above the first ILD layer 304. The second ILD layer 404 has an opening exposing the conductive interconnect 306 from a top down perspective. The opening has sidewalls, for example the sloped sidewalls depicted in Figure 4.

An RRAM element 406 is disposed on the conductive interconnect 306. The RRAM element 406 includes materials of the first electrode layer 122 with grain boundaries 123 therein, the amorphous ballast layer 124, the resistance switching layer 126, the optional oxygen exchange layer 134 (if present), and the second electrode layer 132 formed in the opening of the second ILD layer 404. In one embodiment, the second ILD layer 404 is disposed directly on an uppermost surface 402 of the first ILD layer 304, as is depicted in Figure 4. In another embodiment, an etch stop layer is disposed between the first ILD layer 304 and the second ILD layer 404.

In another aspect, a conductive interconnect of an associated RRAM element stack may be coupled to a drain region of an underlying select transistor disposed on a substrate. As an example, Figure 5 illustrates a cross-sectional view of an RRAM element coupled to a drain side of a transistor selector and having an amorphous bottom ballast layer, in accordance with an embodiment of the present invention.

Referring to Figure 5, a memory structure 500 includes a transistor 502 disposed in or above an active region 504 of a semiconductor substrate 506. The transistor 502 includes a gate electrode 508 with source/drain regions 510 on either side of the gate electrode 508, and in active region 504 of substrate 506. In an embodiment, the source/drain region 510 on the left-hand side of Figure 5 is a source region, and the source/drain region 510 on the right-hand side of Figure 5 is a drain region. An RRAM element 120 is coupled to the drain region of the transistor 502, but not to the source region of the transistor 502. The arrangement enables driving of the RRAM

element 120 by the drain side only. The RRAM element 120 and portions of the transistor 502 may be included in an inter-layer dielectric (ILD) layer 550, as is depicted in Figure 5.

The RRAM element 120 includes a top (second) electrode layer 132, an optional oxygen exchange layer 134 (if present), a resistance switching layer 126, a bottom amorphous ballast layer 124, and a bottom (first) electrode layer 122 with grain boundaries 123 therein. The RRAM element 120 is, in an embodiment, included as an interrupting feature along a conductive drain contact 530. In one such embodiment, corresponding gate contact 534 and source contact 532 are not coupled to, or interrupted by the RRAM element 120, as is depicted in Figure 5. It is to be appreciated that although the RRAM element 120 is shown generically along the drain contact 530 without a lateral reference, the actual layer in which the RRAM element 120 is included may be viewed as an interconnect layer (e.g., M1, M2, M3, M4, etc.) corresponding to a logic region in another area of the substrate 506. It is also to be appreciated that additional interconnect layer(s) may be formed on top of the structure 500 shown in Figure 5, e.g., using standard dual damascene process techniques that are well-known in the art.

In an embodiment, transistor 502 is a metal-oxide-semiconductor field-effect transistor (MOSFET or simply MOS transistor), fabricated on a substrate. In various implementations of the invention, the MOS transistors described herein may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors.

In an embodiment, each MOS transistor includes a gate stack formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide (SiO_2) and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

The gate electrode layer of each MOS transistor is formed on the gate dielectric layer and may consist of at least one P-type workfunction metal or N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the

gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a fill metal layer.

For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV.

In some implementations, the gate electrode may consist of a “U”-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the invention, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

In some implementations of the invention, a pair of sidewall spacers may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In an alternate implementation, a plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

As is well known in the art, source and drain regions are formed within the substrate adjacent to the gate stack of each MOS transistor. The source and drain regions are generally formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to form recesses at the locations of the source and drain regions. An epitaxial deposition process may then be

carried out to fill the recesses with material that is used to fabricate the source and drain regions. In some implementations, the source and drain regions may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some implementations the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In
5 further embodiments, the source and drain regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. And in further embodiments, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

To provide further context, integrating memory directly onto a microprocessor chip
10 would be advantageous since it enables higher operation speeds compared to having physically separate logic and memory chips. Unfortunately, traditional charge-based memory technologies such as DRAM and NAND Flash are now facing severe scalability issues related to increasingly precise charge placement and sensing requirements. As such, embedding charge-based memory directly onto a high performance logic chip is not very attractive for future technology nodes.
15 However, a memory technology that does have the potential to scale to much smaller geometries compared to traditional charge-based memories is resistive random access memory (RRAM), since it relies on resistivity rather than charge as the information carrier. However, in order to exploit the potential benefits of a high performance logic chip with embedded RRAM memory, an appropriate integrated logic plus RRAM structure and fabrication method is needed.
20 Embodiments of the present invention include such structures and fabrication processes.

Relating to one or more embodiments described herein, it is to be appreciated that traditional DRAM memory is facing severe scaling issues and, so, other types of memory devices are being actively explored in the electronics industry. One future contender is RRAM devices. Embodiments described herein include a fabrication method for embedding RRAM bit cell
25 arrays into a logic process technology. Embodiments described may be advantageous for processing schemes involving the fabrication of logic processors with embedded memory arrays.

In an aspect, an RRAM element may be included in an integrated circuit in regions typically referred to as back end or back end of line (BEOL) layers of the integrated circuit. As examples, Figure 6A illustrates schematic views of several options for positioning an RRAM
30 element in an integrated circuit, the RRAM element including an amorphous bottom ballast layer, in accordance with an embodiment of the present invention.

Referring to Figure 6A, five examples (A)-(E) of an RRAM cell situated above a second metal logic layer (M2) or higher are provided. In each case, a memory region 600 and a logic region 602 of an integrated circuit are depicted schematically. Each memory region 600 and
35 logic region 602 is associated with a corresponding transistor (or group of transistors) 604 or

606, respectively. Stacks of metallization layers (as housed in encompassing dielectric layer or layers 697) include metal lines 608 and vias 610 that are generally alternating. Thus, all arrangements depicted include an RRAM element disposed above a second metal line (M2) in the stack. The RRAM element typically includes a resistance switching layer, such as a
5 conductive oxide memory layer, sandwiched between a bottom electrode and a top electrode, and may be formed in an opening of an insulating layer. In accordance with an embodiment of the present invention, an amorphous ballast layer is sandwiched between the bottom electrode and the resistance switching layer. The described arrangements can enable integration of both logic and memory on a same die versus stand-alone memory. Although depicted at a very high level
10 conceptual view for the sake of illustrating general placement options, it is to be appreciated that, in accordance with an embodiment of the present invention, elements labeled RRAM in Figure 6A includes a stack of multiple layers such as those described above.

Referring again to Figure 6A, in a first example (A), an RRAM element is fabricated on top of a unique via 650 intended for memory devices. In a second example (B), an RRAM
15 element is fabricated first and an upper unique via 660 contacts the RRAM from above. In a third example (C), an RRAM element has a top electrode with an increased thickness such that the RRAM element occupies a full via depth, between metal lines. In a fourth example (D), an RRAM element has a top electrode with an increased thickness such that the RRAM element occupies a full metal line height. In a fifth example (E), an RRAM element has a top electrode
20 with an increased thickness such that the RRAM element occupies a full interconnect level (via plus metal line). Accordingly, in an embodiment, an RRAM element or an array of RRAM elements can be embedded in a logic chip.

An RRAM array may be embedded in a logic chip. As an example, Figure 6B illustrates a cross-sectional view of a logic region together with an RRAM memory array integrated on a
25 common substrate, in accordance with an embodiment of the present invention. Referring to Figure 6B, a structure 4000 includes a logic region 4020 and an RRAM array region 4040.

Referring to the RRAM array region 4040 of Figure 6B, in a first layer, metal 2 (M2) 4080 and via 1 (V1) 4100 structures are formed above a substrate 4060. The M2 4080 and V1 4100 structures are formed in an inter-layer dielectric layer 4120 disposed over an etch stop layer
30 4140.

Referring again to the RRAM array region 4040 of Figure 6B, in a second layer, a plurality of RRAM stacks 120 is formed in the inter-layer dielectric layer 4200 disposed over the etch stop layer 4220. The plurality of RRAM stacks 120 may be coupled to corresponding ones of the M2 4080 structures by a conductive layer 4240, as is depicted in Figure 6B. A dielectric
35 spacer layer 340 may be formed on sidewalls of portions of the RRAM stacks, as is also depicted

in Figure 6B. Each of the RRAM stacks 120 includes a first electrode layer 122 with grain boundaries 123 therein, an amorphous ballast layer 124, a switching layer 126, an optional oxygen exchange layer 134 (if present), and a second electrode layer 132. A top electrode 4340 may also be included as an additional upper electrode layer, as is depicted in Figure 6B.

5 Referring again to the RRAM array region 4040 of Figure 6B, in a third layer, an etch stop layer 4360 is disposed on the inter-layer dielectric layer 4200. Metal 4 (M4) 4380 and via to memory 4400 structures are formed in the inter-layer dielectric layer 4420 disposed over the etch stop layer 4360. It is to be appreciated that additional interconnect layer(s) may be formed on top of the M4/via to memory layers of the RRAM array region 4040 of Figure 6B, e.g., using
10 standard dual damascene process techniques that are well-known in the art.

It is to be appreciated that although the RRAM stacks may actually include numerous layers of very thin films, for the sake of simplicity the RRAM stacks 120 are depicted as describe above. It is also to be appreciated that although in the illustrations the RRAM stacks are shown embedded into a corresponding logic metal 3 (M3) layer, they may instead be embedded into
15 some other interconnect layer (e.g., M1, M2, M4, etc.)

Referring again to Figure 6B, in an embodiment, the conductive metal layer 4240 is a tantalum nitride (TaN) layer. In one embodiment, the conductive metal layer 4240 is referred to as a “thin via” layer. In an embodiment, the top electrode 4340 is composed of a material or stack of materials suitable for electrically contacting the RRAM stack 120. In an embodiment,
20 the top electrode 4340 is a topographically smooth electrode. In one such embodiment, the top electrode 4340 has a thickness suitable for good conductivity but has little to no columnar structure formation that would otherwise lead to a rough top surface. Such a topographically smooth electrode may be referred to as amorphous in structure. In an embodiment, the top electrode 4340 begins as a hardmask layer, such as a titanium nitride hardmask layer, used for
25 patterning the RRAM stack and is ultimately retained as a conductive contact.

Referring now to the logic region 4020 of Figure 6B, in the first layer, metal 2 (M2) 4500 and via 1 (V1) 4520 structures are formed in the inter-layer dielectric layer 4120 disposed over the etch stop layer 4140. In the second layer, the etch stop layer 4220 is disposed on the inter-layer dielectric layer 4120. Metal 3 (M3) 4540 and via 2 (V2) 4560 structures are formed in the
30 inter-layer dielectric layer 4200 disposed over the etch stop layer 4220. In the third layer, the etch stop layer 4360 is disposed on the inter-layer dielectric layer 4200. Metal 4 (M4) 4580 and via 3 (V3) 4600 structures are formed in the inter-layer dielectric layer 4420 disposed over the etch stop layer 4360. It is to be appreciated that additional interconnect layer(s) may be formed on top of the M4/V3 layers of the logic region 4020 of Figure 6B, e.g., using standard dual
35 damascene process techniques that are well-known in the art.

In another aspect, upon fabrication of an RRAM element associated with an insulating metal oxide material layer, the RRAM may be subjected to an intentional one-time “break-down” process for filament formation in the resulting RRAM device fabricated from the RRRAM memory element. To illustrate the above aspect, Figures 7A and 7B illustrate a schematic and
5 corresponding I-V plot, respectively, demonstrating concepts involved with filament formation in an RRAM element having an amorphous bottom ballast layer, in accordance with an embodiment of the present invention.

Referring to Figure 7A, a material stack 700 includes a bottom electrode (BE) 702, an oxide layer 704 such a hafnium oxide layer (HfO_2), which may be considered a dielectric oxide
10 layer), and a top electrode (TE) 706. An amorphous ballast layer 124 is between the bottom electrode 702 and the oxide 704. Oxide vacancies 708 may be depicted as circles in Figure 7A. Oxide RRAM cell filament formation begins with a stoichiometric oxide layer 704 which is subjected to a forming (soft breakdown) operation (1) to provide a low resistance state (LRS). A first reset operation (2) is then performed to provide switching to a high resistance state (HRS).
15 A set operation (3) is then performed to return to the LRS. Performing operations (1)-(3) involves motion of oxygen vacancies and redox phenomena. Plot 710 of Figure 7B illustrates the I-V characteristics association with operations (1), (2) and (3) of Figure 7A.

In another aspect, an RRAM element or device may be an anionic-based conductive oxide memory element. Figure 8 illustrates an operational schematic representing a changing of
20 states for an anionic-based metal-conductive oxide-metal RRAM memory element having an amorphous bottom ballast layer, in accordance with an embodiment of the present invention. Referring to Figure 8, a memory element 800 includes an electrode 1/amorphous ballast layer 124/conductive oxide/electrode 2 material stack. The memory element 800 may begin in a less conductive state (1), with the conductive oxide layer being in a less conductive state 804A. An
25 electrical pulse, such as a duration of a positive bias (2) may be applied to provide memory element 800 in a more conductive state (3), with the conductive oxide layer being in a more conductive state 804B. An electrical pulse, such as a duration of a negative bias (4) may be applied to again provide memory element 800 having the less conductive state (1). Thus, electrical pulsing may be used to change resistance of the memory element 800.

As such, in an embodiment, a memory element includes an anionic-based conductive oxide layer sandwiched between two electrodes. Resistivity of the conductive oxide layer in low field (when device is read) is, in some embodiments, in the range found typical of conductive
30 films of metal compounds, e.g. TiAlN . For example, in a specific embodiment, the resistivity for such a layer is approximately in the range of 0.1 Ohm cm – 10 kOhm cm when measured at low field. Resistivity of the film is tuned depending in the memory element size to achieve final
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resistance value in the range compatible with fast read. Composition of the conductive oxide layer may be tuned in such a way that a small change in its composition results in a large change in resistance. Resistance change occurs, in some embodiments, due to a Mott transition, e.g., when injected/extracted charge causes phase transition in the conductive oxide layer between more and less resistive phase configurations. In other embodiments, the resistance change can be induced by changing the concentration of oxygen vacancies in the conductive oxide layer.

As an example of one approach, Figure 9 illustrates a schematic representation of resistance change in an anionic-based conductive oxide layer induced by changing the concentration of oxygen vacancies in the conductive oxide layer, in accordance with an embodiment of the present invention. Referring to Figure 9, a memory element 900 is shown as deposited (A). The memory element includes a conductive oxide layer 904 between a palladium (Pd) electrode 902 (which may be associated with an intervening amorphous ballast layer 124) and a tungsten (W) electrode 906. Oxygen atoms and oxygen vacancies may be distributed as shown in (A). Referring to (B) of Figure 9, upon application of a positive bias, the memory element 900 can be made more conductive. In that state, oxygen atoms migrate to the electrode 906, while vacancies remain throughout the layer 904. Referring to (C) of Figure 9, upon application of a negative bias, the memory element can be made less conductive. In that state, oxygen atoms are distributed more evenly throughout layer 904. Accordingly, in an embodiment, effective composition (e.g., the location of oxygen atoms versus vacancies) of a conductive oxide layer is modified to change resistance of a memory element. In a specific embodiment, an applied electrical field, which drives such compositional change, is tuned to values approximately in the range of $1\text{e}6\text{-}1\text{e}7$ V/cm. Referring again to Figure 9, although surface stage are demonstrated, it is to be appreciated that if filament formation is used, such as described in association with Figures 7A and 7B, vacancies will penetrate the film to a greater extent.

As mentioned briefly above, in an embodiment, one electrode in a memory element including an anionic-based conductive oxide layer is a noble metal based electrode, while the other electrode in is a transition metal for which some of the lower valence oxides are conductive (e.g., to act as an oxygen reservoir). That is, when oxygen atoms migrate to the transition metal oxide, the resulting interfacial transition metal oxide formed remains conductive. Examples of suitable transition metals which form conductive oxides include but are not limited to, W, V, Cr, or Ir. In other embodiments, one or both of the electrodes is fabricated from an electro-chromic material. In other embodiments, one or both of the electrodes is fabricated from a second, different conductive oxide material. In an embodiment, examples of suitable conductive oxides include, but are not limited to: ITO ($\text{In}_2\text{O}_{3-x}\text{SnO}_{2-x}$), $\text{In}_2\text{O}_{3-x}$, sub-stoichiometric yttria doped zirconia ($\text{Y}_2\text{O}_{3-x}\text{ZrO}_{2-x}$), or $\text{La}_{1-x}\text{Sr}_x\text{Ga}_{1-y}\text{Mg}_y\text{O}_{3-x-0.5(x+y)}$. In another embodiment, the conductive

oxide layer is composed of a material with two or more metal elements (e.g., as contrasted to common RRAM memories using one metal such as found in binary oxides, such as HfO_x or TaO_x). In such ternary, quaternary, etc. alloys, the metals used are from adjacent columns of the periodic table. Specific examples of suitable such conductive oxides include, but are not limited to: Y and Zr in $\text{Y}_2\text{O}_{3-x}\text{ZrO}_{2-x}$, In and Sn in $\text{In}_2\text{O}_{3-x}\text{SnO}_{2-x}$, or Sr and La in $\text{La}_{1-x}\text{Sr}_x\text{Ga}_{1-y}\text{Mg}_y\text{O}_3$. Such materials may be viewed as compositions selected to have aliovalent substitution to significantly increase the number of oxygen vacancies. It is to be appreciated that in some embodiments the change of resistance of such electrode during programming can contribute to the total resistance change.

In an embodiment, examples of suitable noble metals include, but are not limited to Pd or Pt. In a specific embodiment, a more complex, yet still all-conductive, stack includes an approximately 10nm Pd first electrode layer, an approximately 3nm $\text{In}_2\text{O}_{3-x}$ and/or SnO_{2-x} conductive oxide layer, and a second electrode stack composed of approximately 20nm tungsten/10nm Pd/100nm TiN /55nm W.

In another aspect, an RRAM element or device may be a cationic-based conductive oxide memory element. As an example, Figure 10 illustrates an operational schematic representing a changing of states for a cationic-based metal-conductive oxide-metal RRAM memory element having an amorphous bottom ballast layer 124, in accordance with an embodiment of the present invention. Referring to Figure 10, memory element 1000 may begin in a more conductive state (1), with a cationic-based conductive oxide layer being in a more conductive state 1004A. An electrical pulse, such as a duration of a positive bias (2) may be applied to provide memory element 1000 in a less conductive state (3), with the cationic-based conductive oxide layer being in a less conductive state 1004B. An electrical pulse, such as a duration of a negative bias (4) may be applied to again provide memory element 1000 having the more conductive state (1). Thus, electrical pulsing may be used to change resistance of the memory element 1000. Polarity applied is such as to attract active cations of in the memory layer to the intercalation electrode under negative bias.

As such, in an embodiment, a memory element includes a cationic-based conductive oxide layer sandwiched between two electrodes, the bottom electrode of which may be associated with an amorphous ballast layer. Resistivity of the cationic-based conductive oxide layer in low field (when device is read) is, in some embodiments, can be as low as found typical of conductive films of metal compounds, e.g. TiAlN. For example, in a specific embodiment, the resistivity for such a layer is approximately in the range of 0.1 Ohm cm – 10 kOhm cm when measured at low field (measured for the specific thickness used in the stack). Resistivity of the

film is tuned depending in the memory element size to achieve final resistance value in the range compatible with fast read.

As an example of one approach, Figure 11 illustrates a schematic representation of resistance change in a cationic-based conductive oxide layer induced by changing the concentration of cation vacancies (such as lithium cation vacancies) in the conductive oxide layer, in accordance with an embodiment of the present invention.

Referring to Figure 11, a memory element 1100 is shown as deposited (A). The memory element includes a cationic-based conductive oxide layer 1104 between a bottom electrode 1102 (which may be associated with an amorphous ballast layer 124) and a top electrode 1106. In a specific example, the layer 1104 is a lithium cobalt oxide layer, described in greater details below, and lithium atoms and lithium vacancies are distributed as shown in (A). Referring to (B) of Figure 11, upon application of a negative bias, the memory element 1100 can be made more conductive. In that state, lithium atoms migrate to the top electrode 1106, while vacancies remain throughout the layer 1104. Referring to (C) of Figure 11, upon application of a positive bias to one of the electrodes, the memory element can be made less conductive. In that state, lithium atoms are distributed more evenly throughout layer 1104. Accordingly, in an embodiment, effective composition (e.g., the location of lithium atoms (or cations) versus vacancies) of a cationic-based conductive oxide layer is modified to change resistance of a memory element, in some embodiments due to stoichiometry-induced Mott transition. In a specific embodiment, an applied electrical field, which drives such compositional change during write operation, is tuned to values approximately in the range of $1\text{e}6\text{-}1\text{e}7$ V/cm.

In an embodiment, referring again to Figure 11, the cationic-based conductive oxide layer 1104 is composed of a material suitable for cation-based mobility within the layer itself. In a specific exemplary embodiment, layer 1104 of Figure 11 part (A) is composed of lithium cobalt oxide (LiCoO_2). Then, in part (B), the corresponding layer becomes lithium deficient (e.g., $\text{Li}_{<0.75}\text{CoO}_2$) when a negative bias is applied and lithium atoms (e.g., as cations) migrate toward electrode 1106. By contrast, in part (C), the corresponding layer becomes lithium rich (e.g., $\text{Li}_{>0.95}\text{CoO}_2$) when a positive bias is applied and lithium atoms (e.g., as cations) migrate away from electrode 1106. In other embodiments, other suitable compositions with cationic conductivity include, but are not limited to, LiMnO_2 , $\text{Li}_4\text{TiO}_{12}$, LiNiO_2 , LiNbO_3 , $\text{Li}_3\text{N:H}$, LiTiS_2 (all of which are lithium atom or Li^+ mobility based), Na β -alumina (which is sodium atom or Na^+ mobility based), or AgI , RbAg_4I_5 , AgGeAsS_3 (all of which are silver atom or Ag^+ mobility based). In general, these examples provide materials based on cation mobility or migration, which is typically much faster than anionic-based mobility or migration (e.g., for oxygen atoms or O^{2-} anions).

In an embodiment, referring again to Figure 11, one electrode (e.g., bottom electrode 1102) in a memory element including a cationic conductive oxide layer is a noble metal based electrode. In one embodiment, examples of suitable noble metals include, but are not limited to palladium (Pd) or platinum (Pt). In a specific embodiment, a memory stack includes a bottom electrode composed of an approximately 10 nanometer thick Pd layer.

In an embodiment, referring again to Figure 11, the other electrode (e.g., top electrode 1106) in a memory element including a cationic conductive oxide layer is an “intercalation host” for migrating cations. The material of the top electrode is a host in a sense that the material is conductive with or without the presence of the migrating cations and is not substantially altered in the absence or presence of the migrating cations. In an exemplary embodiment, the top electrode is composed of a material such as, but not limited to, graphite, or metal chalcogenides such as disulfides (e.g., TaS₂). Such materials are conductive as well as absorbing of cations such as Li⁺. This is in contrast to an electrode for an anionic based conductive oxide which may include a metal with a corresponding conductive oxide to accommodate migrating oxygen atoms or anions.

Referring again to the description associated with Figures 8-11 above, a stack of conductive layers including a conductive metal oxide layer may be used to fabricate as memory bit cell. For example, Figure 12 illustrates a schematic of a memory bit cell 1200 which includes a metal-conductive oxide-metal RRAM memory element 1210, in accordance with an embodiment of the present invention. Such an RRAM memory element may be suitable for manufacture on a substrate in common with logic regions of the substrate.

Referring to Figure 12, the RRAM memory element 1210 may include a first conductive electrode 1212 (which may have grain boundaries 123 and may be associated with an amorphous ballast layer 124) with a conductive metal oxide layer 1214 adjacent the first conductive electrode 1212. A second conductive electrode 1216 is adjacent the conductive metal oxide layer 1214. The second conductive electrode 1216 may be electrically connected to a bit line 1232. The first conductive electrode 1212 may be coupled with a transistor 1234. The transistor 1234 may be coupled with a wordline 1236 and a source line 1238 in a manner that will be understood to those skilled in the art. The memory bit cell 1200 may further include additional read and write circuitry (not shown), a sense amplifier (not shown), a bit line reference (not shown), and the like, as will be understood by those skilled in the art, for the operation of the memory bit cell 1200. It is to be appreciated that a plurality of the memory bit cells 1200 may be operably connected to one another to form a memory array, wherein the memory array can be incorporated into a non-volatile memory region of a substrate in common with a logic region. It is to be

appreciated that the transistor 1234 may be connected to the second conductive electrode 1216 or the first conductive electrode 1212, although only the latter is shown.

Figure 13 illustrates a block diagram of an electronic system 1300, in accordance with an embodiment of the present invention. The electronic system 1300 can correspond to, for example, a portable system, a computer system, a process control system, or any other system that utilizes a processor and an associated memory. The electronic system 1300 may include a microprocessor 1302 (having a processor 1304 and control unit 1306), a memory device 1308, and an input/output device 1310 (it is to be appreciated that the electronic system 1300 may have a plurality of processors, control units, memory device units and/or input/output devices in various embodiments). In one embodiment, the electronic system 1300 has a set of instructions that define operations which are to be performed on data by the processor 1304, as well as, other transactions between the processor 1304, the memory device 1308, and the input/output device 1310. The control unit 1306 coordinates the operations of the processor 1304, the memory device 1308 and the input/output device 1310 by cycling through a set of operations that cause instructions to be retrieved from the memory device 1308 and executed. The memory device 1308 can include a memory element having a conductive oxide and electrode stack as described in the present description. In an embodiment, the memory device 1308 is embedded in the microprocessor 1302, as depicted in Figure 13. In an embodiment, the processor 1304, or another component of electronic system 1300, includes an array of RRAM devices, each having an amorphous bottom ballast layer.

Figure 14 illustrates a computing device 1400 in accordance with one embodiment of the invention. The computing device 1400 houses a board 1402. The board 1402 may include a number of components, including but not limited to a processor 1404 and at least one communication chip 1406. The processor 1404 is physically and electrically coupled to the board 1402. In some implementations the at least one communication chip 1406 is also physically and electrically coupled to the board 1402. In further implementations, the communication chip 1406 is part of the processor 1404.

Depending on its applications, computing device 1400 may include other components that may or may not be physically and electrically coupled to the board 1402. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communication chip 1406 enables wireless communications for the transfer of data to and from the computing device 1400. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1406 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 1400 may include a plurality of communication chips 1406. For instance, a first communication chip 1406 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1206 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 1404 of the computing device 1400 includes an integrated circuit die packaged within the processor 1404. In some implementations of embodiments of the invention, the integrated circuit die of the processor includes one or more arrays, such as RRAM memory arrays integrated into a logic processor, built in accordance with embodiments of the present invention. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 1406 also includes an integrated circuit die packaged within the communication chip 1406. In accordance with another implementation of an embodiment of the invention, the integrated circuit die of the communication chip includes RRAM memory arrays integrated into a logic processor, built in accordance with embodiments of the present invention.

In further implementations, another component housed within the computing device 1400 may contain a stand-alone integrated circuit memory die that includes one or more arrays, such as RRAM memory arrays integrated into a logic processor, built in accordance with embodiments of the present invention.

In various implementations, the computing device 1400 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital

video recorder. In further implementations, the computing device 1400 may be any other electronic device that processes data.

Accordingly, one or more embodiments of the present invention relate generally to the fabrication of embedded microelectronic memory. The microelectronic memory may be non-volatile, wherein the memory can retain stored information even when not powered. One or more embodiments of the present invention relate to the fabrication of RRAM memory arrays integrated into a logic processor. Such arrays may be used in an embedded non-volatile memory, either for its non-volatility, or as a replacement for embedded dynamic random access memory (eDRAM). For example, such an array may be used for 1T-1R memory or 2T-1R memory (R = resistor) at competitive cell sizes within a given technology node.

Figure 15 illustrates an interposer 1500 that includes one or more embodiments of the invention. The interposer 1500 is an intervening substrate used to bridge a first substrate 1502 to a second substrate 1504. The first substrate 1502 may be, for instance, an integrated circuit die. The second substrate 1504 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 1500 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 1500 may couple an integrated circuit die to a ball grid array (BGA) 1506 that can subsequently be coupled to the second substrate 1504. In some embodiments, the first and second substrates 1502/1504 are attached to opposing sides of the interposer 1500. In other embodiments, the first and second substrates 1502/1504 are attached to the same side of the interposer 1500. And in further embodiments, three or more substrates are interconnected by way of the interposer 1500.

The interposer 1500 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

The interposer may include metal interconnects 1508 and vias 1510, including but not limited to through-silicon vias (TSVs) 1512. The interposer 1500 may further include embedded devices 1514, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 1500. In accordance with

embodiments of the invention, apparatuses or processes disclosed herein may be used in the fabrication of interposer 1500.

Thus, embodiments of the present invention include approaches for fabricating RRAM stacks with an amorphous bottom ballast layer, and the resulting structures and devices.

5 In an embodiment, a resistive random access memory (RRAM) device includes a conductive interconnect disposed in an inter-layer dielectric (ILD) layer disposed above a substrate. An RRAM element is disposed on the conductive interconnect. The RRAM element includes a first electrode layer disposed on the uppermost surface of the conductive interconnect. An amorphous ballast layer is disposed on the first electrode layer. A resistance switching layer
10 is disposed on the amorphous ballast layer. The amorphous ballast layer is separate and distinct from the first electrode layer and from the resistance switching layer. A second electrode layer is disposed above the resistance switching layer.

In one embodiment, the first electrode layer includes a plurality of crystal grain boundaries therein. The amorphous ballast layer is a continuous layer in direct contact with
15 exposed ones of the plurality of crystal grain boundaries.

In one embodiment, the amorphous ballast layer includes an oxynitride derivative of a transition metal species.

In one embodiment, the oxynitride derivative of the transition metal species is a TiO_xN_y -based oxynitride derivative, where both x and y are greater than 0.

20 In one embodiment, the second electrode layer is disposed on the resistance switching layer.

In one embodiment, the second electrode layer is disposed on an oxygen exchange layer disposed on the resistance switching layer.

In one embodiment, the amorphous ballast layer has a thickness approximately in the
25 range of 1-2 nanometers.

In one embodiment, the RRAM device of further includes a dielectric sidewall spacer laterally adjacent to and in contact with sidewalls of the second electrode layer, the resistance switching layer, the amorphous ballast layer, and the first electrode layer of the RRAM element.

In one embodiment, the conductive interconnect is a conductive line further coupled to a
30 second RRAM element.

In one embodiment, the conductive interconnect is a conductive via.

In one embodiment, the conductive interconnect is coupled to a drain region of an underlying select transistor disposed in or above the substrate.

In an embodiment, a resistive random access memory (RRAM) device includes a
35 conductive interconnect disposed in a first inter-layer dielectric (ILD) layer disposed above a

substrate. A second ILD layer is disposed above the first ILD layer. The second ILD layer has an opening exposing at least a portion of the conductive interconnect. An RRAM element is disposed in the opening of the second ILD layer and on the exposed portion of the conductive interconnect. The RRAM element includes a first electrode layer disposed on the uppermost surface of the conductive interconnect and having sidewall portions along sidewalls of the opening in the second ILD layer. The RRAM element also includes an amorphous ballast layer disposed on the first electrode layer and having sidewall portions along the sidewall portions of the first electrode layer. The amorphous ballast layer is separate and distinct from the first electrode layer. The RRAM element also includes a resistance switching layer disposed on the amorphous ballast layer and having sidewall portions along the sidewall portions of the amorphous ballast layer. The resistance switching layer is separate and distinct from the amorphous ballast layer. The RRAM element also includes a second electrode layer disposed above the resistance switching layer and having sidewall portions along the sidewall portions of the resistance switching layer.

In one embodiment, the first electrode layer includes a plurality of crystal grain boundaries therein. The amorphous ballast layer is a continuous layer in direct contact with exposed ones of the plurality of crystal grain boundaries.

In one embodiment, the amorphous ballast layer includes an oxynitride derivative of a transition metal species.

In one embodiment, the oxynitride derivative of the transition metal species is a TiO_xN_y -based oxynitride derivative, where both x and y are greater than 0.

In one embodiment, the second electrode layer is disposed on the resistance switching layer.

In one embodiment, the second electrode layer is disposed on an oxygen exchange layer disposed on the resistance switching layer.

In one embodiment, the amorphous ballast layer has a thickness approximately in the range of 1-2 nanometers.

In one embodiment, the conductive interconnect is a conductive line further coupled to a second RRAM element.

In one embodiment, the conductive interconnect is a conductive via.

In one embodiment, the conductive interconnect is coupled to a drain region of an underlying select transistor disposed in or above the substrate.

In an embodiment, a method of fabricating a resistive random access memory (RRAM) device includes forming a conductive interconnect in an inter-layer dielectric (ILD) layer formed above a substrate. The method also includes forming a first electrode layer on the conductive

interconnect by a physical vapor deposition (PVD) process. A plurality of crystal grain boundaries is formed in the first electrode layer during the PVD process. The method also includes forming an amorphous ballast layer on the first electrode layer. The amorphous ballast layer is formed as a continuous layer in direct contact with exposed ones of the plurality of
5 crystal grain boundaries of the first electrode layer. The method also includes forming a resistance switching layer on the amorphous ballast layer. The method also includes forming a second electrode layer above the resistance switching layer.

In one embodiment, forming the amorphous ballast layer includes using a deposition process selected from the group consisting of a chemical vapor deposition (CVD) process and an
10 atomic layer deposition (ALD) process.

In one embodiment, materials of the first electrode layer, the amorphous ballast layer, the resistance switching layer, and the second electrode layer are patterned to form an RRAM element of the RRAM device using a subtractive etching process. The method further includes forming a dielectric sidewall spacer laterally adjacent to and in contact with sidewalls of the first
15 electrode layer, the amorphous ballast layer, the resistance switching layer, and the second electrode layer.

In one embodiment, materials of the first electrode layer, the amorphous ballast layer, the resistance switching layer, and the second electrode layer are formed in an opening of a second ILD layer formed above the ILD layer, the opening exposing at least a portion of an uppermost
20 surface of the conductive interconnect.

CLAIMS

What is claimed is:

1. A resistive random access memory (RRAM) device, comprising:
 - 5 a conductive interconnect disposed in an inter-layer dielectric (ILD) layer disposed above a substrate; and
 - an RRAM element disposed on the conductive interconnect, the RRAM element comprising:
 - a first electrode layer disposed on the uppermost surface of the conductive interconnect;
 - 10 an amorphous ballast layer disposed on the first electrode layer;
 - a resistance switching layer disposed on the amorphous ballast layer, wherein the amorphous ballast layer is separate and distinct from the first electrode layer and from the resistance switching layer; and
 - a second electrode layer disposed above the resistance switching layer.
- 15 2. The RRAM device of claim 1, wherein the first electrode layer comprises a plurality of crystal grain boundaries therein, and wherein the amorphous ballast layer is a continuous layer in direct contact with exposed ones of the plurality of crystal grain boundaries.
- 20 3. The RRAM device of claim 1, wherein the amorphous ballast layer comprises an oxynitride derivative of a transition metal species.
4. The RRAM device of claim 3, wherein the oxynitride derivative of the transition metal species is a TiO_xN_y -based oxynitride derivative, where both x and y are greater than 0.
- 25 5. The RRAM device of claim 1, wherein the second electrode layer is disposed on the resistance switching layer.
6. The RRAM device of claim 1, wherein the second electrode layer is disposed on an oxygen exchange layer disposed on the resistance switching layer.
- 30 7. The RRAM device of claim 1, wherein the amorphous ballast layer has a thickness approximately in the range of 1-2 nanometers.
- 35 8. The RRAM device of claim 1, further comprising:

a dielectric sidewall spacer laterally adjacent to and in contact with sidewalls of the second electrode layer, the resistance switching layer, the amorphous ballast layer, and the first electrode layer of the RRAM element.

- 5 9. The RRAM device of claim 1, wherein the conductive interconnect is a conductive line further coupled to a second RRAM element.
- 10 10. The RRAM device of claim 1, wherein the conductive interconnect is a conductive via.
- 10 11. The RRAM device of claim 1, wherein the conductive interconnect is coupled to a drain region of an underlying select transistor disposed in or above the substrate.
12. A resistive random access memory (RRAM) device, comprising:
a conductive interconnect disposed in a first inter-layer dielectric (ILD) layer disposed above
15 a substrate;
a second ILD layer disposed above the first ILD layer, the second ILD layer having an opening exposing at least a portion of the conductive interconnect; and
an RRAM element disposed in the opening of the second ILD layer and on the exposed portion of the conductive interconnect, the RRAM element comprising:
20 a first electrode layer disposed on the uppermost surface of the conductive interconnect and having sidewall portions along sidewalls of the opening in the second ILD layer;
an amorphous ballast layer disposed on the first electrode layer and having sidewall portions along the sidewall portions of the first electrode layer, the amorphous
25 ballast layer separate and distinct from the first electrode layer;
a resistance switching layer disposed on the amorphous ballast layer and having sidewall portions along the sidewall portions of the amorphous ballast layer, the resistance switching layer separate and distinct from the amorphous ballast layer;
and
30 a second electrode layer disposed above the resistance switching layer and having sidewall portions along the sidewall portions of the resistance switching layer.
13. The RRAM device of claim 12, wherein the first electrode layer comprises a plurality of crystal grain boundaries therein, and wherein the amorphous ballast layer is a continuous layer in
35 direct contact with exposed ones of the plurality of crystal grain boundaries.

14. The RRAM device of claim 12, wherein the amorphous ballast layer comprises an oxynitride derivative of a transition metal species.

5 15. The RRAM device of claim 14, wherein the oxynitride derivative of the transition metal species is a TiO_xN_y -based oxynitride derivative, where both x and y are greater than 0.

16. The RRAM device of claim 12, wherein the second electrode layer is disposed on the resistance switching layer.

10

17. The RRAM device of claim 12, wherein the second electrode layer is disposed on an oxygen exchange layer disposed on the resistance switching layer.

18. The RRAM device of claim 12, wherein the amorphous ballast layer has a thickness
15 approximately in the range of 1-2 nanometers.

19. The RRAM device of claim 12, wherein the conductive interconnect is a conductive line further coupled to a second RRAM element.

20 20. The RRAM device of claim 12, wherein the conductive interconnect is a conductive via.

21. The RRAM device of claim 12, wherein the conductive interconnect is coupled to a drain region of an underlying select transistor disposed in or above the substrate.

25 22. A method of fabricating a resistive random access memory (RRAM) device, the method comprising:

forming a conductive interconnect in an inter-layer dielectric (ILD) layer formed above a substrate;

forming a first electrode layer on the conductive interconnect by a physical vapor deposition
30 (PVD) process, wherein a plurality of crystal grain boundaries is formed in the first electrode layer during the PVD process;

forming an amorphous ballast layer on the first electrode layer, the amorphous ballast layer formed as a continuous layer in direct contact with exposed ones of the plurality of crystal grain boundaries of the first electrode layer;

35 forming a resistance switching layer on the amorphous ballast layer; and

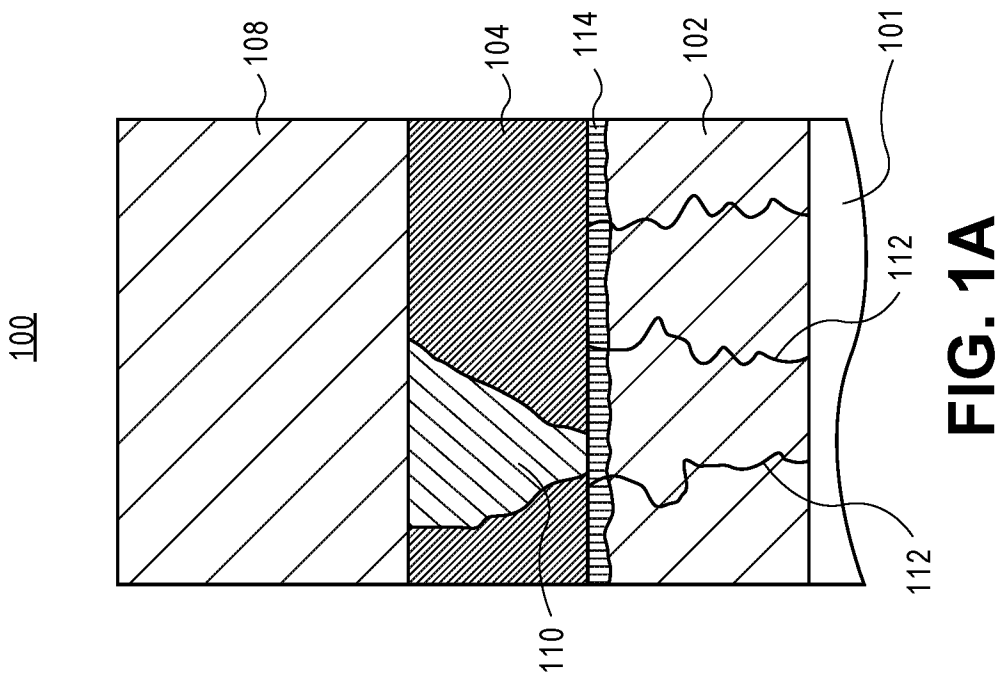
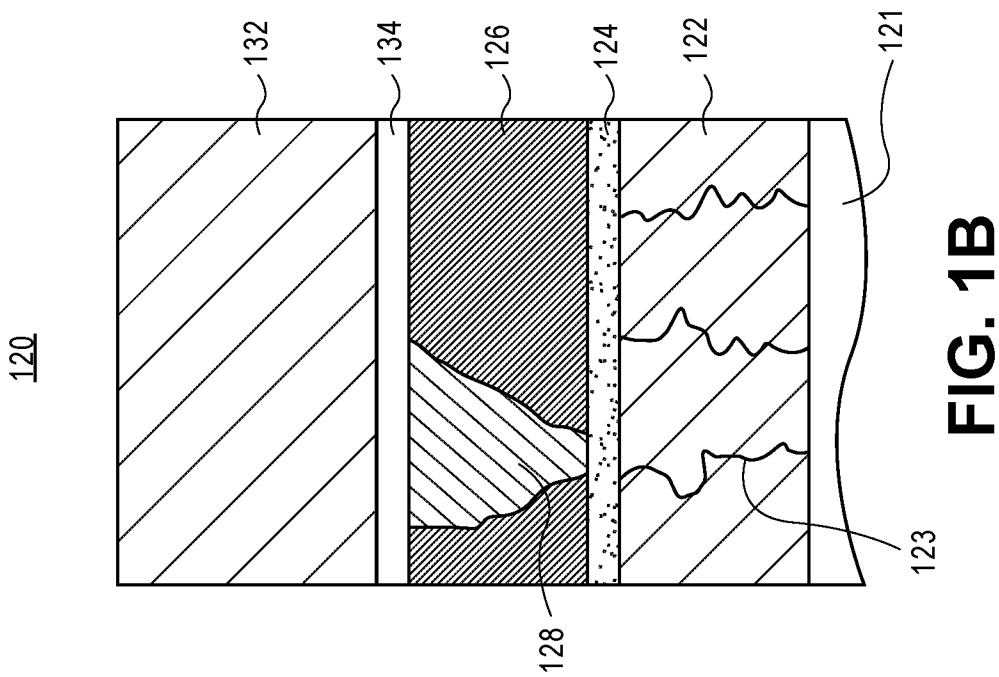
forming a second electrode layer above the resistance switching layer.

23. The method of claim 22, wherein forming the amorphous ballast layer comprises using a deposition process selected from the group consisting of a chemical vapor deposition (CVD) process and an atomic layer deposition (ALD) process.

24. The method of claim 22, wherein materials of the first electrode layer, the amorphous ballast layer, the resistance switching layer, and the second electrode layer are patterned to form an RRAM element of the RRAM device using a subtractive etching process, the method further comprising:

forming a dielectric sidewall spacer laterally adjacent to and in contact with sidewalls of the first electrode layer, the amorphous ballast layer, the resistance switching layer, and the second electrode layer.

25. The method of claim 22, wherein materials of the first electrode layer, the amorphous ballast layer, the resistance switching layer, and the second electrode layer are formed in an opening of a second ILD layer formed above the ILD layer, the opening exposing at least a portion of an uppermost surface of the conductive interconnect.



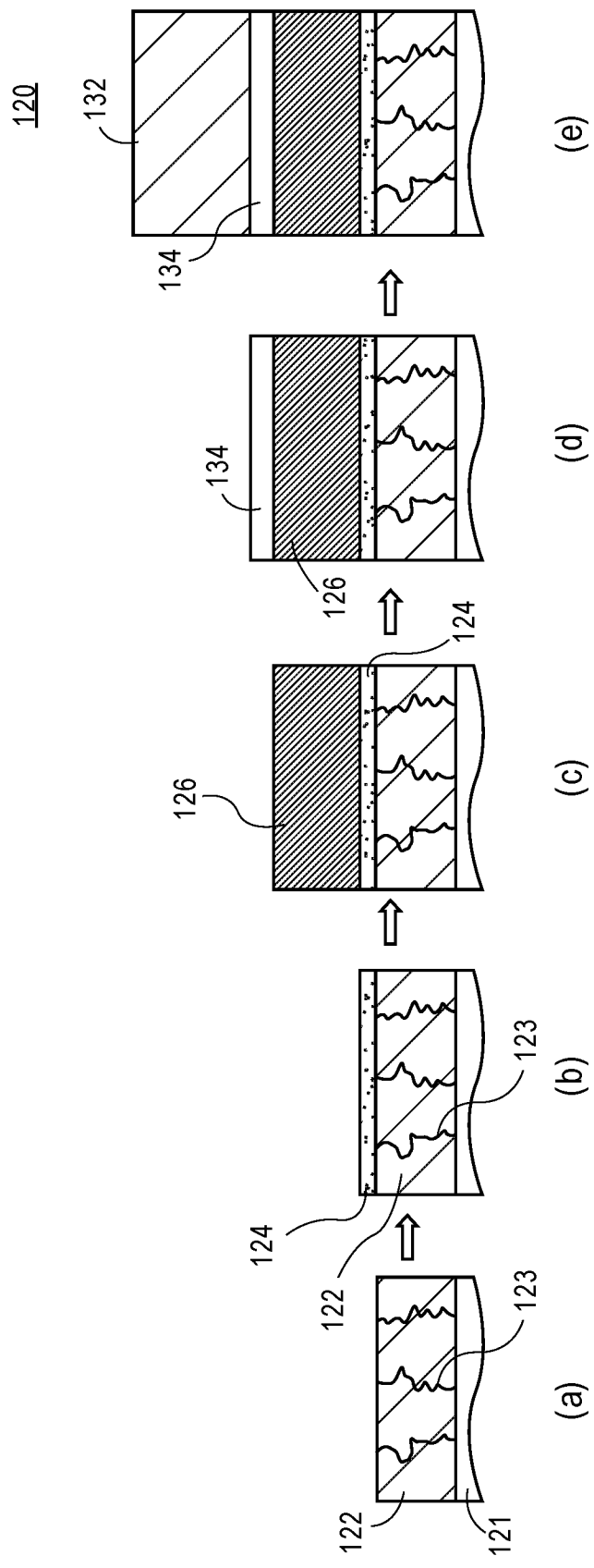
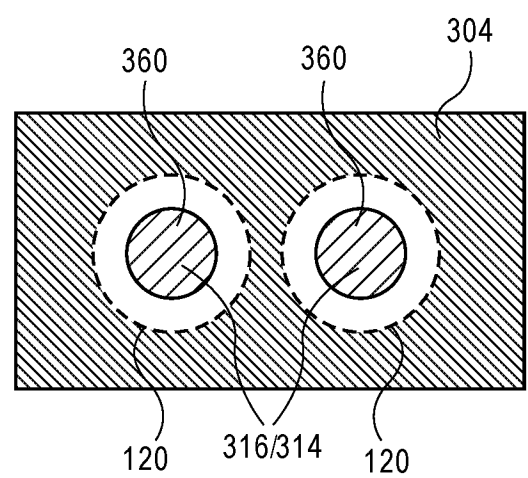
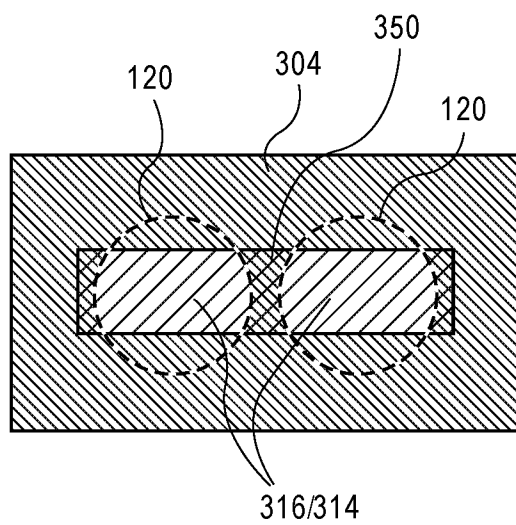
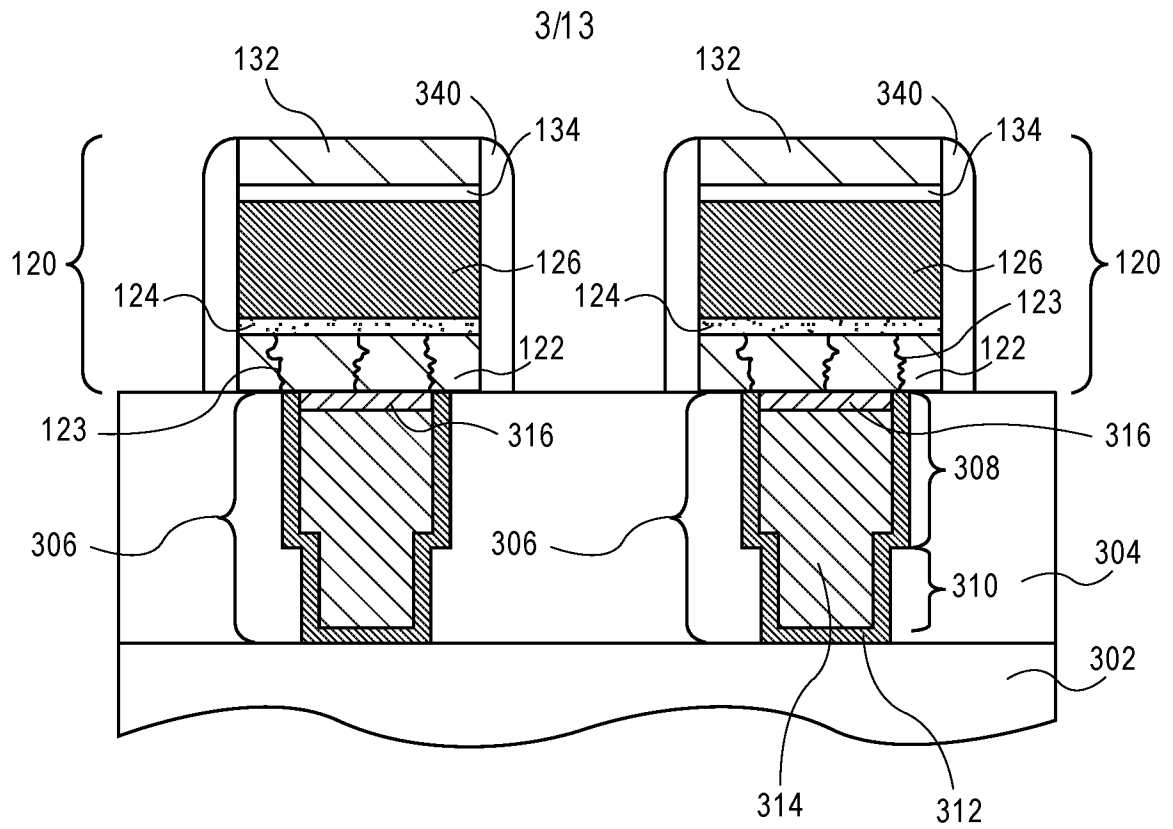


FIG. 2



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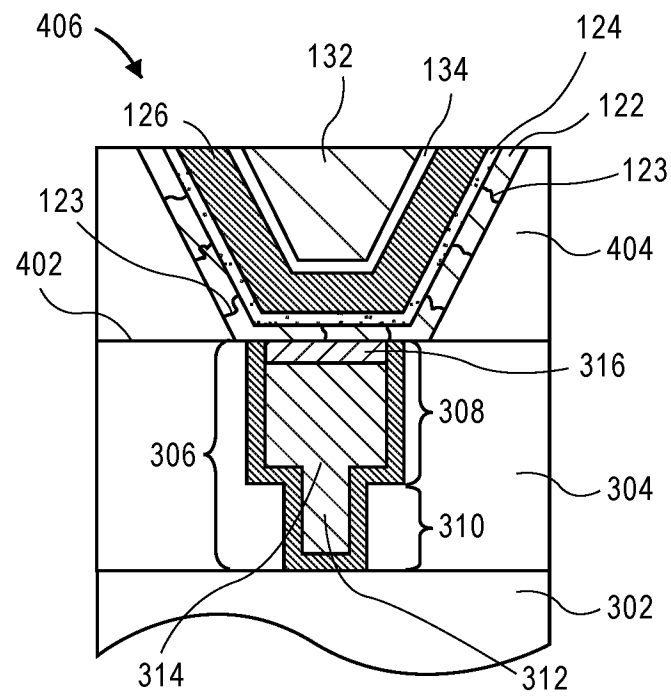


FIG. 4

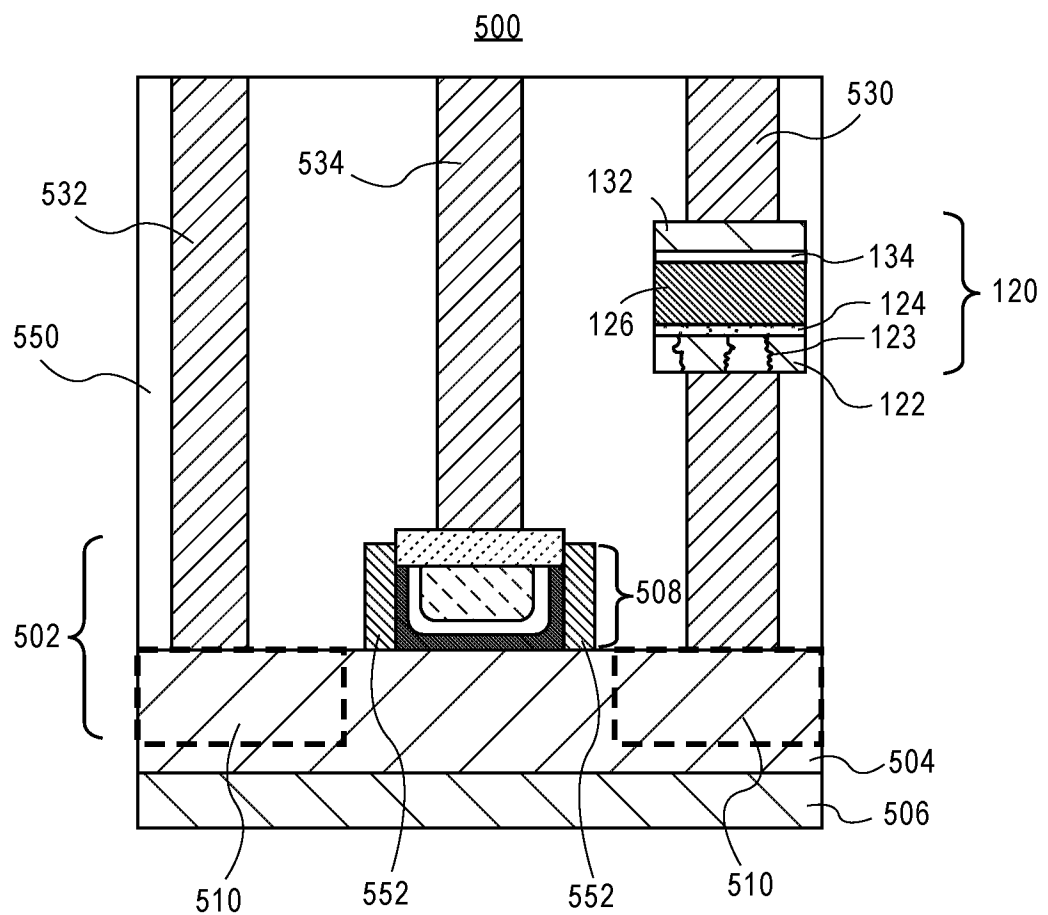


FIG. 5

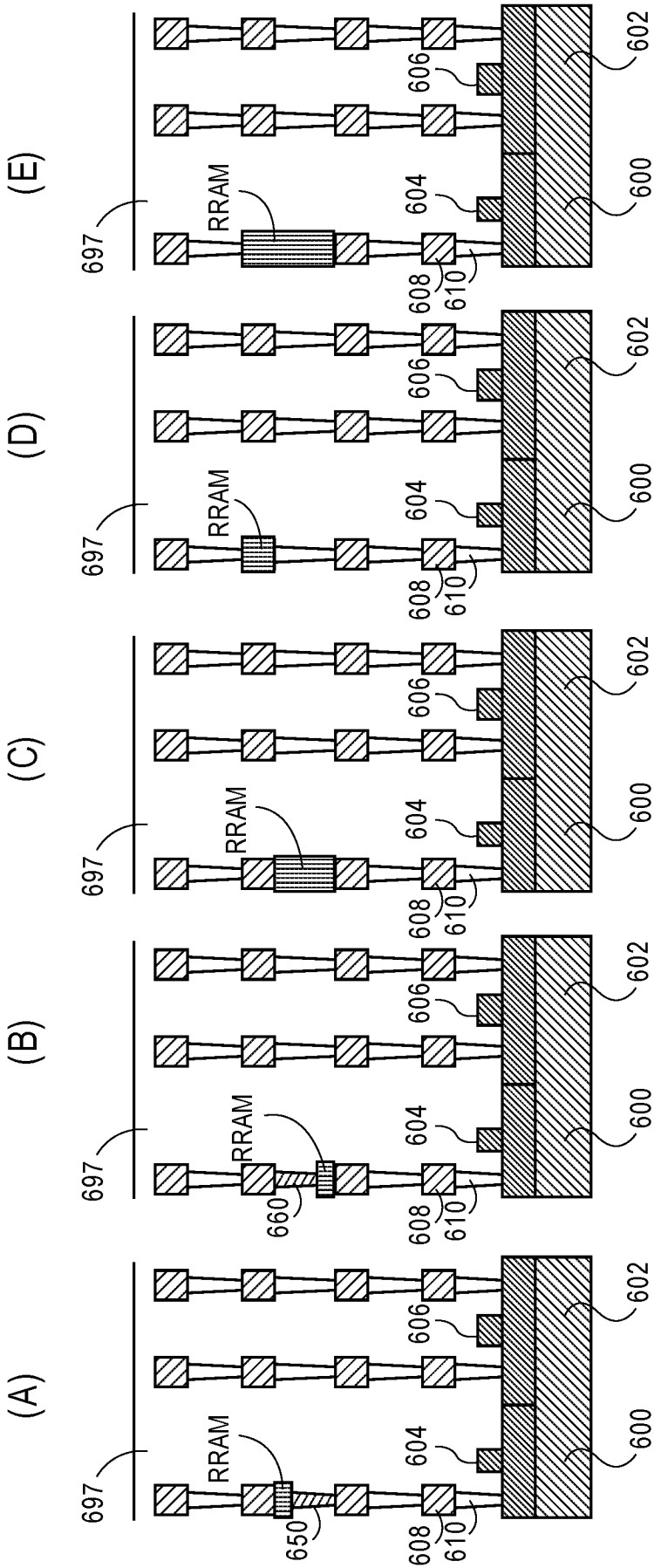


FIG. 6A

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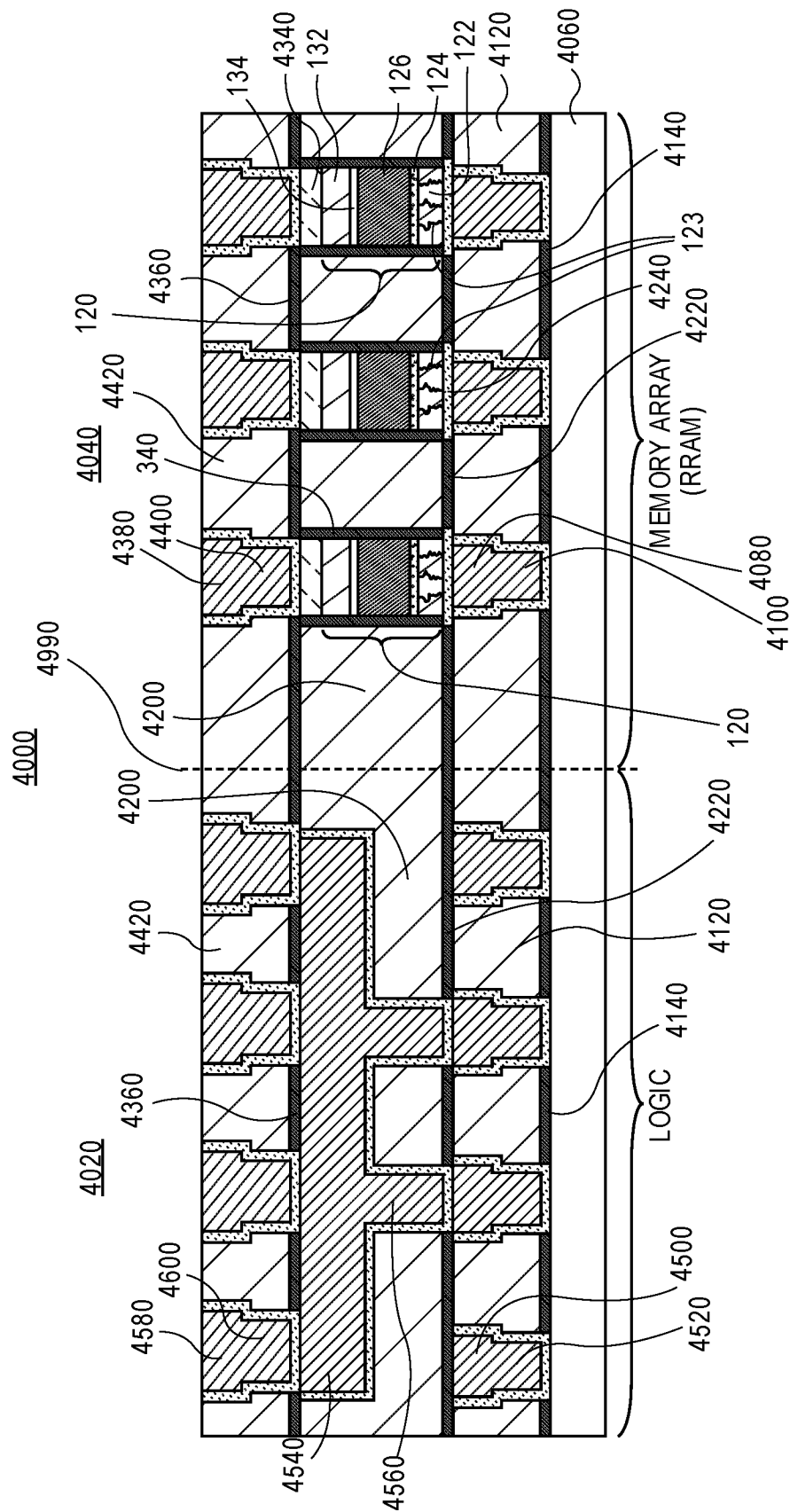


FIG. 6B

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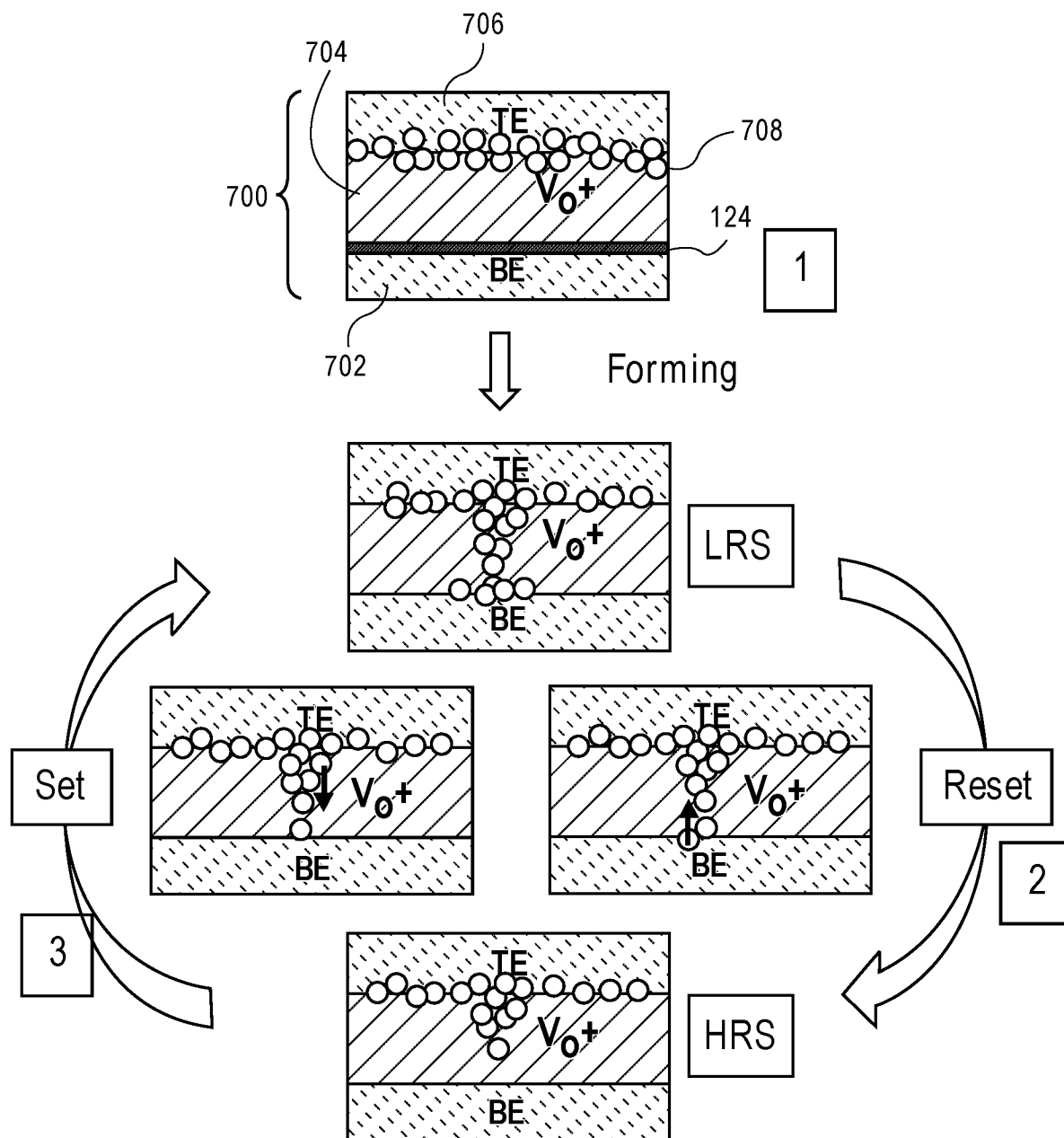
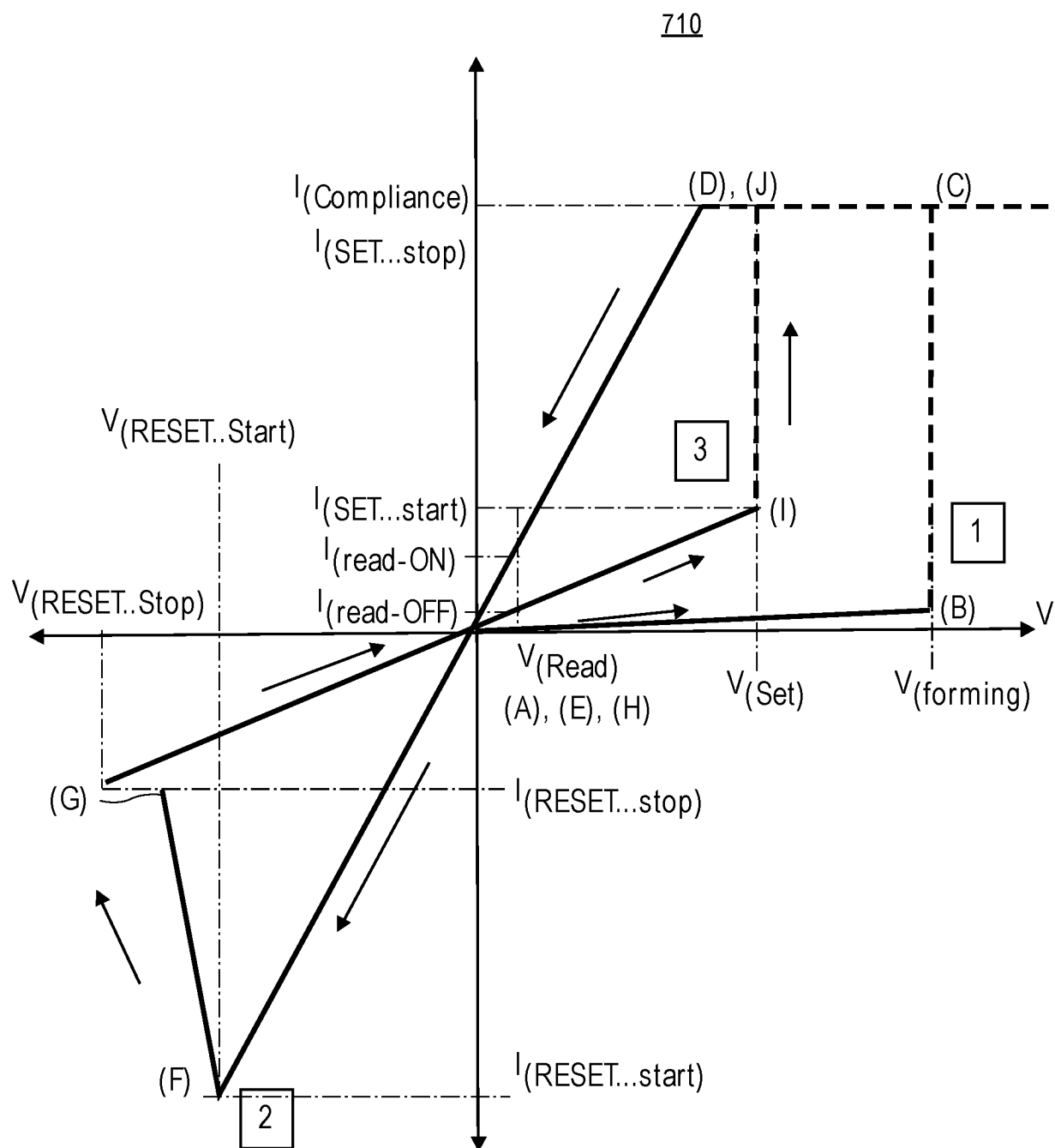


FIG. 7A

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**FIG. 7B**

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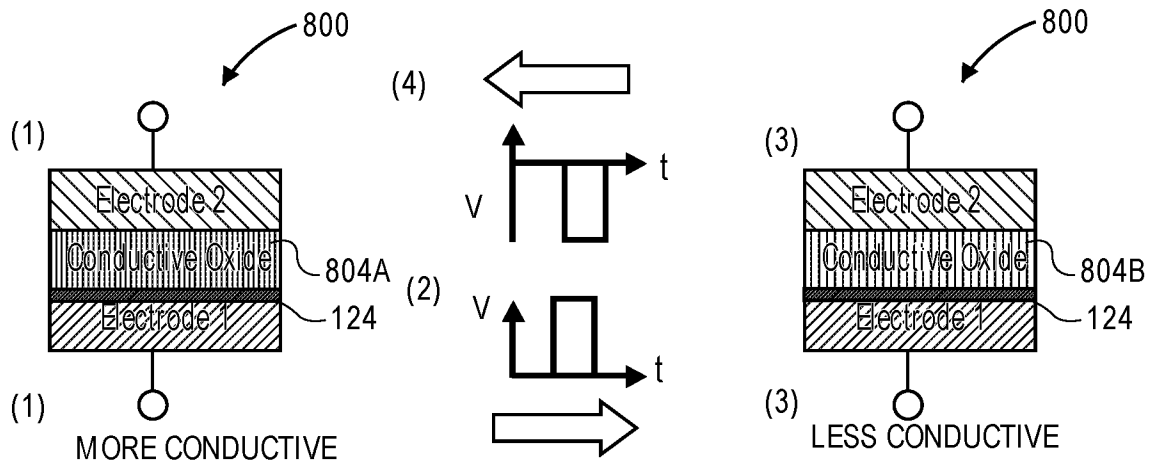


FIG. 8

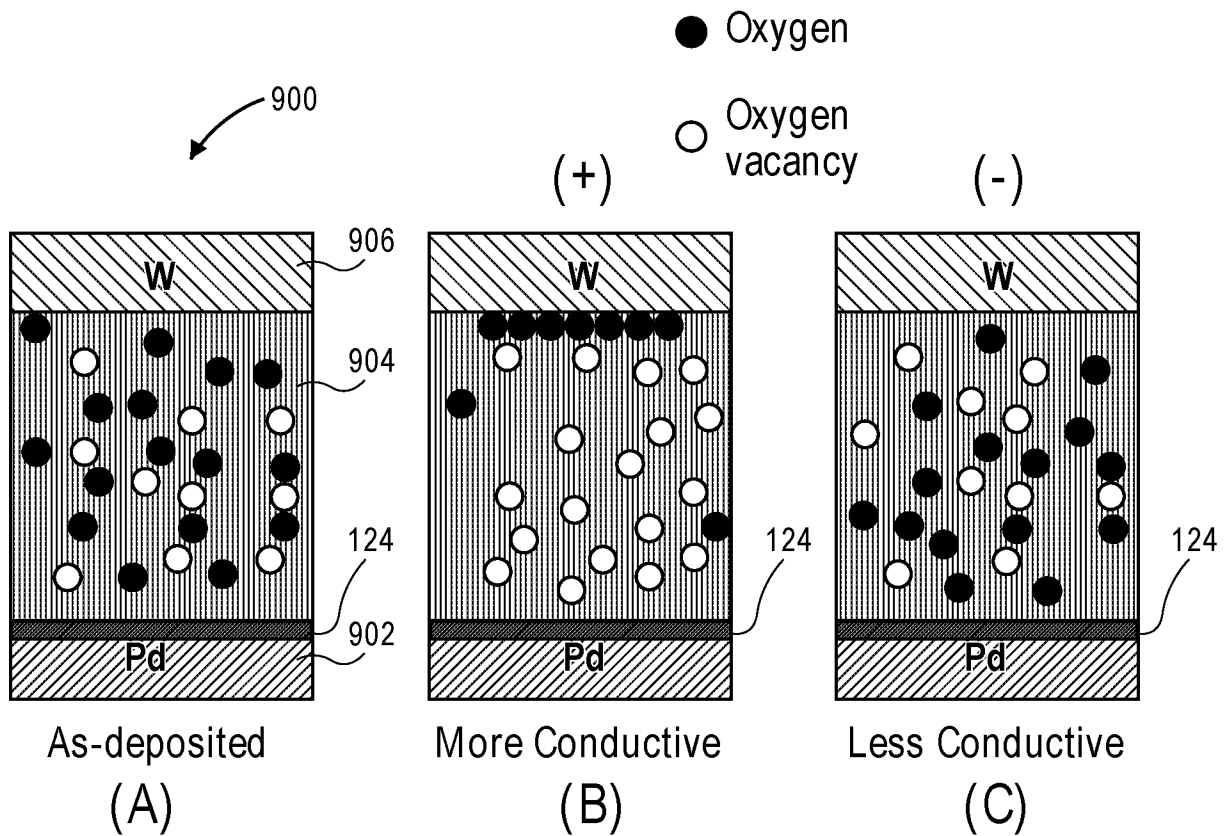


FIG. 9

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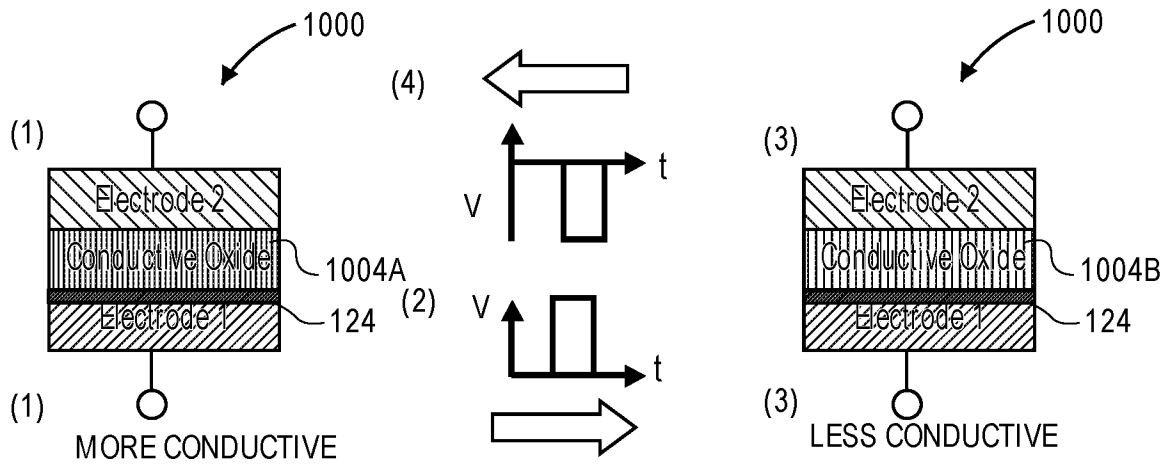


FIG. 10

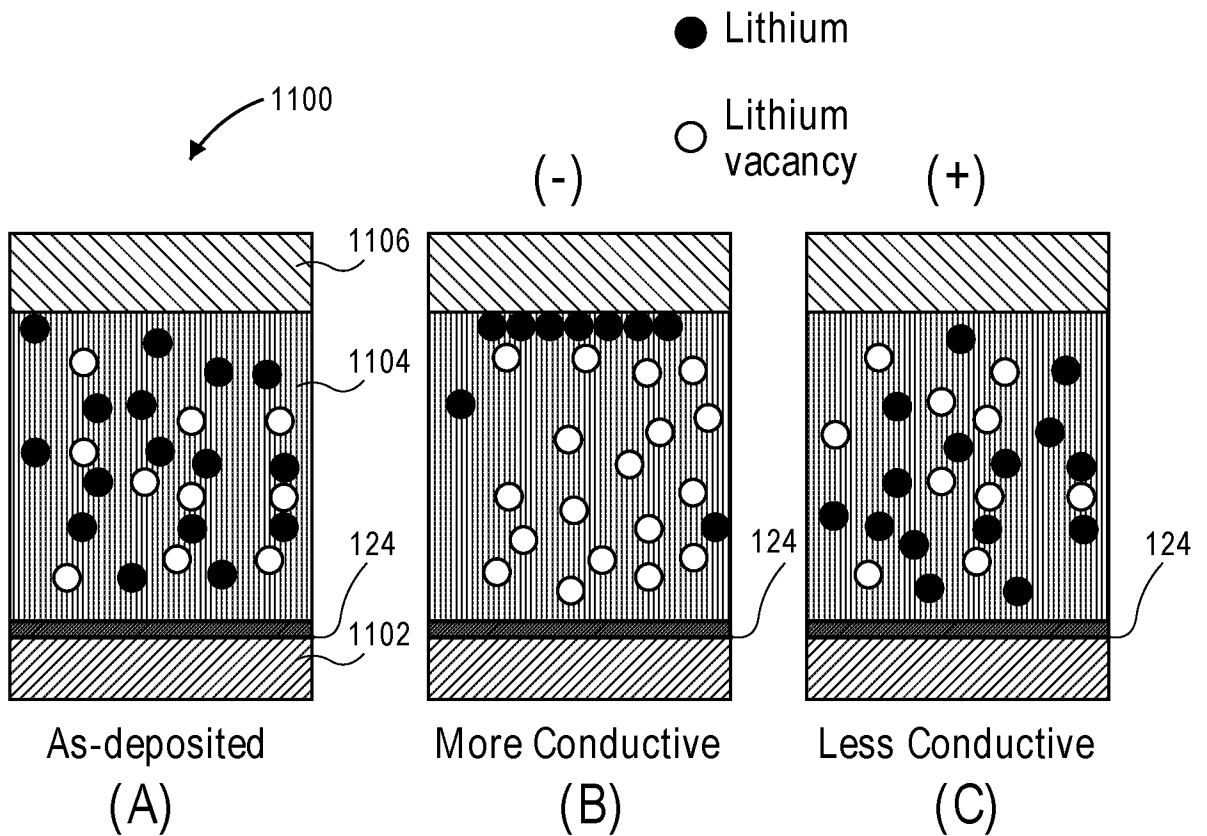
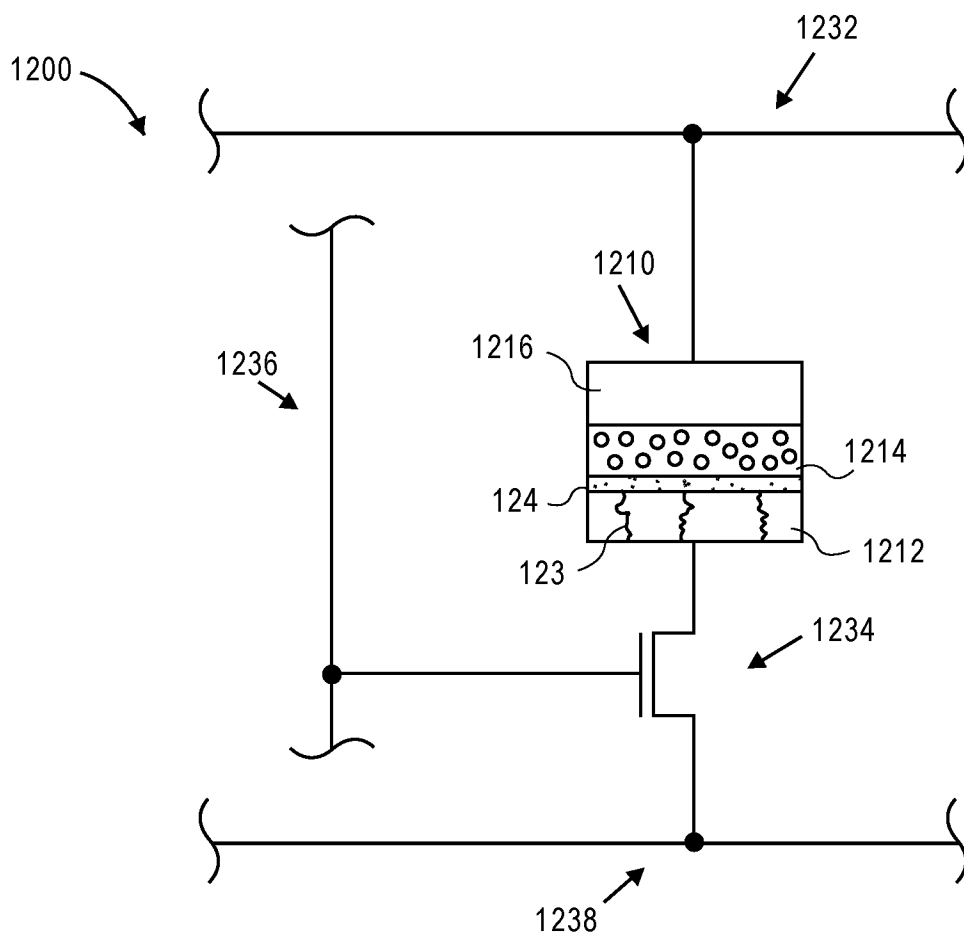
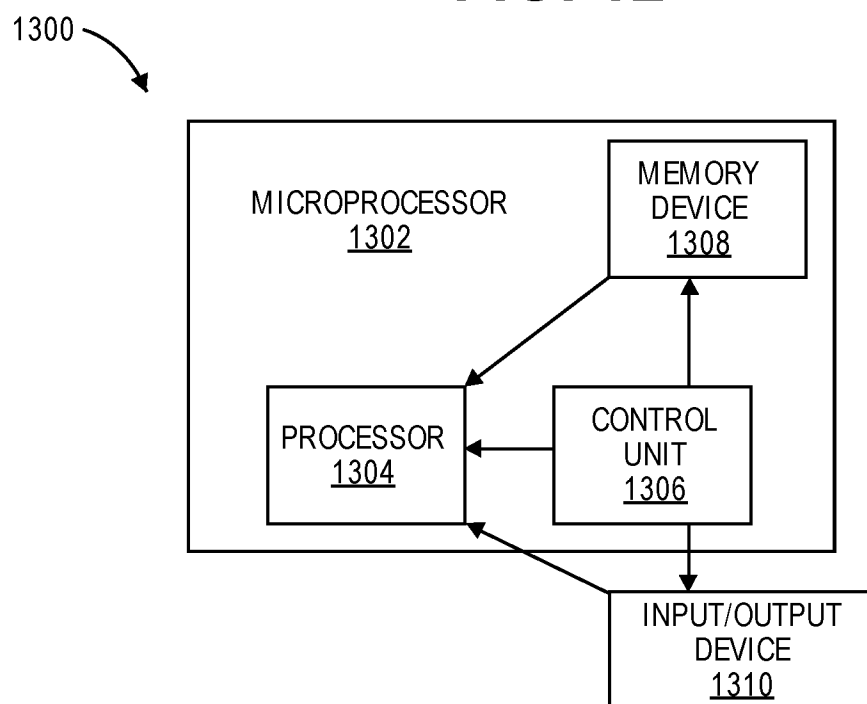


FIG. 11

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**FIG. 12****FIG. 13**

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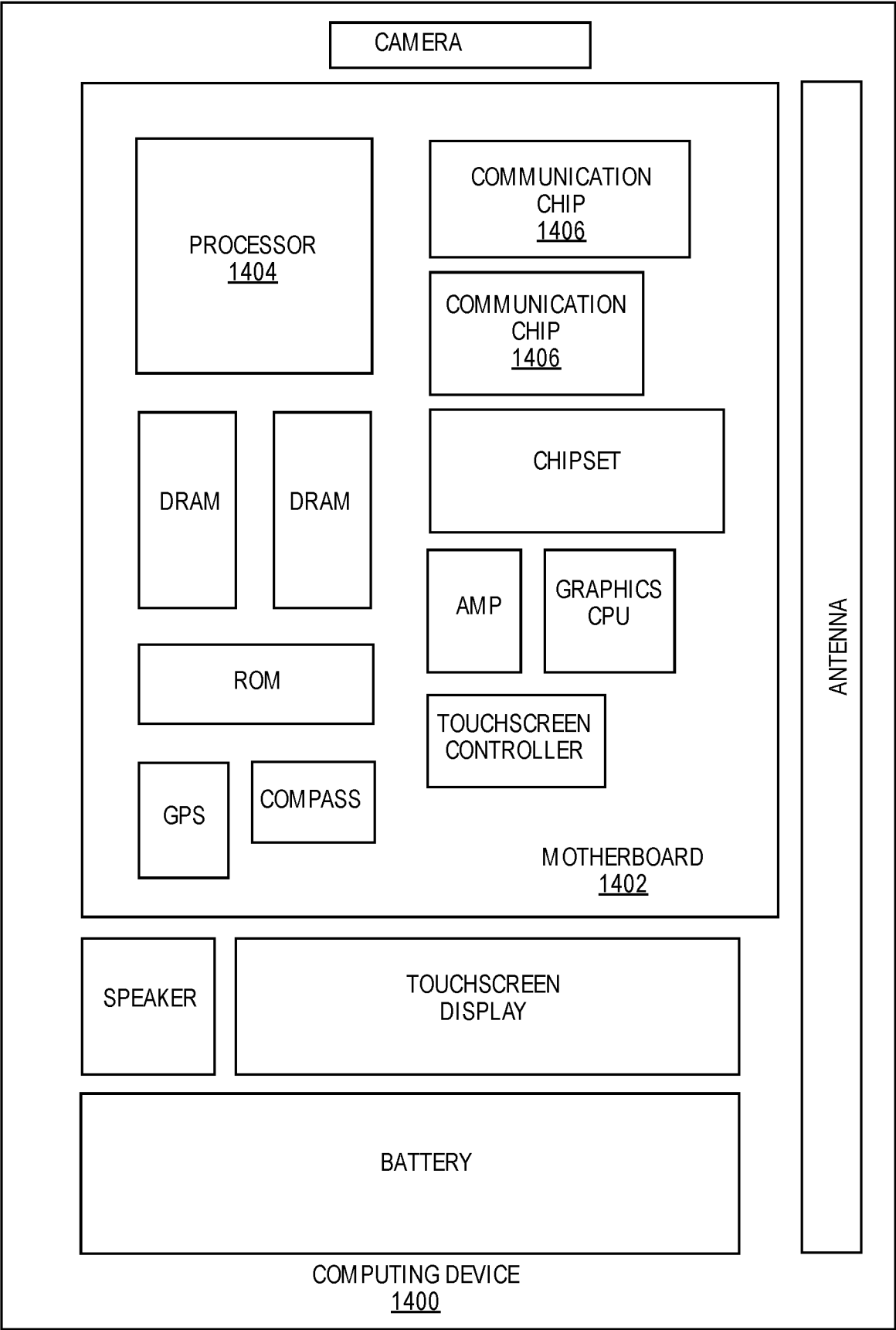


FIG. 14

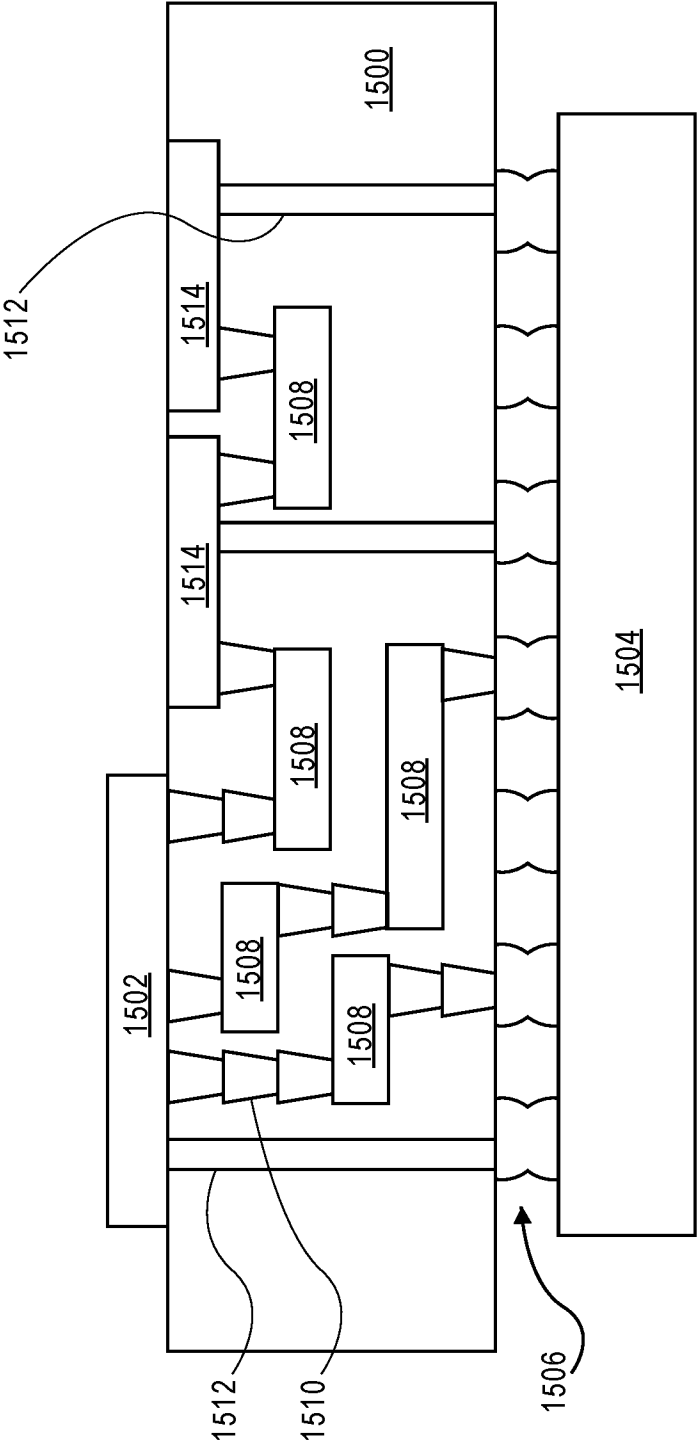


FIG. 15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/040203**A. CLASSIFICATION OF SUBJECT MATTER****G11C 13/00(2006.01)i, H01L 27/24(2006.01)i, H01L 45/00(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 13/00; H01L 21/4763; H01L 45/00; H01L 47/00; H01L 23/538; H01J 1/30; H01L 29/02; H01L 27/24

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: RRAM, inter-layer dielectric(ILD), layer, memory, amorphous, ballast, and similar terms

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 9178144 B1 (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.) 03 November 2015 See column 3, line 42 - column 4, line 34; column 4, line 56 - column 5, line 4; column 6, lines 16-18; column 6, lines 30-34; column 6, lines 54-59; and figures 2, 5.	1-25
Y	US 6882100 B2 (ZHIZHANG CHEN et al.) 19 April 2005 See column 5, lines 20-63; column 10, lines 56-65; column 11, lines 19-24; figures 1, 11C, 11G; and claims 10-11.	1-25
Y	US 2014-0166961 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 19 June 2014 See paragraphs [0024], [0027]; and figure 2.	22-25
A	US 8536558 B1 (SHYUE SENG (JASON) TAN et al.) 17 September 2013 See column 6, line 10 - column 7, line 62; and figures 18-29.	1-25
A	US 7833898 B2 (YU JIN LEE) 16 November 2010 See column 3, line 16 - column 4, line 65; and figures 1A-1E.	1-25

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

22 March 2017 (22.03.2017)

Date of mailing of the international search report

23 March 2017 (23.03.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

BYUN, Sung Cheal

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/040203

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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US 8536558 B1	17/09/2013	None	

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/040203Patent document
cited in search reportPublication
datePatent family
member(s)Publication
date

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16/11/2010

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29/07/2011

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