(54) Title: CELL BALANCING METHOD AND SYSTEM
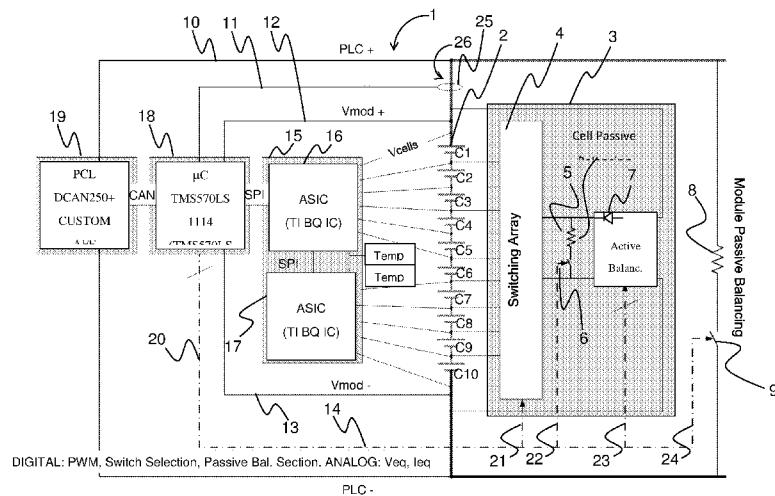
Fig. 1

(57) Abstract: The invention relates to a system for battery cell balancing comprising a cell monitoring block (16) configured to monitor the voltage or a related quantity across individual cells (C_1, C_2,....C_N) in a battery cell module; a microcontroller (18) con-figured for monitoring the positive terminal voltage (12) and the negative terminal voltage (13) of said battery cell module, and for monitoring (11) the output current I_{mod} of said module, and monitored cell voltage of said individual cells (C_1, C_2,....C_N), where the microcontroller (18) is configured to provide a control signal (20) based at least said positive terminal voltage (12), said negative ter-minal voltage (13), said output current I_{mod} of said module, and said monitored cell voltage of said individual cells; and a hybrid module balancing block configured to provide either an active or a passive cell balancing or a combination of active and passive cell balancing of the cells (C_1, C_2,....C_N) in the specific module under the control of the control signal provided by the microcontroller. The invention further relates to a method for battery cell balancing in a battery comprising one or more modules each comprising one or more cells.

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

CELL BALANCING METHOD AND SYSTEM

TECHNICAL FIELD

The present invention relates generally to systems and methods for cell balancing in battery
5   systems and more specifically to such systems and methods that apply a combination of active
and passive cell balancing in order to optimize cell balancing under different conditions.

BACKGROUND OF THE INVENTION

Cell balancing systems and methods are known within the art of battery management and such
10   systems and methods are vital in optimizing the performance of batteries composed of a large
number of cells such as those required in electrochemical storage systems of medium and
large scale, for instance designed to operate in electric vehicles.

The main purpose of such systems and methods is to maintain homogeneous conditions
between all cells of the battery, thus allowing optimal operation in terms of efficiency, stored
15   energy and lifetime. In order to reach the desired operating voltage of a battery pack, cells are
connected in series. If the cells are perfectly balanced, the total voltage will be equally divided
per cell. However, in practice, the cells will be unbalanced. Cell balancing process equalizes
the charge on all the cells in the chain and thus increasing battery capacity. This process is
required because maximum charge is limited by the highest cell voltage, and maximum
20   discharge is limited by the lowest. Its use is desirable in almost every technology (the only
exception is the technology Redox-Flow) and is essential in some cases as in ion-lithium
batteries.

During a charging and discharging cycle, batteries in a series string may not operate in a
uniform manner. Batteries are inter alia characterized by their internal resistance, which can
25   vary within certain tolerance limits of a given type of battery cell. Batteries with more efficient
cells (i.e. with cells having a relatively low internal resistance) tend to have a higher voltage
while batteries with less efficient cells remain at a lower voltage. Once the imbalance occurs,
it will tend to increase with additional usage. Thus, when charging batteries, some reach full
charge long before others. Likewise, weaker cells will tend to discharge much more rapidly
30   than the rest of the pack. This leads to under-utilization of most of the cells. In summary, when

these imbalanced batteries are left in use without any control, such as cell equalization, the energy storage capacity decreases severely.

Series-connected battery strings have been used for many applications, such as electric vehicles, hybrid electric vehicles (HEVs), electric scooters, and uninterruptible power supplies.

5   Of these, an HEV battery is severely exposed to a charge and discharge environment. This exposure occurs because an HEV can recover energy from the wheels during regenerative braking (an energy source that was wasted in the past) and reuse it to propel the vehicle at low speeds or provide extra power for high acceleration. This repeated charge and discharge phenomenon aggravates the cell mismatch problem.

10   The imbalances between cells can be defined in terms of voltage or SOC (state of charge). By their nature, as previously mentioned, if no corrective actions are taken, imbalances for instance due to the internal resistance of cells will increase as time passes and charge and discharge cycles are performed on the battery, which may give rise to the case where one or more elements to reach a state of overcharge or deep-discharge while others still have a valid

15   SOC. These extreme situations can lead to a significant deterioration of the battery that along with other external factors can raise a premature failure of the entire system. The severity and rapidity with which both the imbalance and deterioration occur, largely depends on such factors as:

- Process Technology: Some technologies such as Lead Acid or NiCd among others are

20   able to tolerate certain levels of overcharge and/or deep-discharge. In some of these technologies a slight overcharge process is even used to periodically achieve balancing battery. However, other technologies such as Li-Ion, are totally intolerant to overcharge or deep-discharge conditions which may damage the battery, shortening its lifetime, and even causing hazardous situations.

25 - Battery use Cycle: Depending on the overall SOC variation of the charge and discharge currents and temperature, the process of imbalance can vary significantly. For example, in technologies in which a slight overcharge is forced, the use of an incomplete charging cycle which does not provide a 100% charging load is detrimental.

In any case it is necessary to establish a mechanism to restore the balance between all the

30   cells comprising a battery system. Even in the case of technologies that allow balancing by overcharge, they benefit both concerning efficiency and extension of life of the system.

In this sense in battery systems of a certain size (number of series-connected elements), it is desirable (or perhaps even necessary) to use balancing techniques. The benefits obtained by using equalization systems comprise (i) extension of the life span of the battery system; (ii) increased efficiency of the battery system; (iii) increased usable energy of the battery system; and (iv) improved operation safety of the battery system.

It is hence desirable to have access to cell balancing systems and methods that provide optimal cell balancing under all practical operating conditions.

DISCLOSURE OF THE INVENTION

The above and further objects and advantages are according to the present invention obtained by a cell balancing system and a cell balancing method, where the system and method apply a combination of active and passive cell balancing.

Active cell balancing is the method to apply when dissipation of cell energy as heat is to be avoided. Active cell balancing is more efficient than passive cell balancing and does not give raise to the generation of heat and hence makes it possible to apply higher balancing currents than passive balancing.

During normal use the most discharged cells in a given module are balanced obtaining the energy from their specific module.

When a specific module is in a low state of charge (SOC), active cell balancing helps to take advantage of the energy stored in the specific module by raising the SOC of cells having a SOC below the average of that specific module up to the average value and thus allowing to discharge the full module until the minimum allowed SOC for almost every cell, instead of being limited by just one cell that reaches the minimum SOC floor.

During the end of charge process if there is one or a few cells below the SOC average value, active balancing can be used too.

Passive cell balancing can for instance be applied advantageously (at least) in the following situations:

During the end of a charge process passive balancing can be used in order to reduce the SOC of a single or a few cells that are above the SOC average value of the module and then finish

the charging process with all the cells at their maximum SOC possible. If during the charging process, only a relatively few cells are insufficiently charged, active balancing can be applied in order to raise their state of charge rapidly. On the contrary, if a relatively few cells are charged above their maximum allowable state of charge, passive balancing can advantageously be applied.

According to a first aspect of the present invention, the above and further objects and advantages are provided with a system comprising:

- a cell monitoring block configured to monitor the voltage or a related quantity across individual cells (C_1, C_2,....C_N) in a battery cell module;
- a microcontroller configured for monitoring the positive terminal voltage and the negative terminal voltage of the battery cell module, and for monitoring the output current I_{mod} of the module, and monitored cell voltage of the individual cells (C_1, C_2,....C_N), where the microcontroller is configured to provide a control signal based at least the positive terminal voltage, the negative terminal voltage, the output current I_{mod} of the module and the monitored cell voltage of said individual cells;
- a hybrid module balancing block configured to provide either an active or a passive cell balancing or a combination of active and passive cell balancing of the cells (C_1, C_2,....C_N) in the specific module under the control of the control signal provided by the microcontroller.

In an embodiment of the first aspect of the invention, the hybrid module balancing block comprises:

- a switching array configured to provide active or passive or a combination of active and passive balancing to one or more of the individual cells (C_1, C_2,....C_N) in the specific module under the control of the control signal;
- a passive cell balancing means configured to provide the passive balancing under the control of said control signal;
- an active cell balancing means configured to provide the active balancing under the control of the control signal (20).

In an embodiment of the first aspect of the invention, the system comprises a passive module balancing means coupled between the positive and negative terminals of the specific module.

In an embodiment of the first aspect of the invention, the active cell balancing means is a flyback DC/DC converter.

5   In an embodiment of the first aspect of the invention, the passive cell balancing means is a resistor in series with a switch, such as for instance a MOSFET.

In an embodiment of the first aspect of the invention, the passive module balancing means is a resistor in series with a switch, such as for instance a MOSFET.

In an embodiment of the first aspect of the invention, the flyback DC/DC converter extracts
10   power from all of the cells (C_1, C_2,....C_N) of a module, and injects a controlled current to balance the most discharged cell until it is in balance with the other cells.

In an embodiment of the first aspect of the invention the controlled current is constant.

In an embodiment of the first aspect of the invention, the microcontroller is a microcontroller in a battery management system (BMS) that manages the overall performance of the battery.

15   In an embodiment of the first aspect of the invention, active balancing as applied in the modules making up a battery, whereas passive balancing is applied between modules making up the battery.

In an embodiment of the first aspect of the invention, the system comprises module state of charge (SOC) monitoring means or voltage monitoring means that monitors the SOC or voltage
20   of the modules in a battery and when an imbalance between the SOC or voltage is detected between two or more modules, passive balancing between the two or more modules in the battery is performed.

In an embodiment of the first aspect of the invention, the passive balancing between two or more modules in a battery is controlled by the hybrid module balancing block or the battery
25   management system (BMS).   According to a second aspect of the invention there is provided a method for battery cell balancing in a battery comprising at least one module comprising a plurality of cells, the method comprising the steps of:- determining if a charging process is in progress;

- choosing a module (M1);

- applying active cell balancing between cells of said module (M1);

- determining if one or more cells are charged above a predefined upper limit;

- if one or more cells are charged above said upper limit, applying passive cell balancing to this or those cells in order to reduce their charge to a value at or below said upper limit;

5   - when all cells within said module (M1) are charged, determine if there are further modules (M2, M3....) in the battery, and if this is the case repeat the above steps for the remaining modules (M2, M3....);

- when all modules of the battery have been charged, determine if there is an imbalance between the state of charge or a similar parameter of the respective modules in the battery,
10   and if this is the case, apply either passive or active balancing between respective modules in order to reduce said imbalance between modules to a required level.

In an embodiment of the second aspect of the invention, the active balancing as applied in modules making up a battery, whereas passive balancing is applied between modules making up the battery.

15   In an embodiment of the second aspect of the invention, the state of charge (SOC) or voltage is monitored by monitoring means that monitors the SOC or voltage of two or more modules in a battery and when an imbalance between the SOC or voltage is detected between two or more modules, passive balancing between the two or more modules in the battery is performed.

20   Further features of the invention will appear from the following detailed description of the invention and from the figures.

BRIEF DESCRIPTION OF THE DRAWINGS

Further benefits and advantages of the present invention will become apparent after reading the detailed description of non-limiting exemplary embodiments of the invention in conjunction
25   with the accompanying drawings, wherein

figure 1 shows an embodiment of a cell balancing system according to the present invention;

figure 2 shows a flow chart illustrating the basic steps of an embodiment of a method according to the present invention;

figure 3a and b show a schematic diagram of an isolated fly-back converter used in embodiments of the present invention;

figure 4 shows a fly-back control block used in embodiments of the present invention;

figure 5a through g show a schematic diagram of the interface with a Hercules microcontroller used in an embodiment of the invention;

figure 6a through e show a schematic diagram of a dual switch isolated flyback converter used in an embodiment of the invention;

figure 7a through g show a schematic diagram of a relay selection circuitry comprising a de-multiplexer used in an embodiment of the invention;

figure 8 shows a plot of simulation results for a 16 cell module; and

figure 9 shows a plot of simulation results for a 8 cell module.

DETAILED DESCRIPTION OF THE INVENTION

A non-limiting embodiment of a cell balancing system according to the invention is described in detail in the following. It is however understood that the invention may be implemented in other ways and that all such embodiment of the invention will fall within the scope of protection defined by the patent claims.

It is expressly noted that although specific numerical values for various parameters etc. will be mentioned in the following, such specific numerical values are only to be regarded as examples and they do not, consequently, limit the scope of the patent protection.

With reference to figure 1 there is shown an embodiment of a cell balancing system according to the present invention generally indicated by reference numeral 1 comprising means for applying a combination of active and passive cell balancing.

The system shown in figure 1 comprises a battery module that in the shown embodiment contains a series connection of ten cells C1, C2, ... C10. It is of cause understood that a different number of cells could be present in the module and that the principles of the invention would apply equally well to such modules.

It is further understood that although the term "module" is used repeatedly in the description of the embodiment shown in figure 1, the present invention is not restricted to one or more physical modules making up a total battery. A battery could thus simply comprise a number of cells coupled in series without any subdivision into specific modules or a module may simply be a fictive subdivision of a given number of cells in a battery. Thus, reference to the term "module" implies no restriction to the scope of the present invention.

The system comprises a hybrid module balancing block 3 that comprises a switching array 4, a passive balancing means, such as the resistor 5 that can be activated through a controllable switch 6, such as a MOSFET, and an active balancing device, such as a DC/DC converter 7.

Coupled across the entire module there is further connected a module passive balancing means, such as the resistor 8 that can be activated through the switch 9, such as a MOSFET.

The switching array 4, the cell passive balancing means 5 and 6, the DC/DC converter 7 and the module passive balancing means 8 and 9 are controlled by appropriate control signals, as symbolically indicated be control lines 20 through 25.

The voltages over each respective cells C1 through C10 are measured by means of a cells monitoring block 15 that in the shown embodiment comprises the two ASIC's 16 and 17 connected to the terminals of the respective cells through cell voltage measuring lines Vcells.

In order to optimize the performance of the system according to this embodiment of the invention and to maximize the balancing current and thus reducing the balancing time, the flyback converter can be controlled from the main microcontroller in the battery management system (BMS). An example of such a microcontroller is the HERCULES MCU 32-bit ARM Cortex R4 manufactured by Texas Instruments. The system and method according to the present invention can be implemented in the BMS main microcontroller, but could alternatively be implemented in a separate microcontroller. The controlling microcontroller is in the shown embodiment designated by reference numeral 18 and is in connection with the ASIC's 16 and 17 in the cells monitoring block 15 through the serial peripheral interfaces SPI.

The microcontroller 18 receives a signal indicating the positive module voltage Vmod+ via signal line 12 and a signal indication the negative module voltage Vmod- via signal line 13. Further, the microcontroller 18 received a signal indicating the output current Imod 26 from the module via signal line 11. The output current 26 is measured by suitable means as symbolically indicated by 25. The microcontroller 18 provides, based inter alia on these signals the control

signal 20 to the various functional blocks of the balancing system, i.e. the control signals 21, 22, 23 and 24.

This Switched DC/DC converter that is used in the shown embodiment of the invention is based on a "Module to Cell" topology and allows, without too much extra costs, to monitor the current
5   injected on each cell while balancing, thus enabling to obtain a better SOC considering the current injected during the balancing process.

The DC/DC Converter 7 is an isolated flyback converter that extracts the power from all the module cells (C1 through C10 in the embodiment shown in figure 1) and injects a controlled constant current (CC) to balance the most discharged cell until it is in balance with the other
10   cells. The connection of the isolated flyback converter to the most discharged cell is done with an array of relays 4 and only one can be switched at the same time to avoid dangerous short circuits.

The design of the DC/DC converter that can be used in embodiments of the invention is described in some detail in the following. The converter can as mentioned above for example
15   be implemented into the HERCULES microcontroller, if desired.

The converter control needs an analog signal for measuring the balancing current (and close the feedback loop for control), a PWM digital output, and a digital output per cell (built using an external de-multiplexing system) to activate the switches that connect the DC/DC converter to the cell that requires balancing.

20   The Switched DC/DC converter according to an embodiment of the invention is based on a "Module to Cell" topology and allows, without limited extra costs, to monitor the current injected on each cell while balancing, thus making it possible to obtain a more optimal state of charge (SOC) considering the current injected during the balancing process.

Referring to figure 2 there is shown a flowchart illustrating an embodiment of a cell balancing
25   method according to the invention that can for instance be applied for a battery comprising one or more modules, each comprising a number of cells, as for instance shown in figure 1.

The balancing method is initiated at step 27 and a given battery module is chosen at step 28. In step 29 it is determined by appropriate means if a charging process is in taking place and if this is the case the method proceeds to step 30, thereby applying active cell balancing
30   between cells in the given module, i.e. the module chosen in step 28.

Towards the end of the charging it may happen that one or a few cells of the given module are charged above a predefined upper limit L_u of SOC or cell voltage. If this is detected in step 31, according to the embodiment of the method shown in figure 2, that this or these cells are charged above the predefined upper limit L_u, passive cell balancing is applied to these cells in

5   step 32 in order to reduce their charge to the required value. If it is determined in step 31 the no cells are above the upper limit the process proceeds to step 33 in which it is determined if further modules that have to be charged are present in the battery, after which the above described process is repeated for the next module.

If no further modules are present in the battery, it is in step 34 determined, if there is an

10   imbalance between the SOC of voltage between modules. If this is the case, the process applies either passive or active balancing between modules, for instance (in case of passive balancing) by means of the resistor 8 shown in figure 1. This inter module balancing proceeds until a required balance between modules have been obtained, after which the process terminates in step 38.

15   In functional block 36, the upper limit L_u can be determined and provided as indicated by 39 to the functional step 31.

Referring to figure 3a and b there is shown a schematic circuit diagram of an embodiment of an isolated flyback converter circuitry (MOSFETS, filters, isolation transformer, etc.), where the flyback Control block and the cell C1, C2 and C3 connected to the output of the flyback

20   converter. It is noted that other numbers of cells than the three actually shown in the figure could be used according to the invention. There are other parts in the schematic used to measure currents and voltages all along the circuit. The energy needed to correct the unbalance status of one specific cell is obtained from all the cells of the module and is then injected on that specific cell.

25   The DC/DC converter topology is an isolated flyback converter, acting like a buck converter with isolation. The PWM signal allows controlling the output current and voltage of the DC/DC converter.

An objective of the system and method of the present invention is to re-charge the unbalanced cell with a controlled current, for instance a 1A current, that is extracted from the full array of

30   cells that composes a module.

In order to design the control algorithm that later will be implemented in the HERCULES microcontroller, the simulation schematic includes filtering and discretization of the output current feedback measurement. This resembles the way an analog stage and an Analog to Digital Converter (ADC) work in a real electronic system. Also, the flyback control block works in the way it is expected to work in the HERCULES microcontroller, this means that the control code is executed one time for each sample acquisition of the analog signal.

The sampling frequency has in the results of the simulations shown in the following been set to 2kHz and the resolution of the ADCs is 12 bits . The output current will be sensed using a shunt resistor (in this example 50mOhm) and an instrumentation amplifier (for instance INA282) with a fixed gain of 50x in the results shown in the following. The PWM switching frequency has been set at 100kHz, but other switching frequencies could also be used.

Referring to figure 4 there is shown a flyback_Control block that implements the control algorithm that allows re-charging a specific cell from its initial unbalanced state up to the desired balanced state. The parameters needed to control the start-stop and current injection are:

- Desired output current: fixed at 1A (Iout)
- Output current feedback: IoutDC
- Cell SOC: SOC_1
- Desired final SOC: Final_SOC

There are other control parameters in the flyback_Control block related with the simulation process in PSIM (fs) and PI regulator parameters (Kp, Ki) for controlling the output current. The flyback_Control block is in an embodiment programmed in C code to make it easily portable to the HERCULES microcontroller, but it is understood that other programing languages could alternatively be used.

The most important part of the control algorithm (PI controller) implemented in the "flyback_Control" block is shown in the following:

```
…
if (SOC <= Final_SOC) //run the algorithm until Final_SOC is reached
{
// do nothing until 1ms. Simulates initialsation state of the uController
if (Tdis <= 0.001)
{
        Iout = 0;
        IoutDC_s = 0;
        Tdis = 0;
        Kp = 0;
        Ki = 0;
        err = 0;
        err_k1 = 0;
        Int = 0;
        Out = 0;
        PI_out = 0;
        y1= 0;
        y2 = 0;
        y3 = 0;
        y4 = 0;
}

else // Flyback PI control algorithm
{
        Iout = x1; // output current objective
        IoutDC_s = x2; // discretized output current feedback

// PI Controller
        err = Iout - IoutDC_s; // Error calculation
        Int = Int + (err/fs); // Integral calculation
        Out = Kp*err + Ki*Int; // PI result
        PI_out = Out;

// Saturation to avoid excesive PWM duty cycle or below 0
        if (PI_out >= 0.44)
        {
        PI_out = 0.44;
        sat = 1;
        }
          else if (PI_out <= 0)
        {
        PI_out = 0;
        sat = 2;
        }
        else sat=0;

        y1 = PI_out;
        y2 = err;
        y3 = sat;
        y4 = 1;

}// end if
}// end if SOC
else
{
        y1 = 0;
        y4 = 0;
}
```

The Hercules μC generates the PWM signal, switch (relay) selection signals, possible passive balancing activation signal/signals? for the full module and receives the feedback of the balancing output current signal to close the control loop.

The PWM signal will control? the isolated flyback DC/DC converter in order to generate the desired amount (magnitude) of current to re-charge the selected cell.

With reference to figure 5a through g there is shown the interface with the Hercules μC evaluation board, and also the power supply needed to generate the different supply levels, including the isolated voltage (such as 5V) needed for the output current and cell voltage measuring operational amplifiers. The schematic in figure 2 also shows the interface components needed to manage the different voltage levels in all the signals present in this embodiment of the invention. The analog and digital signals can be routed to different pins in the μC to allow compatibility with different combinations and configurations.

In this embodiment of the invention, the connection with the TI BQ76PL536EVM is done with an SPI bus and some digital signals, and it is present in connector J1 and J2.

With reference to figure 6a through e there is shown the Dual Switch isolated flyback converter. To manage both MOSFETs PWM signal, the IC U114 (UCC27201) acts as a High and Low Gate Driver, receiving the PWM signal from the μC.

The current sensor used to send the current signal to the microcontroller is in this embodiment a combination of a 25mOhm shunt resistor and two analog amplifiers. The first one in the chain is the AMC1200-Q1. It is a balanced isolation amplifier with a fixed gain of 8x and it is powered with 5V by the TMV-1205SHI isolated DC/DC converter. The balanced output of this isolation amplifier is amplified again by the INA332 (11x for the current measurement and 5x for the voltage measurement). Both signals are given to the HERCULES μC ADC inputs on Ieq_Out and Veq_Out ports. The Module voltage is also measured by the resistor divider network and is given to the uC on Vmod port.

In this – and possibly also further embodiments of the invention, a Wurth WE750312503 isolation transformer for the flyback converter that works between 36V and 72V input voltage is used. The selected topology is the dual switch flyback and the MOSFETs reference is STN2NF10. The output diode D19 (PMEG3030EP) has been selected for its low Vf to reduce conduction looses.

With reference to figure 7a through g there is shown an embodiment of a Relay selection circuitry provided with de-multiplexer to avoid having 2 relays connected at the same time to different parts of the cell that would lead to a short circuit between two or more cells. The selection of the relay that connects one single cell to the flyback output is done with a logic circuitry based on SN74HC238D de-multiplexers. In this way it is ensured that only one single relay is activated at the same time, avoiding dangerous short-circuits between cells. Finally the relay is driven by a ULQ2003A darlington array that manages the relay coil activation.

There last two relays (RLY17 and RLY18) are in this embodiment used to connect a resistor in series with a single cell or with the full module to allow passive balancing and thus obtaining the Hybridized Balancing prototype. The relay selected for this application is the IMR6

Software design

The HERCULES µC has been configured and programmed in order to control the flyback converter, using the following peripherals:

- General Purpose In/Out (GPIO) pins to manage the logic circuitry that controls the Relays.

- Analog to Digital Converter (ADC) Module to measure the output current.

- High-End Timer (HET) Module to generate internal interruptions for the control algorithm.

- Enhanced Pulse Width Modulator (ePWM) Module to generate the PWM signal.

The uC peripherals are configured as follows:

```
GIO:      - PORT A (A5, C2, C1, E1, A6, B5, H3, M1)
ADC:      - JUMPER J8 TO SELECT ADREFHI 3.3V
          - PIN -> ADC1IN2 (V18)
          - TRIGGER -> HET1 8
          - RESOLUTION -> 12BIT
          - SAMPLE TIME -> 1µs
HET:      - PIN -> HET1 8 (E18)
          - PWM1
          - PERIOD -> 500µs
ETPWM:    - PERIOD -> 100kHz        - PIN -> ETPWM6B (P2)
```

With the ePWM module the HERCULES µC generates a PWM signal capable to control the flyback converter. With the HET Module a signal is generated to trigger the conversion of the

ADC at an appropriate frequency, such as 2kHz, which captures the measured value of the current sensor. The μC receives the analog signal from the current sensor in order to close the control loop, performing as a PI controller. Using the GPIO of the Port A, the μC selects the cell to be recharged. If desired, the μC also enables the passive balancing for one cell or for the full module.

Tests have been carried out with the Dual Switch flyback converter charging one Cell at a fixed and controlled current of 1A. The core of the active balancing circuitry is the isolated flyback converter. The flyback converter is controlled by the HERCULES μC with a PWM signal (ETPWM 6B pin) and the control loop is feed by the analog signal that corresponds with the output current (AD1IN2 pin).

The HERCULES uC is able to select the cell that needs to be recharged thanks to the logic circuitry attached to GIOA port. Lines GIOA0 to GIOA3 are used to select the cell from 1 to 16 and GIOA5 is used to enable the output from the 3.3V-to-5V buffer and GIOA4 is used to enable the output of the de-multiplexers. Both enable signals are active low signals.

Once the cell is selected, the μC starts to control the PWM signal of the flyback converter in order to recharge the selected cell at 1A rate. .The cell model used in these tests is the Kokam SLPB90255255H.

The measurements done during the balancing tests show that the circuitry and control code designed are able to control the amount of current injected into the selected cell.

The precision of the output current value is ±1.5%.

The efficiency of the power conversion in the flyback converter is above 82.5% in most input/output conditions, arriving to efficiency peaks of around 87.5% when the input voltage is around 55V.

Passive balancing has also been tested by connecting one 4Ω resistor (5W) to discharge a single cell at a rate of around 1A, and one 68Ω resistor (100W) to discharge the full 16 cell module at a rate of around 1A. It is understood that different resistor values could be used and that passive balancing could be carried out by other means than by resistors.

Simulation results.

In the following results of PSIM simulations for 16 and 8 cells modules are shown.

Referring to figure 8 there is shown results obtained for a simulation of a balancing process of 1 cell that needs to go from a 90% SOC until a 95%SOC. The input voltage for the flyback is 64.45V, equivalent to 16 cells where 15 cells are charged at SOC 95% and 1 cell is charged at 90%. This last cell is the one that will be balanced.

5   The current "IoutDC" is increased until it reaches 1A and then remains steady until the SOC reaches a charge of 95%, then it stops.

The SOC (SOC_1) and the Cell Voltage (VoutDC) as a function of time are also shown.

Finally the bottom graph of figure 8 shows the power conversion efficiency in the simulation considering conduction losses, during the time when the flyback converter is ON. The value of
10   the efficiency in this simulation is 89%.

Referring to figure 9 there is shown results obtained for a simulation of a balancing process of 1 cell that needs to be charged from a 90% SOC until a 95% SOC. The input voltage for the flyback is 32.18V, equivalent to 8 cells where 7 cells are charged at 95% SOC and 1 cell is charged at 90%. This last cell is the one that will be balanced. The rest of the signals are the
15   same as for the results shown in figure 8..

In summary, it can be seen from the plots shown in figures 8 and 9 that the controlled flyback power supply according to an embodiment of the invention is able to recharge the specific cell at a constant current of 1A until its SOC reaches the desired value.

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CLAIMS

1. A system for battery cell balancing comprising:

- a cell monitoring block (16) configured to monitor the voltage or a related quantity across individual cells (C_1, C_2,....C_N) in a battery cell module;
- a microcontroller (18) configured for monitoring the positive terminal voltage (12) and the negative terminal voltage (13) of said battery cell module, and for monitoring (11) the output current I_{mod} of said module, and monitored cell voltage of said individual cells (C_1, C_2,....C_N), where the microcontroller (18) is configured to provide a control signal (20) based at least said positive terminal voltage (12), said negative terminal voltage (13), said output current I_{mod} of said module, and said monitored cell voltage of said individual cells;
- a hybrid module balancing block configured to provide either an active or a passive cell balancing or a combination of active and passive cell balancing of the cells (C_1, C_2,....C_N) in the specific module under the control of the control signal provided by the microcontroller.

2. A system according to claim 1, wherein said hybrid module balancing block (3) comprises:

- a switching array (4) configured to provide active or passive or a combination of active and passive balancing to one or more of said individual cells (C_1, C_2,....C_N) in said specific module under the control of said control signal (20);
- a passive cell balancing means (5, 6) configured to provide said passive balancing under the control of said control signal (20);
- an active cell balancing means (7) configured to provide said active balancing under the control of said control signal (20).

3. A system according to claim 1 or 2 comprising a passive module balancing means (8, 9) coupled between the positive and negative terminals (12, 13) of said specific module.

4. A system according to claim 2, wherein said active cell balancing means (7) is a flyback DC/DC converter.

5. A system according to claim 2, wherein said passive cell balancing means (5, 6) is a resistor (5) in series with a switch (6), such as for instance a MOSFET.

6. A system according to claim 3, wherein said passive module balancing means (8, 9) is a resistor (8) in series with a switch (9), such as for instance a MOSFET.

7. A system according to claim 4, wherein the flyback DC/DC converter extracts power from all of the cells (C_1, C_2,....C_N) of a module, and injects a controlled current to balance the most discharged cell until it is in balance with the other cells.

8. A system according to claim 7, wherein said controlled current is constant.

9. A system according to any of the preceding claims, wherein said microcontroller is a microcontroller in a battery management system (BMS) that manages the overall performance of the battery.

10. A system according to any of the preceding claims, wherein active balancing as applied in the modules making up a battery, whereas passive balancing is applied between two or more modules making up the battery.

11. A system according to claim 10, wherein the system comprises module state of charge (SOC) monitoring means or voltage monitoring means that monitors the SOC or voltage of the modules in a battery and when an imbalance between the SOC or voltage is detected between two or more modules, passive balancing between the two or more modules in the battery is performed.

12. A system according to claim 10 or 11, wherein the passive balancing between two or more modules in a battery is controlled by said hybrid module balancing block (3) or said battery management system (BMS).   13. A method for battery cell balancing in a battery comprising at least one module comprising a plurality of cells, the method comprising the steps of:- determining if a charging process is in progress;

- choosing a module (M1);

- applying active cell balancing between cells of said module (M1);

- determining if one or more cells are charged above a predefined upper limit;

- if one or more cells are charged above said upper limit, applying passive cell balancing to this or those cells in order to reduce their charge to a value at or below said upper limit;

- when all cells within said module (M1) are charged, determine if there are further modules (M2, M3....) in the battery, and if this is the case repeat the above steps for the remaining modules (M2, M3....);

- when all modules of the battery have been charged, determine if there is an imbalance between the state of charge or a similar parameter of the respective modules in the battery, and if this is the case, apply either passive or active balancing between respective modules in order to reduce said imbalance between modules to a required level.

14. A method according to any of the preceding claims, wherein active balancing as applied in modules making up a battery, whereas passive balancing is applied between modules making up the battery.

15. A method according to claim 14, wherein the state of charge (SOC) or voltage is monitored by monitoring means that monitors the SOC or voltage of two or more modules in a battery and when an imbalance between the SOC or voltage is detected between two or more modules, passive balancing between the two or more modules in the battery is performed.

Fig. 1

End — 38

No — Imbalance between modules? — 34

Yes — Apply passive or active balancing between modules of the battery — 37

Apply passive cell balancing of cells $C_{v1}, C_{v2} \ldots$ within the given module — 32

Yes — Are one or more cells $C_{v1}, C_{v2} \ldots$ charged above predefined upper limit L_v? — 31

No

No further modules

If further modules in battery, go to next module — 33

Apply active cell balancing between cells within the given module — 30

Yes — Is charging process in progress? — 29

No — End — 35

Chose module 1 — 28

Start — 27

Define upper limit L_v for SOC or cell voltage — 36 — 39
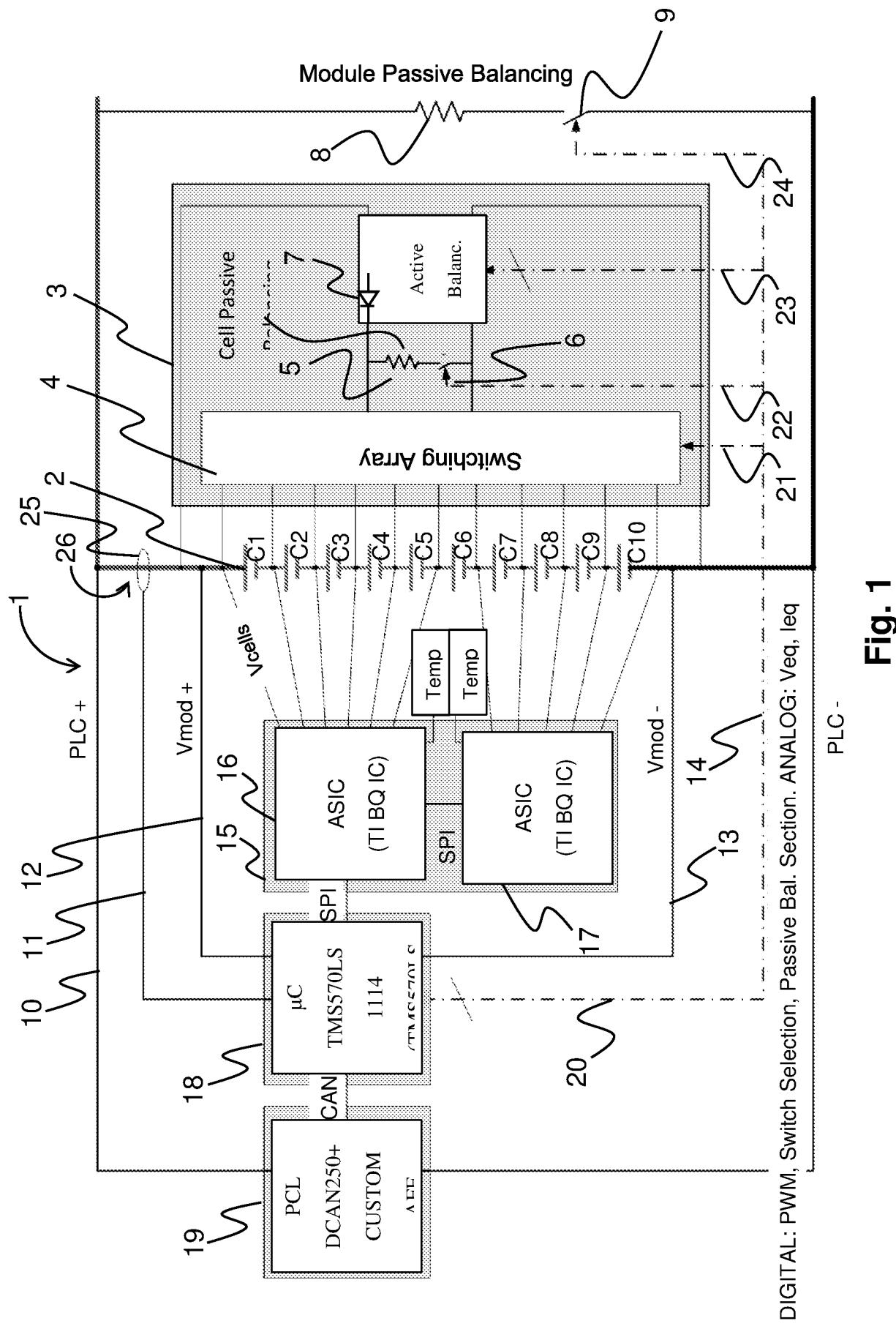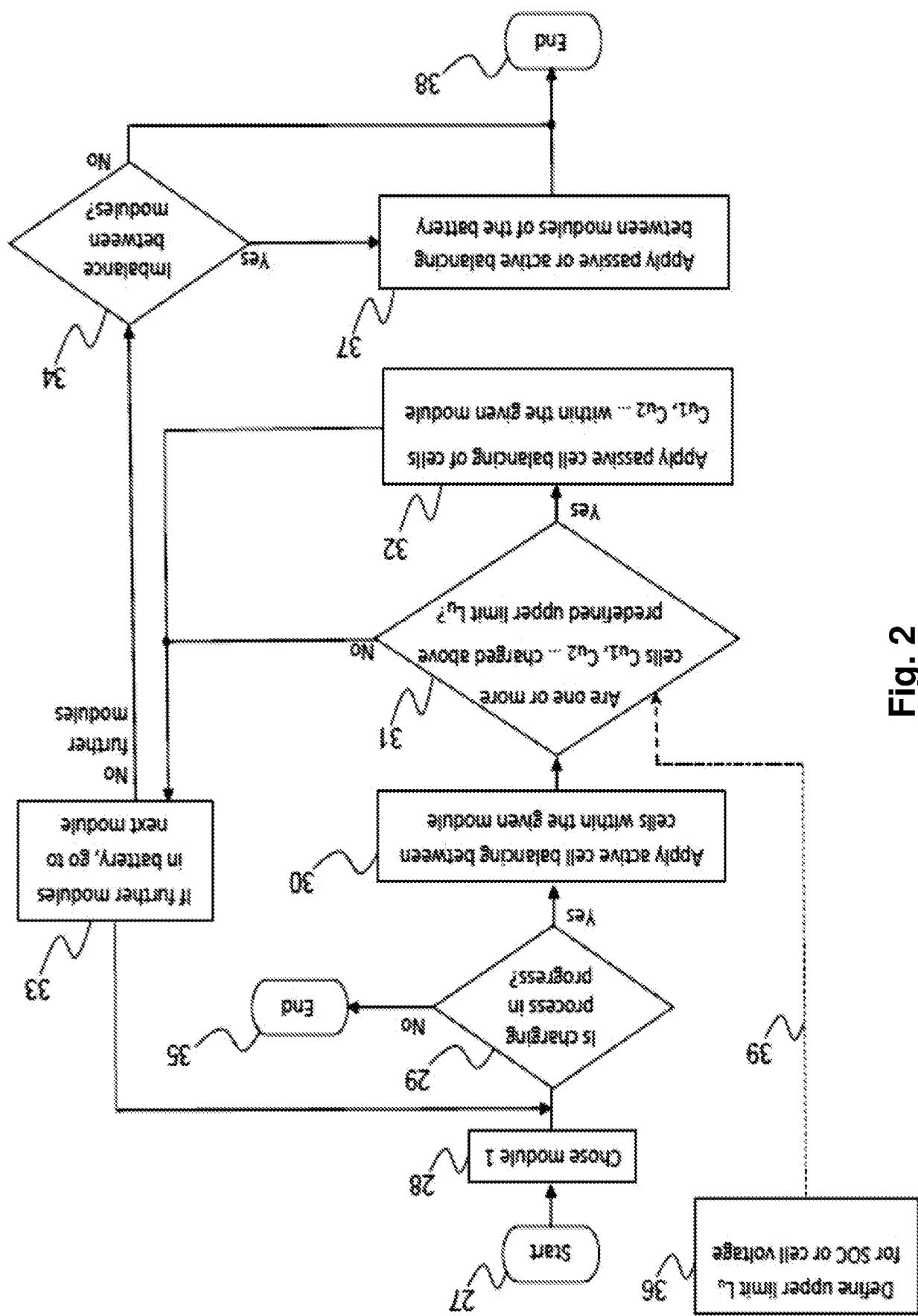
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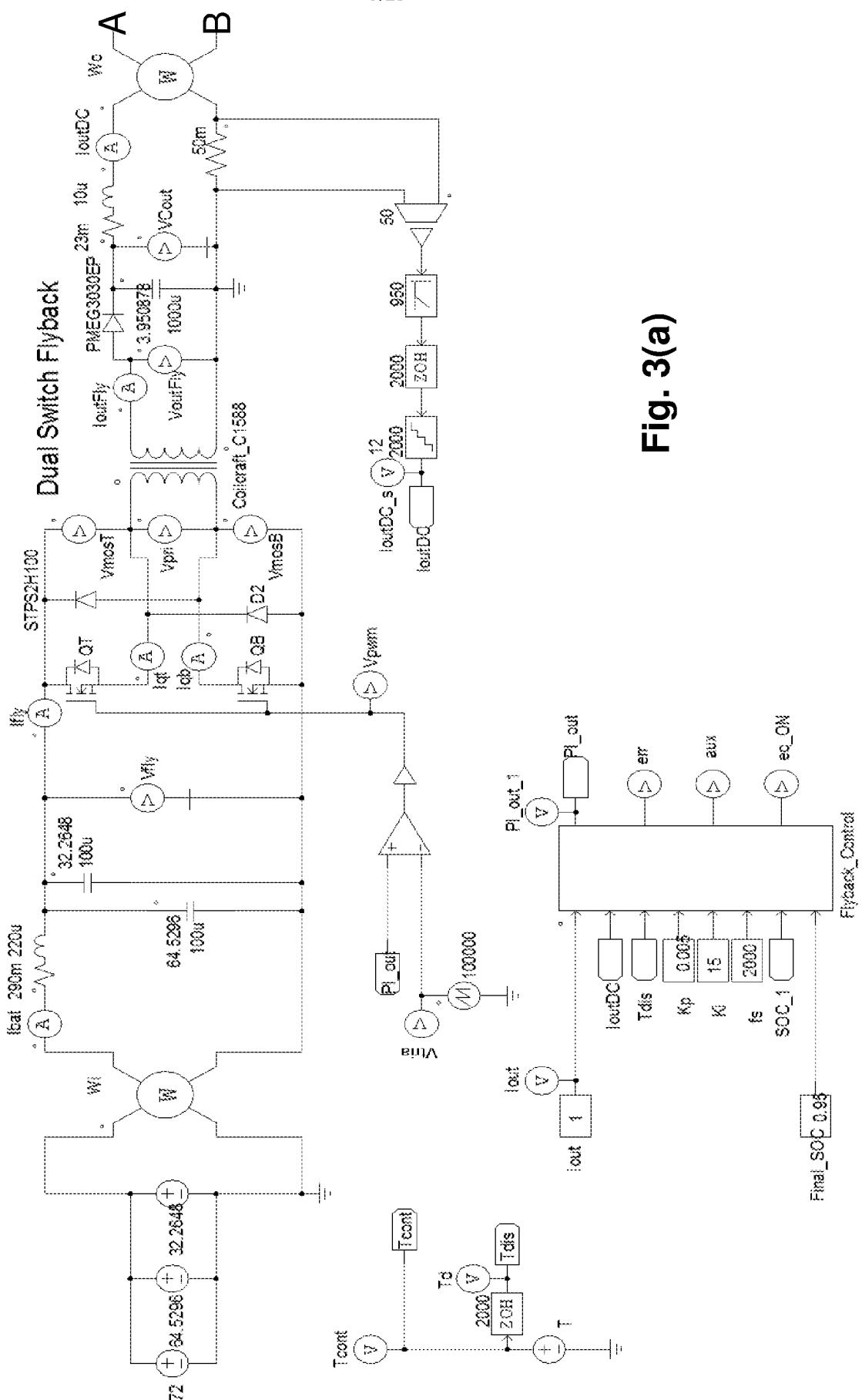
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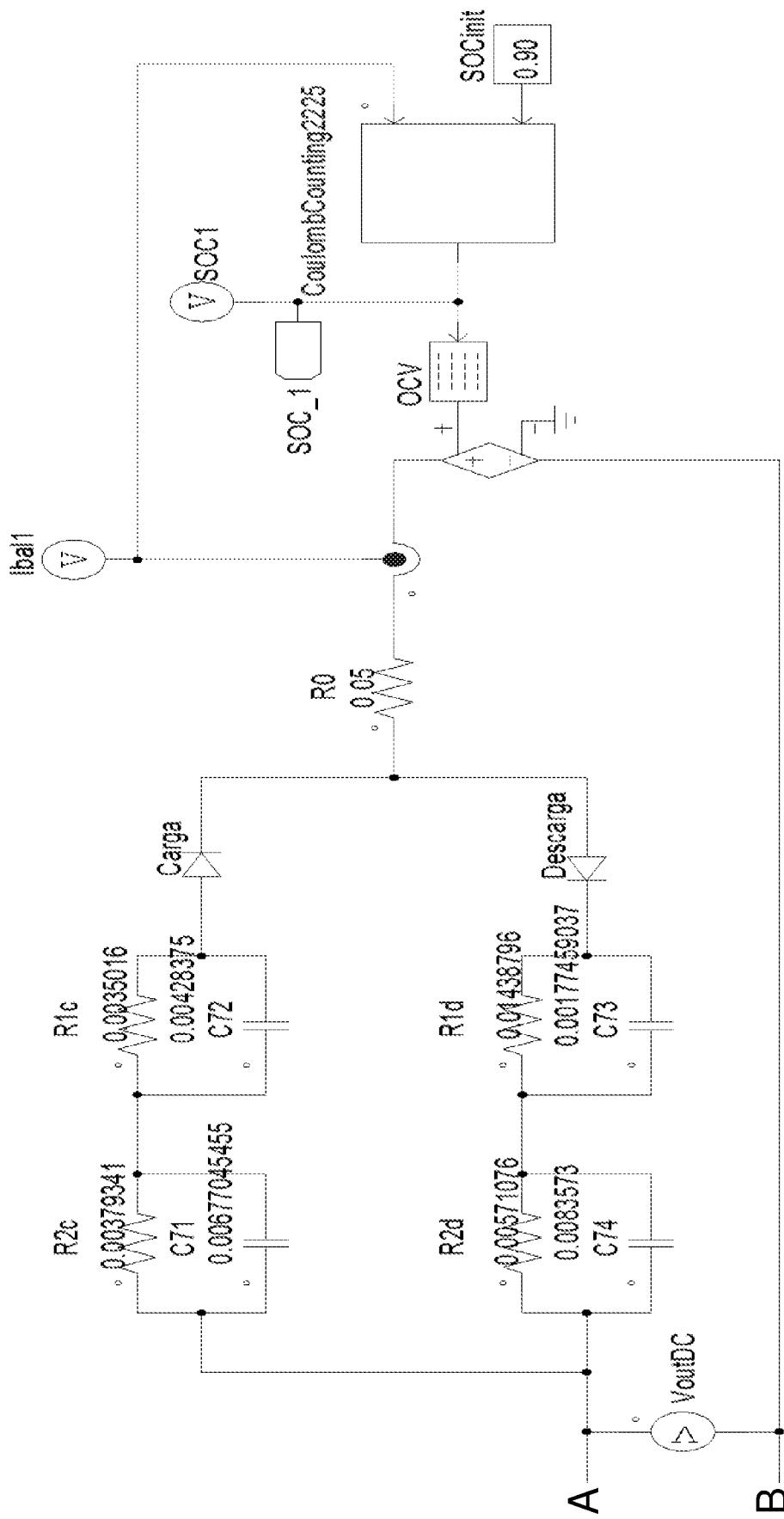
Fig. 3(b)
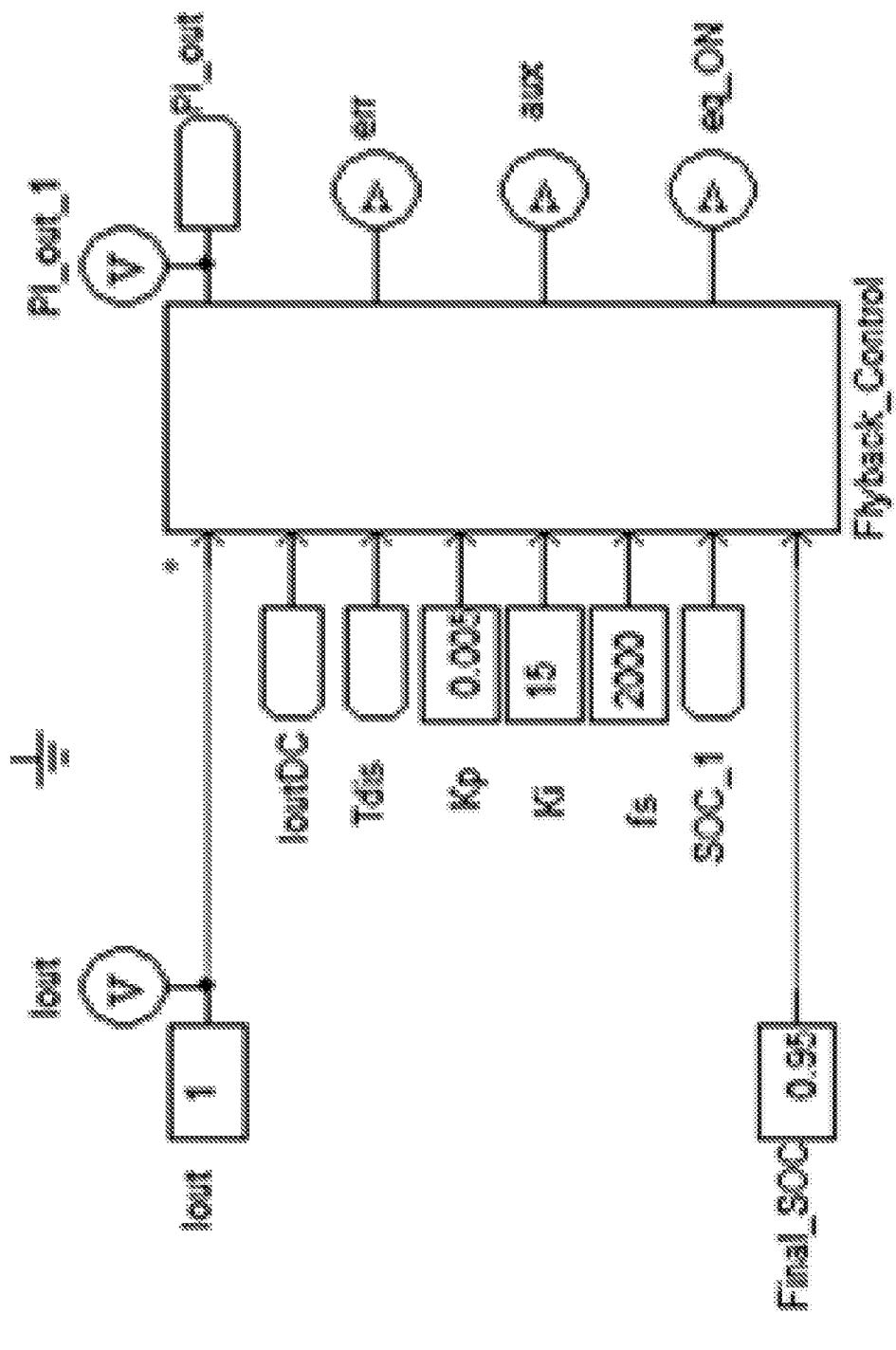
Fig. 4

Fig. 5(a)

Fig. 5(b)

Fig. 5(c)

Fig. 5(d)

Fig. 5(e)

Fig. 5(f)

PWM/GPO 3.3V => 5V
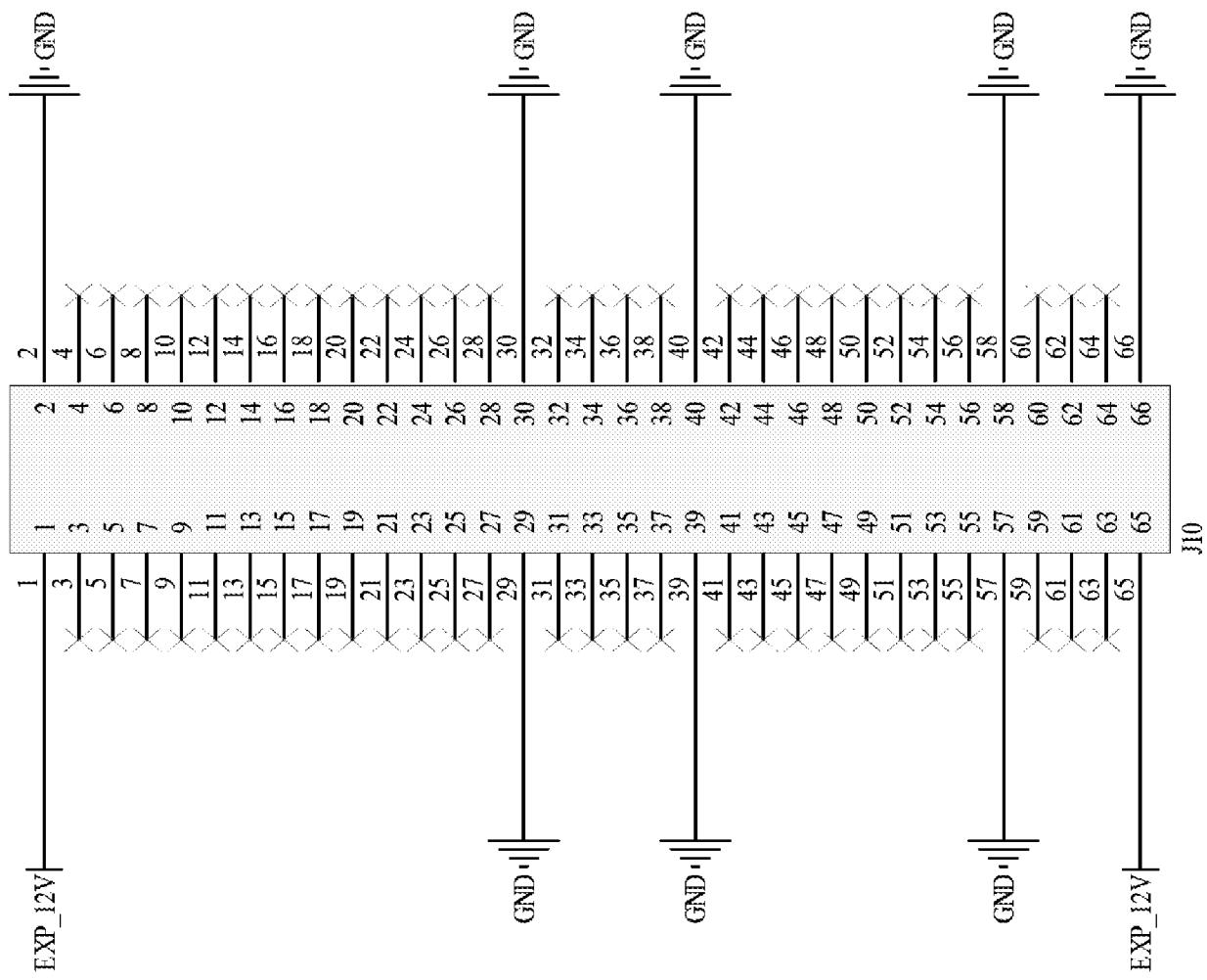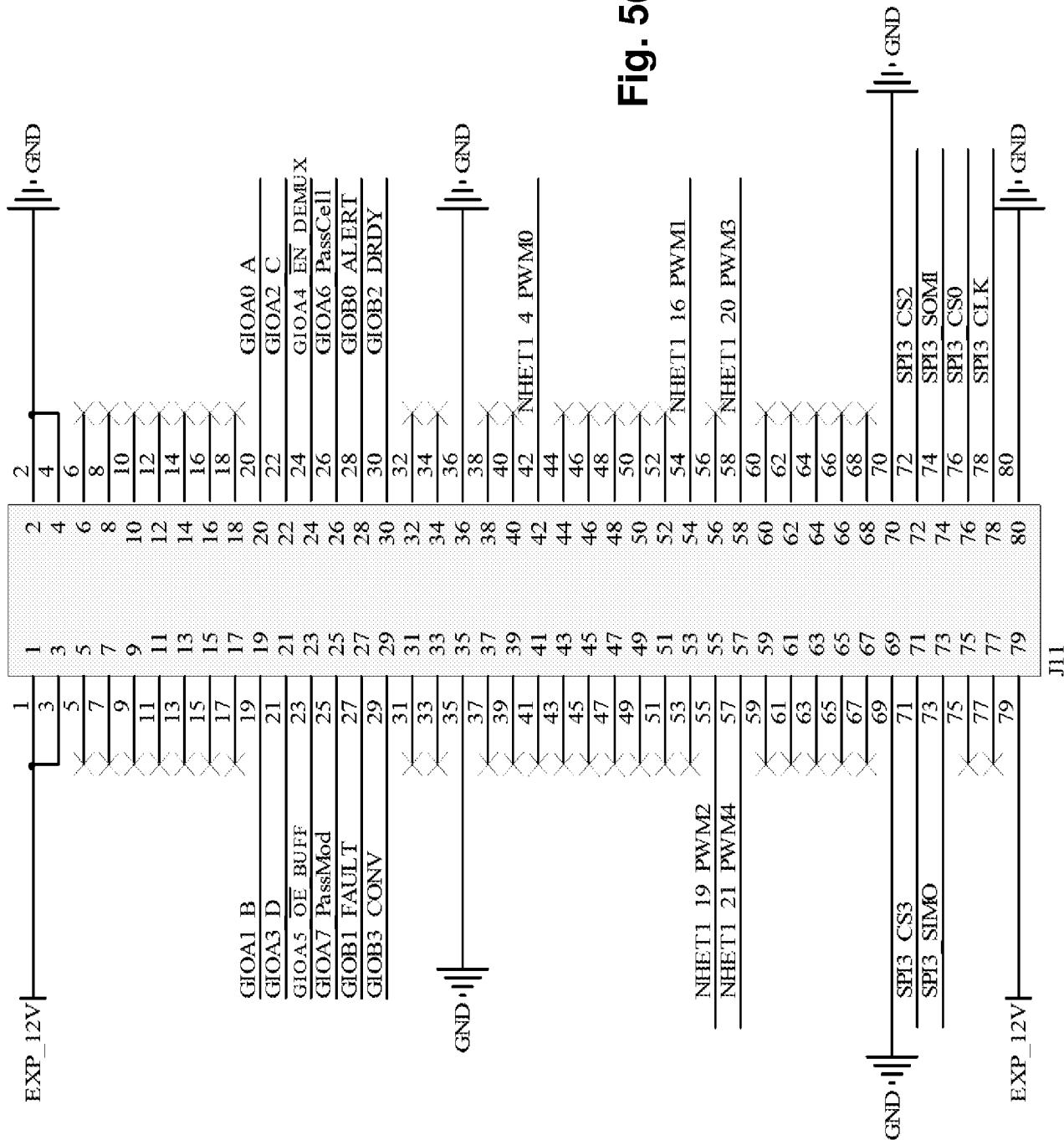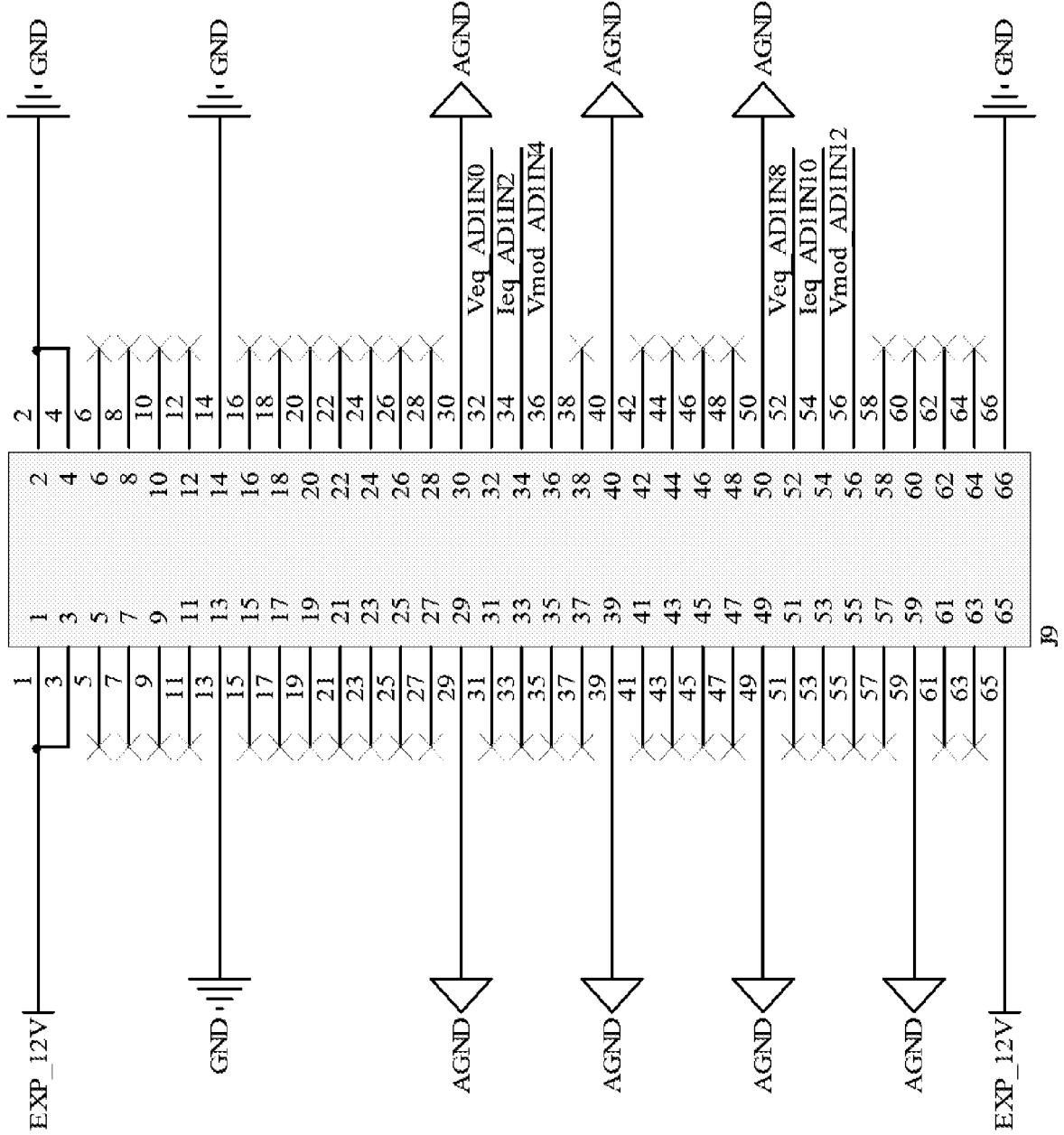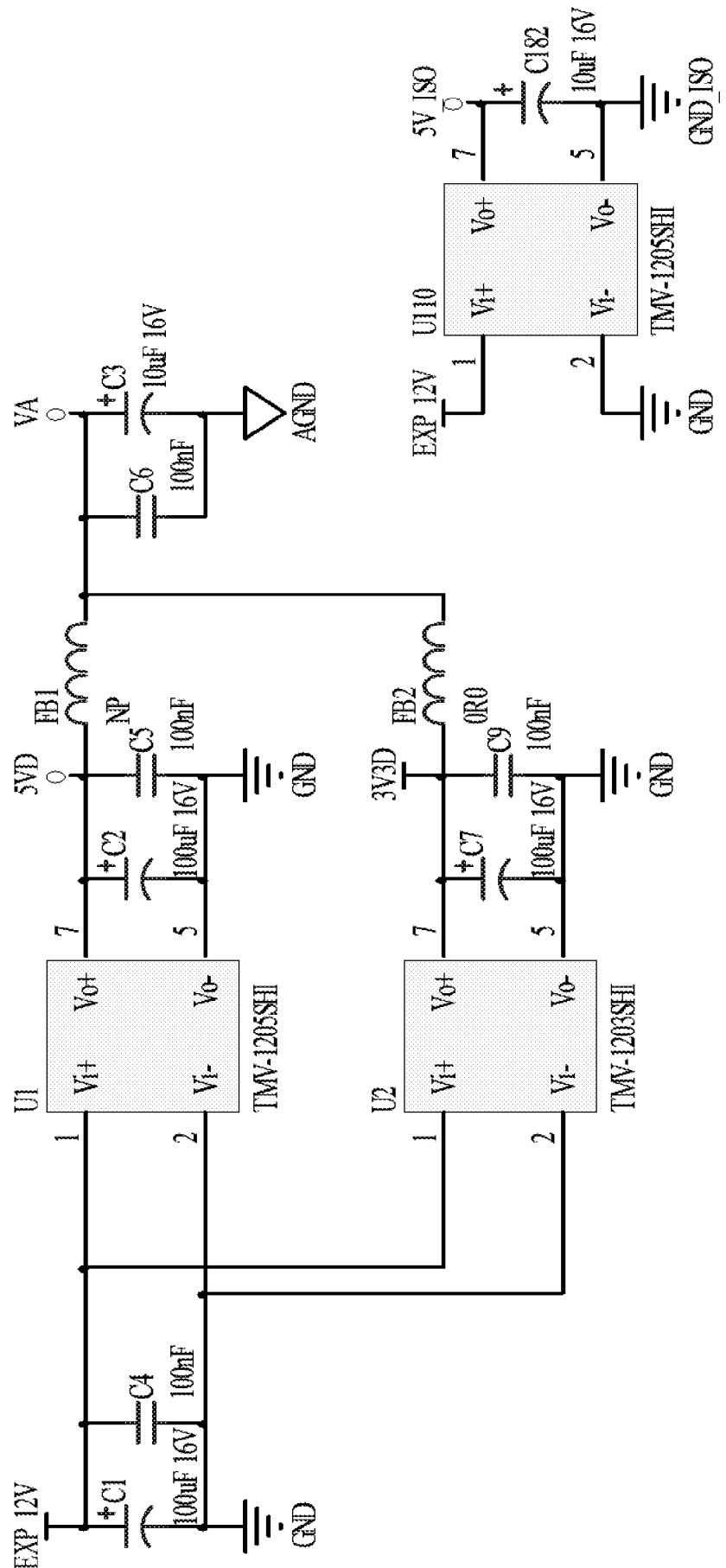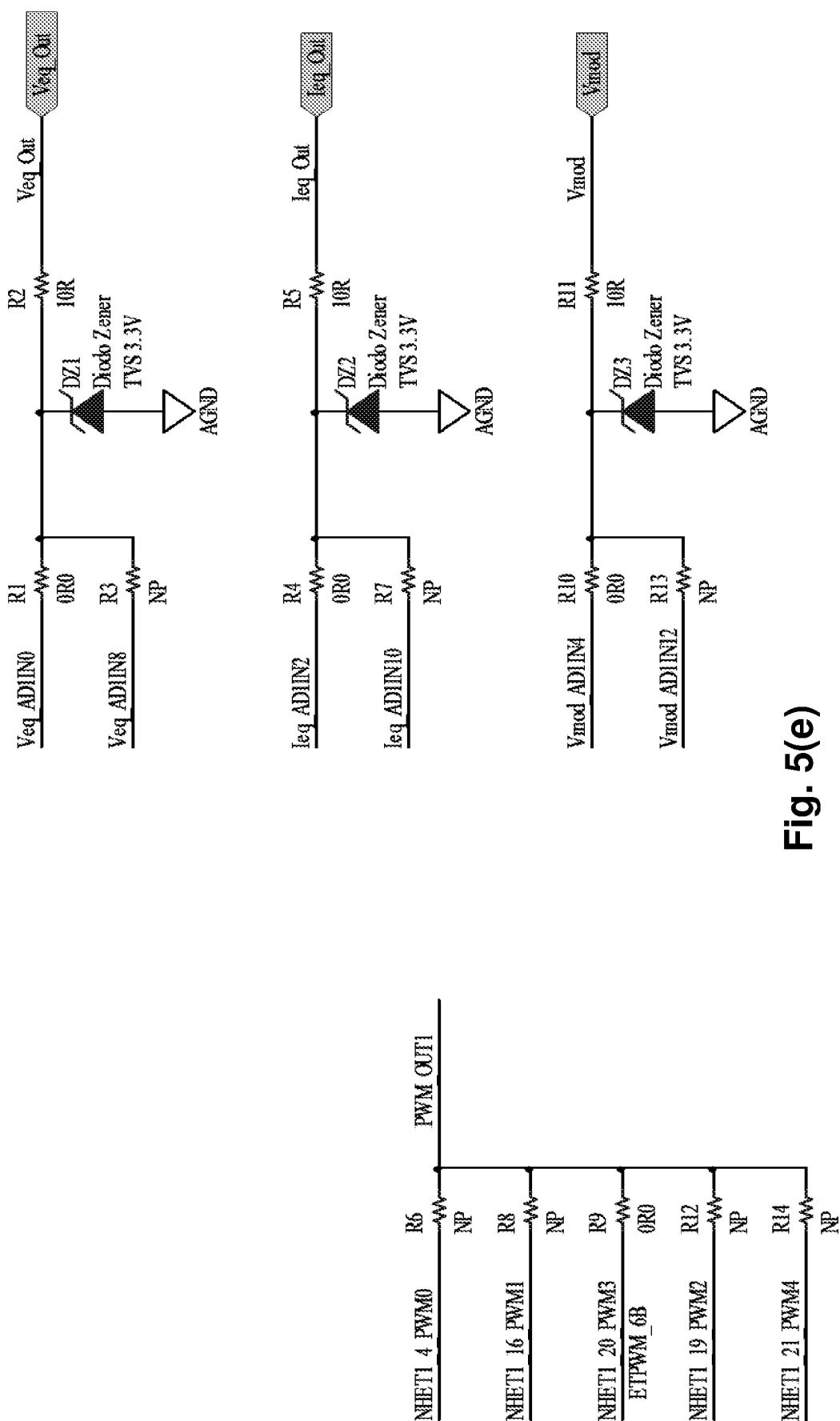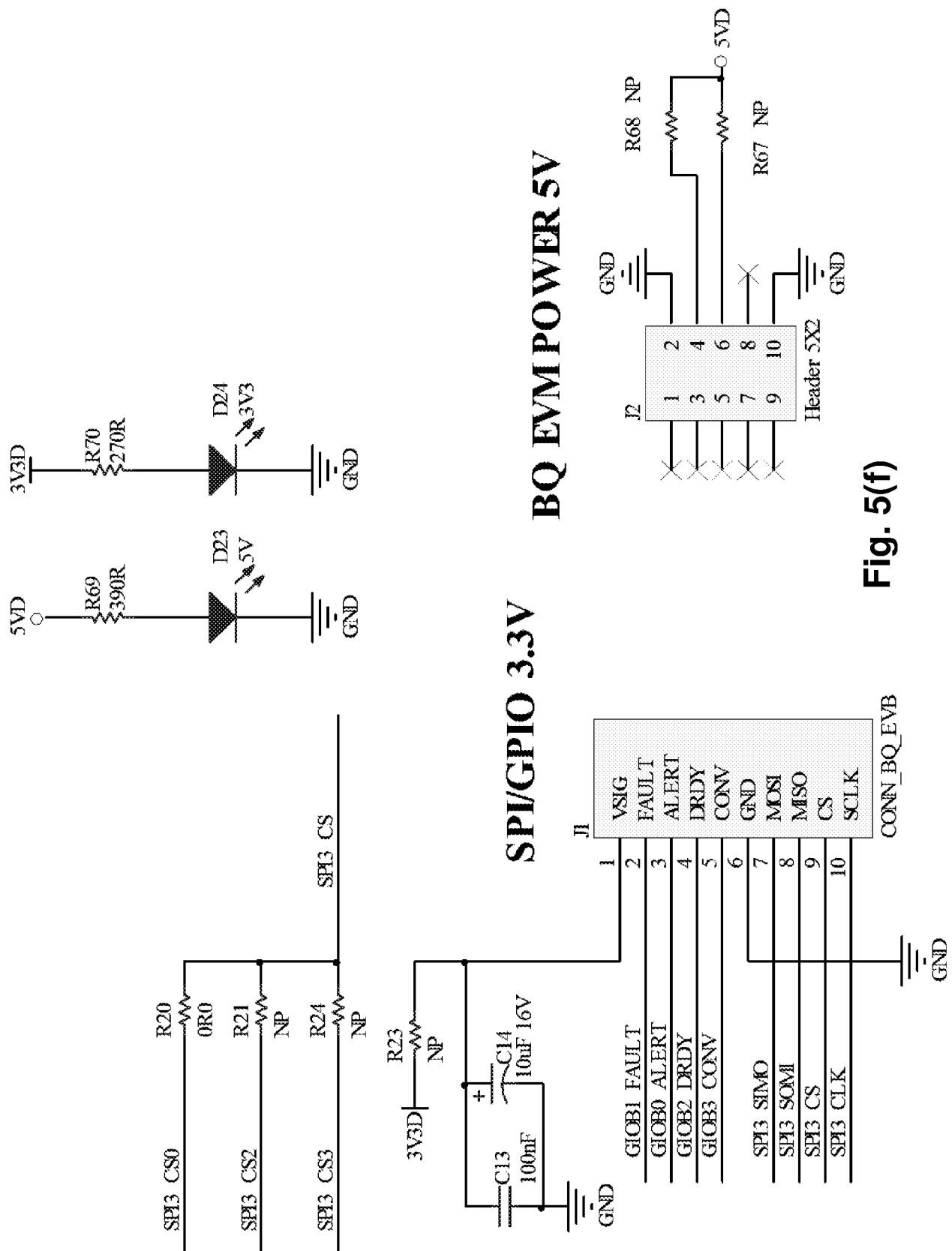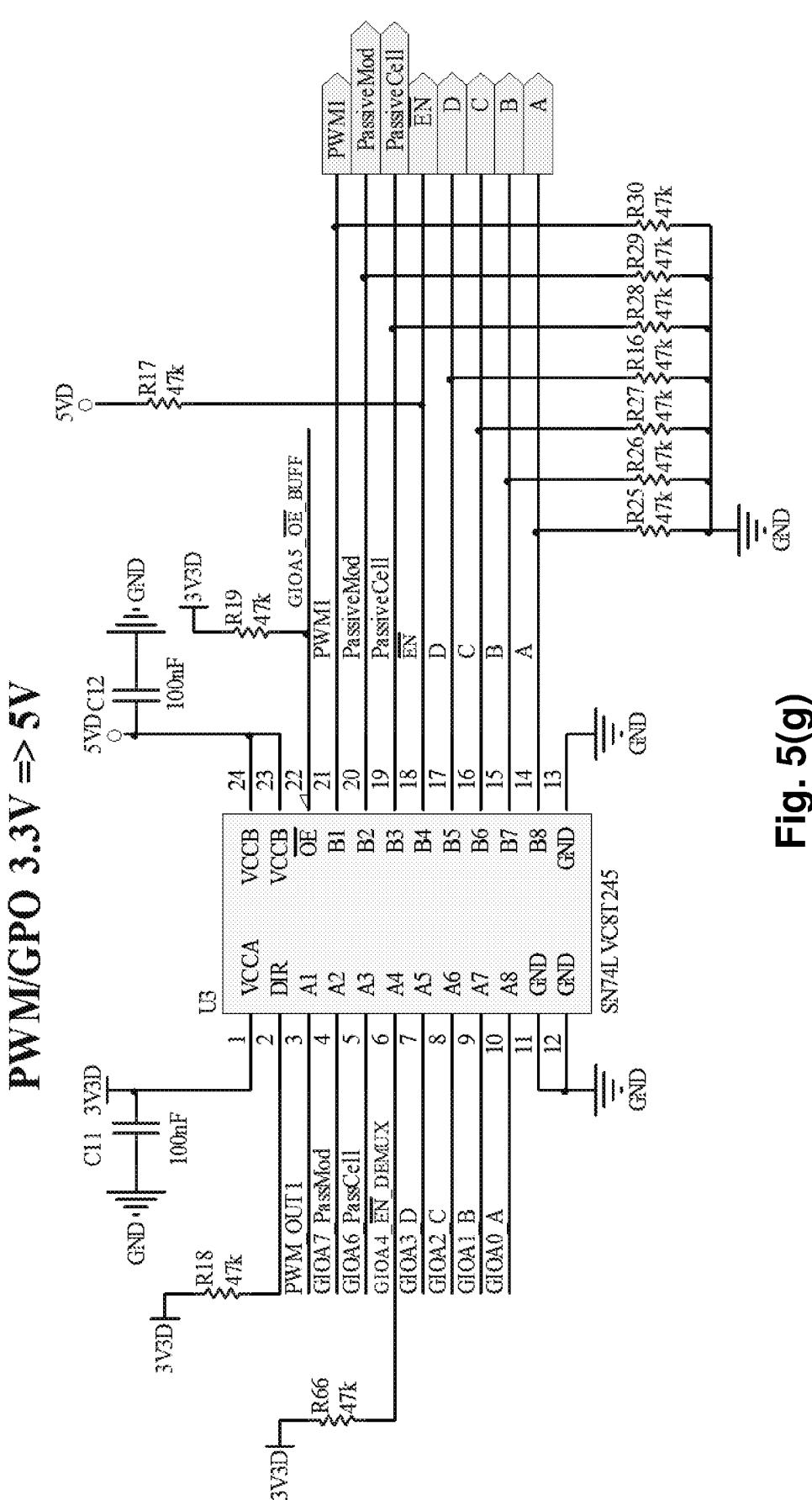
Fig. 5(g)
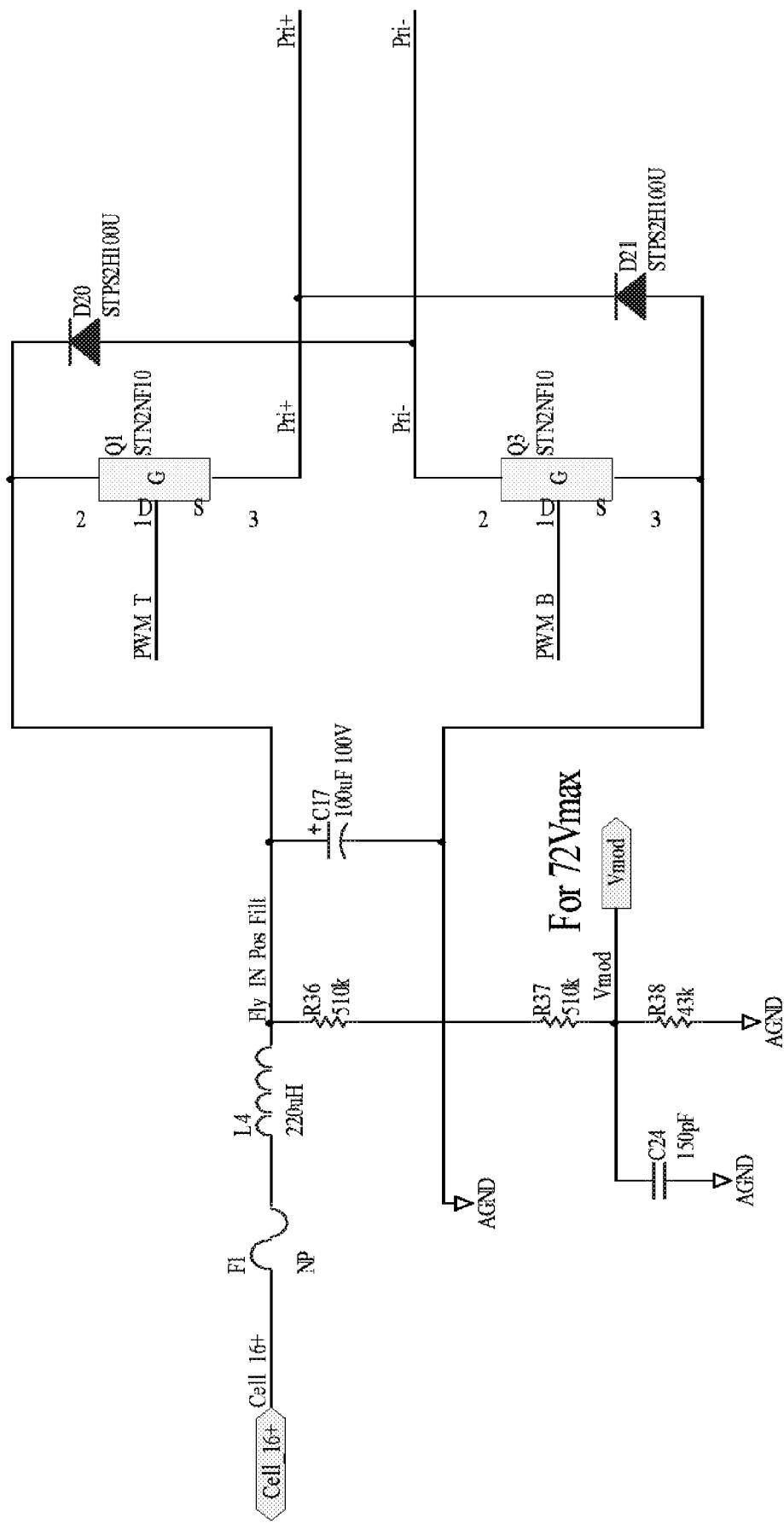
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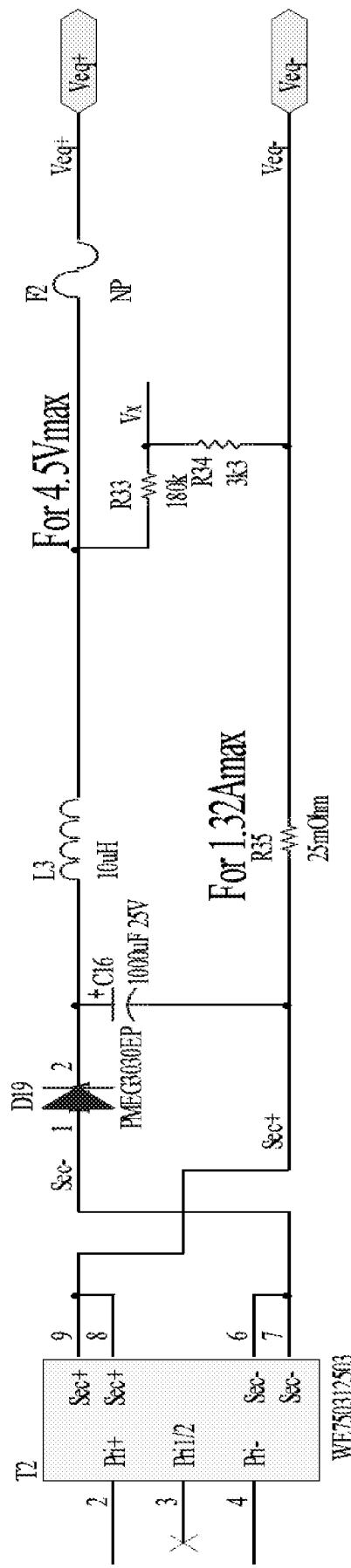
Fig. 6(b)

Fig. 6(c)

Fig. 6(d)

Fig. 6(e)

RELAY DRIVERS

4-to-16 DEMUX
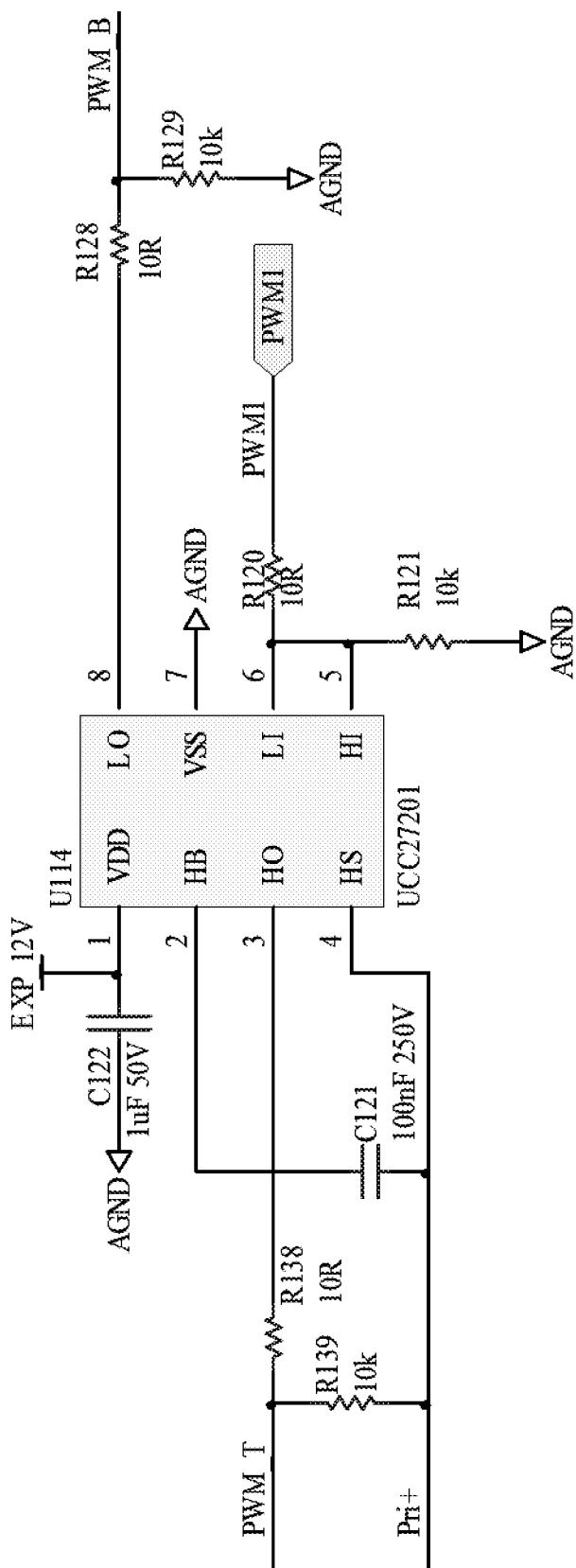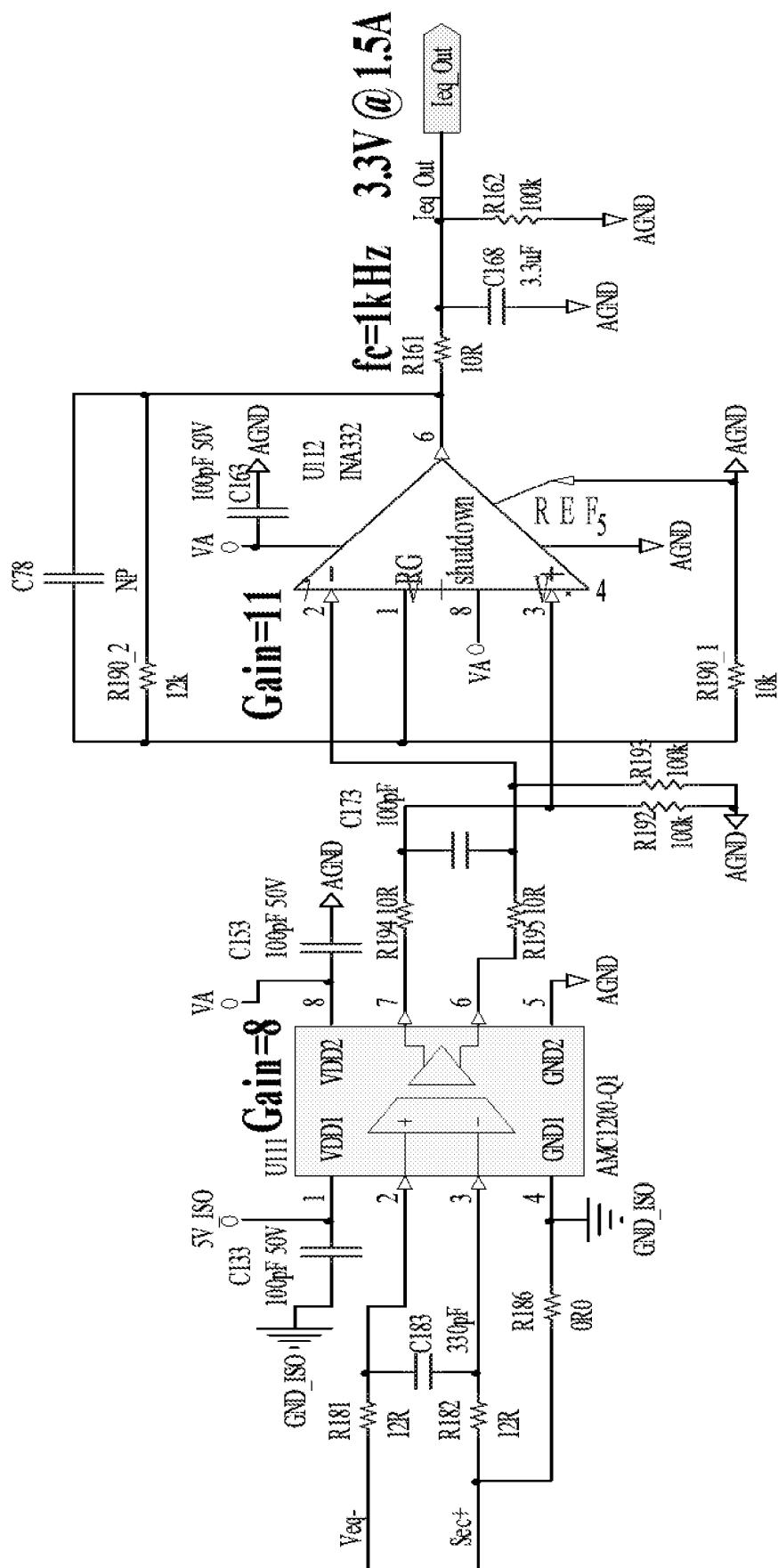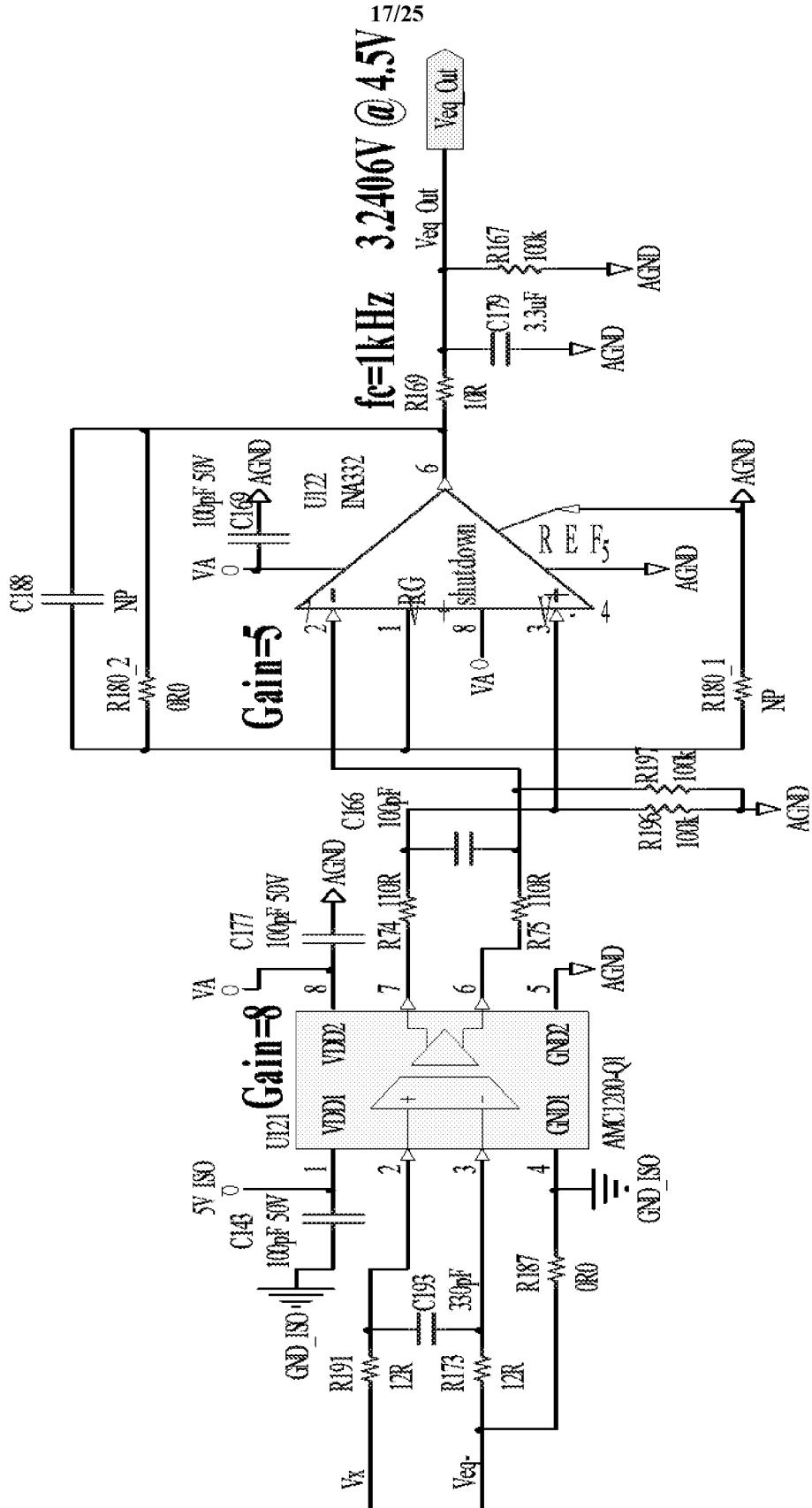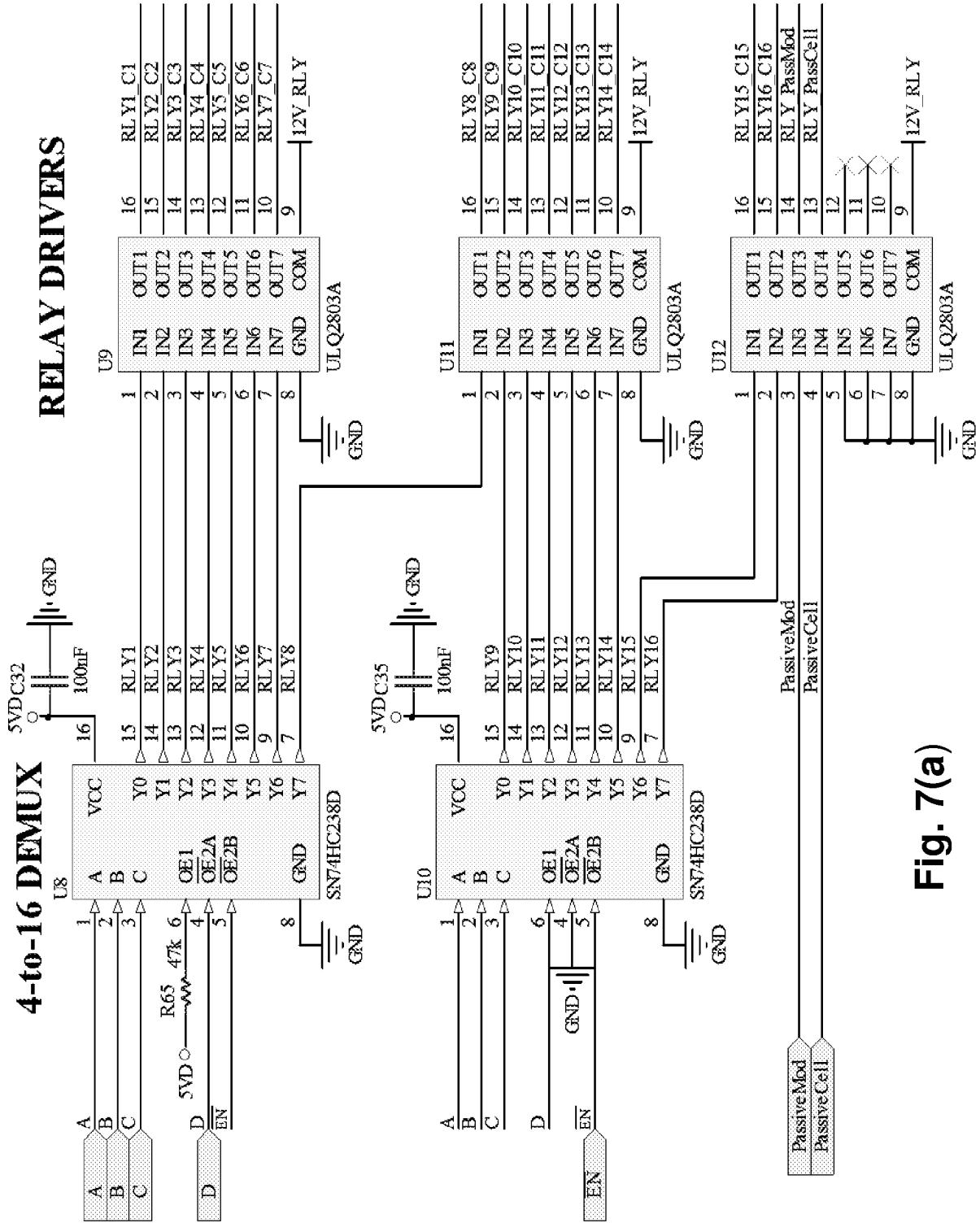
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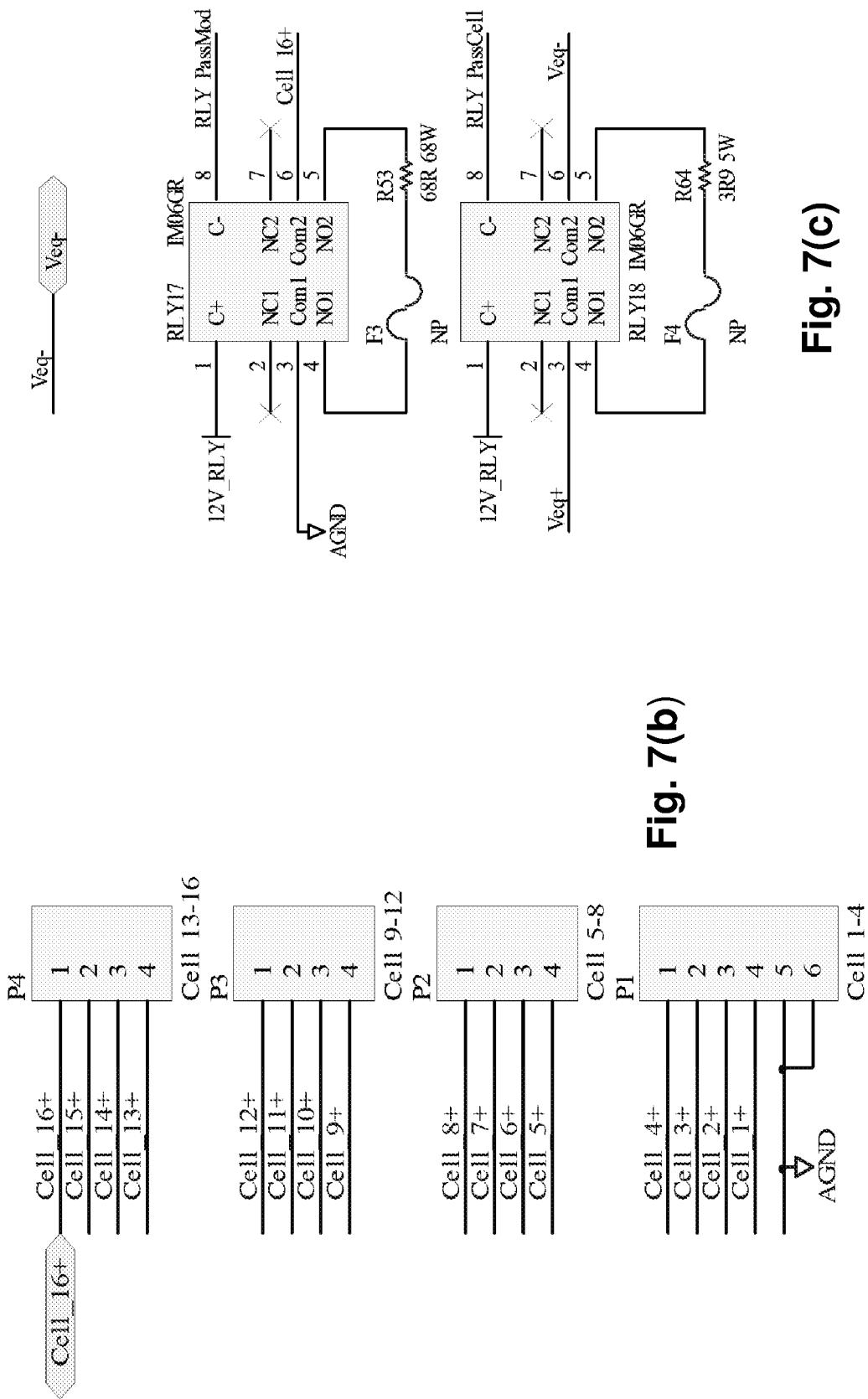
Fig. 7(c)

**Fig. 7(b)**
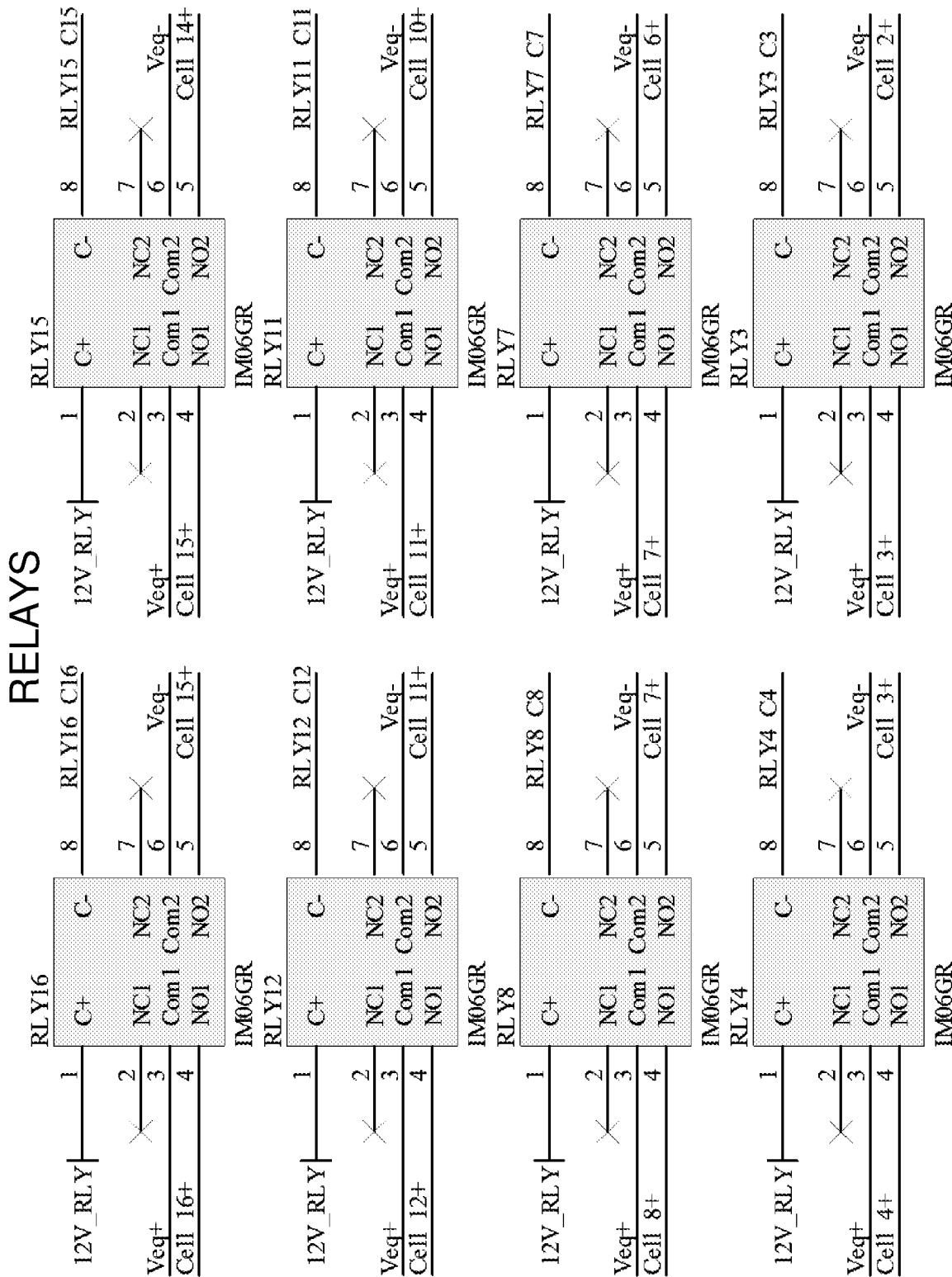
Fig. 7(d)
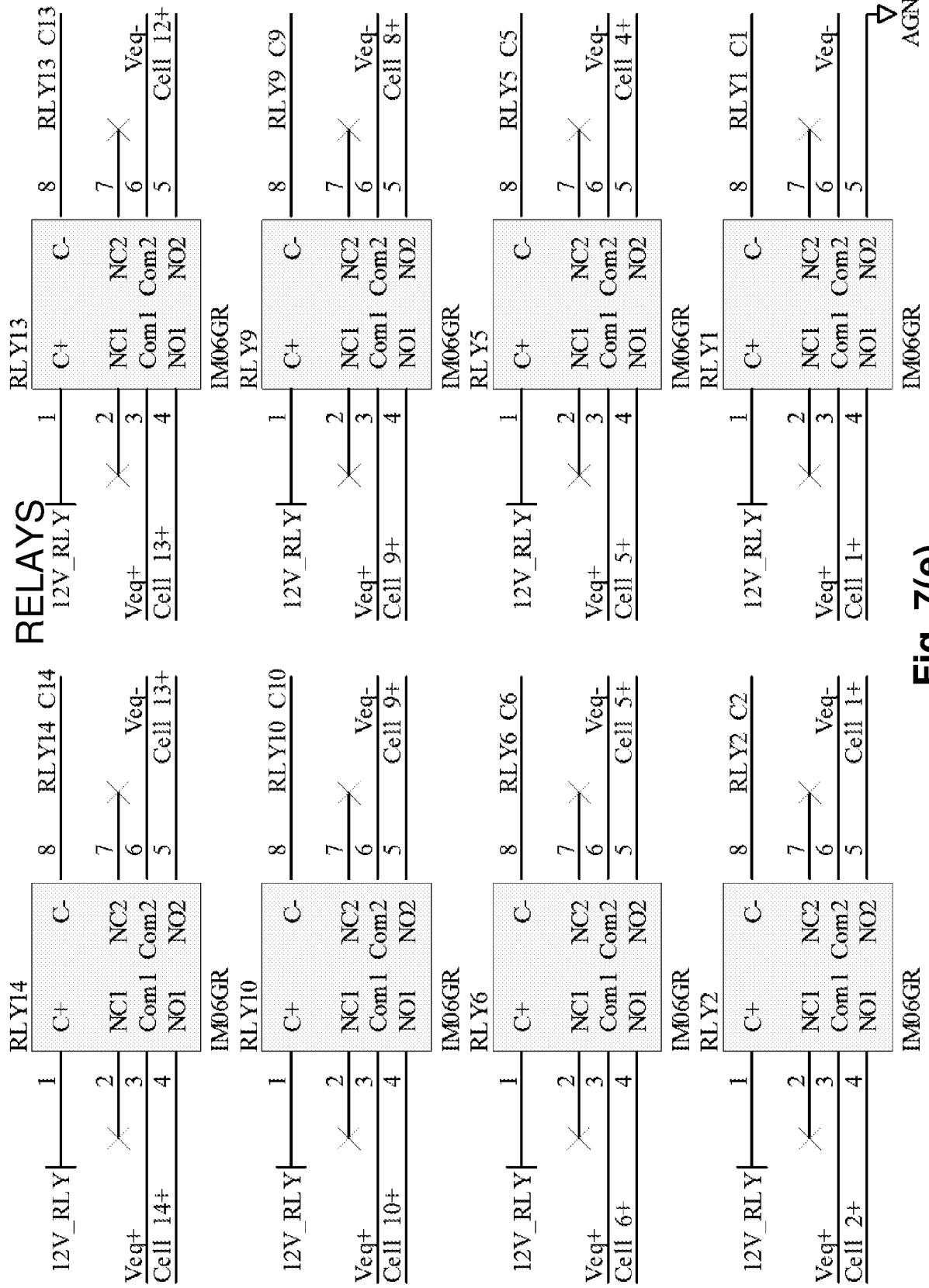
Fig. 7(e)
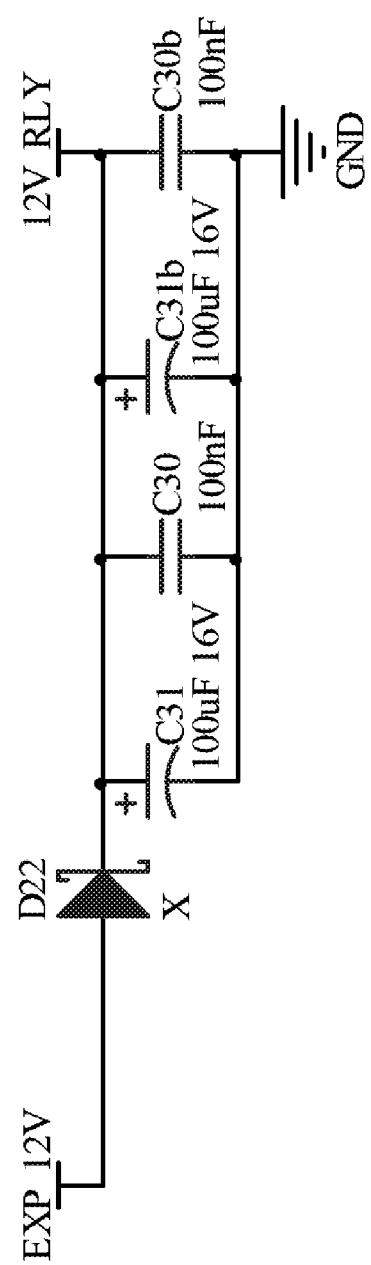
Fig. 7(f)
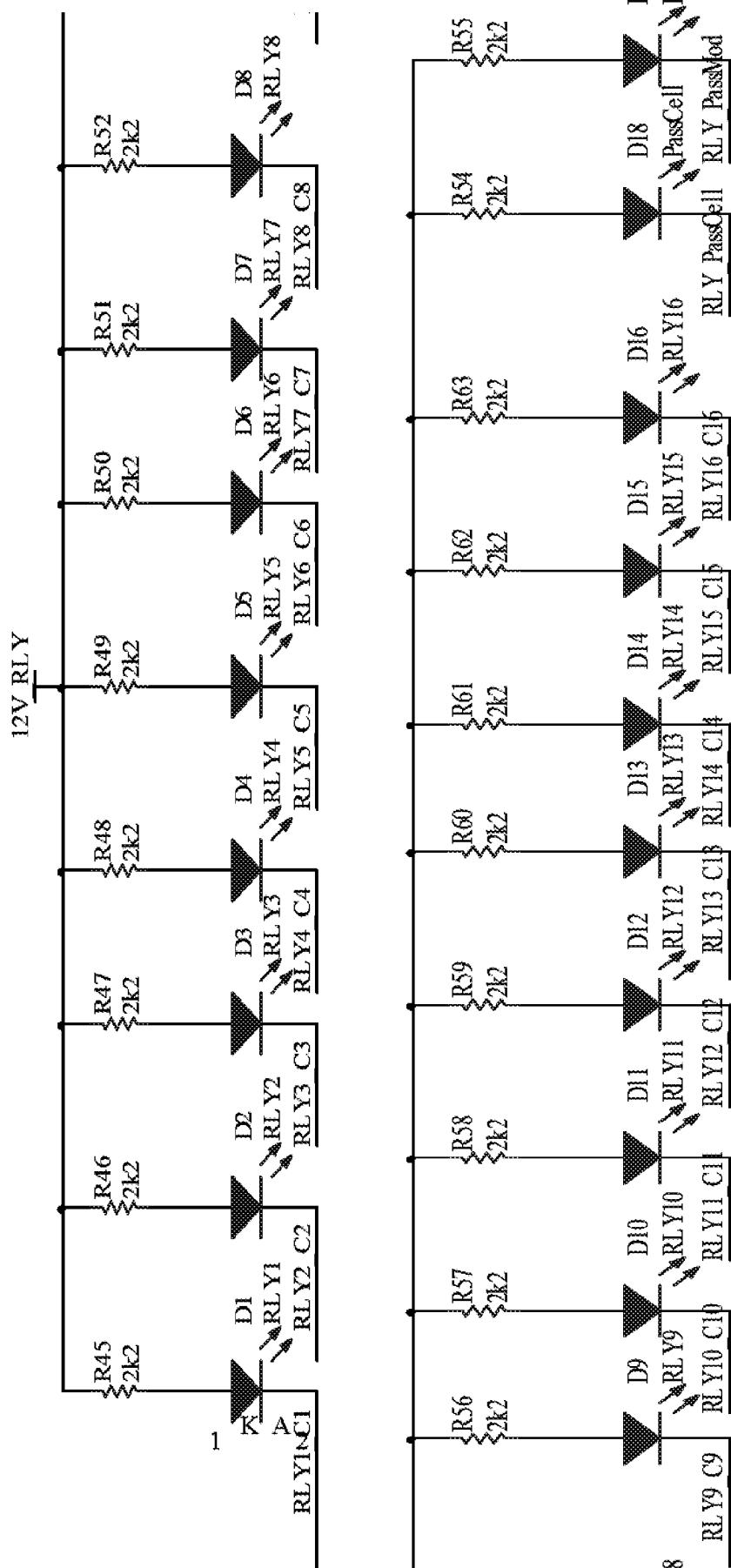
INDICATION LEDS

Fig. 7(g)
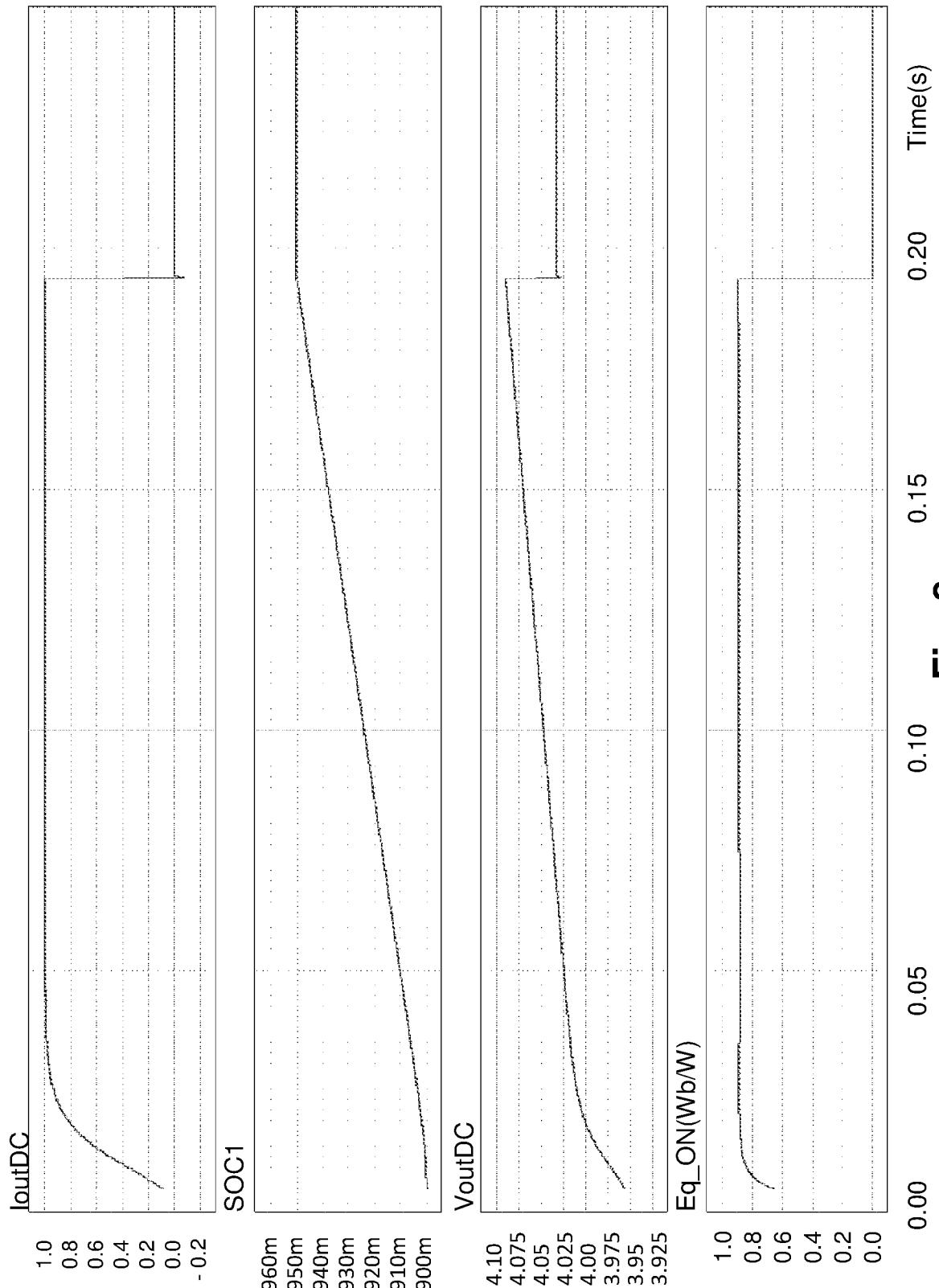
Fig. 8
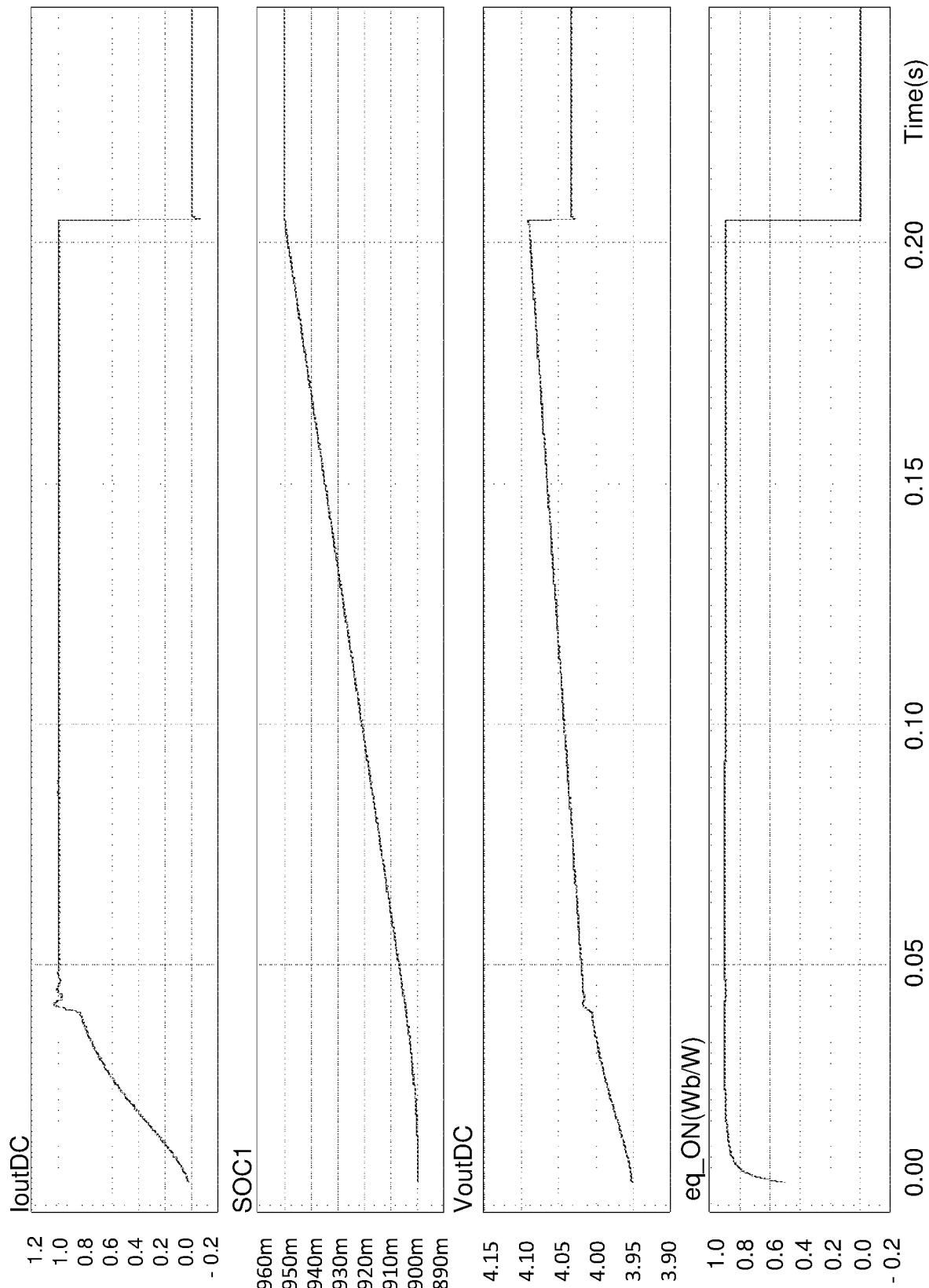
Fig. 9

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

INV. H02J7/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H02J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 289 096 A2 (HITACHI LTD [JP]; SHIN KOBE ELECTRIC MACHINERY [JP]) 5 March 2003 (2003-03-05) paragraph [0042] - paragraph [0153]; figures 1-10 -----	1-15
X	US 2006/022639 A1 (MOORE STEPHEN W [US]) 2 February 2006 (2006-02-02) paragraph [0026] - paragraph [0044]; figure 1a -----	1-15
X	EP 2 075 892 A2 (02MICRO INC [US]) 1 July 2009 (2009-07-01) paragraph [0012] - paragraph [0024]; figure 1a -----	1-15

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| X | Further documents are listed in the continuation of Box C. | | X | See patent family annex. |

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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Date of the actual completion of the international search	Date of mailing of the international search report
14 September 2017	06/10/2017

| Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016 | Authorized officer Kreutz, Joseph |

Form PCT/ISA/210 (second sheet) (April 2005)

1

C(Continuation).	DOCUMENTS CONSIDERED TO BE RELEVANT	
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A	WO 2008/137764 A1 (SENDYNE CORP [US]; OKUTO TADASHI [US]; MILIOS IOANNIS [US]) 13 November 2008 (2008-11-13) abstract; figure 1 -----	1-15

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